

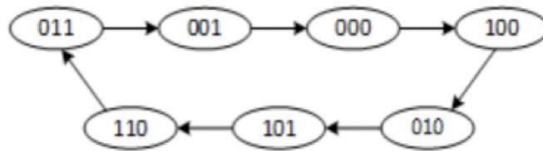
PROIECT CIRCUITE INTEGRATE DIGITALE

VLAS DENISA GEORGIANA

GRUPA 2122

proiect ciD

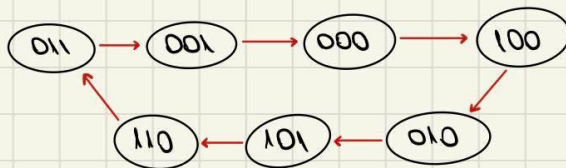
23.



Bistabile JK

F.	r	clk	Action
	0	x	Reset
	1		$Q^+ = JK$
	otherwise		Wait

MUX 2:1 și porți logice



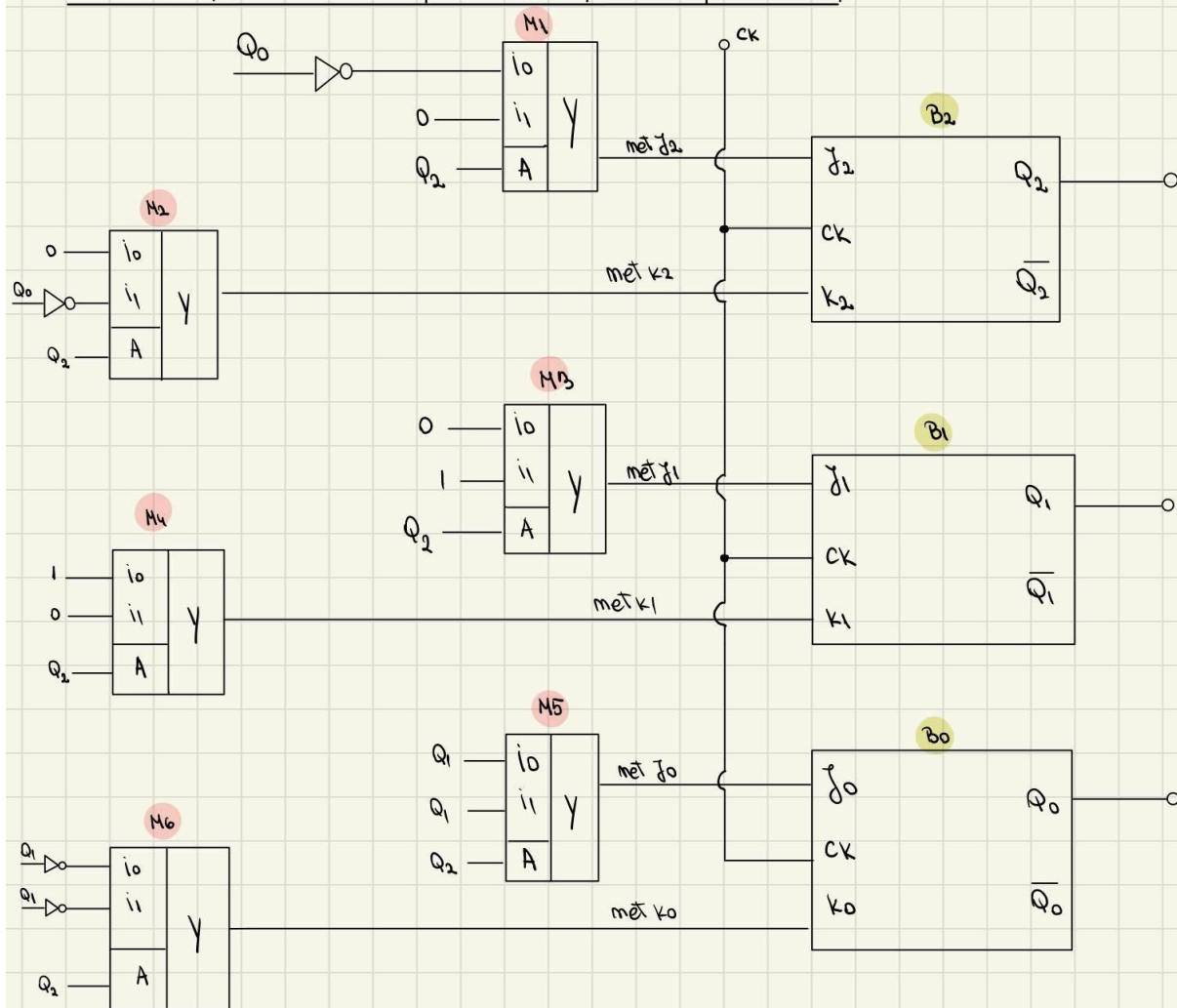
$Q_2 Q_1$	JK
0 0	0 x
0 1	1 x
1 0	x 1
1 1	x 0

$Q_2 Q_1 Q_0$	$Q_2^+ Q_1^+ Q_0^+$	$J_2 K_2$	$J_1 K_1$	$J_0 K_0$
0 0 0	1 0 0	1 x	0 x	0 x
0 0 1	0 0 0	0 x	0 x	x 1
0 1 0	1 0 1	1 x	x 1	1 x
0 1 1	0 0 1	0 x	x 1	x 0
1 0 0	0 1 0	x 1	1 x	0 x
1 0 1	1 1 0	x 0	1 x	x 1
1 1 0	0 1 1	x 1	x 0	1 x
1 1 1	x x x	x x	x x	x x

Bistabile JK



$Q_2 Q_1 Q_0$	$Q_2^+ Q_1^+ Q_0^+$	$J_2 K_2$	$J_1 K_1$	$J_0 K_0$
0 0 0	1 0 0	1	0	0
0 0 1	0 0 0	0	0	1
0 1 0	1 0 1	1	1	1
0 1 1	0 0 1	0	1	0
1 0 0	0 1 0	1	1	0
1 0 1	1 1 0	0	1	1
1 1 0	0 1 1	1	0	1
1 1 1	X X X	X	X	X



Project_Denisa_Georgia - [C:/Users/Denisa/Music/Project_Denisa_Georgia/Project_Denisa_Georgia.xpr] - Vivado 2018.2

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Default Layout

Flow Navigator

PROJECT MANAGER

- Settings
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IP INTEGRATOR

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SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream

Design Sources

Scope Sources

- Design Sources (1)
- automat (Behavioral) (automat.vhd) (11)
- Constraints
- Simulation Sources (1)
- sim_1 (1)
- test_automat (Behavioral) (test_automat.vhd)
- Utility Sources

Hierarchy Libraries Compile Order

Objects

Name	Value	Dir
clk	1	Lc
r	1	Lc
q2	5	Ar

automat.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity automat is
    Port ( clk : in STD_LOGIC;
          r : in STD_LOGIC;
          q : out STD_LOGIC_VECTOR (2 downto 0));
end automat;

architecture Behavioral of automat is
    component mux2 is
```

Tcl Console

INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_automat_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 807.887 ; gain = 16.598

Type a Tcl command here

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Hierarchy Libraries Compile Order

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Name	Value	Dir
clk	1	Lc
r	1	Lc
q2	5	Ar

automat.vhd

```
component mux2 is
    Port ( i0 : in STD_LOGIC;
          i1 : in STD_LOGIC;
          a : in STD_LOGIC;
          y : out STD_LOGIC);
end component mux2;

component bistJK is
    Port ( clk : in STD_LOGIC;
          r : in STD_LOGIC;
          s : in STD_LOGIC;
          k : in STD_LOGIC;
          q : out STD_LOGIC;
          qn : out STD_LOGIC);
end component bistJK;

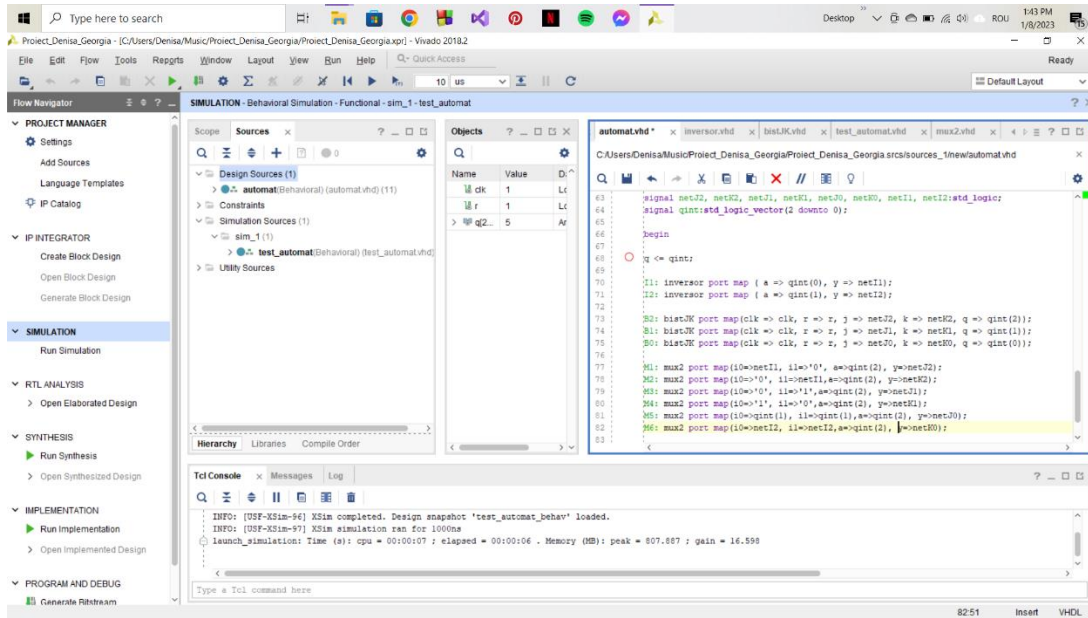
component inverter is
    Port ( a : in STD_LOGIC;
          y : out STD_LOGIC);
end component inverter;
```

Tcl Console

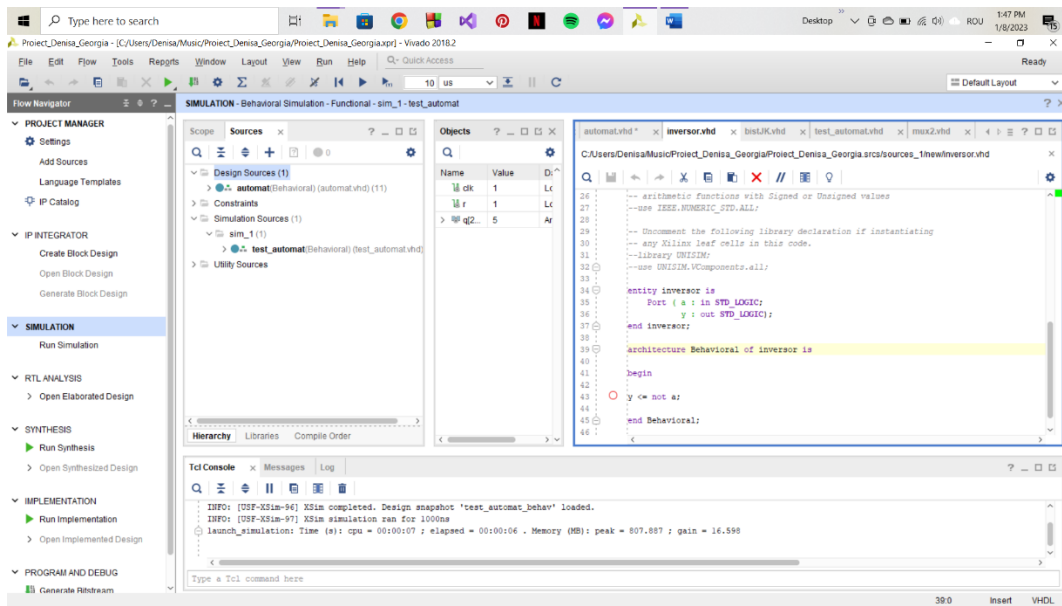
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_automat_behav' loaded.
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launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 807.887 ; gain = 16.598

Type a Tcl command here

82:51 Insert VHDL



Program Inversor.vhd



Program bistabile JK

The screenshot shows the Vivado 2018.2 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, Run, and Help. The top status bar shows the project name "Project_Denisa_Georgia" and the path "[C:/Users/Denisa/Music/Project_Denisa_Georgia/Project_Denisa_Georgia.xpr] - Vivado 2018.2".

The left sidebar contains the Project Manager, which is organized into several sections:

- PROJECT MANAGER
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 - Open Synthesized Design
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 - Generate Bitstream

The main editor area is divided into three panes:

- Scope**: Shows the design hierarchy. The selected source is "test_automat(Behavioral) (test_automat.vhd)".
- Objects**: A table showing the current state of the design. The table has columns for Name, Value, and Data Type.
- Sources**: A list of design sources. The selected source is "test_automat(Behavioral) (test_automat.vhd)".

The main editor displays the VHDL code for the "bistJK" entity. The code is as follows:

```
entity bistJK is
    Port ( clk : in STD_LOGIC;
          z : in STD_LOGIC;
          k : in STD_LOGIC;
          q : out STD_LOGIC;
          qn : out STD_LOGIC);
end bistJK;

architecture Behavioral of bistJK is
    signal input : std_logic_vector (1 downto 0);
    signal stare : std_logic;
begin
    input <= j & k;
    process(clk,z)
    begin
```

The Tcl Console at the bottom shows the following output:

```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_automat_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ms
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 807.887 ; gain = 16.598
```

The bottom status bar shows the current line number (430) and the current mode (Insert VHDL).

Project_Denisa_Georgia - [C:/Users/Denisa/Music/Project_Denisa_Georgia/Project_Denisa_Georgia.xpr] - Vivado 2018.2

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Scope Sources

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- Utility Sources

Objects

Name	Value	Dir
clk	1	Lc
r	1	Lc
q2	5	Ar

Tcl Console

```
INFO: [USF-XSim-94] XSim completed. Design snapshot 'test_automat_behav' loaded.  
INFO: [USF-XSim-97] XSim simulation ran for 1000ns  
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 807.887 ; gain = 16.598
```

430 Insert VHDL

Project_Denisa_Georgia - [C:/Users/Denisa/Music/Project_Denisa_Georgia/Project_Denisa_Georgia.xpr] - Vivado 2018.2

File Edit Flow Tools Reports Window Layout View Run Help Quick Access

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- Utility Sources

Objects

Name	Value	Dir
clk	1	Lc
r	1	Lc
q2	5	Ar

Tcl Console

```
INFO: [USF-XSim-94] XSim completed. Design snapshot 'test_automat_behav' loaded.  
INFO: [USF-XSim-97] XSim simulation ran for 1000ns  
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 807.887 ; gain = 16.598
```

430 Insert VHDL

Sharing Scri
A link to yo
to your clip

Show

Test_automat.vhd

The image displays two screenshots of the Vivado IDE interface, showing the simulation of a VHDL testbench named `test_automat.vhd`.

Top Screenshot:

- Project Manager:** Shows the project structure with `Design Sources (1)` containing `automat Behavioral (automat.vhd) (11)` and `Simulation Sources (1)` containing `sim_1 (1)` and `test_automat Behavioral (test_automat.vhd)`.
- Objects:** A table showing the current values of signals:

Name	Value	D.
clk	1	Lc
r	1	Lc
q2	5	Ar
- Code Editor:** Displays the VHDL code for `test_automat.vhd`. The code defines an entity `test_automat` with a port `clk` and a component `automat` that takes `clk` and `r` as inputs and outputs a `std_logic_vector` of size 2.
- Tcl Console:** Shows the simulation results, including the message: `INFO: [DSE-XSim-94] XSim completed. Design snapshot 'test_automat_behav' loaded.` and the simulation time: `launch_simulation: Time (s): cpu = 00:00:07; elapsed = 00:00:06; Memory (MB): peak = 807.887; gain = 16.598`.

Bottom Screenshot:

- Code Editor:** Displays the updated VHDL code for `test_automat.vhd`. The code now includes a `process` block that sets the `clk` signal to `'0'` and `'1'` for a duration of 1.2 ns, and a `begin` block that sets the `r` signal to `'0'` and `'1'` after 0 ns and 1 ns, respectively.
- Tcl Console:** Shows the simulation results, including the message: `INFO: [DSE-XSim-94] XSim completed. Design snapshot 'test_automat_behav' loaded.` and the simulation time: `launch_simulation: Time (s): cpu = 00:00:07; elapsed = 00:00:06; Memory (MB): peak = 807.887; gain = 16.598`.

A Dropbox sharing screenshot notification is visible in the bottom right corner of the second screenshot.

Mux2.vhd

The screenshot displays the Vivado 2018.2 IDE interface during a behavioral simulation. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, Run, and Help. The status bar at the top right shows the time as 1:49 PM on 1/8/2023.

The left sidebar contains the Project Manager, which is expanded to show the Simulation Sources. The Simulation Sources list includes:

- Design Sources (1)
 - automat Behavioral (automat.vhd) (11)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - test_automat Behavioral (test_automat.vhd)
- Utility Sources

The main workspace is divided into several panes:

- Scope:** Shows the current simulation scope, including the test_automat Behavioral (test_automat.vhd).
- Objects:** A table showing the current values of signals in the simulation.
- Code Editor:** Displays the VHDL code for the mux2.vhd file. The code defines a 2-to-1 multiplexer.
- Tcl Console:** Shows the results of the simulation, including the time taken for the simulation to complete.

The Objects pane shows the following signals and their values:

Name	Value	Dir
clk	1	Lc
r	1	Lc
q2	5	Ar

The Code Editor shows the following VHDL code for mux2.vhd:

```
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 library UNISIM;
32 use UNISIM.VComponents.all;
33
34 entity mux2 is
35     Port (
36         i0 : in STD_LOGIC;
37         i1 : in STD_LOGIC;
38         a : in STD_LOGIC;
39         y : out STD_LOGIC);
40 end mux2;
41
42 architecture Behavioral of mux2 is
43 begin
44     y <= i1 when a = '1' else i0;
45 end Behavioral;
```

The Tcl Console shows the following output:

```
INFO: [DSF-XSim-94] XSim completed. Design snapshot 'test_automat_behav' loaded.
INFO: [DSF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 807.887 ; gain = 16.598
```

Implementare finala

