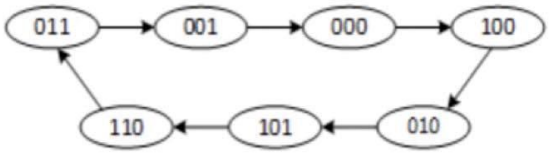
PROIECT CIRCUITE INTEGRATE DIGITALE

VLAS DENISA GEORGIANA

GRUPA 2122

Proiect CID

23.

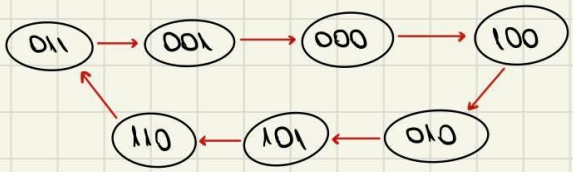


Bistabile JK

F.

r	clk	Action
0	x	Reset
1	↓	$Q^+ = JK$
otherwise		Wait

MUX 2:1 și porți logice

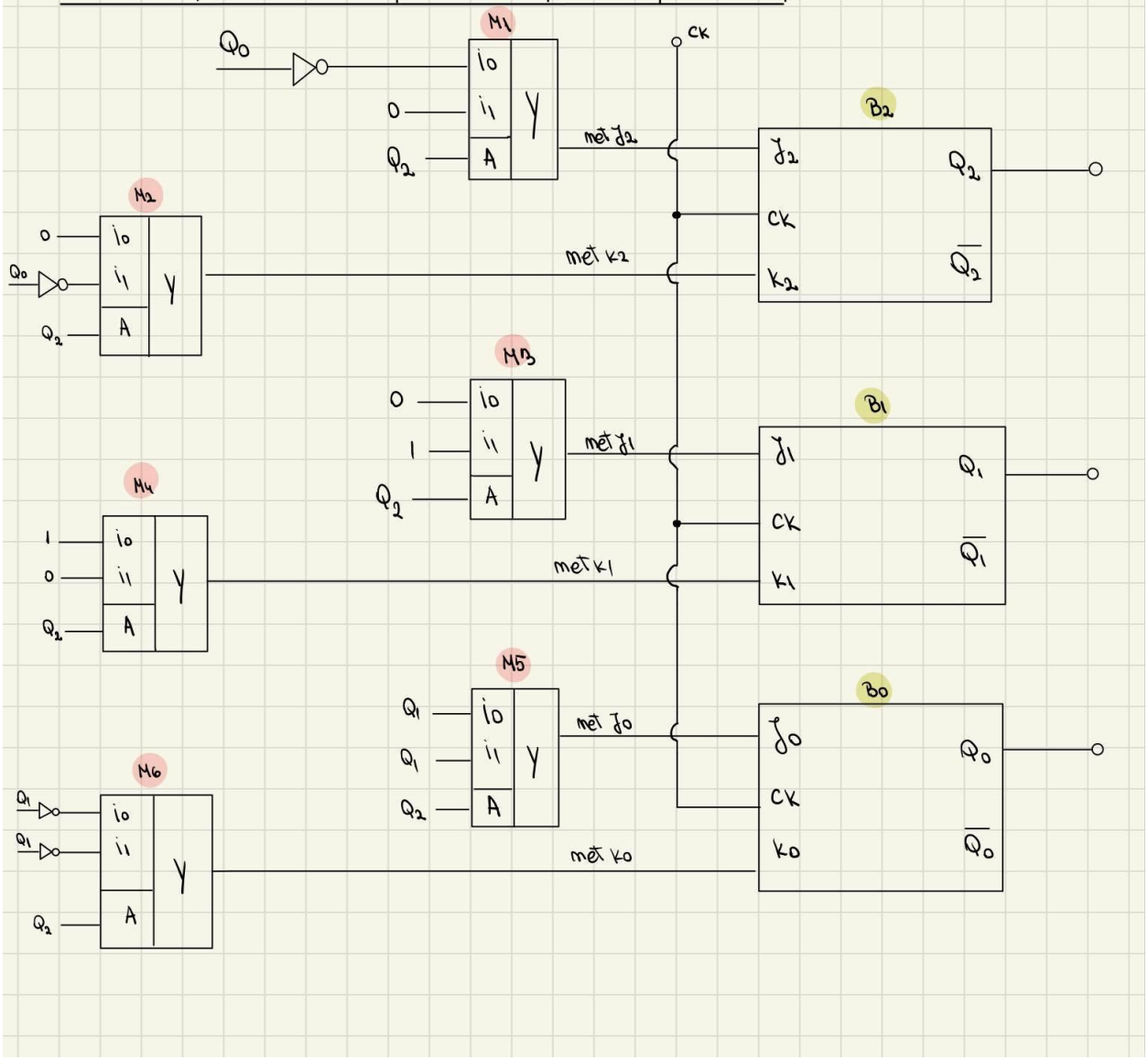


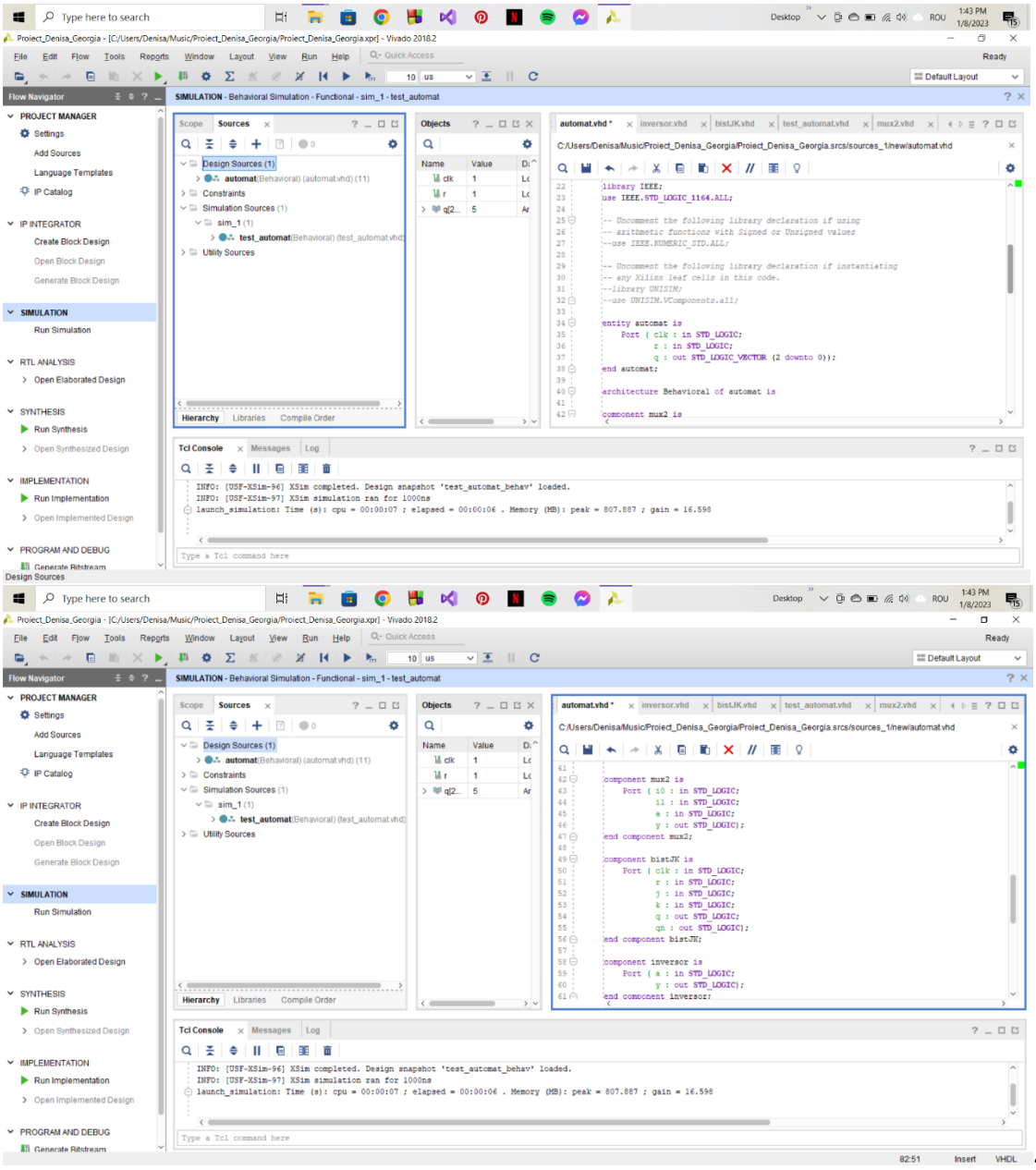
$Q_2Q_1Q_0$	$Q_2^+Q_1^+Q_0^+$	J_2K_2	J_1K_1	J_0K_0
0 0 0	1 0 0	1 X	0 X	0 X
0 0 1	0 0 0	0 X	0 X	X 1
0 1 0	1 0 1	1 X	X 1	1 X
0 1 1	0 0 1	0 X	X 1	X 0
1 0 0	0 1 0	X 1	1 X	0 X
1 0 1	1 1 0	X 0	1 X	X 1
1 1 0	0 1 1	X 1	X 0	1 X
1 1 1	X X X	X X	X X	X X

QQ^+	JK
0 0	0 X
0 1	1 X
1 0	X 1
1 1	X 0

Bistabile JK

$Q_2Q_1Q_0$	$Q_2^+Q_1^+Q_0^+$	J_2K_2	J_1K_1	J_0K_0
0 0 0	1 0 0	1	0	0
0 0 1	0 0 0	0 (Q_2^+)	0	1
0 1 0	1 0 1	1	1	1
0 1 1	0 0 1	0	1	0
1 0 0	0 1 0	1	1	0
1 0 1	1 1 0	0	1	1
1 1 0	0 1 1	1	0	1
1 1 1	X X X	X	X	X




Proiect_Denisa_Georgia - [C:/Users/Denisa/Music/Proiect_Denisa_Georgia/Proiect_Denisa_Georgia.xpr] - Vivado 2018.2
SIMULATION - Behavioral Simulation - Functional - sim_1 - test_automat
C:/Users/Denisa/Music/Proiect_Denisa_Georgia/Proiect_Denisa_Georgia.srcs/sources_1/new/automat.vhd
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_automat_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 807.887 ; gain = 16.598

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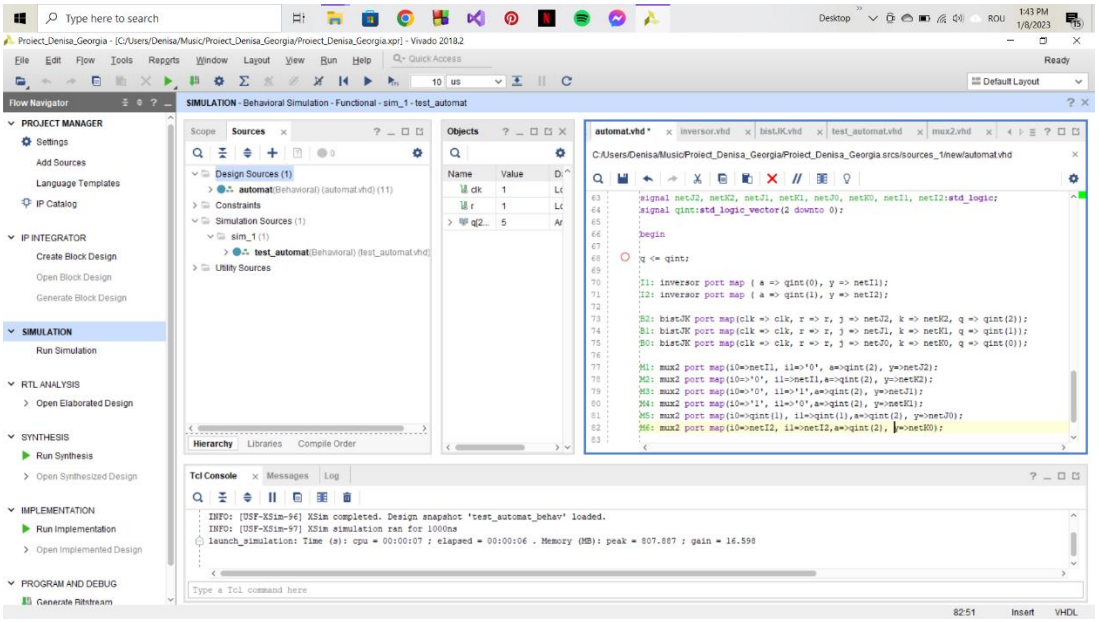
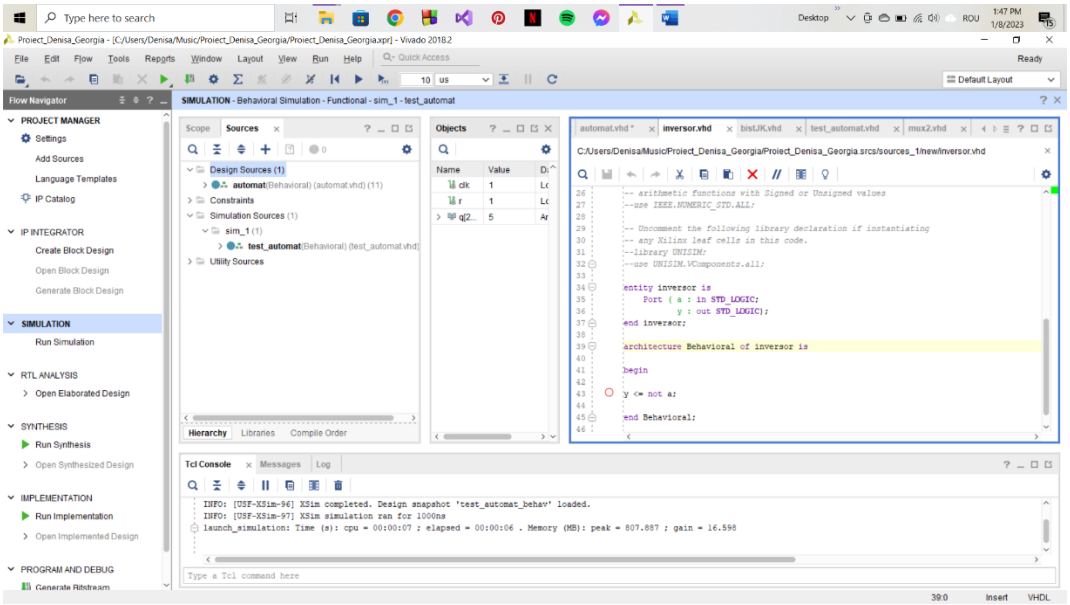
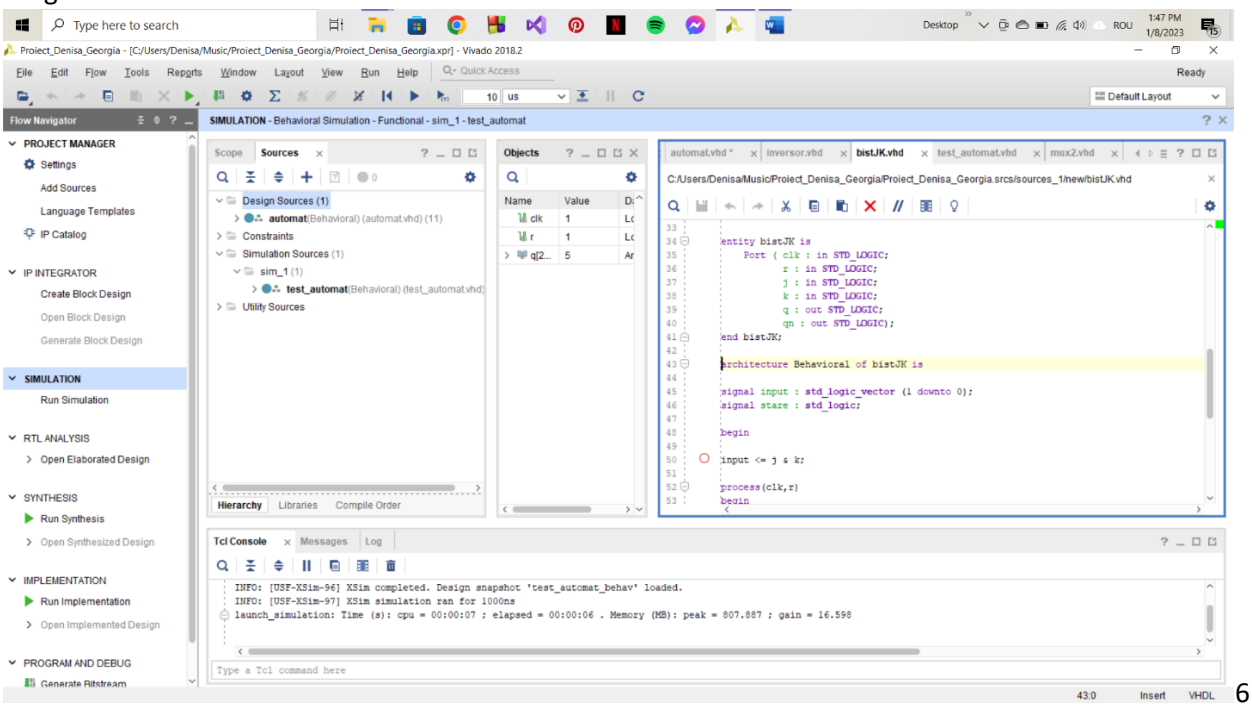
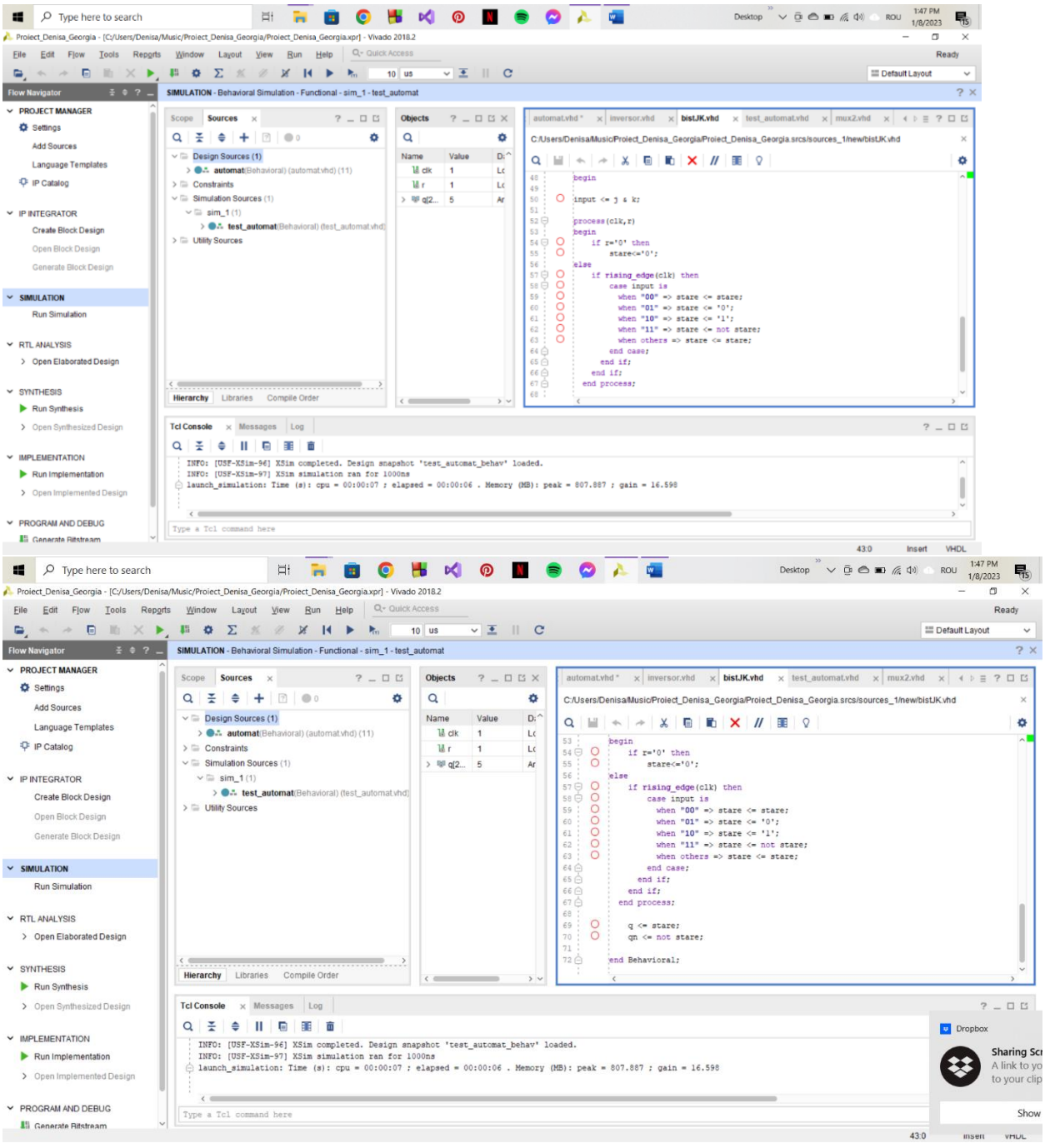


Program Inversor.vhd



Program bistabile JK

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Proiect_Denisa_Georgia - [C:/Users/Denisa/Music/Proiect_Denisa_Georgia/Proiect_Denisa_Georgia.xpr] - Vivado 2018.2
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Generate Bitstream
SIMULATION - Behavioral Simulation - Functional - sim_1 - test_automat
Scope
Sources
Design Sources (1)
automat(Behavioral) (automat.vhd) (11)
Constraints
Simulation Sources (1)
sim_1 (1)
test_automat(Behavioral) (test_automat.vhd)
Utility Sources
Hierarchy
Libraries
Compile Order
Objects
Name
Value
clk
r
automat.vhd *
inversor.vhd
bistJK.vhd
test_automat.vhd
mux2.vhd
C:/Users/Denisa/Music/Proiect_Denisa_Georgia/Proiect_Denisa_Georgia.srcs/sources_1/new/bistJK.vhd
begin
input <= j & k;
process(clk,r)
begin
if r='0' then
stare<='0';
else
if rising_edge(clk) then
case input is
when "00" => stare <= stare;
when "01" => stare <= '0';
when "10" => stare <= '1';
when "11" => stare <= not stare;
when others => stare <= stare;
end case;
end if;
end if;
end process;
Tcl Console
Messages
Log
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_automat_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 807.887 ; gain = 16.598
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test_automat.vhd
mux2.vhd
C:/Users/Denisa/Music/Proiect_Denisa_Georgia/Proiect_Denisa_Georgia.srcs/sources_1/new/bistJK.vhd
begin
if r='0' then
stare<='0';
else
if rising_edge(clk) then
case input is
when "00" => stare <= stare;
when "01" => stare <= '0';
when "10" => stare <= '1';
when "11" => stare <= not stare;
when others => stare <= stare;
end case;
end if;
end if;
end process;
q <= stare;
qn <= not stare;
end Behavioral;
Tcl Console
Messages
Log
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INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 807.887 ; gain = 16.598
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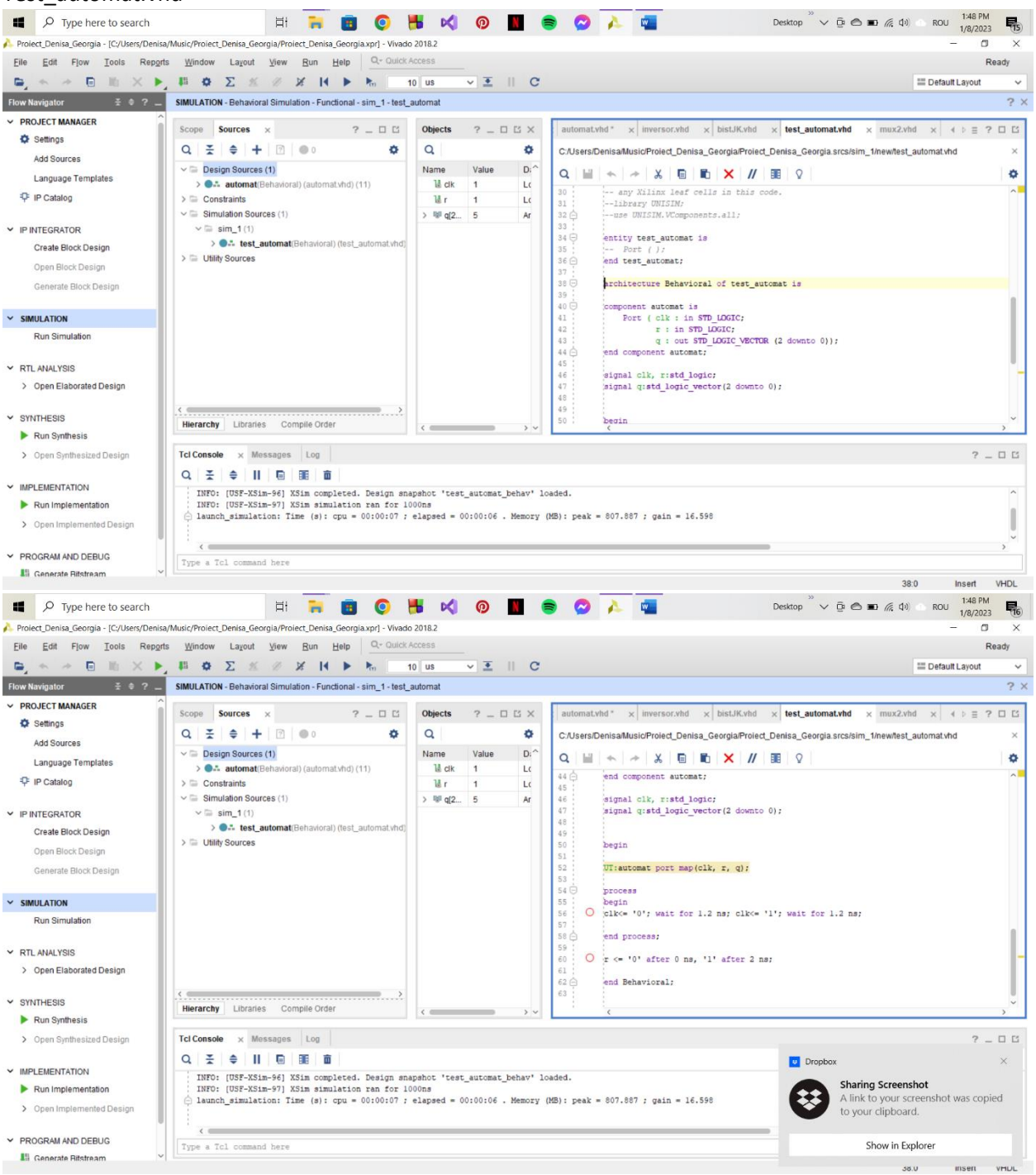
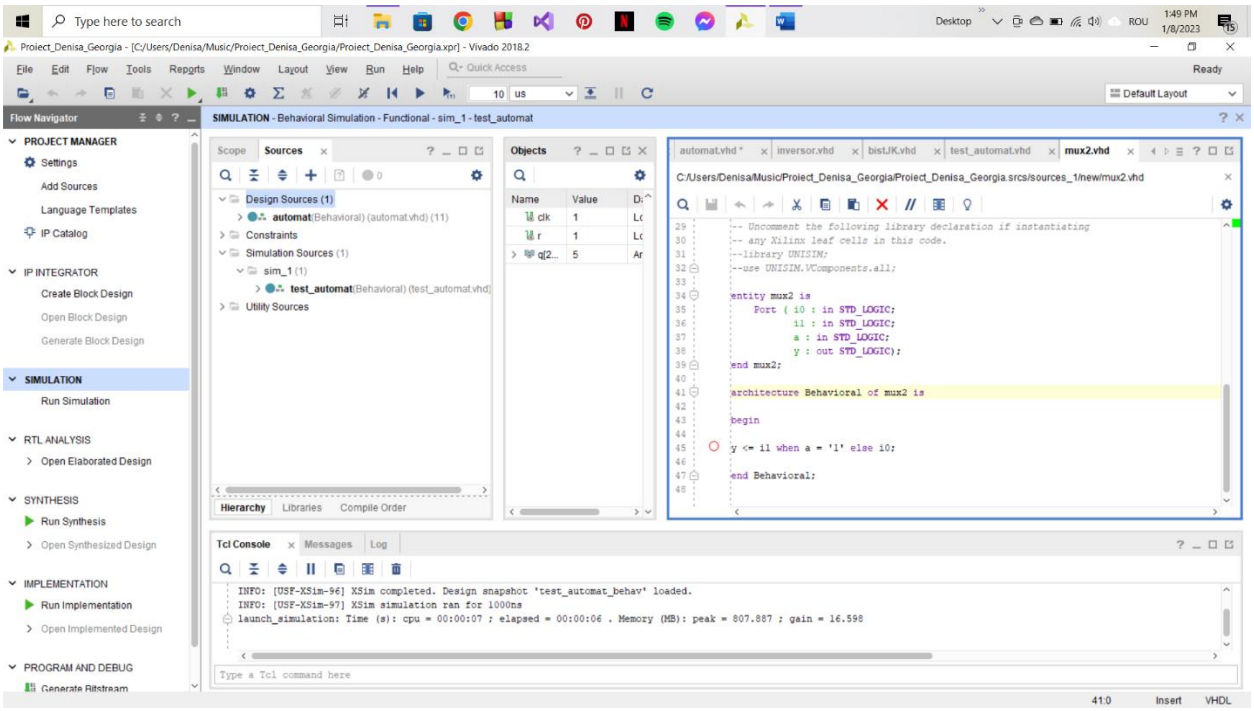
Test_automat.vhd



Mux2.vhd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bistJK.vhd
test_automat.vhd
mux2.vhd
C:/Users/Denisa/Music/Proiect_Denisa_Georgia/Proiect_Denisa_Georgia.srcs/sources_1/new/mux2.vhd
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity mux2 is
Port (i0 : in STD_LOGIC;
i1 : in STD_LOGIC;
a : in STD_LOGIC;
y : out STD_LOGIC);
end mux2;
architecture Behavioral of mux2 is
begin
y <= i1 when a = '1' else i0;
end Behavioral;
Tcl Console
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Type a Tcl command here
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Insert
VHDL

Implementare finala