IP Core Generation Report for minimalIpCore

Summary

IP core name	minimal_ip
IP core version	1.0
IP core folder	hdl_prj/ipcore/minimal_ip_v1_0
IP core zip file name	minimal_ip_v1_0.zip
IP repository	/home/cotti/Desktop/Proyecto_final/vlc_utn/vivado_tutorial/09_ip_core_debugging/ip_repo
Target platform	Generic Xilinx Platform
Target tool	Xilinx Vivado
Target language	VHDL
Model	minimalIpCore
Model version	1.8
HDL Coder version	24.1
IP core generated on	25-Aug-2024 17:37:10
IP core generated for	minimal_IP

Target Interface Configuration

Target platform interface table:

Port Name	Port Type	Data Type	Target Platform Interfaces	Interface Mapping	Interface Options
in_a	Inport	uint8	External Port		
in_b	Inport	uint8	External Port		
a_times_b	Outport	uint16	External Port		
a_plus_b	Outport	ufix9	External Port		

IP Core User Guide

Theory of Operation

This IP core also support the **External Port** interface. To connect the external ports to the FPGA external IO pins, add FPGA pin assignment constraints in the Xilinx Vivado environment.

Xilinx Vivado Environment Integration

This IP Core is generated for the Xilinx Vivado environment. The following steps are an example showing how to integrate the generated IP core into Xilinx Vivado environment:

1. The generated IP core is a zip package file under the IP core folder. Please check the Summary section of this report for the IP zip file name and folder.
2. In the Vivado project, go to Project Settings -> IP -> Repository Manager, add the folder containing the IP zip file as IP Repository.
3. In Repository Manger, click the "Add IP" button to add IP zip file to the IP repository. This step adds the generated IP into the Vivado IP Catalog.
4. In the Vivado project, find the generated IP core in the IP Catalog under category "HDL Coder Generated

IP". In you have a Vivado block design open, you can add the generated IP into your block design.
5. Connect the AXI4SlaveEmpty port of the IP core to the embedded processor's AXI master port.
6. Connect the clock and reset ports of the IP core to the global clock and reset signals.
7. Assign an Offset Address for the IP core in the Address Editor.
8. Connect external ports and add FPGA pin assignment constraints to constraint file.
9. Generate FPGA bitstream and download the bitstream to target device.

If you are targeting Xilinx Zynq hardwares supported by HDL Coder Support Package for Xilinx FPGA and SoC Devices, you can select the board you are using in the Target platform option in the Set Target > Set Target Device and Synthesis Tool task. You can then use Embedded System Integration tasks in HDL Workflow Advisor to help you integrate the generated IP core into Xilinx Vivado environment.

IP Core File List

The IP core folder is located at:
hdl_prj/ipcore/minimal_ip_v1_0
Following files are generated under this folder:

IP core zip file
minimal_ip_v1_0.zip

IP core report
doc/minimalIpCore_ip_core_report.html

IP core HDL source files
hdl/minimal_ip_src_minimal_IP.vhd
hdl/minimal_ip_reset_sync.vhd
hdl/minimal_ip_dut.vhd
hdl/minimal_ip.vhd