About HME-H7 Family FPGA

HME-H7 combines the extreme flexibility of an FPGA with high performance Cortex-m3 MCU core and peripherals, and large on chip SRAM.

HME-H7 family is a high-performance device which can be used in a wide range of applications such as high performance MCU control and processing, and especially are optimized for Embedded Vision applications – supporting a variety of high bandwidth sensor and display interfaces, video processing such as LED display and TCON and industry control.

By using these configurable soft IP cores as standardized blocks, hardened IPs and MCU, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

See *Figure 1* for architecture of HME-H7.

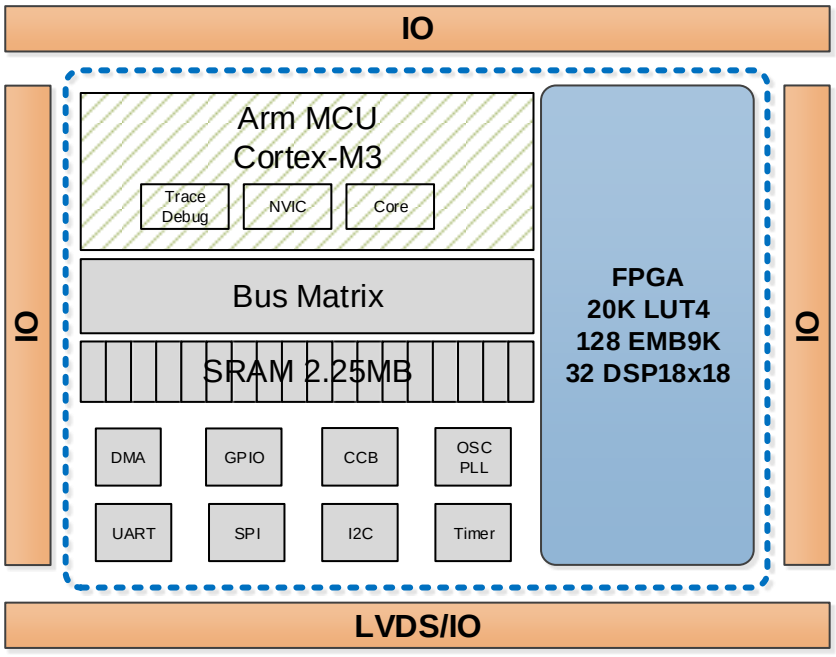

Figure 1 HME-H7 FAMILY Architecture

HME-H7 Family FPGA Features

FPGA

- 6-input Look-up Tables High Performance FPGA Fabric
  - 20K logic cells
  - DFF-based registers, up to 23,040
- Embedded Memory Block
  - 128 programmable true-dual-port EMB block, 9Kb
  - Totaling 1152Kb
- Embedded DSP Blocks
  - 32 DSP (MAC) blocks (18 x 18)
  - or 64 DSP (MAC) blocks (18 x 9)
  - or 128 DSP (MAC) blocks (10 x 10)
- Clock Network
  - 32 de-skew global clocks
  - Flexible hierarchical clock network
  - 1 OSC
  - 2 PLLs
  - Dynamic clock management in system
- I/O
  - Support the following single-ended standards:
    3.3/2.5/1.8/1.5/1.2V LVTTL/LVCMOS
    1.8/1.5/1.35/1.2V SSTL/HSTL
  - Support the following differential standards:
    LVDS RX/TX, BLVDS, LVPECL
  - Support for on-chip termination resistors
  - Support for MIPI D-PHY level standard
  - Up to 1200 Mb/s per LVDS I/O
  - Supports IDDR2/ODDR2 input/output modes
  - Supports input/output serial-to-parallel and parallel-to-serial conversion functions

MCU

- ARM Cortex-M3 MCU
  - High performance 32-bit processor, frequency up to 268MHz
  - Outstanding processing performance combined with fast interrupt handling
  - Enhanced system debug with extensive breakpoint and trace capabilities
  - Efficient processor core, system, and memories
  - Integrated sleep mode
- Peripheral
  - 2 Timers
  - 1 Watch Dog Timer
  - 3 I2C interfaces
  - 3 SPI interfaces
  - 1 QSPI interface
  - 3 UART interfaces
  - 2 GPIOs, 32-bit
  - 1 DMA

Memory

- Embedded SRAM Block
  - 18 SRAMs, 32Kx32b, totaling 2304KB
- External Memory (Optional)
  - 32Mb pSRAM, 64Mb pSRAM or 128Mb pSRAM
  - 1 SDRAM, 64Mb

Configuration

- Configuration Mode
  - JTAG Mode
  - AS Mode
  - PS Mode
- In System Configuration
- JTAG Interface
  - JTAG Chip Configuration
  - JTAG Cortex-M3 Debugging

eFuse

- 128-bit eFuse

Package

- LQFP176
- FBGA256
- VFBGA324

- TFBGA213
- LQFP128

HME-H7 Family FPGA Feature Summary

Table 1 HME-H7 FPGA Feature Summary

Part Number		H7P20-M0H1	H7P20-M1H1	H7P20-M2H1	H7P20-S1H1	H7P20-M0X1	H7P20-M0A1	H7P20-M3H1
Programmable Logic Block (PLB)	Logic cells (K)	20	20	20	20	20	20	20
	LUT6	11,520	11,520	11,520	11,520	11,520	11,520	11,520
	Register	23,040	23,040	23,040	23,040	23,040	23,040	23,040
Embedded Memory Block (EMB)	9Kb	128	128	128	128	128	128	128
	Max (Kb)	1,152	1,152	1,152	1,152	1,152	1,152	1,152
DSP	18b*18b	32	32	32	32	32	32	32
PLL		2	2	2	2	2	2	2
OSC		1	1	1	1	1	1	1
MCU	Cortex-M3	1	1	1	1	1	1	1
	UART	3	3	3	3	3	3	3
	I2C	3	3	3	3	3	3	3
	SPI	3	3	3	3	3	3	3
	GPIO	2	2	2	2	2	2	2
	Timer	2	2	2	2	2	2	2
	WDG	1	1	1	1	1	1	1
	DMA	1	1	1	1	1	1	1
SRAM	32Kx32b(128KB)	18	18	18	18	18	18	18
	Total (KB)	2304	2304	2304	2304	2304	2304	2304
pSRAM	32Mb	0	1	2	0	0	0	0
	128Mb	0	0	0	0	0	0	1
	Total (Mb)	0	32	64	0	0	0	128
SDRAM	64Mb	0	0	0	1	0	0	0
	Total (Mb)	0	0	0	64	0	0	0
eFuse	128b	1	1	1	1	1	1	1
Package (unit: mm)		Max user I/O/LVDS						
LQFP176 (22.00x22.00x1.60, 0.4 pitch)		142/0	142/0	142/0	-	-	-	-
FBGA256 (17.00x17.00x1.45, 1.0 pitch)		-	-	-	-	186/0	179/0	-
VFBGA324 (15.00x15.00x1.30, 0.8 pitch)		-	-	-	-	210/24	-	-
TFBGA213 (12.00×12.00×1.17, 0.8 pitch)		173/18	-	-	173/18	-	-	-
LQFP128 (16.00×16.00×1.60, 0.4 pitch)		-	-	-	-	-	-	96/10