

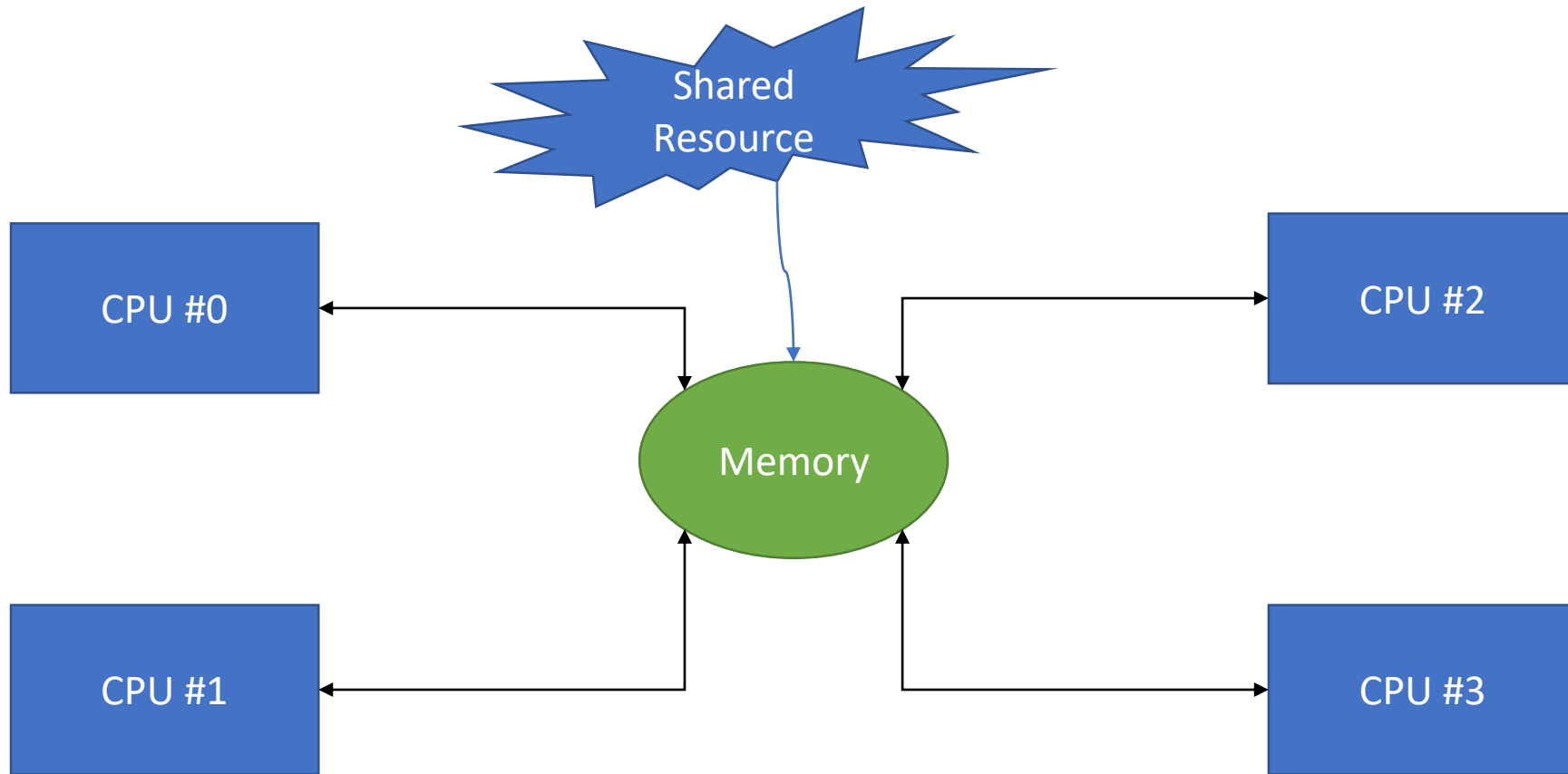
# Verilog HDL Design, Simulation & Synthesis of Round Robin Arbiter (Fixed Time Slices)

*Video Lecture [Link](#)*

# Verilog HDL Design of Round Robin Arbiter (Fixed Time Slices)

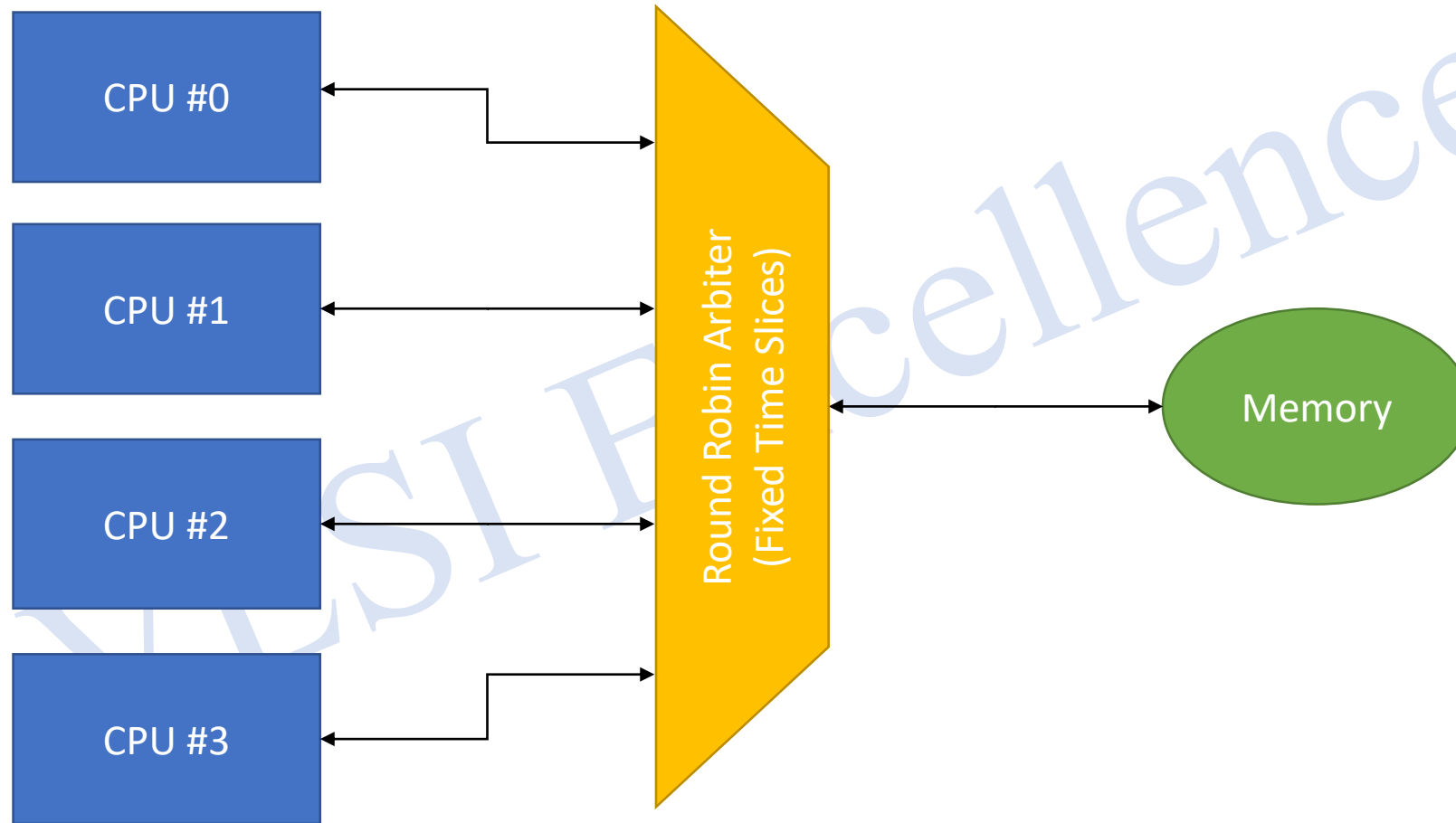
- ☐ What is an Arbiter ?
- ☐ Applications/ Examples
- ☐ Advantages/Disadvantages
- ☐ Verilog HDL Design
- ☐ Synthesizing the Design
- ☐ Test Bench Design
- ☐ Analysing Simulation Waveforms

# Verilog HDL Design of Round Robin Arbiter (Fixed Time Slices)



*Figure #01: Shared Resource Access by 4 CPUs*

## Verilog HDL Design of Round Robin Arbiter (Fixed Time Slices)



*Figure #02: Application of Arbiter to Access a Shared Resource*

# Verilog HDL Design of Round Robin Arbiter (Fixed Time Slices)



Figure #03: Arbiter Block Diagram

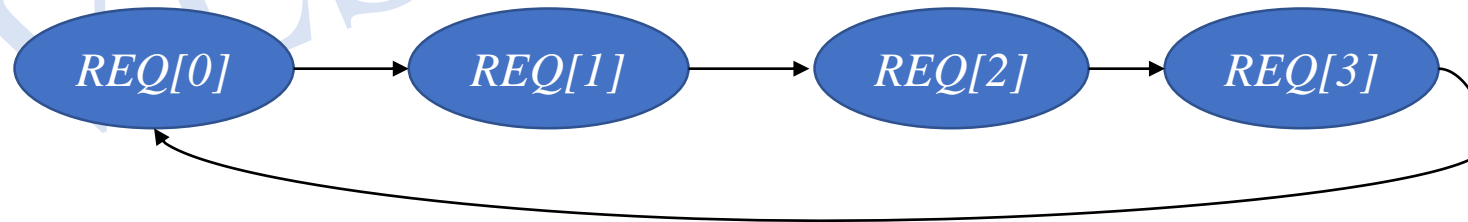


Figure #04: Arbiter Finite State Machine

# Verilog HDL Design of Round Robin Arbiter (Fixed Time Slices)

## Applications/Examples :

1. Accessing a memory location by multiple process
2. Routers where users are competing for a switch

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# Verilog HDL Design of Round Robin Arbiter (Fixed Time Slices)

## Advantages and Disadvantages of Round Robin Arbiter (Fixed Time Slices)

### **Advantage:**

Shared resource is allocated uniformly to all requesters and hence does not lead the requesters to starvation

### **Disadvantage:**

Since, all requesters are treated equally, we can not give importance to a specific requester

# Verilog HDL Design of Round Robin Arbiter (Fixed Time Slices)

## Specification:

1. The arbiter takes 4 input requests and outputs a single grant in the form of ONE HOT
2. Round Robin Scheduling  $REQ[0] > REQ[1] > REQ[2] > REQ[3] > REQ[0] \dots$



# Verilog HDL Design of Round Robin Arbiter (Fixed Time Slices)

Verilog HDL Design and Test-Bench Simulation:

We will be using **EDA Playground** (<https://www.edaplayground.com>) to design Fixed Priority Round Robin Arbiter in Verilog HDL.

**Synthesis** using Open Source Synthesis Tool : **Yosys** (Available in EDA Playground)

**Simulation** using Open Source Simulation Tool : **Riviera** (Available in EDA Playground)

*Verilog Project [Link](#)*

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Thank You !!!