Verilog HDL Design, Simulation & Synthesis of Round Robin Arbiter (Variable Time Slices)

Video Lecture Link

Verilog HDL Design of Round Robin Arbiter (Variable Time Slices)

- What is an Arbiter ?
- Applications/ Examples
- Advantages/Disadvantages
- Verilog HDL Design
- Synthesizing the Design
- Test Bench Design
- Analysing Simulation Waveforms

Verilog HDL Design of Round Robin Arbiter (Variable Time Slices)

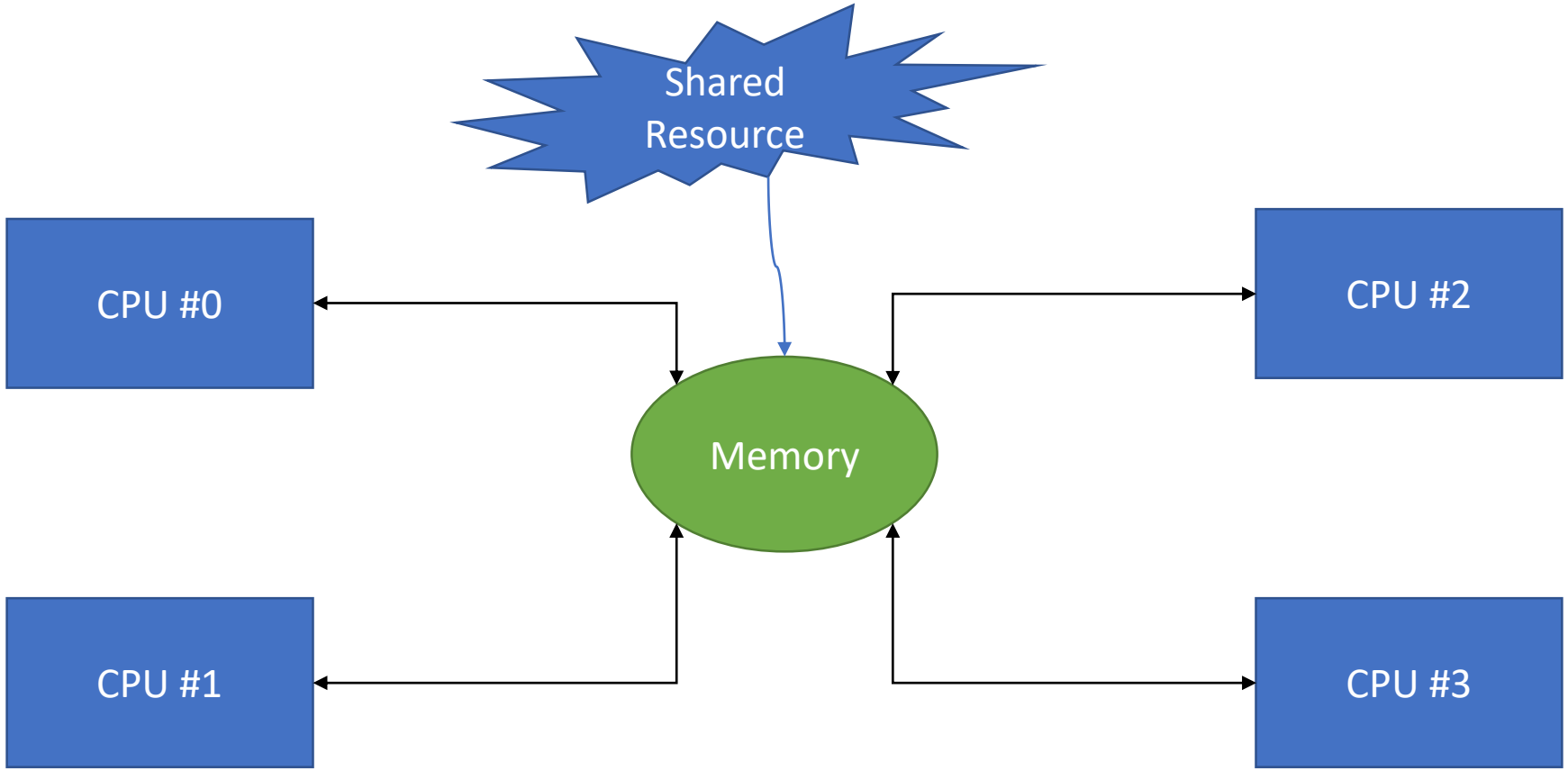

Figure #01: Shared Resource Access by 4 CPUs

Verilog HDL Design of Round Robin Arbiter (Variable Time Slices)

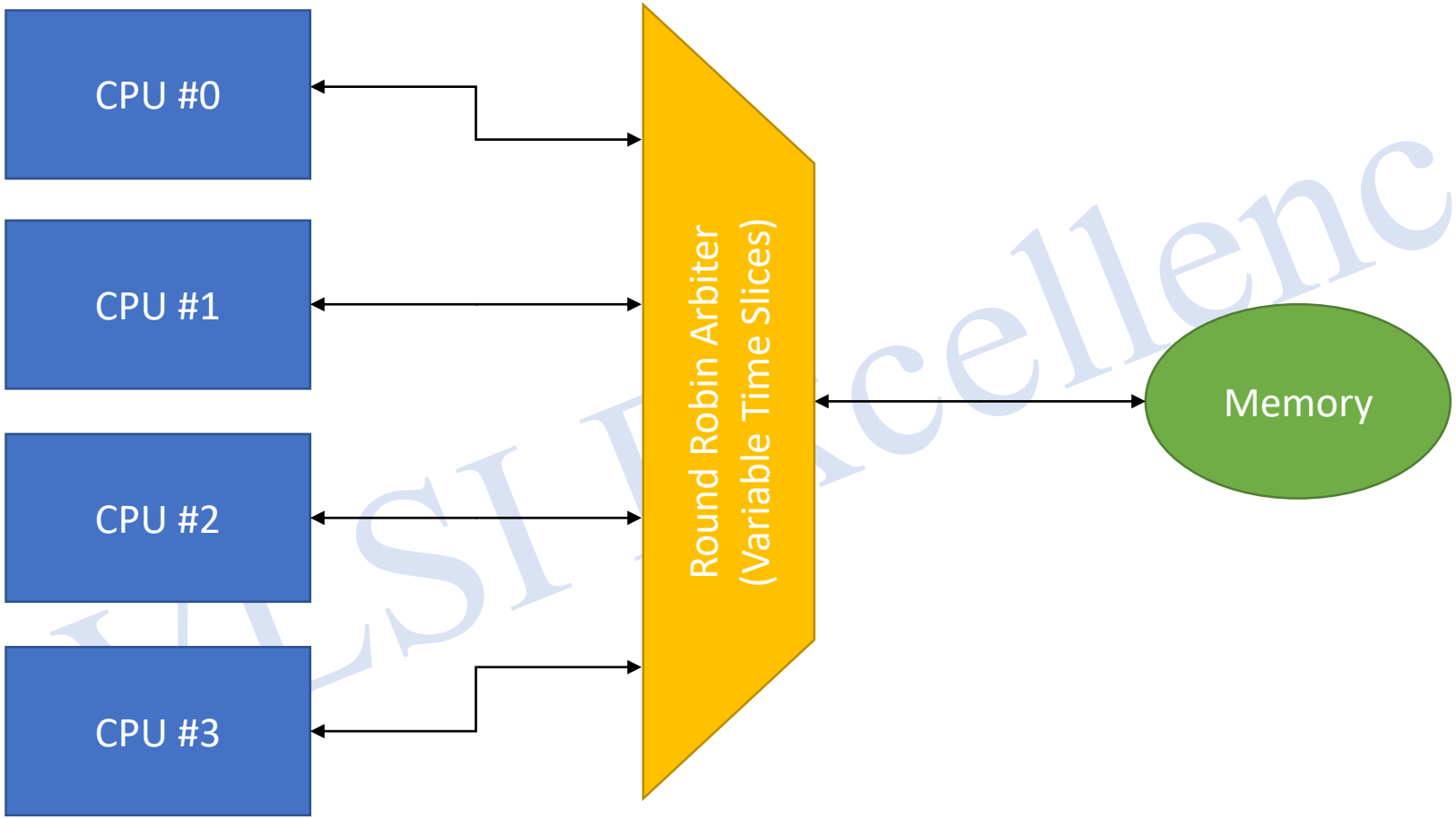

Figure #02: Application of Arbiter in Accessing Shared Resource

Verilog HDL Design of Round Robin Arbiter (Variable Time Slices)

Figure #03: Arbiter Block Diagram

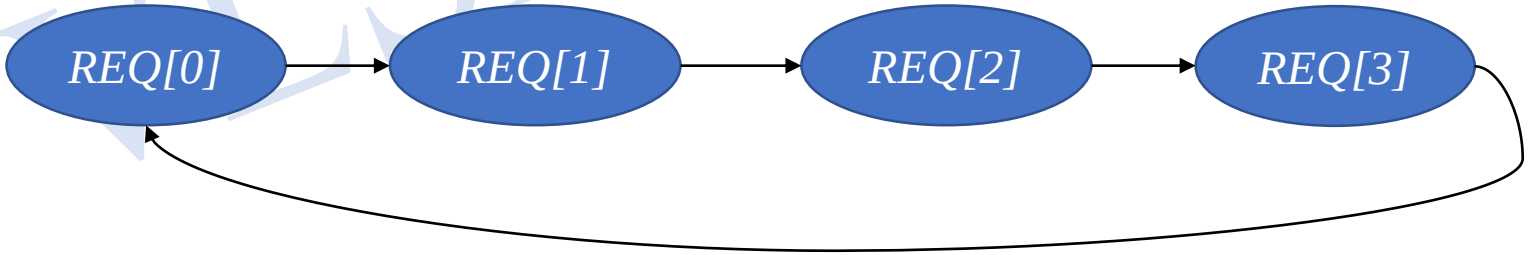

Figure #04: Arbiter Finite State Machine

Verilog HDL Design of Round Robin Arbiter (Variable Time Slices)

Applications/Examples :

1. Accessing a memory location by multiple process
2. Routers where users are competing for a switch

Verilog HDL Design of Round Robin Arbiter (Variable Time Slices)

Advantages and Disadvantages of Round Robin Arbiter (Variable Time Slices)

Advantage:

Shared resource is allocated uniformly to all requesters and hence does not led the requesters to starvation

Disadvantage:

Since, all requesters are treated equally, we can not give importance to a specific requester

Verilog HDL Design of Round Robin Arbiter (Variable Time Slices)

Specification:

1. The arbiter takes 4 input requests and outputs a single grant in the form of ONE HOT
2. Round Robin Scheduling REQ[0] > REQ[1] > REQ[2] > REQ[3] > REQ[0] . . .
3. 4 clock cycles are allocated to each requester
4. However, to save the time the 4 clock cycle slices are variable in nature
5. That means, if a particular requester is only using the shared resource for 2 clock cycles then the another 2 clock cycles can be allocated to the next requester. Hence saving the time

Verilog HDL Design of Round Robin Arbiter (Variable Time Slices)

Verilog HDL Design and Test-Bench Simulation:

We will be using **EDA Playground (https://www.edaplayground.com)** to design Fixed Priority Round Robin Arbiter in Verilog HDL.

Synthesis using Open Source Synthesis Tool : **Yosys** (Available in EDA Playgound)

Simulation using Open Source Simulation Tool : **Riviera** (Available in EDA Playground)

Verilog Project Link

If you find the video content valuable, Please do not forget to hit the 

Also, please do subscribe and enable the notification to get notified for next such designs

I would appreciate your suggestions, any queries and any digital design you would like to understand starting from circuit to HDL design. Please write them down in the comment section !!!

Thank You !!!