Verilog HDL Design, Simulation & Synthesis of an Event Detector in Verilog HDL

Video Lecture – Circuit Design Link

Video Lecture – Verilog Design Link

Design of an Event Detector

- Event Detector (Explanation)
- Circuit Diagram
- Verilog HDL Design
- Synthesizing the Design
- Test Bench Design
- Analysing Simulation Waveforms

Design of a Event Detector

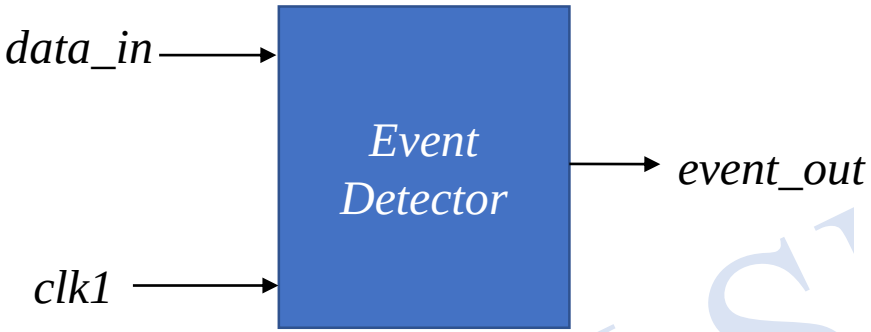


Figure #01: Event Detector Block Diagram

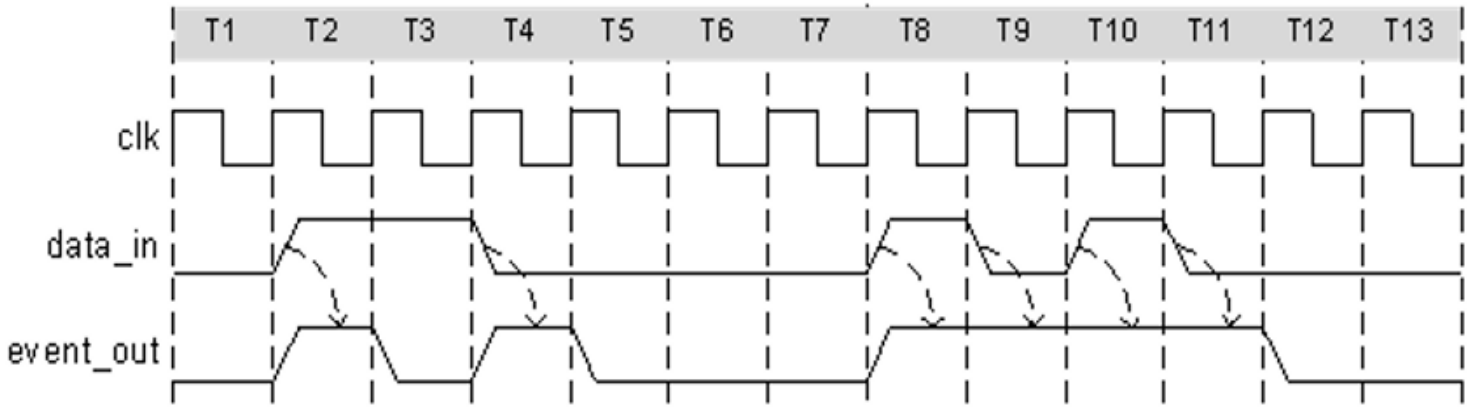
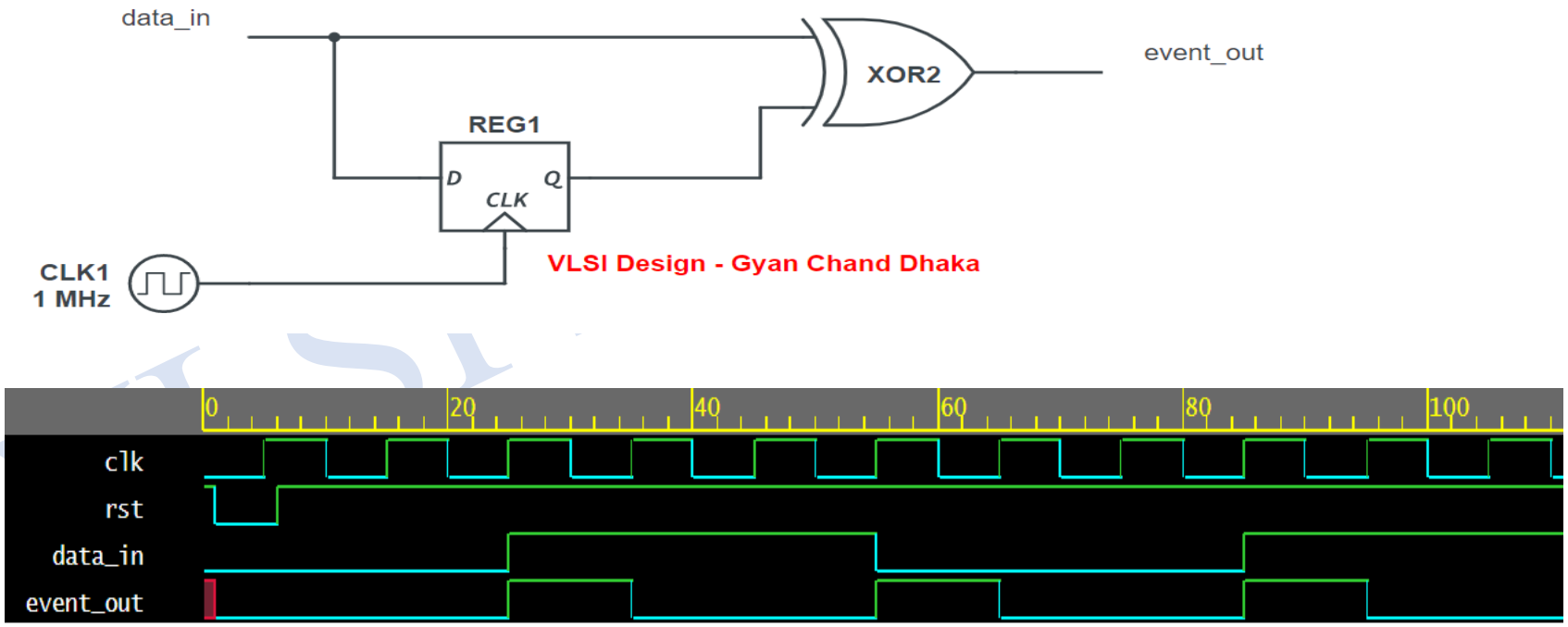


Figure #02: Event Detector Waveform

Design of a Event Detector

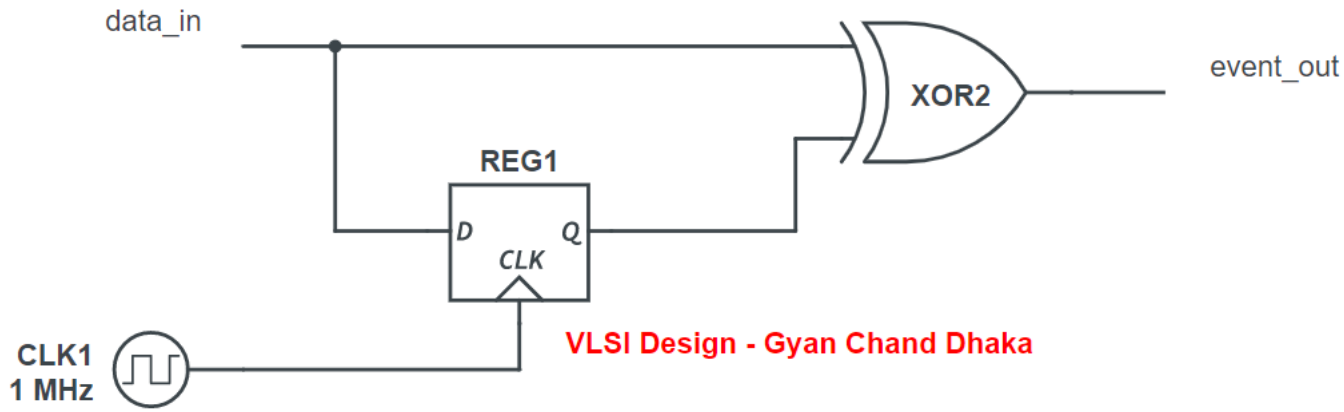
2 Scenarios : The data_in can be Async OR Sync to the CLK1 Domain

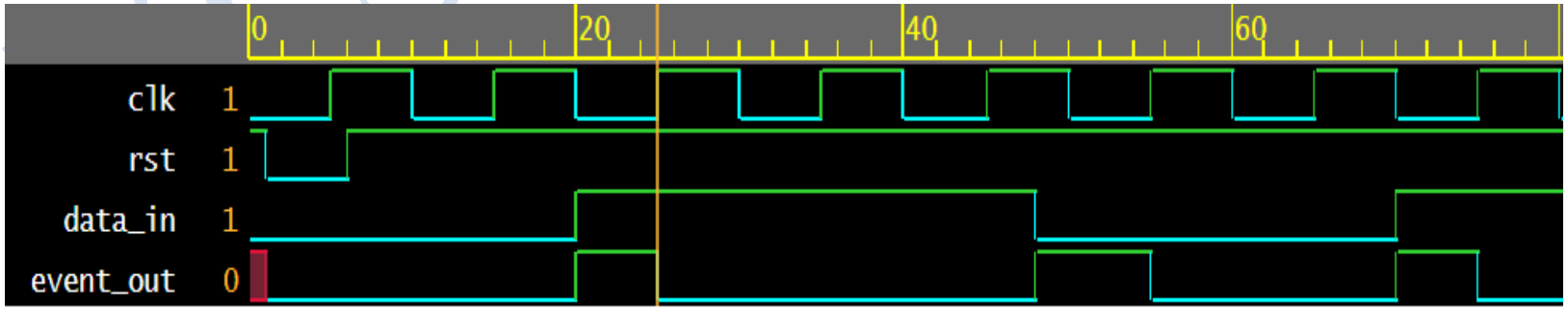
Sync Data Input –



Design of a Event Detector

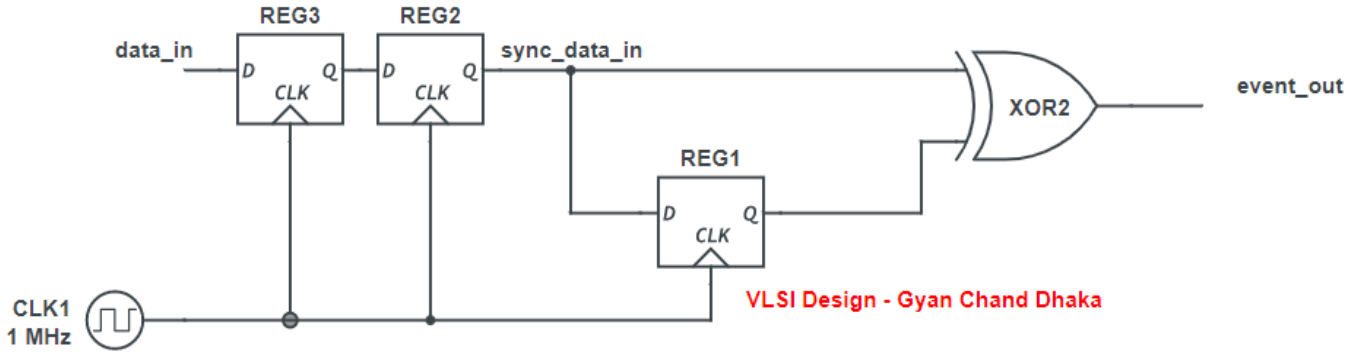
Async Data Input –

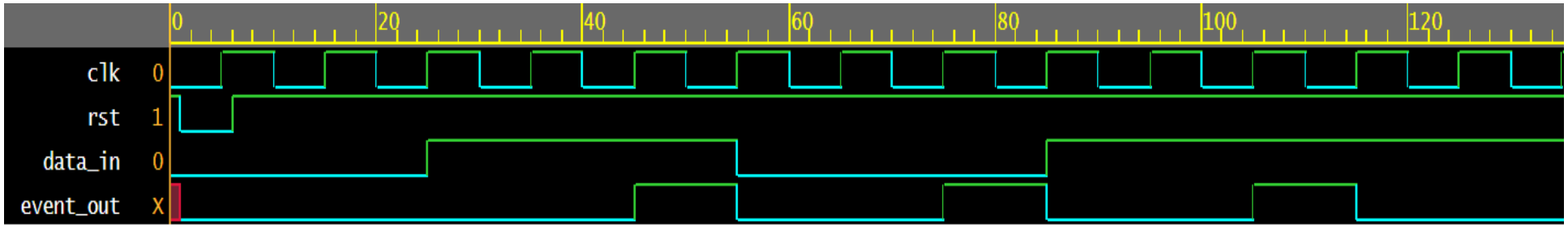




Design of a Event Detector

Async Data Input – Sync in CLK1 Domain





Design of a Event Detector

Verilog HDL Design and Test-Bench Simulation:

We will be using **EDA Playground (https://www.edaplayground.com)** to design Fixed Priority Round Robin Arbiter in Verilog HDL.

Synthesis using Open Source Synthesis Tool : **Yosys** (Available in EDA Playgound)

Simulation using Open Source Simulation Tool : **Riviera** (Available in EDA Playground)

Verilog Project Link(No Input Data Synchronization)

Verilog Project Link(With Input Data Synchronization)

Design of a Event Detector

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I would appreciate your suggestions, any queries and any digital design you would like to understand starting from circuit to HDL design. Please write them down in the comment section !!!

Thank You !!!