

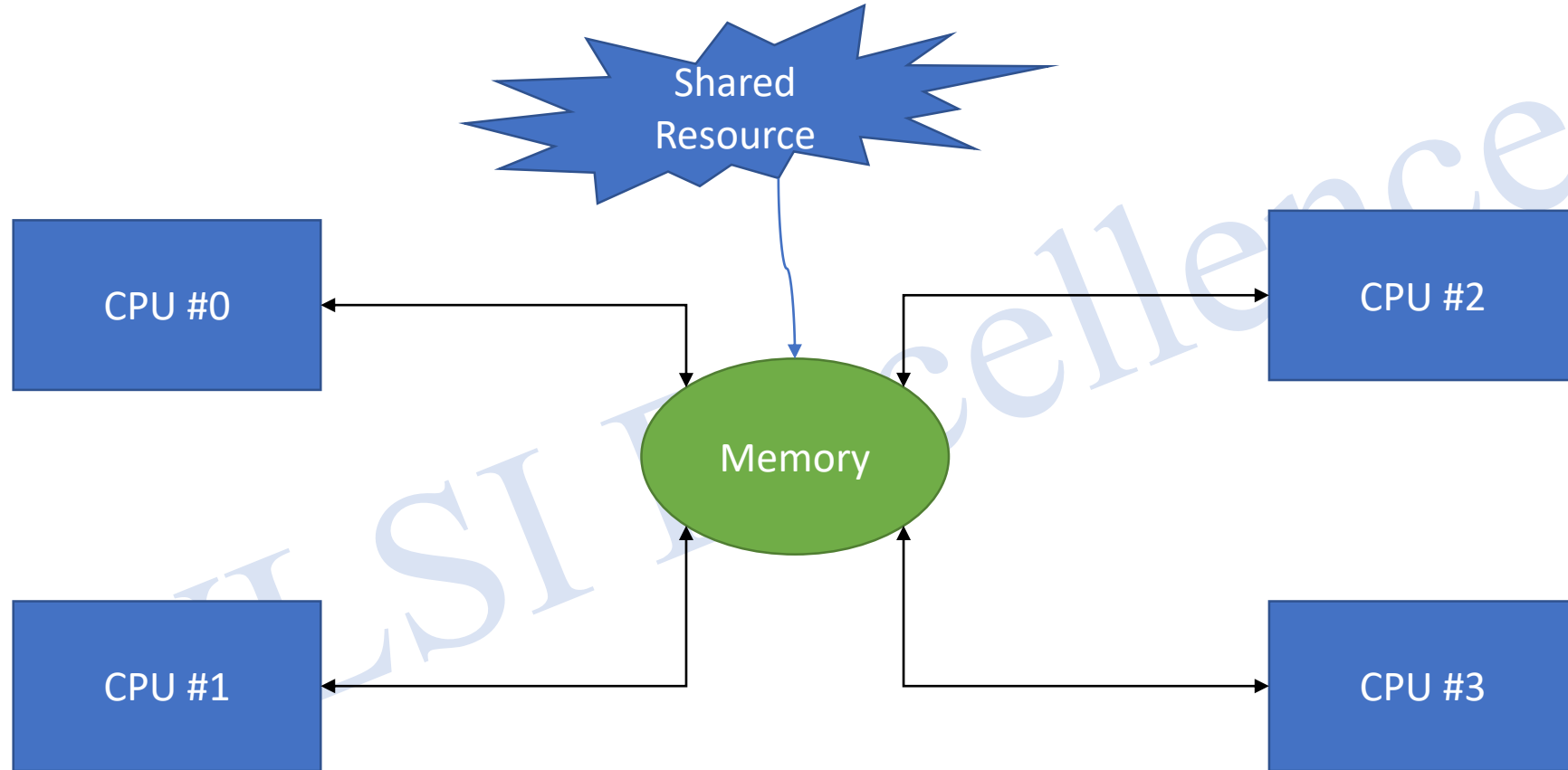
# Verilog HDL Design, Simulation & Synthesis of Fixed Priority Arbiter

*Video Lecture [Link](#)*

# Verilog HDL Design of Fixed Priority Arbiter

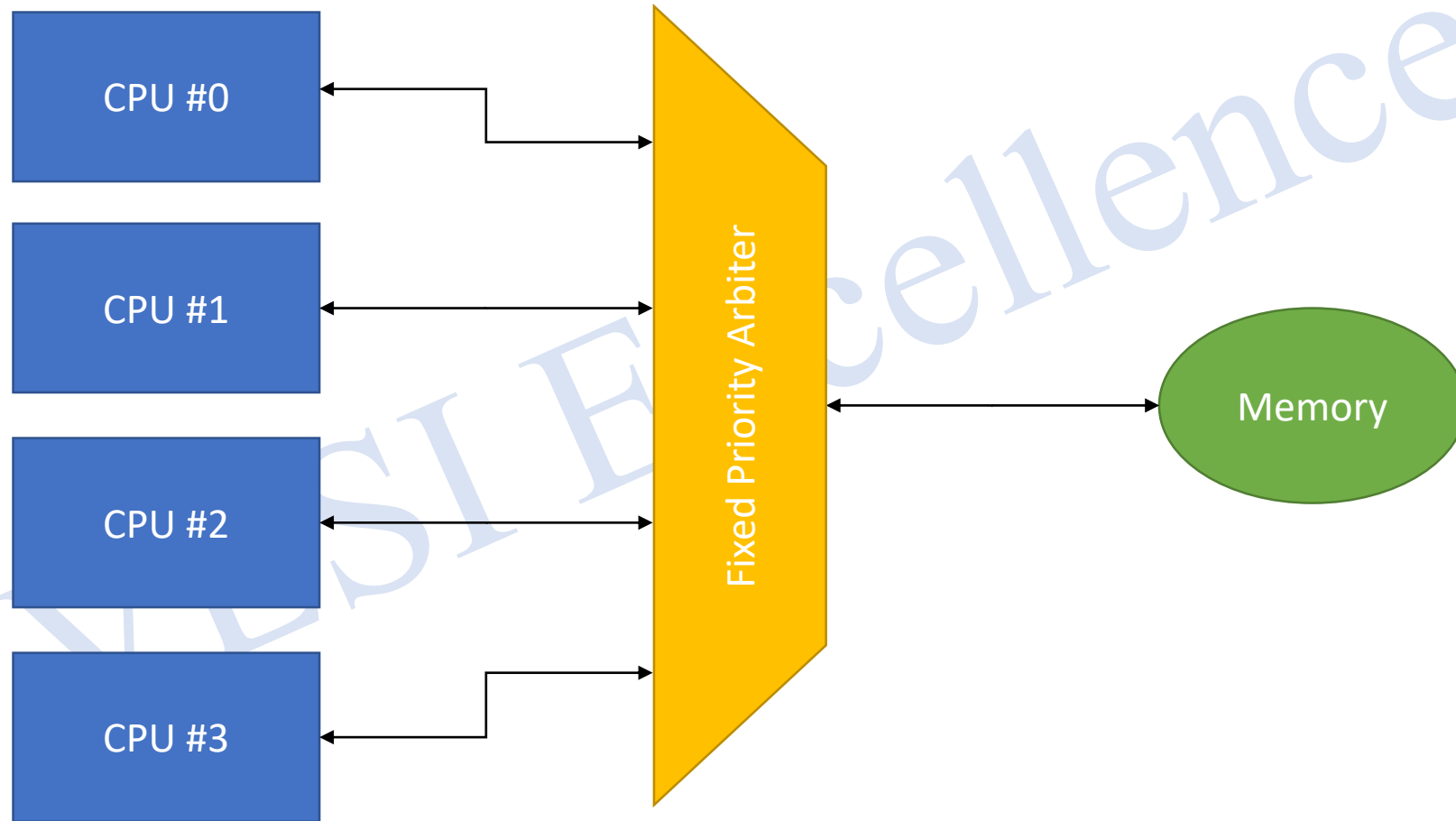
- ❑ What is an Arbiter ?
- ❑ Applications/ Examples
- ❑ Advantages/Disadvantages
- ❑ Verilog HDL Design
- ❑ Synthesizing the Design
- ❑ Test Bench Design
- ❑ Analysing Simulation Waveforms

# Verilog HDL Design of Fixed Priority Arbiter



*Figure #01: Shared Resource Access by 4 CPUs*

## Verilog HDL Design of Fixed Priority Arbiter



*Figure #02: Application of Arbiter in Accessing Shared Resource*

## Verilog HDL Design of Fixed Priority Arbiter

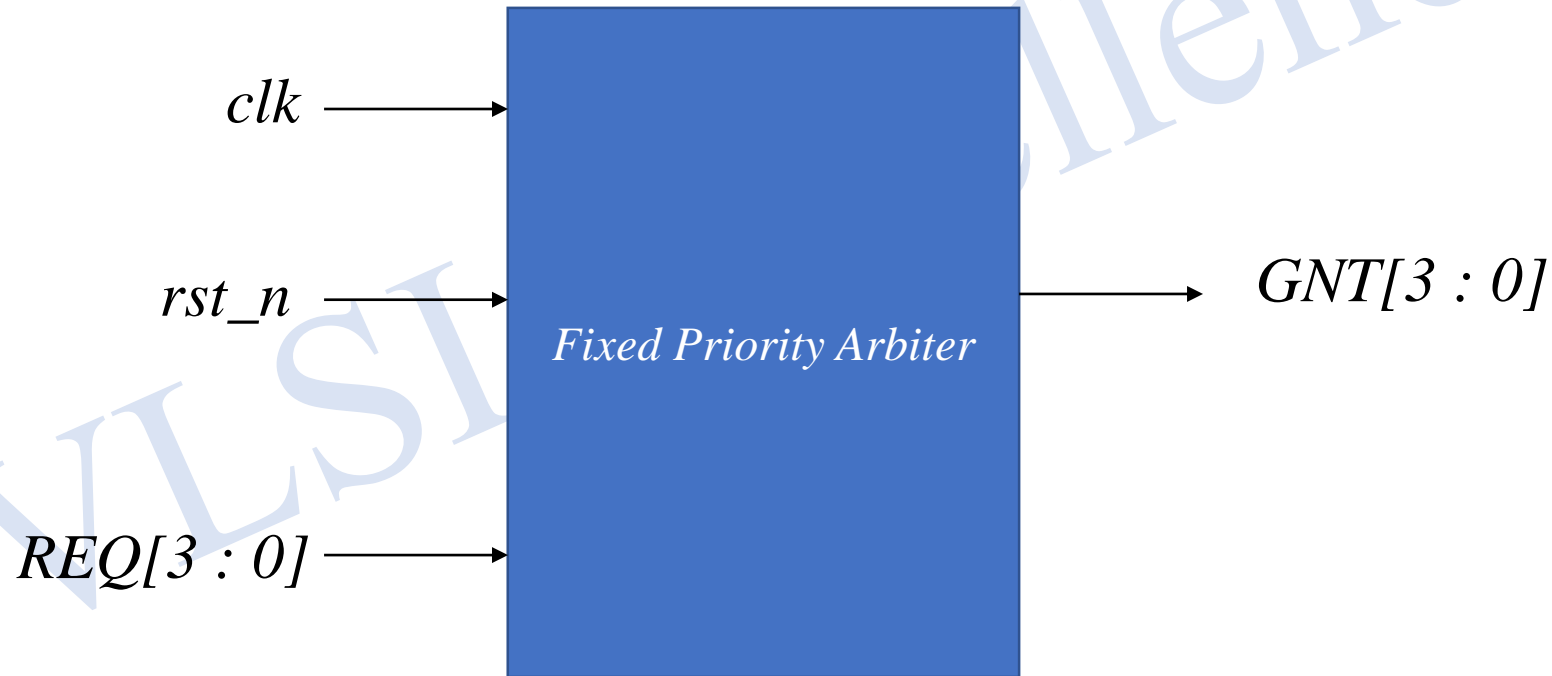


Figure #03: Arbiter Block Diagram

# Verilog HDL Design of Fixed Priority Arbiter

## Applications/Examples :

1. Accessing a memory location by multiple process
2. Routers where users are competing for a switch

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# Verilog HDL Design of Fixed Priority Arbiter

## Advantages and Disadvantages of Fixed Priority Arbiter

### **Advantage:**

We can give preference to a particular requester

### **Disadvantage:**

When a high priority requester keeps requesting frequently for a resource, it will result in **Starvation** of requesters with low priority

Note:

Solution for a Starvation free Arbiter : Round Robin Arbiter

# Verilog HDL Design of Fixed Priority Arbiter

## Specification:

1. The arbiter takes 4 input requests and outputs a single grant in the form of ONE HOT
2. Priority of requests are  $REQ[3] > REQ[2] > REQ[1] > REQ[0]$



# Verilog HDL Design of Fixed Priority Arbiter

Verilog HDL Design and Test-Bench Simulation:

We will be using **EDA Playground** (<https://www.edaplayground.com>) to design Fixed Priority Round Robin Arbiter in Verilog HDL.

**Synthesis** using Open Source Synthesis Tool : **Yosys** (Available in EDA Playground)

**Simulation** using Open Source Simulation Tool : **Riviera** (Available in EDA Playground)

*Verilog Project [Link](#)*

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