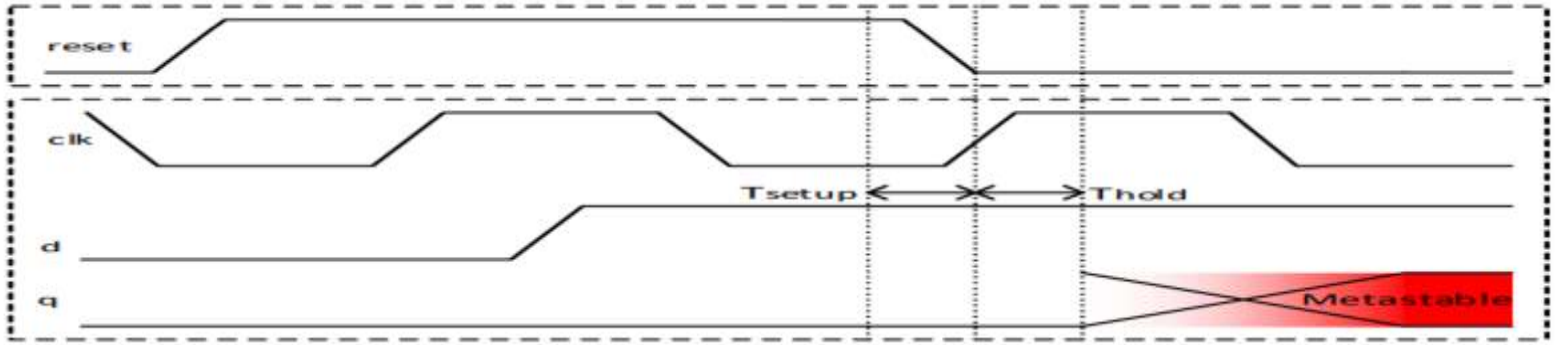
VDD Based Reset Synchronizer

Video Lecture Link

Asynchronous Reset Design Technique

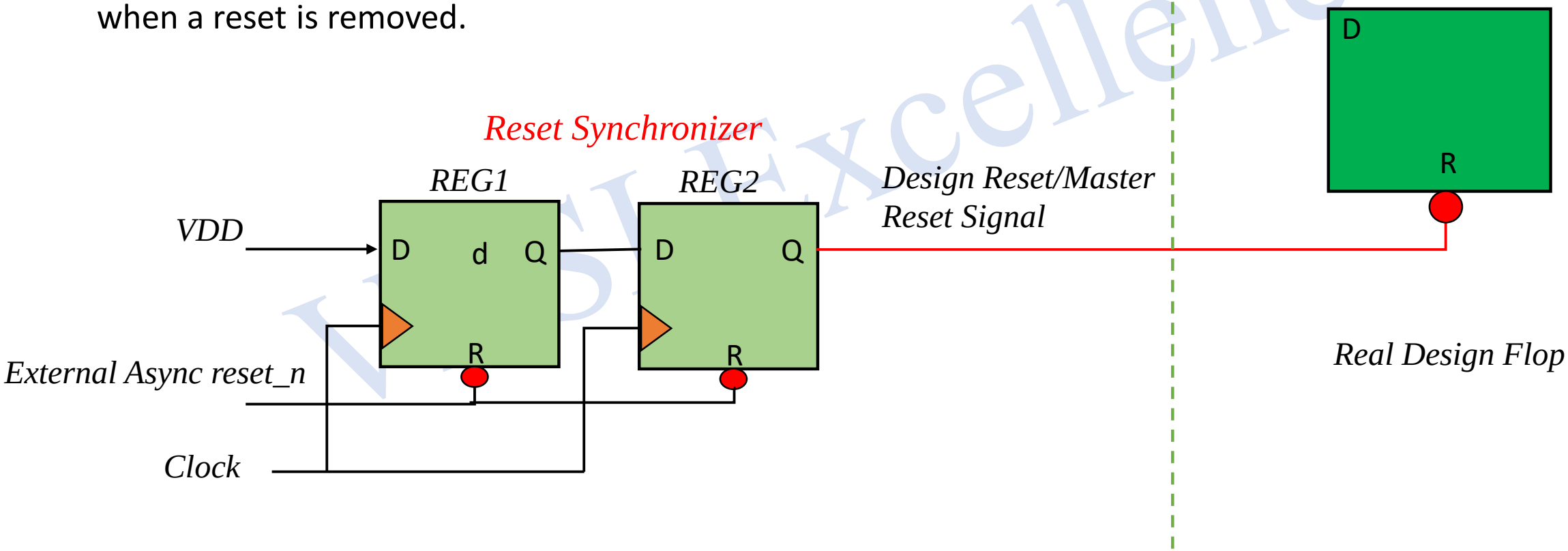
1. The primary disadvantage of using an asynchronous reset is that the reset is asynchronous both at the assertion and de-assertion of the signal.
2. The signal assertion is not the problem on the actual connected flip-flop. Even if the flip-flop moves to a metastable state, the flip-flop remains unstable only for a short period of time after assertion. After reset asserts long enough, all registers eventually settle to a reset state.
3. The problem of the asynchronous reset involves the signal de-assertion. If an asynchronous reset releases at or near the active clock edge, the output of the flipflop could go to a metastable state, violating the reset recovery time of the flip-flop. The flip-flop then goes to an unknown state that can cause unexpected results upon entering normal operation.



Reset De-assertion Issue Causing Metastability

VDD – Based Reset Synchronizer

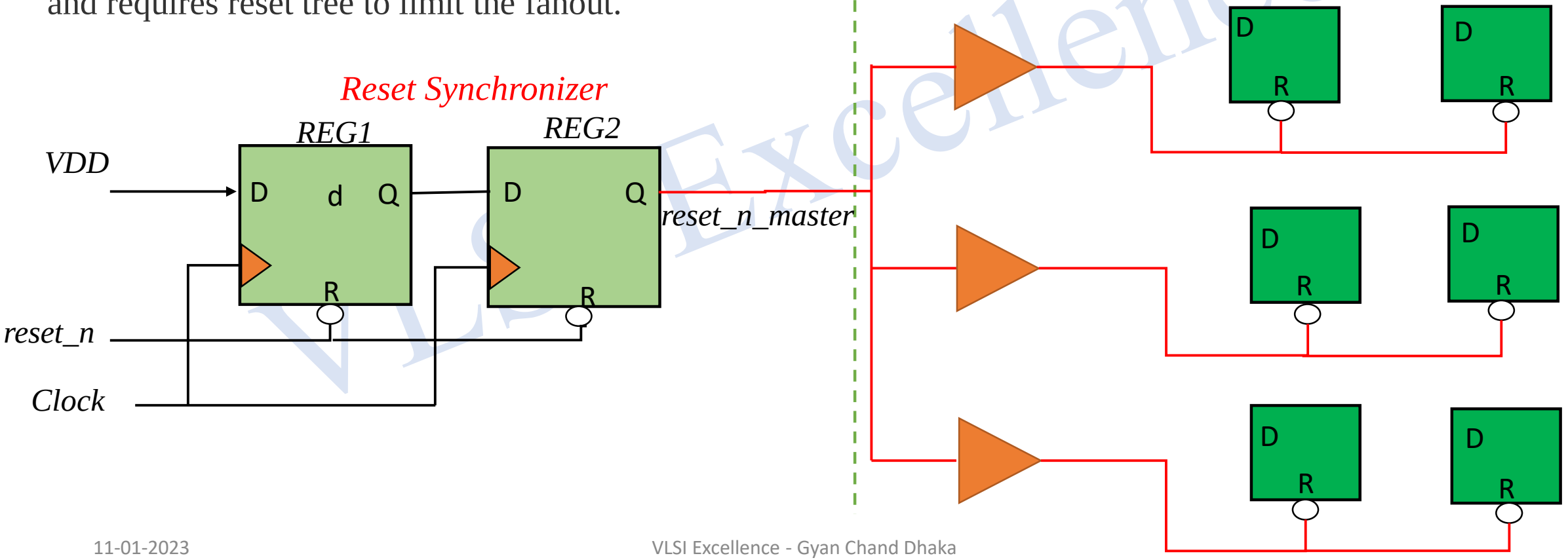
We can insert a synchronously de-asserted reset circuit to prevent this condition. Synchronization of the reset signal on a specific clock domain requires a minimum of two flops. Below circuit shows the first flip-flop (REG1) with output Q reset to 0, and input D tied high. This flip-flop can go to a metastable state if reset_n is de-asserted near a Clock active edge. However, the second flip-flop (REG2) remains stable at 0, since the input and output are both low, preventing any output change due to the input that might occur when a reset is removed.



Reset Tree (Need & Implementation)

Using the VDD-based reset synchronizer, we can generate the main source (reset_n_master) for the asynchronous reset. The reset is typically a high fan-out net. Implement a reset tree to maintain a good fan-out load to help meet the recovery and removal checks on driven registers during de-assertion. (Maintains a sharp slew)

Reset timing closure (reset recovery and removal timing) becomes challenging with high clock frequencies and requires reset tree to limit the fanout.



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