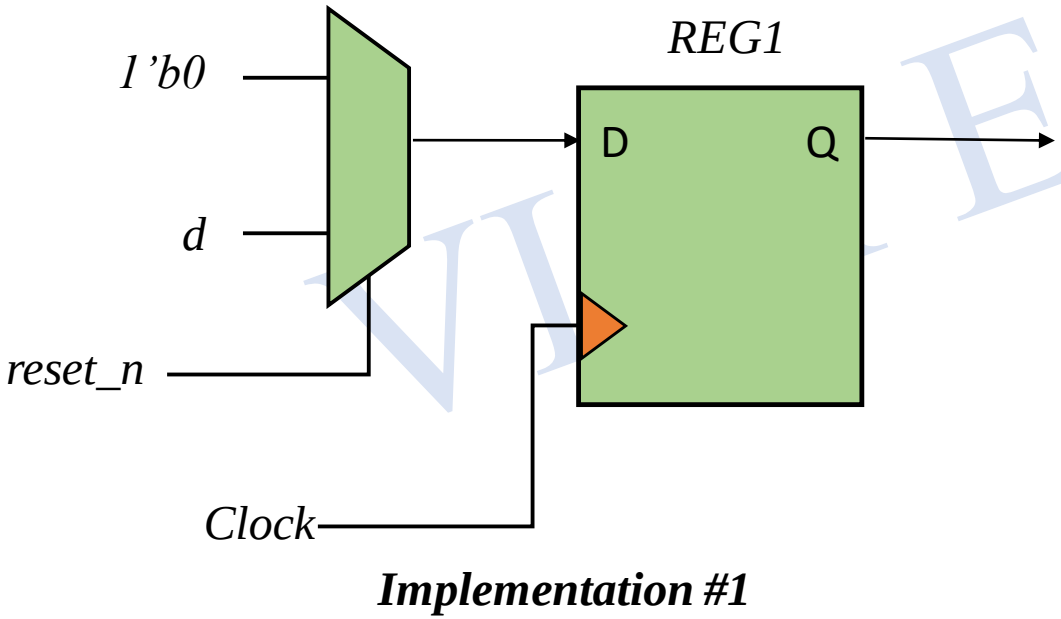
Synchronous V/S Asynchronous Reset
&
Best Reset Design Approach

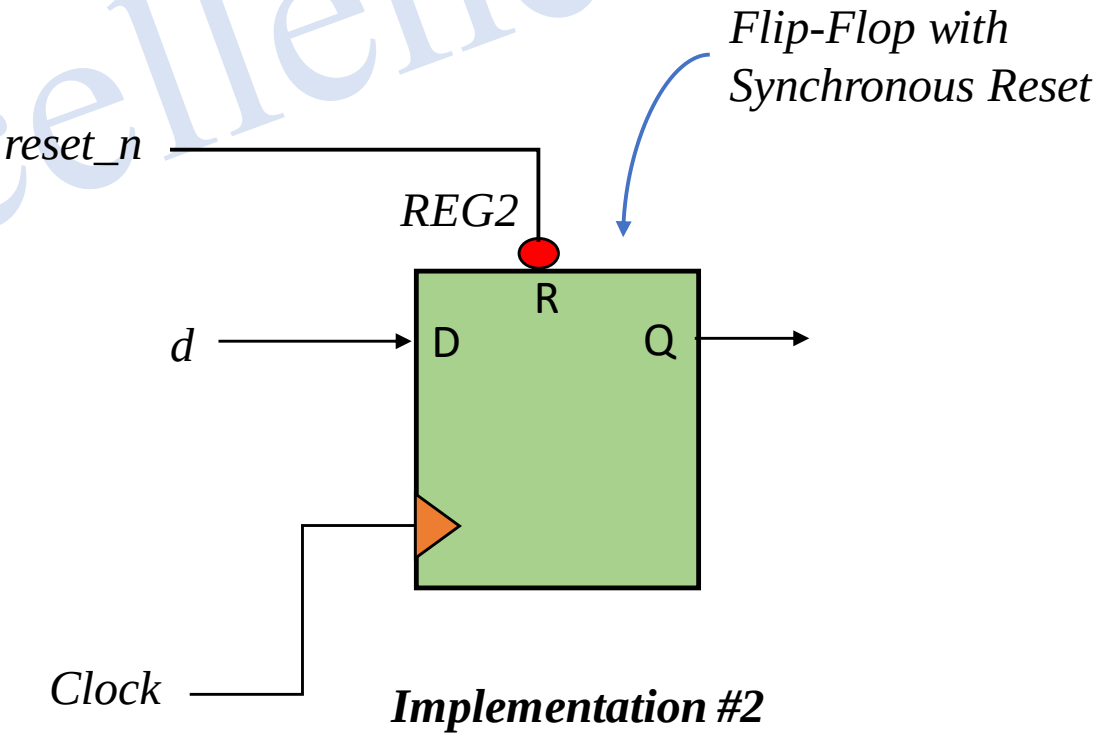
Video Lecture Link

Synchronous Reset

- Reset Signal will only reset the state of the flip-flop on the active edge of the clock signal
- *always @(posedge clock)*
  if(!reset_n)
  q <= 1'b0;
  else
  q <= d;



Implementation #1



Implementation #2

Synchronous Reset

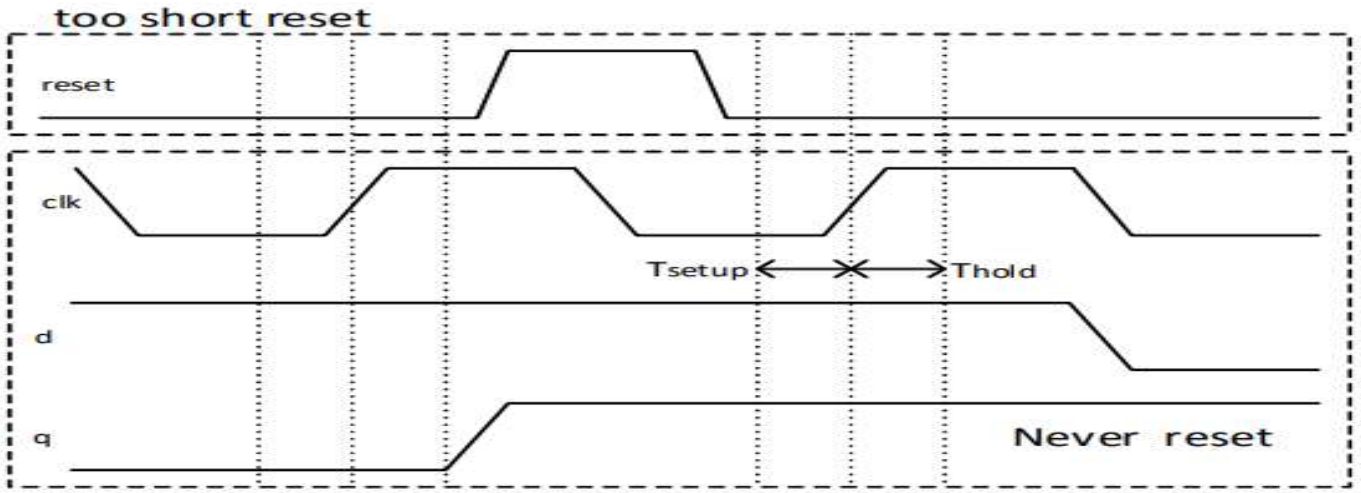
Advantages of Synchronous Reset –

1. Synchronous reset insures that the reset can occur at an active clock edge and hence small reset glitches can be eliminated !!!
2. When the reset is generated by design internal conditions, a synchronous reset is recommended for these types of designs because it will filter the glitches caused by combinational logic equations (Combinational Logic is always prone to GLITCHES because of Logic Gate Delays)
3. Synchronous reset generally insures that the design is 100% synchronous
4. In cycle based simulations, it is easy to work with synchronous resets
5. By using synchronous resets and a number of clocks as part of the reset process, flip-flops can be used within the reset buffer tree to help the timing of the buffer tree keep within a clock period.

Synchronous Reset

Disadvantage of Synchronous Reset –

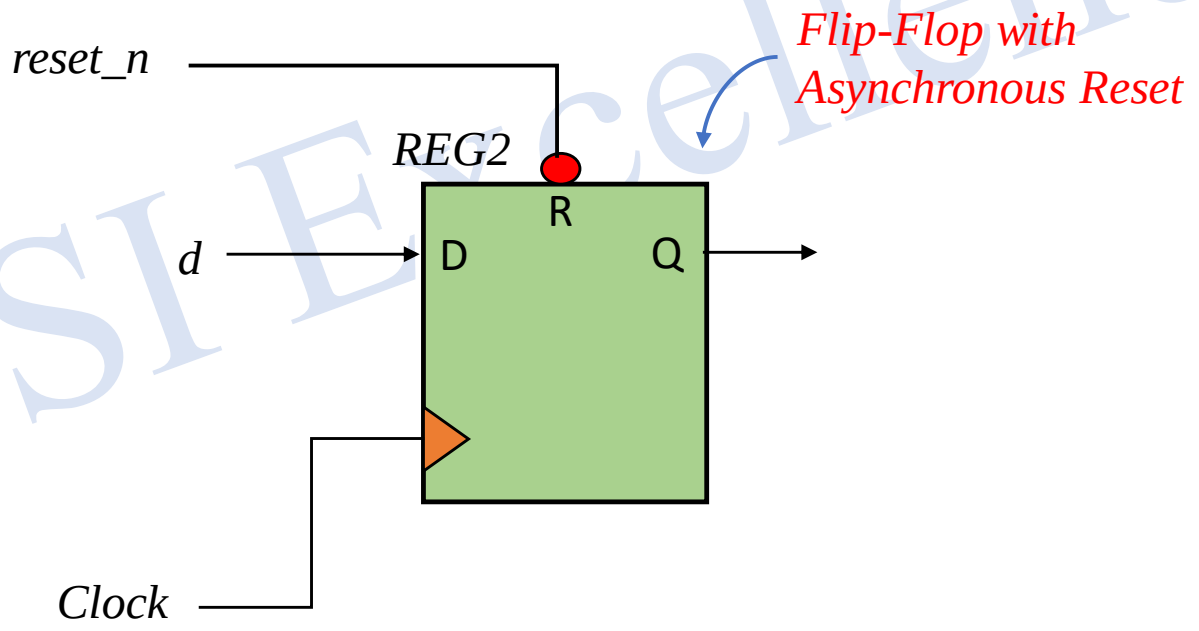
1. A synchronous reset requires a clock signal to reset the design
2. Design should ensure that a reset pulse width should be wide enough to ensure reset is present during an active edge of the clock
3. Extra logic added in the Datapath to handle synchronous reset (Causes data path timing issue)



Asynchronous Reset

- Reset Signal does no require an active clock signal to reset the state of the flip-flop
- *always @(posedge clock or negedge reset_n)*

```
if(!reset_n)
    q <= 1'b0;
else
    q <= d;
```



Implementation #1

Asynchronous Reset

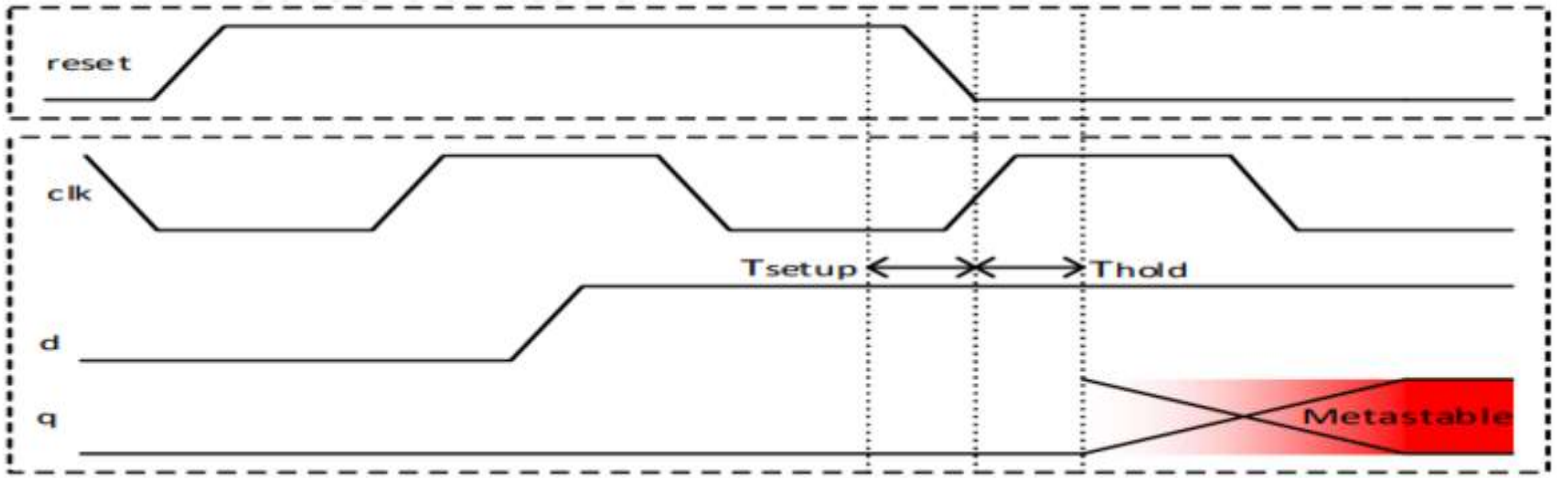
Advantages of Asynchronous Reset –

1. The circuit can be reset with or without a clock signal (Design can be put in a known state)
2. No extra logic added in the Datapath unlike it is done to handle synchronous reset (Avoids any data path timing issue)
3. No reset signal added in the Datapath logic
4. Reset is free from clock signal and hence will get applied always

Asynchronous Reset

Disadvantages of Asynchronous Reset –

1. Asynchronous resets are asynchronous both at reset assertion and reset de-assertion, If the asynchronous reset is released at or near the active edge of the flip-flop clock , the output of the flip-flop could go metastable and thus the reset state of the Design is lost !! The flip-flop then goes to an unknown state that can cause unexpected results upon entering normal operation.



Reset De-assertion Issue Causing Metastability

Asynchronous Reset

Disadvantages of Asynchronous Reset –

2. Prone to noise or glitches. Unwanted Reset pulse can occur
3. Makes it difficult for cycle based simulations

Note: The signal assertion is not the problem on the actual connected flip-flop. Even if the flip-flop moves to a metastable state, the flip-flop remains unstable only for a short period of time after assertion. After reset asserts long enough, all registers eventually settle to a reset state.

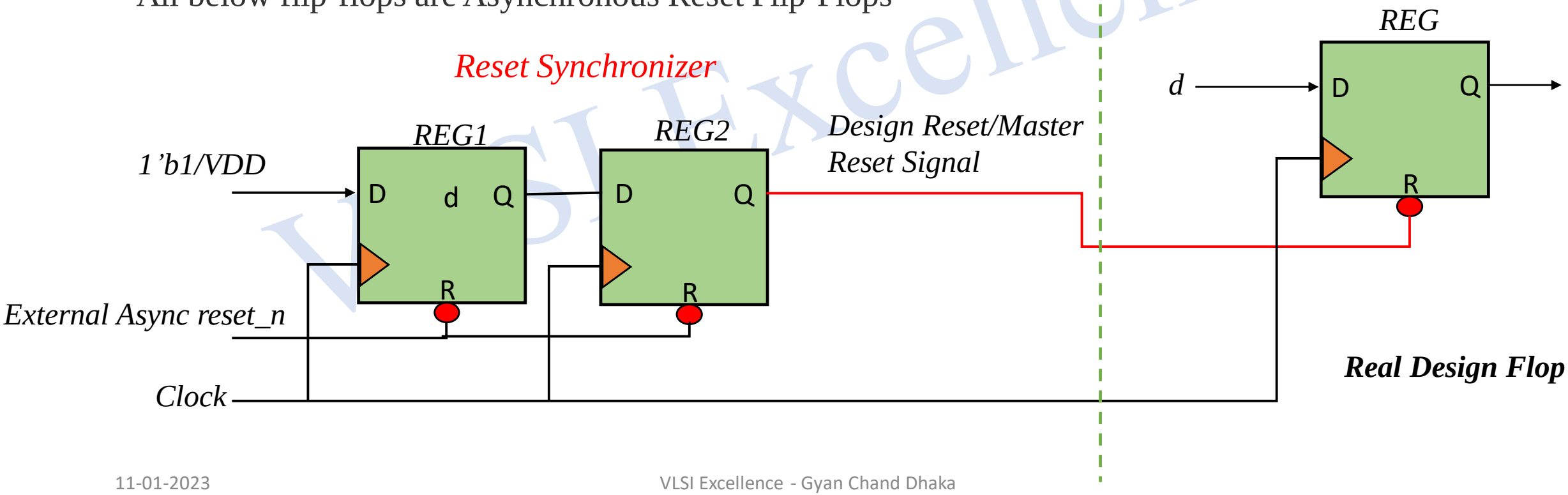
Best Reset Design Approach

Asynchronous Assertion & Synchronous De-assertion-

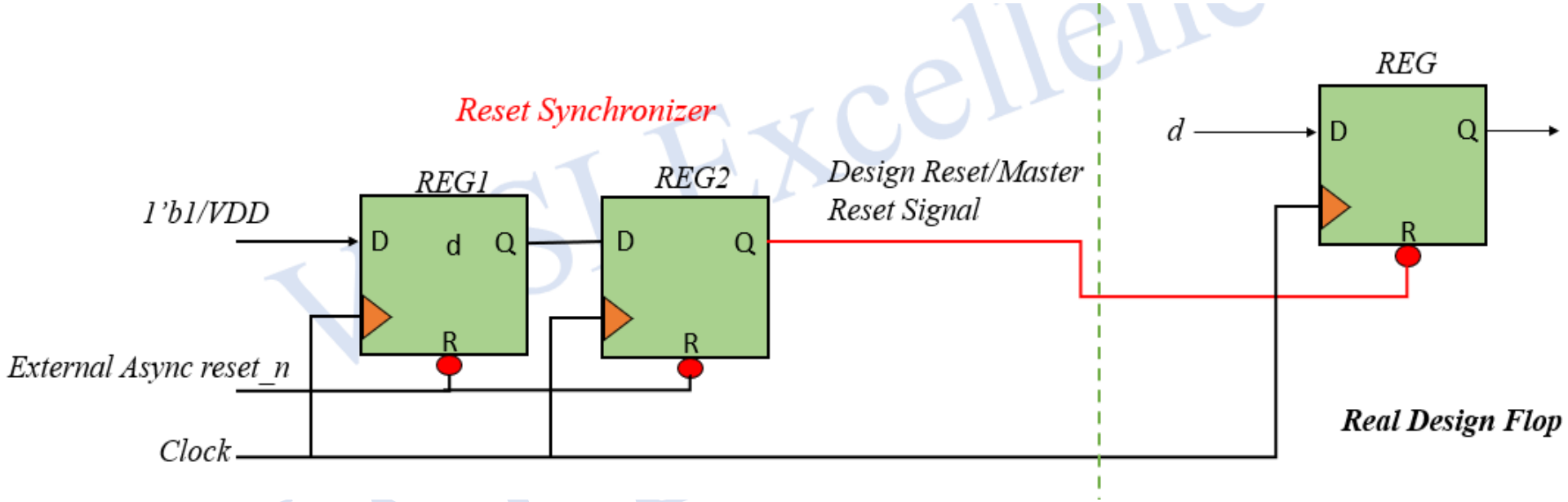
We can insert a synchronously de-asserted reset circuit to prevent this condition.

Synchronization of the reset signal on a specific clock domain requires a minimum of two flops.

- Short reset pulse will reset the design or will put the design in known state during Reset assertion
- 2-DFF mitigated metastability problems during Reset de-assertion
- All below flip-flops are Asynchronous Reset Flip-Flops



Best Reset Design Approach (Async Assertion & Sync De-assertion)



- This flip-flop can go to a metastable state if RSTB is de-asserted near a CLK active edge. However, the second flip-flop (FF2) remains stable at 0, since the input and output are both low, preventing any output change due to the input that might occur when a reset is removed.

Best Free VLSI Content

1. Verilog HDL Crash Course – Link
2. Static Timing Analysis (STA) – Theory Concepts – Link
3. Static Timing Analysis (STA) – Practice/Interview Questions – Link
4. Low Power VLSI Design – Theory Concepts – Link
5. Low Power VLSI Design (LPVLSI) – Practice/Interview Questions – Link
6. Digital ASIC Design Verilog Projects – Link

Please Like, Comment, Share & Subscribe My Channel in Order to Reach Out the Content to a Larger Audience.

Thanks !!