Low Power VLSI Design Concepts

Video Lecture Link

Low Power VLSI Design

Introduction:

- During Desktop PC design era VLSI design efforts were mainly focused on optimizing speed to realize computationally intensive real time functions such as video compressing , graphics, gaming etc.
- While these solutions have addressed the real time issues still the increasing demand of portable operations where the mobile needs to pack all these functions without operating much power is unaddressed
- The strict limitation on power dissipation in portable electronics applications such as smart phones and tablet computers must be met by the VLSI chip designer while still meeting the computational requirements.
- Hence the most important factor while designing SOC for portable devices is '**Low Power VLSI Design**'

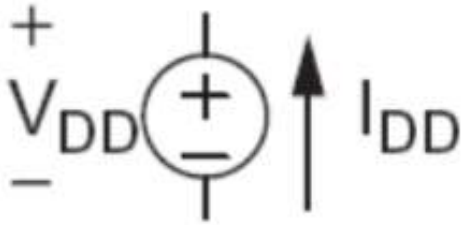
Why Power Matters in SOC?

- Power Management matter in System on Chip due to following concerns-
  a. Packaging and Cooling costs.
  b. Digital noise immunity,
  c. Battery life (in portable systems)
  d. Environmental concerns.

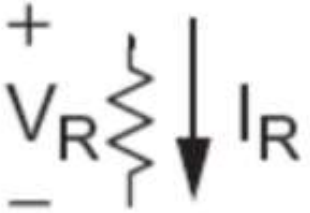
Note: This Episode Covers Low Power Concepts Associated with Circuit Design and Not with Device Fabrication !!!

Power in Circuit Elements

$$P_{VDD}(t) = I_{DD}(t)V_{DD}$$

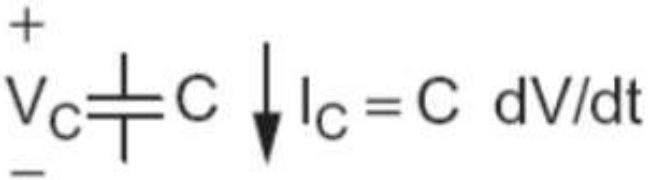


$$P_R(t) = \frac{V_R^2(t)}{R} = I_R^2(t)R$$



$$E_C = \int_0^{\infty} I(t)V(t)dt = \int_0^{\infty} C\frac{dV}{dt}V(t)dt$$

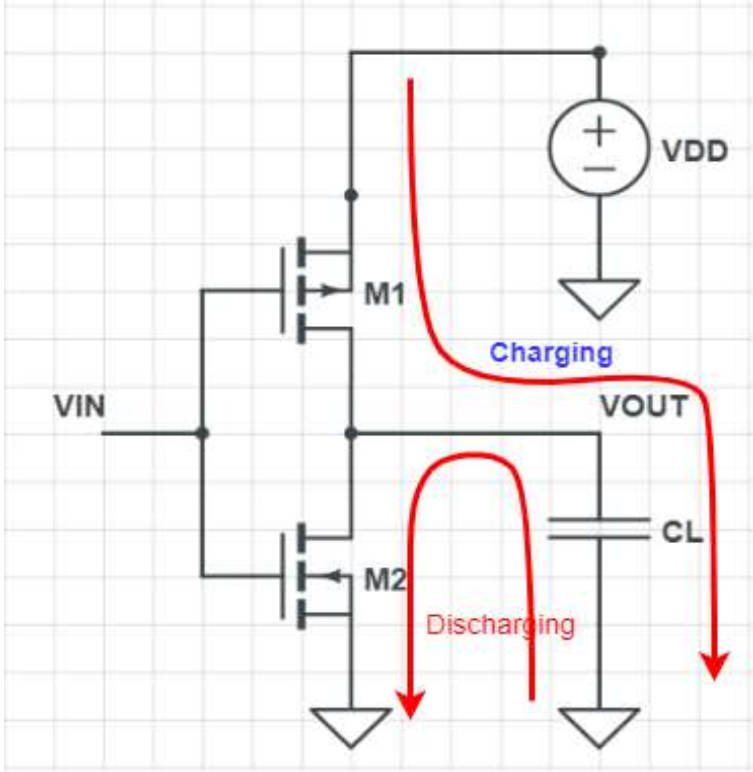
$$= C\int_0^{V_C} V(t)dV = \tfrac{1}{2}CV_C^2$$



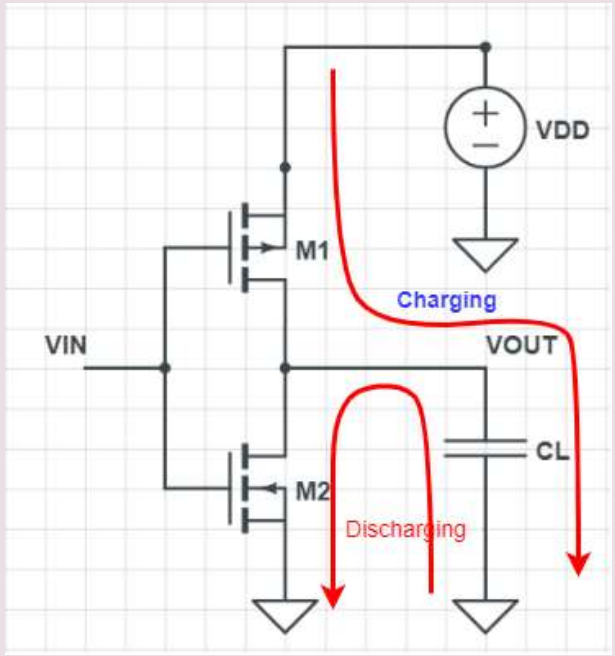
Sources of Power Dissipation in CMOS Circuits?

- The power dissipation in circuit can be classified into three categories as described below-

I) **Dynamic Power Dissipation** ($P_{Dynamic}$): Due to logic transitions causing logic gates to charge/discharge load capacitance.



Charging a Capacitor



$$E_{VDD} = \int_0^\infty I(t) V_{DD} dt = \int_0^\infty C_L \frac{dV}{dt} V_{DD} dt$$
$$= C_L V_{DD} \int_0^{V_{DD}} dV = C_L V_{DD}^2$$

$$E_C = \frac{1}{2} C_L V_{DD}^2$$

- When the Gate output rises –
  - Energy drawn from the supply needed to charge up the capacitor is – E_{VDD}
  - Energy stored in capacitor is - E_C
  - Half the energy from VDD is dissipated in the pMOS transistor as heat, other half stored in capacitor
- When the gate output falls –
  - Energy in capacitor is dumped to GND – Dissipated as heat in the nMOS transistor

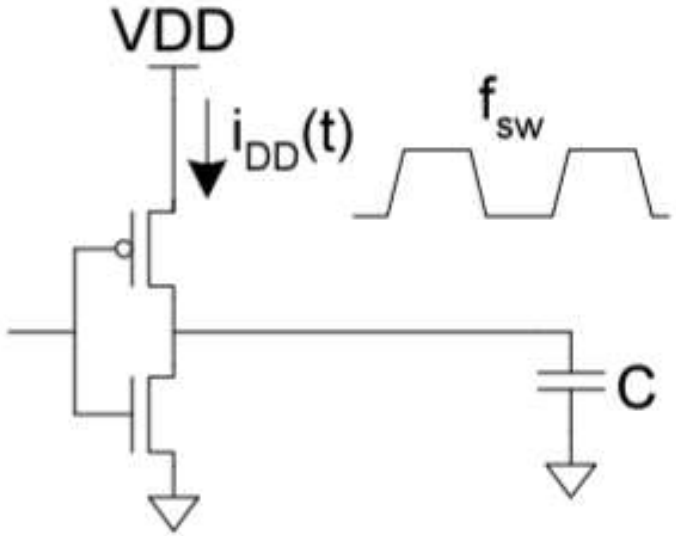
$P_{Dynamic}$

$P_{Dynamic} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\,dt$

$= \frac{V_{DD}}{T}\int_0^T i_{DD}(t)dt$

$= \frac{V_{DD}}{T} * [T f_{sw} V_{DD} C]$; f_{sw} -> Switching Frequency

$= CV_{DD}^2 f_{sw}$



Activity Factor/Switching Activity

- Suppose the system clock frequency = f

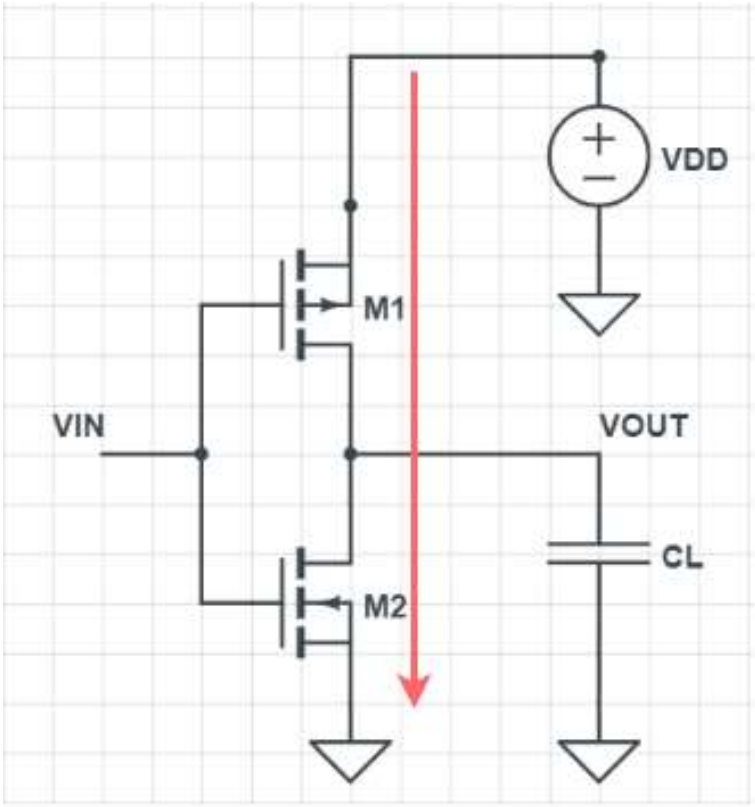
Let f_{sw} = αf, where α = activity factor

- If the signal is a clock, α = 1
- If the signal switches once per cycle, α = ½

- $P_{Dynamic} = \alpha(CV_{DD}^2 f_{sw})$

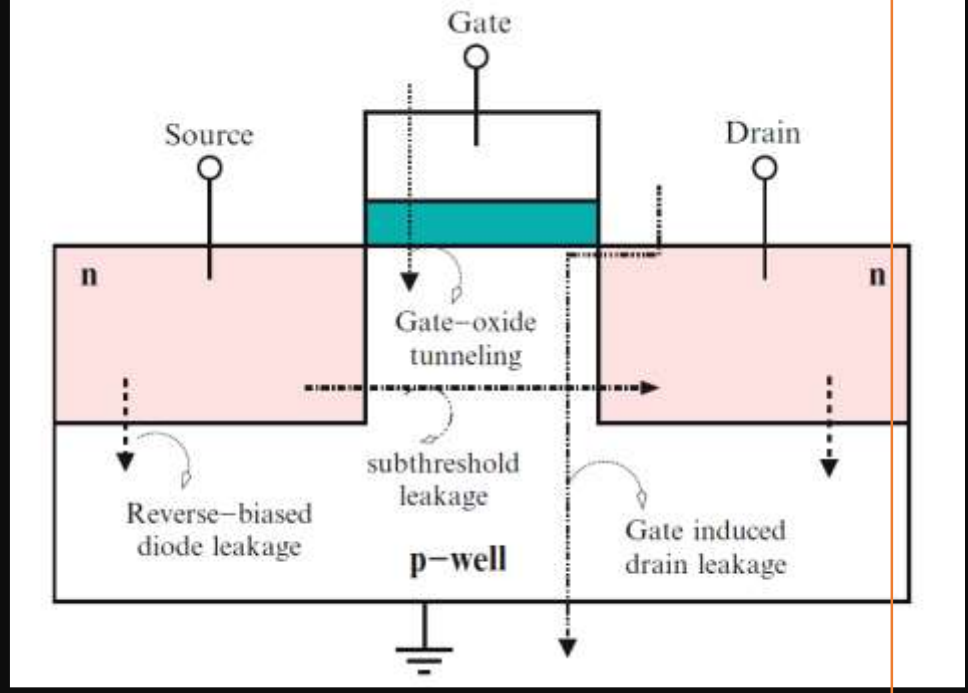
2) Short-Circuit Power Dissipation: In a CMOS logic P-branch and N-branch are momentarily shorted as logic gate changes state resulting in short circuit power dissipation.

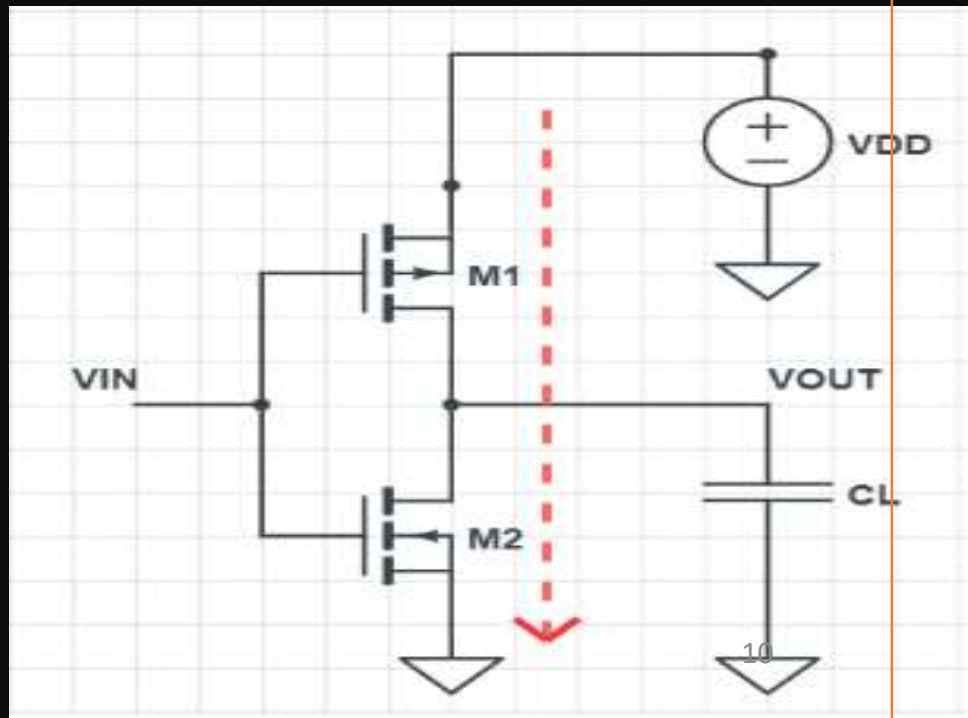
Short-circuit power becomes important because of finite non-zero rise and fall times of transistors, which causes a direct current path between the supply and ground.



3) Leakage Current Power Dissipation: This is the power dissipation that occurs when the system is in standby mode or not powered. There are many sources of leakage current in MOSFET. Diode leakages around transistors and n-wells, Subthreshold Leakage, Gate Leakage, Tunnel Currents etc. Increasing 20 times for each new fabrication technology. Insignificant issues are becoming dominating factors.

For technologies 1 μm and above , $P_{Switching}$ was predominant. However, for deep-submicron processes below 180nm, $P_{Leakage}$ becomes dominant factor.





Low-Power Design Techniques

An integrated low power methodology requires optimization at all design abstraction layers as mentioned below.

1. Circuit Logic: Logic Styles, Energy Recovery, Transistor Sizing
2. System: Partitioning, Power down
3. Algorithm: Complexity, Concurrency, Regularity
4. Architecture: Parallelism, Pipelining, Redundancy, Data Encoding
5. Technology: Threshold Reduction, Multithreshold Devices.

Dynamic power varies as V_{DD}^2. So reducing the supply voltage reduces power dissipation. Also selective frequency reduction technique can be used to reduce dynamic power. Multi threshold voltage can be used to reduce leakage power at system level. Transistor resizing can be used to speed-up circuit and reduce power. Sleep transistors which we will discuss in following tutorials can be used effectively to reduce standby power. Parallelism and pipelining in system architecture can reduce power significantly. Clock disabling, power-down of selected logic blocks, adiabatic computing, software redesign to lower power dissipation are the other techniques commonly used for low power design.

VLSI Circuit Design for Low Power

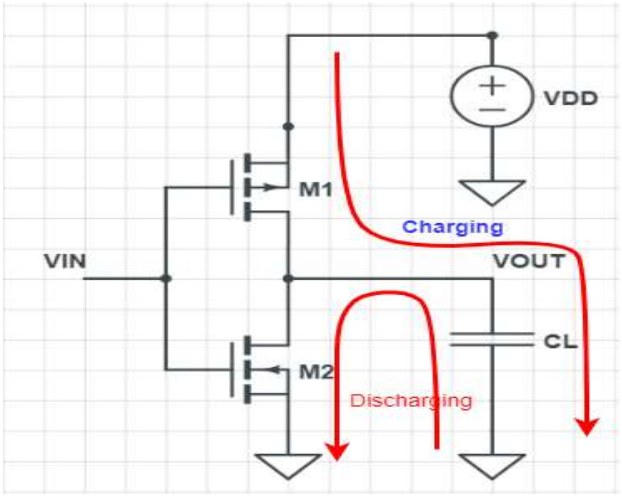
- Power optimization in a processor can be achieved at various abstract levels .
  System/Algorithm/Architecture have a large potential for power saving even these techniques tend to saturate as we integrate more functionality on an IC. So **optimization at Circuit and Technology** level is also very important for miniaturization of ICs.
- Total Power dissipated in a CMOS circuit is sum of dynamic power, short circuit power and static or leakage power.

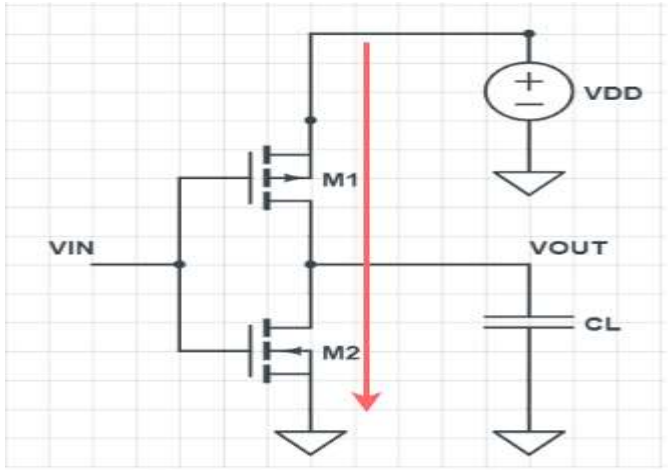
$$P_{total} = P_{dynamic} + P_{short\text{-}circuit} + P_{leakage}$$

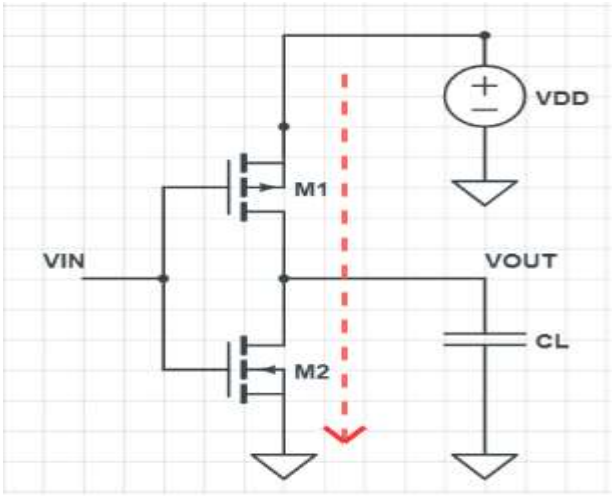
Input switching to ‘1‘ or ‘0’

$V_{Tn} < V_{IN} < (V_{DD} - |V_{Tp}|)$

Input ‘1’ or ‘0’ steady state







Dynamic Power

$(\alpha(CV_{DD}^2 f_{sw})$

Short Circuit Power

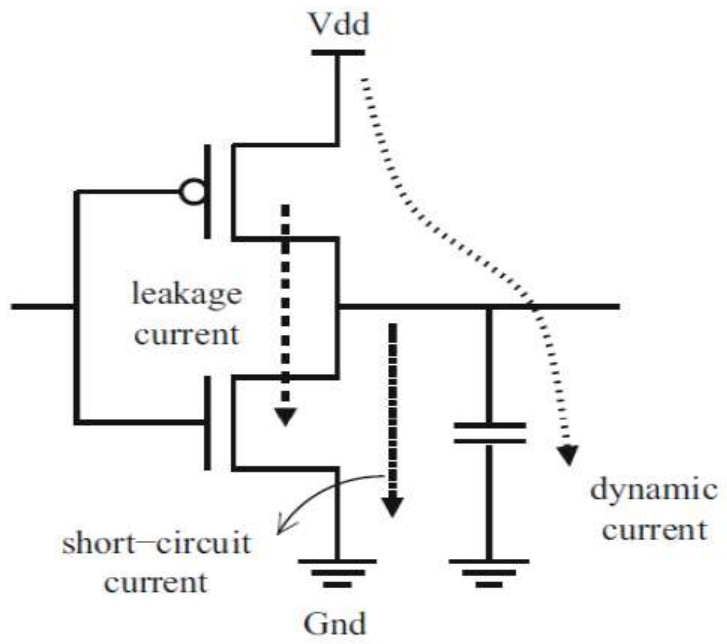
$(V_{DD} I_{SC})$

Leakage Power

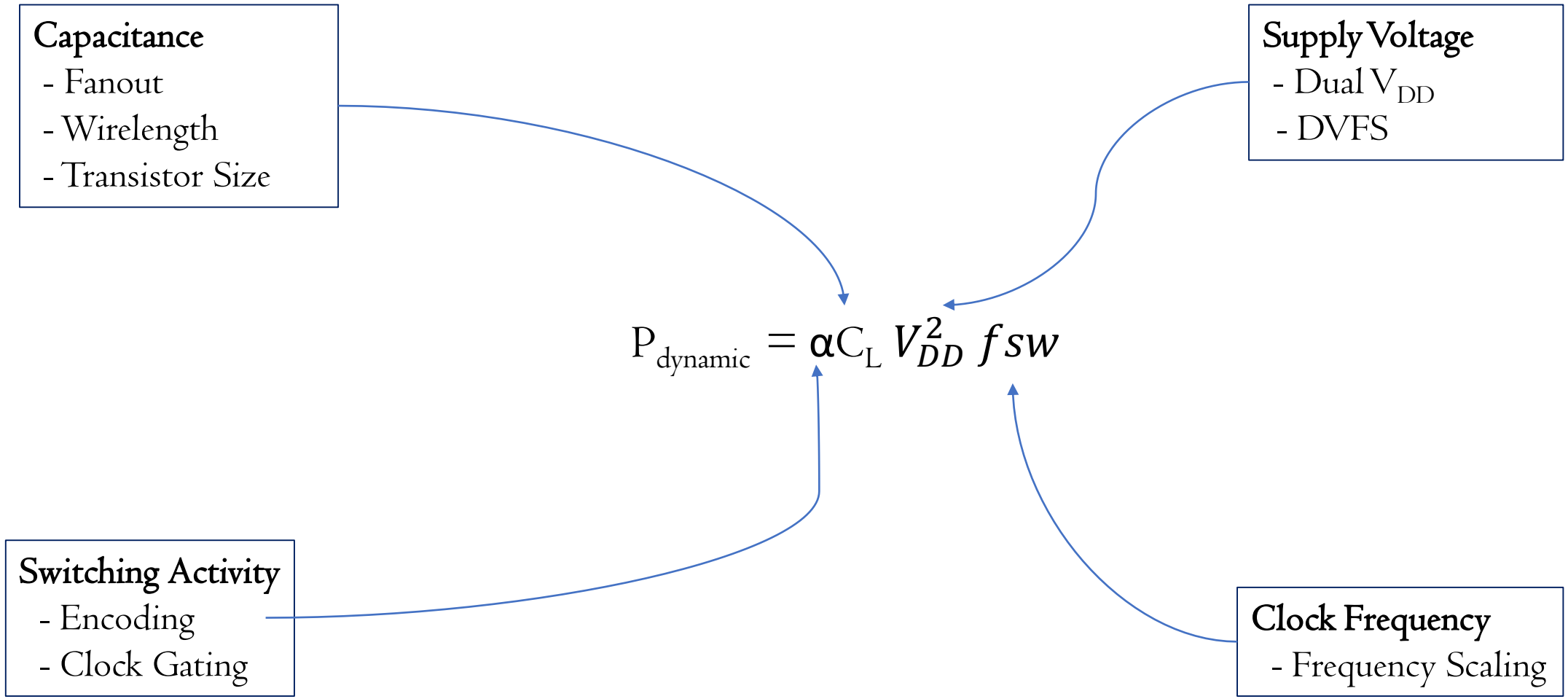
$(V_{DD} I_L)$

All Three Combined Components

The dynamic, short circuit and leakage power components of transistor power consumption. Dynamic and short circuit power are also collectively known as **switching power**, and are consumed when transistors change their logic state, but leakage power is consumed merely because the circuit is "**powered-on**".



Dynamic Power Suppression



Voltage and Frequency Scaling- Supply voltage scaling has been the most adopted approach to power optimization, since it normally yields considerable power savings due to the quadratic dependence of switching/dynamic power Pswitching on supply voltage V_{DD}. However lowering the supply voltage affects circuit speed which is the major short-coming of this approach.

Furthermore, since frequency is directly proportional to supply voltage, the frequency of the circuit can also be lowered, and thereby a cubic power reduction is possible.

Gate Sizing- The power dissipated by a gate is directly proportional to its load capacitive C_L, whose main components are:

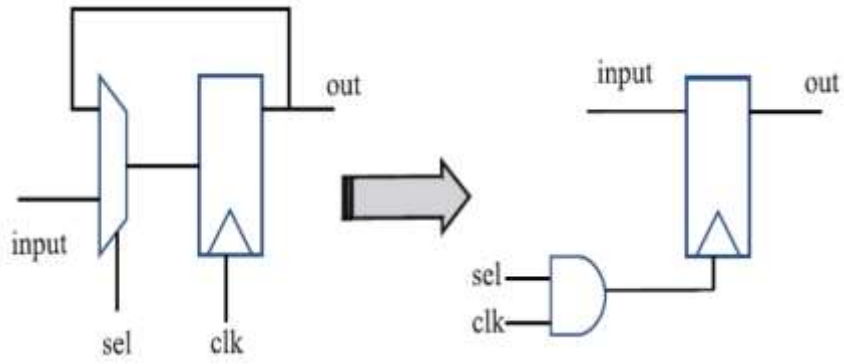
- Output capacitance of the gate itself (due to parasitic)
- The wire capacitance, and
- Input capacitance of the gates in its fanout.

Note: The output and input capacitances of gates are proportional to the gate size. Reducing the gate size reduces its capacitance, but increases its delay. Therefore, in order to preserve the timing behavior of the circuit, not all gates can be made smaller; only the ones that do not belong to a critical path can be slowed down.

Clock Gating

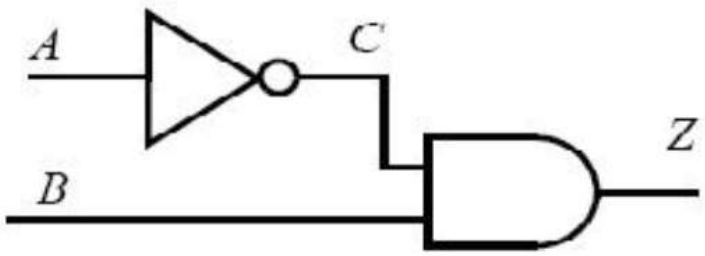
Fundamentally, Clock Gating reduces the dynamic power dissipation by disconnecting the clock from an unused circuit block.

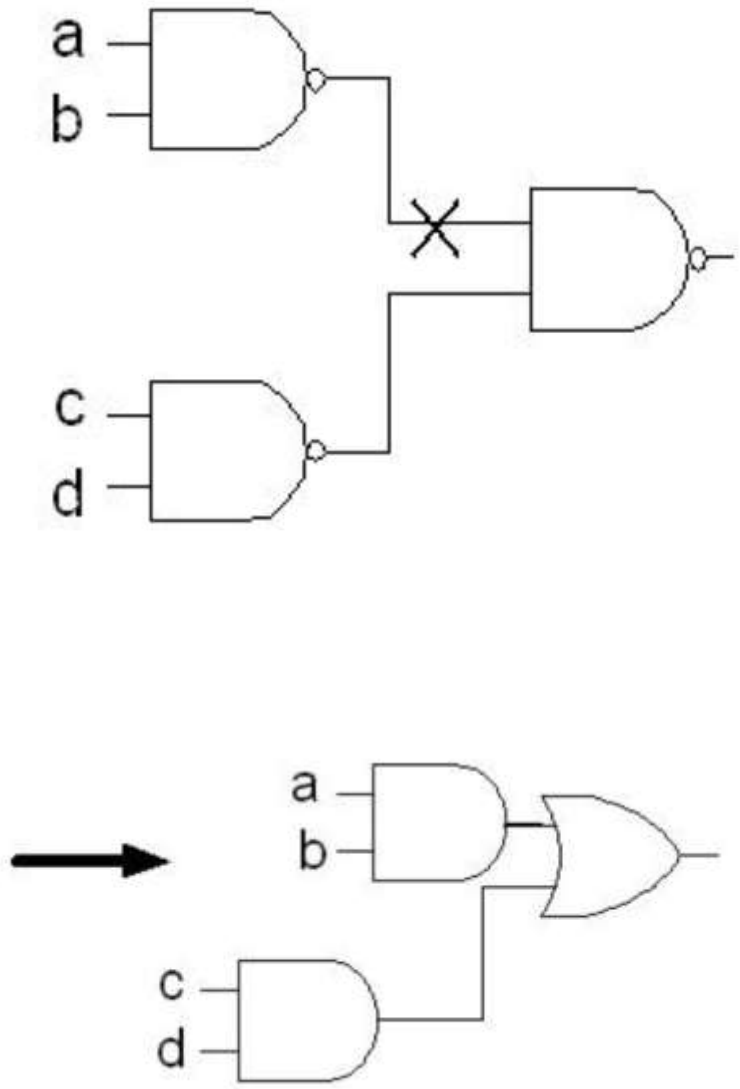
Note: In its simplest form, clock gating can be implemented by finding out the signal that determines whether the latch will have a new data at the end of the cycle. If not, the clock is disabled using the signal.



Reducing Glitches

Glitches occur in a logic chain when two parallel driving common gate arrive at different times. The output momentarily switches to incorrect value before settling to correct result. Consider circuit shown here. Let us assume that in the absence of buffer, path A is high speed and Path B is slow. Initially if A=0 and B=1 then Z=0.Next if B is to switch to 0 and A to 1 since B is slow the data 0 arriving at B will be slow and hence Z switches towards 1 momentarily before switching back to 0 resulting in power dissipation.





Logic Level Power Optimization

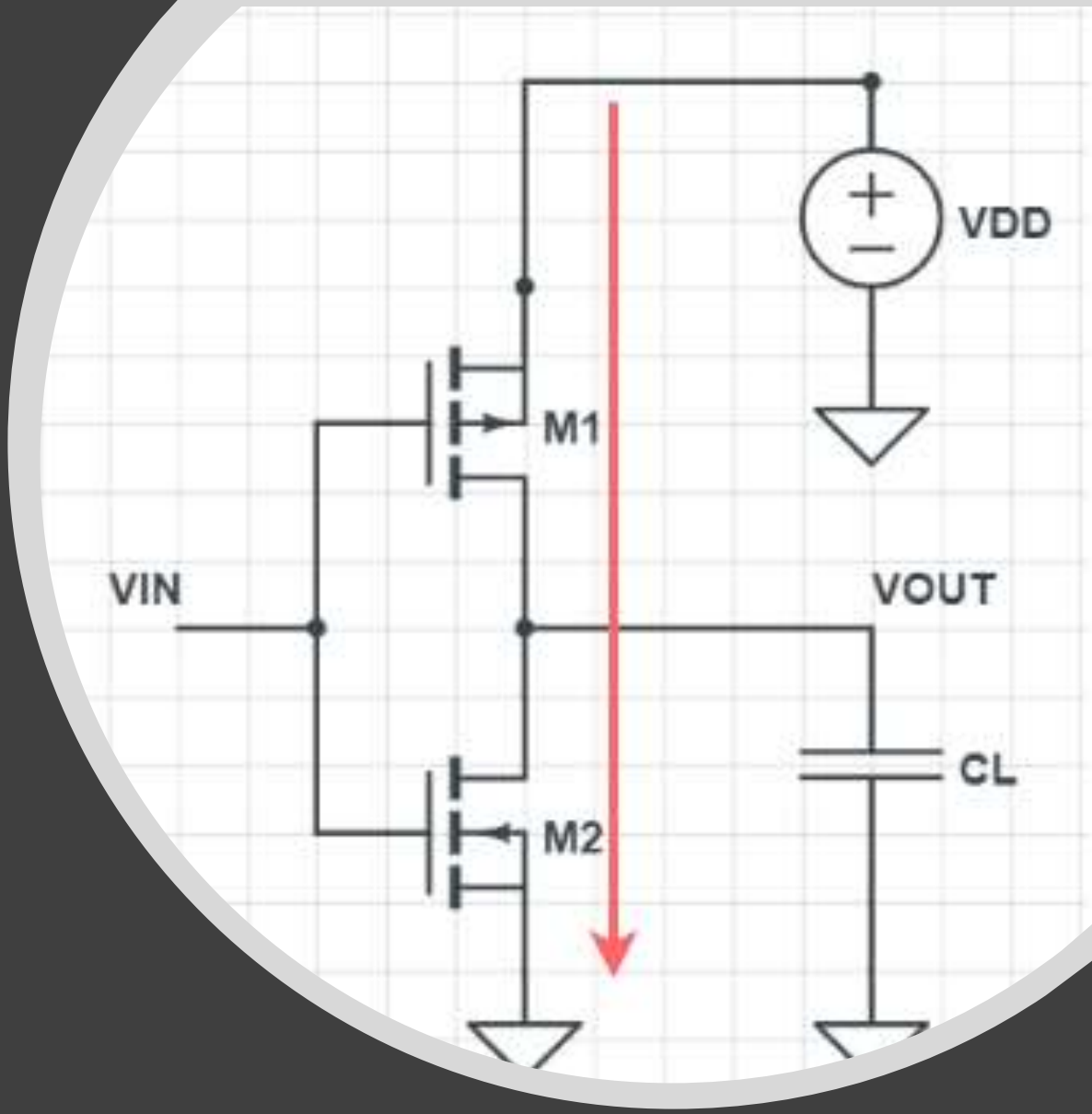
During logic optimization for low power, technology parameters such as supply voltage are fixed, and the degrees of freedom are in selecting the functionality and sizing the gates. Path equalization with buffer insertion is one of the techniques which ensures that signal propagation from inputs to outputs of a logic network follows paths of similar length to overcome glitches. When paths are equalized, most gates have aligned transitions at their inputs, thereby minimizing spurious switching activity/glitches (which is created by misaligned input transitions).

Other logic-level power minimization techniques include local transformations as shown in figure above. A re-mapping transformation is shown, where a high-activity node (marked with x) is removed and replaced by new mapping onto an and or gate.

Short Circuit Power Suppression

Short-circuit power, is caused by the short circuit currents that arise when pairs of PMOS/NMOS transistors are conducting simultaneously. In static CMOS circuits, short-circuit path exists for direct current flow from VDD to ground, when $VTn < Vin < VDD - |VTp|$

One way to reduce short circuit power is to keep the input and output rise/fall times the same. If $Vdd < Vtn + |Vtp|$ then short-circuit power can be eliminated. If the load capacitance is very large, the output fall time is larger than the input rise time. The drain-source voltage of the PMOS transistor is 0.Hence the short-circuit power will be 0. If the load capacitance is very small, the output fall time is smaller than the input rise time. The drain-source voltage of the PMOS transistor is close to VDD during most of the transition period. Hence the short-circuit power will be very large.

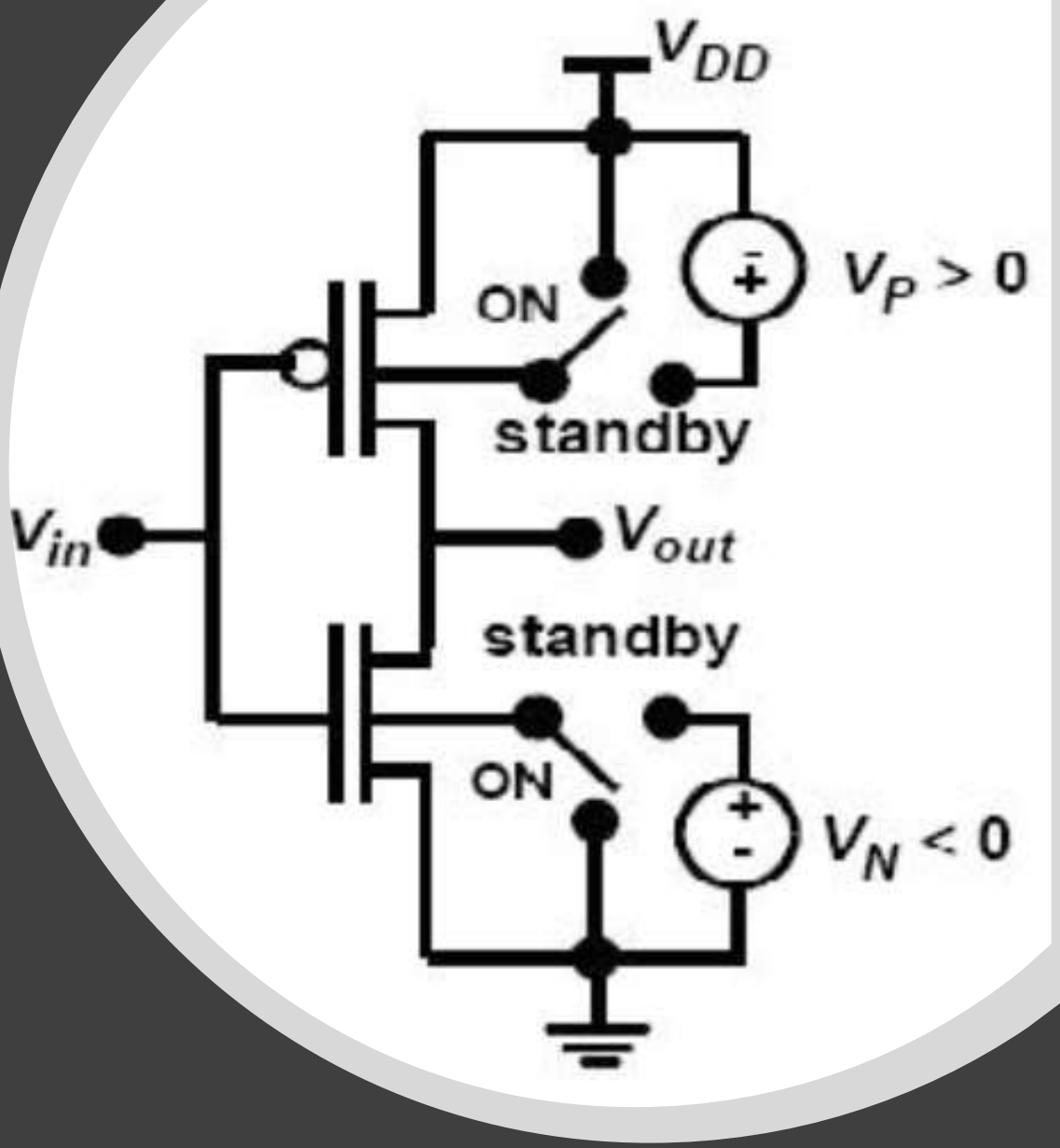


Static/Leakage/Standby Power Suppression

To meet leakage power constraints, multiple-threshold and variable threshold circuit techniques are often used. In multiple-threshold CMOS, the process provides two different threshold transitors. Low-threshold are employed on speed-critical sub-circuits and they are fast and leaky. High-threshold transistors are slower but exhibit low sub-threshold leakage, and they are employed in noncritical/slow paths of the chip. As more transistors become timing-critical multiple-threshold techniques tend to lose effectiveness.

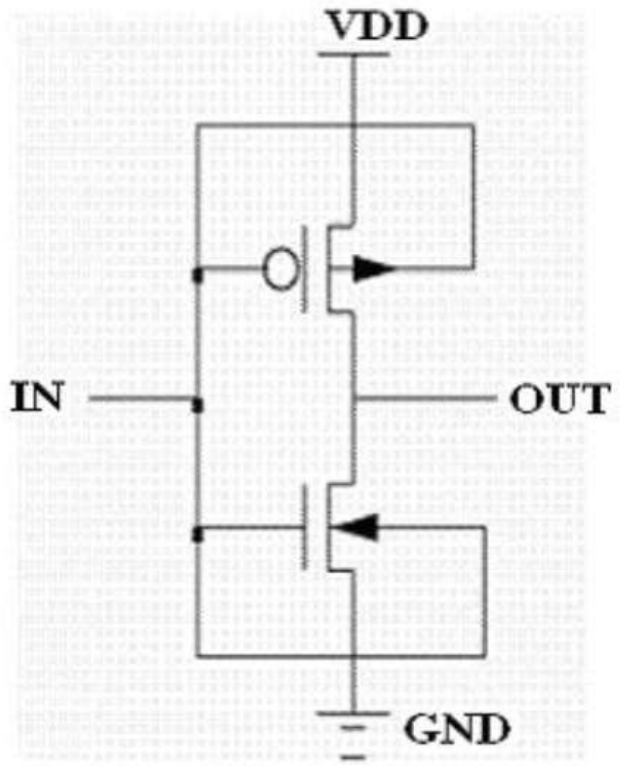
Variable Body Biasing

Variable-threshold circuits dynamically control the threshold voltage of transistors through substrate biasing and hence overcome shortcoming associated with multi-threshold design. When a variable-threshold circuit is in standby, the substrate of NMOS transistors is negatively biased, and their threshold increases because of the body-bias effect. Similarly the substrate of PMOS transistors is biased by positive body bias to increase their Vt in stand-by. Variable-threshold circuits can, in principle, solve the quiescent/static leakage problem, but they require control circuits that modulate substrate voltage in stand-by. Fast and accurate body-bias control with control circuit is quite challenging, and requires carefully designed closed-loop control. When the circuit is in standby mode the bulk/body of both PMOS and NMOS are biased by third supply voltage to increase the Vt of the MOSFET as shown in the Figure. However during normal operation they are switched back to reduce the Vt.



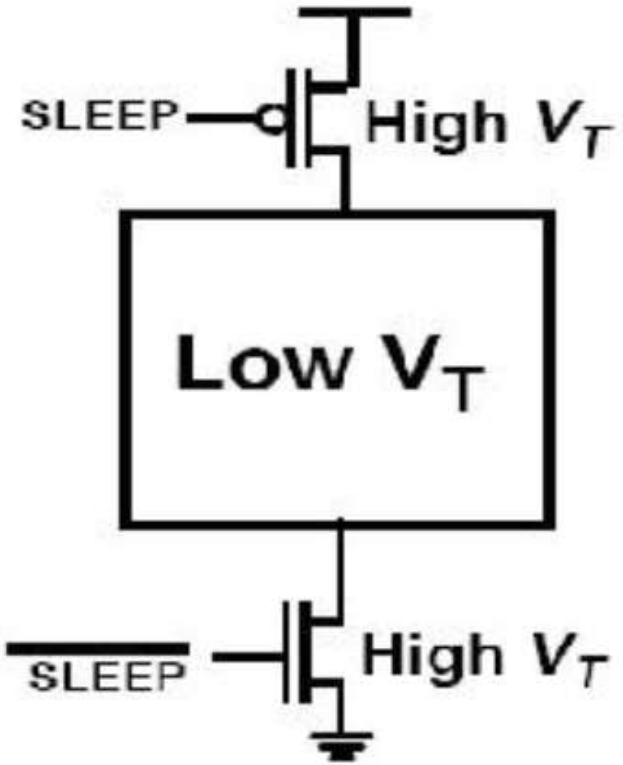
Dynamic Threshold MOS

In dynamic threshold CMOS (DTMOS), the threshold voltage is altered dynamically to suit the operating state of the circuit. A high threshold voltage in the standby mode gives low leakage current, while a low threshold voltage allows for higher current drives in the active mode of operation. Dynamic threshold CMOS can be achieved by tying the gate and body together. The supply voltage of DTMOS is limited by the diode built-in potential in bulk silicon technology. The PN diode between source and body should be reverse biased. Hence, this technique is only suitable for ultralow voltage (0.6V and below) circuits in bulk CMOS.



Sleep Transistor

Sleep Transistors are High Vt transistors connected in series with low Vt logic as shown below .When the main circuit consisting of Low Vt devices are ON the sleep transistors are also ON resulting in normal operation of the circuit. When the circuit is in Standby mode even High Vt transistors are OFF. Since High Vt devices appear in series with Low Vt circuit the leakage current is determined by High Vt devices and is very low. So the net static power dissipation is reduced.



Best Free VLSI Content

1. Verilog HDL Crash Course – Link
2. Static Timing Analysis (STA) – Theory Concepts – Link
3. Static Timing Analysis (STA) – Practice/Interview Questions – Link
4. Low Power VLSI Design – Theory Concepts – Link
5. Low Power VLSI Design (LPVLSI) – Practice/Interview Questions – Link
6. Digital ASIC Design Verilog Projects – Link

Please Like, Comment, Share & Subscribe My Channel in Order to Reach Out the Content to a Larger Audience.

Thanks !!