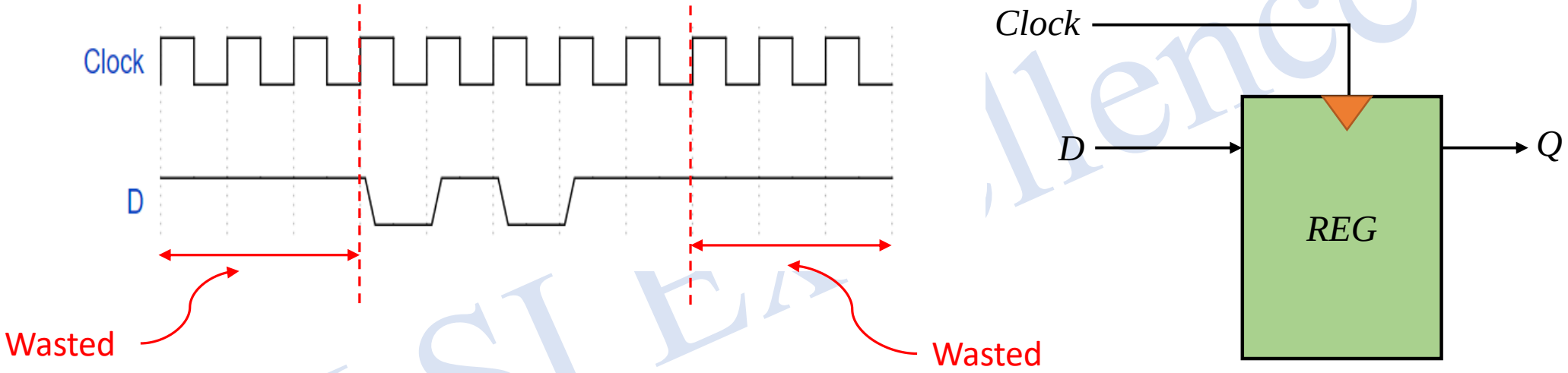
VLSI Low Power Design : Interview Question #01

Video Lecture Link

VLSI Low Power Design : Interview Question #01

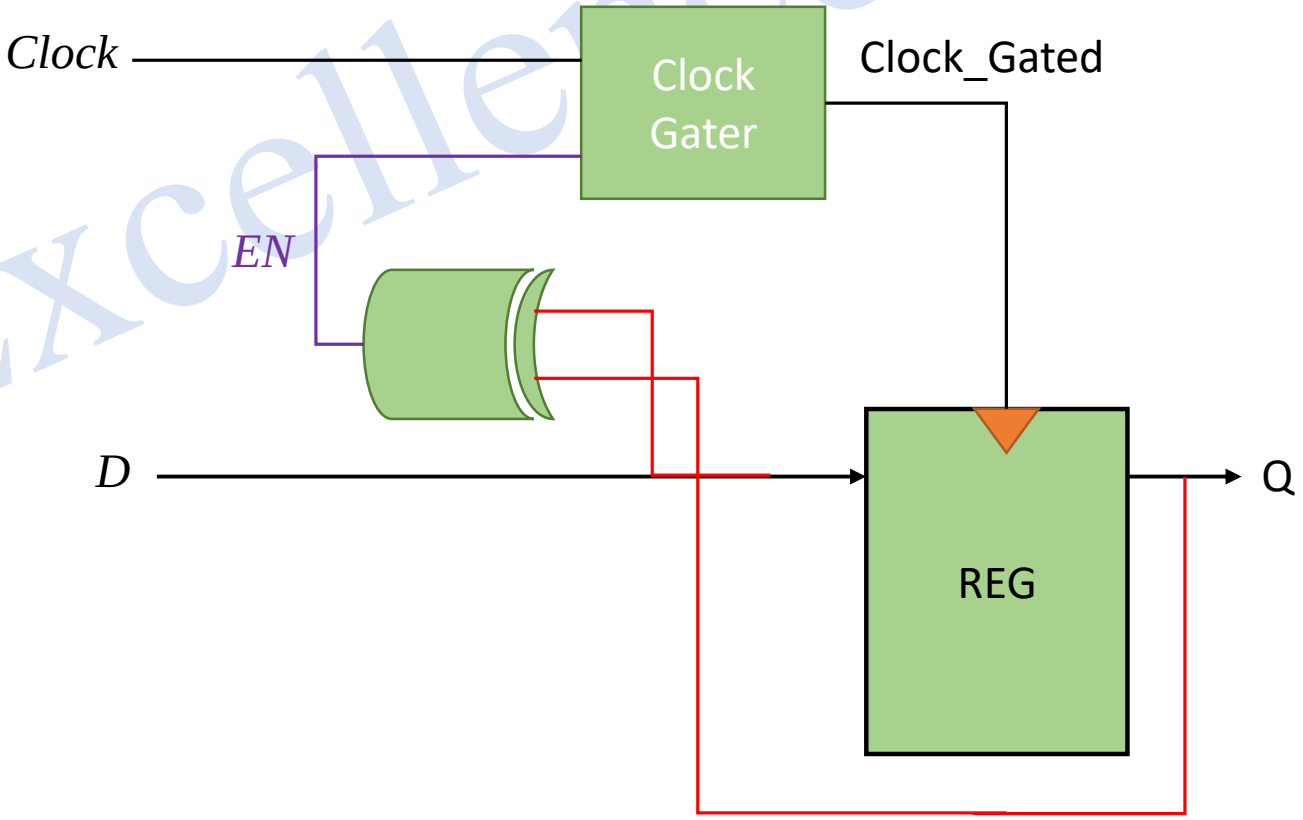


Problem: As you see here, the clock is always enabled for the D-FF and even when there is no new data available (No Data Toggle), the Clock is always toggling and results in the increased switching power (Also known as Dynamic Power).

Modify the above circuit such that switching power can be minimized when there is no new data available.

Given, there is no extra enable signal available to Gate the Clock

VLSI Low Power Design : Interview Question #01- Solution



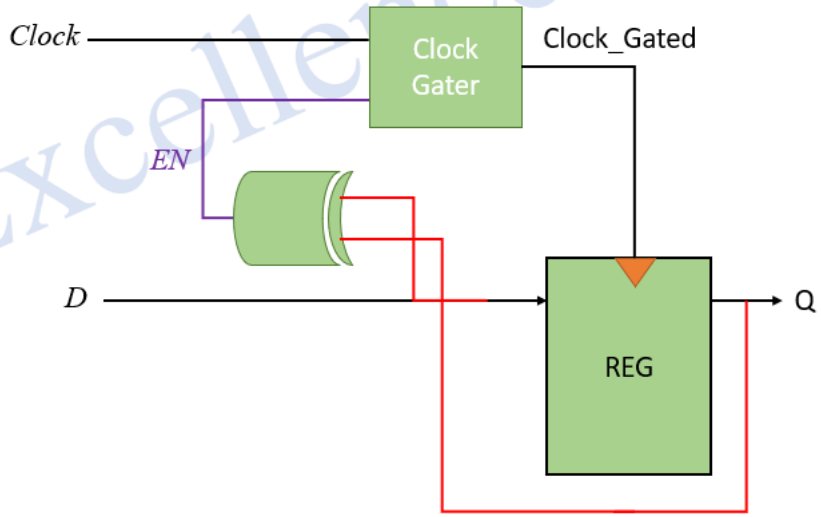
Here, the EN signal is 1 only when there is an activity on D input of the flip-flop OR in other words when there is a new data available and for rest of the time clock will be disabled and there would not be any switching power dissipation.

VLSI Low Power Design : Interview Question #01- Solution

Original Verilog HDL Code :

```
always @(posedge Clock)

q <= d;
```



Modified Verilog HDL Code :

```
//Generate Enable Condition for Clock Gater
en = (q ^ d);

//Instantiate Clock Gater Module
clock_gater CG(Clock_in(Clock), .En(en), Clock_out(Clock_Gated))

always @(posedge Clock_Gated)

  q <= d;
```

VLSI Low Power Design : Interview Question #01- Trade-Off

1. **Area Impact (More Area)**
2. **Power Consumption (More Power Consumption)**
3. **Timing** : The levels of logic between the data and the enable can also impact timing. If a change arrives late at the data inputs, it requires some time to propagate into the enable to allow the clock through

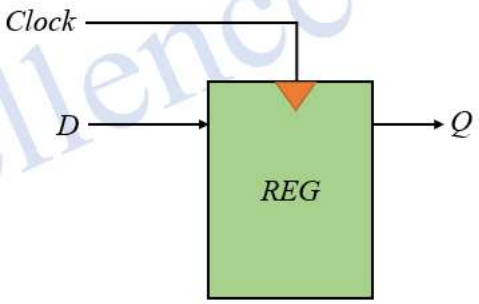


Figure – 1: Original Circuit

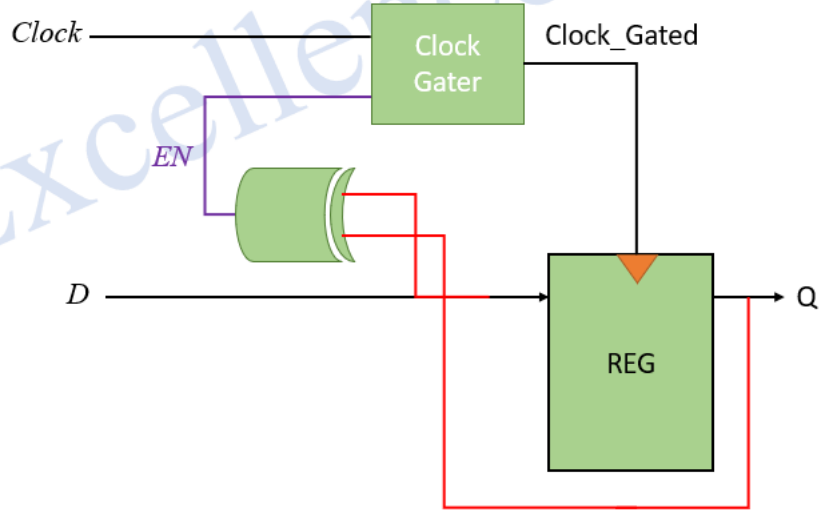


Figure - 2: Modified Circuit

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