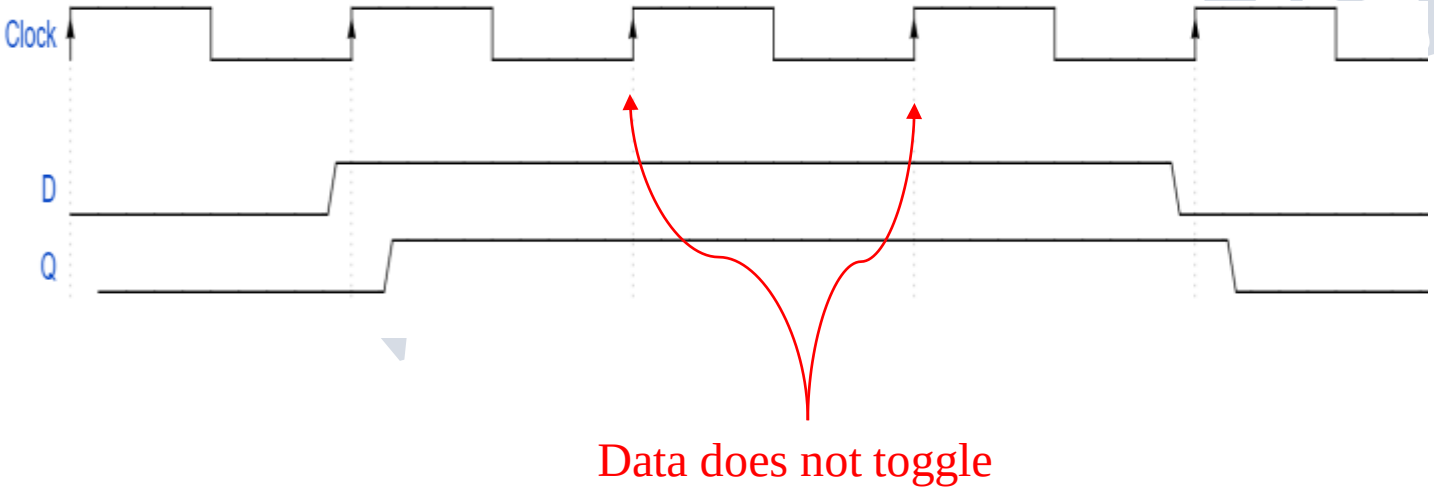
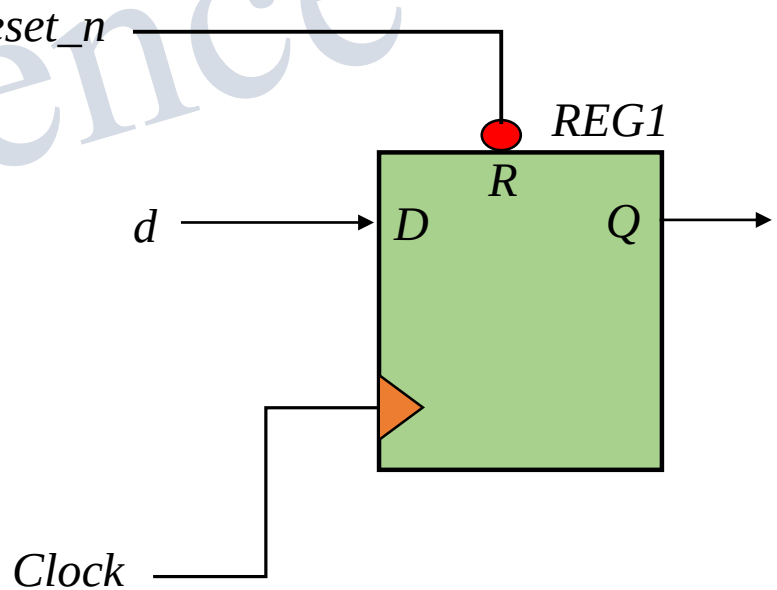
Applications & Types of Clock Gating Circuits in VLSI Design

Video Lecture Link

Clock Gating Circuits & Applications

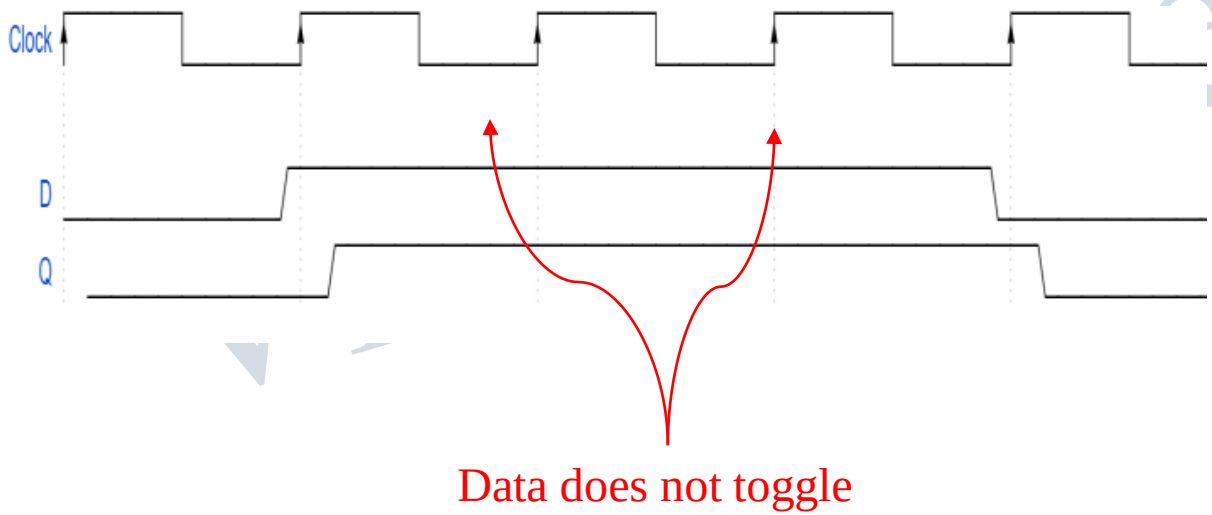
Scenario#1 –

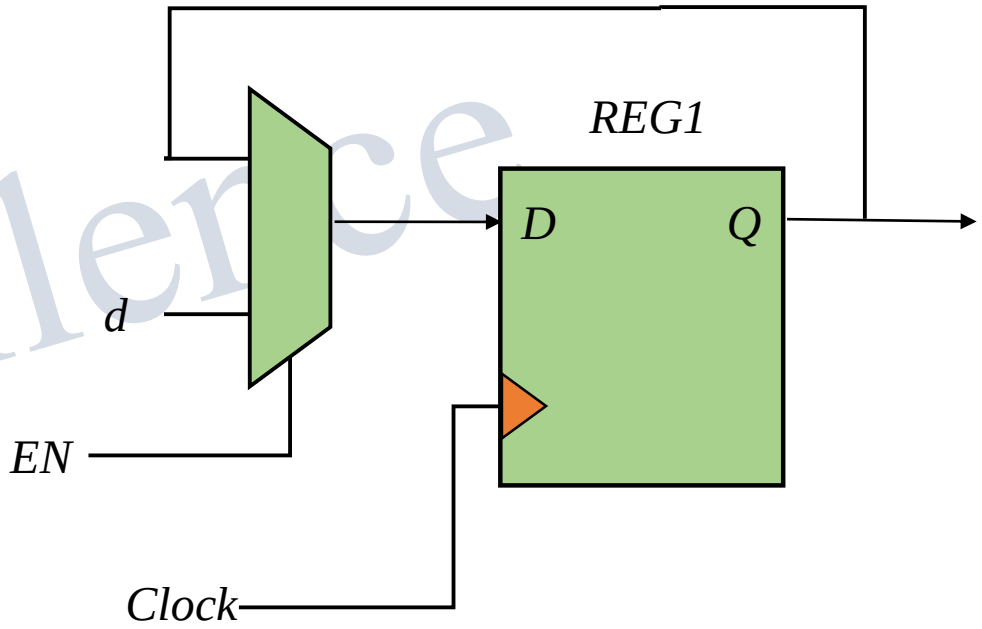




Clock Gating Circuits & Applications

Scenario#2 –





Example :

1) Some part of SoC is always not functioning

2) Configuration Registers – Seldom Update

Clock Gating (Why Do We Need ?)

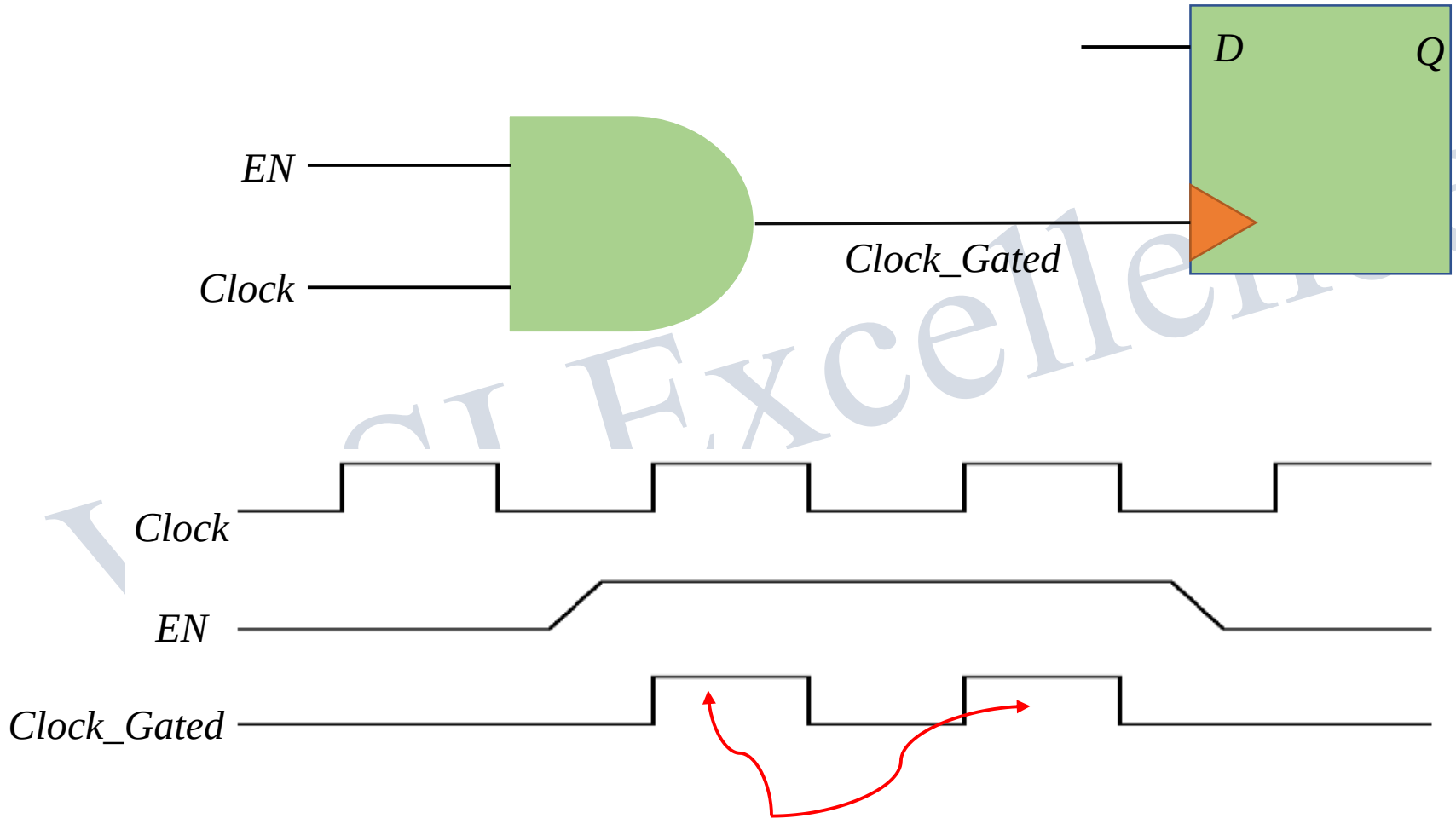
Dynamic Power is directly proportional to Activity Factor, Load Capacitor, Voltage and the Frequency of the clock as shown in the following equation:

$$\textit{Dynamic Power} = \textbf{Activity Factor} * \text{Capacitance} * (\text{Voltage})^2 * (\textbf{Frequency})$$

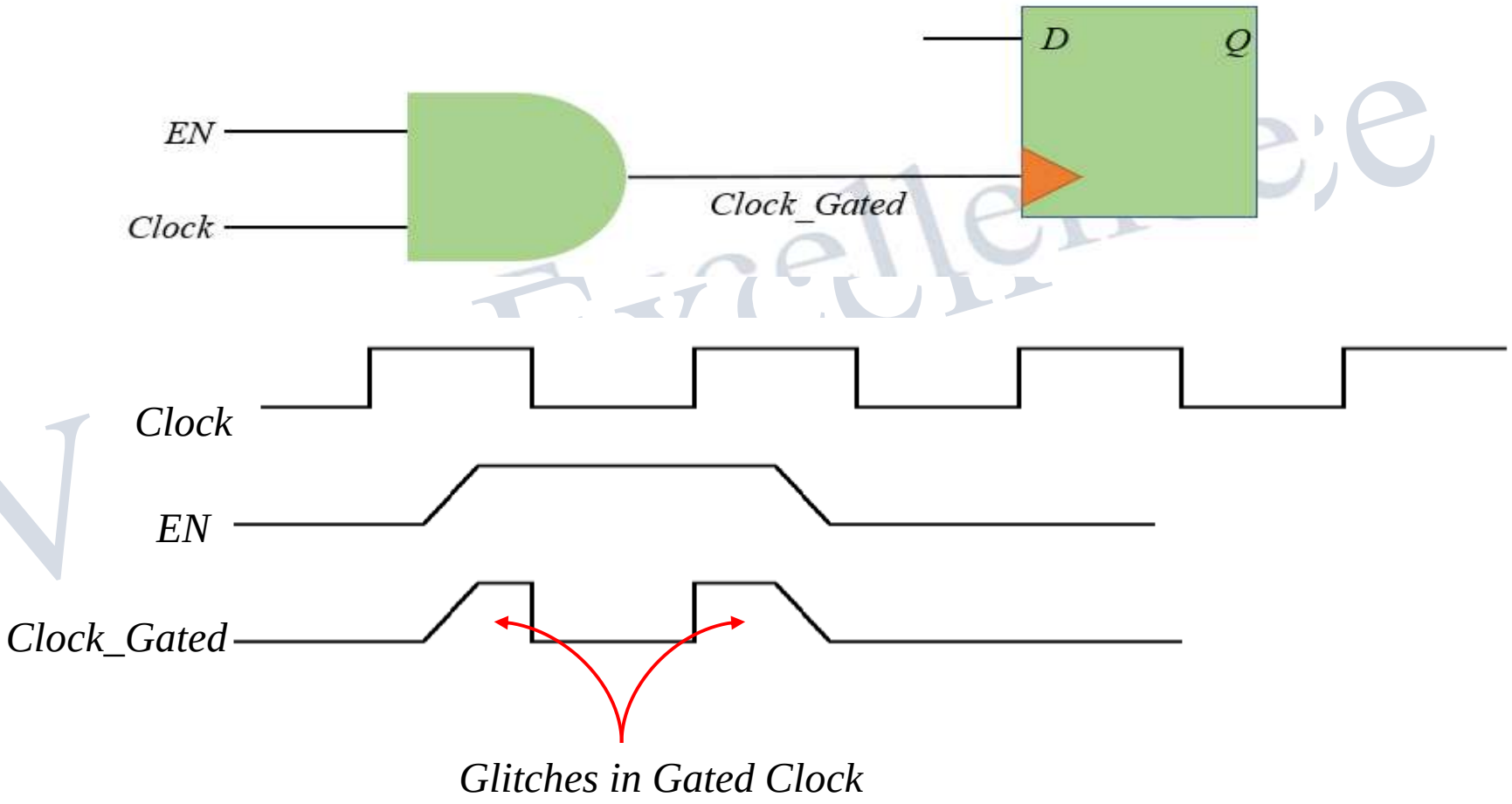
Hence, reducing clock power is very important.

Example : Lower power consumption is mandatory for mobile and handheld applications for longer battery life.

AND Gate Based Clock Gating Circuit



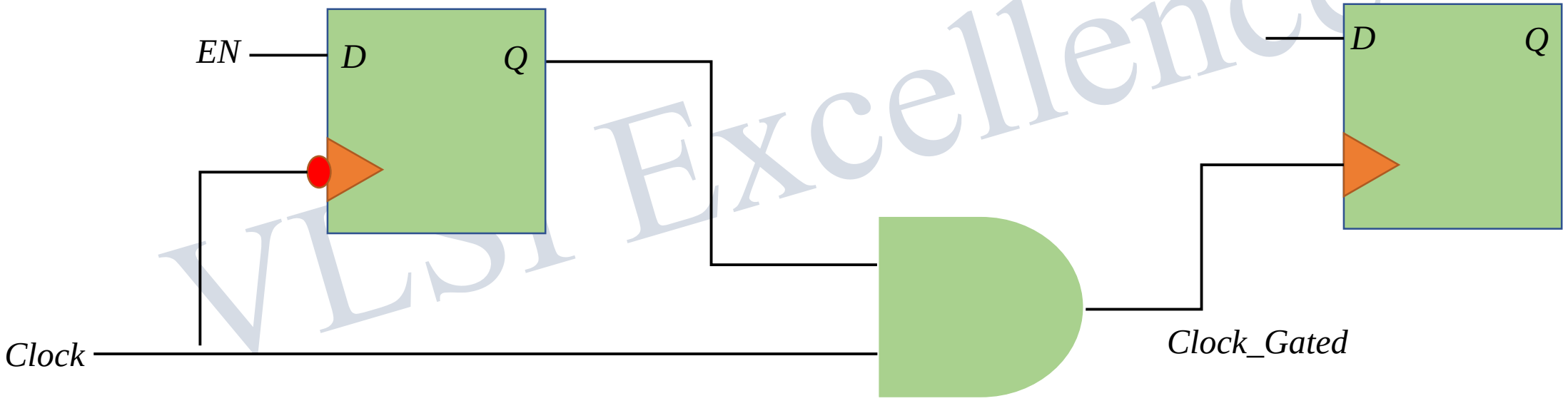
AND Gate Based Clock Gating Circuit



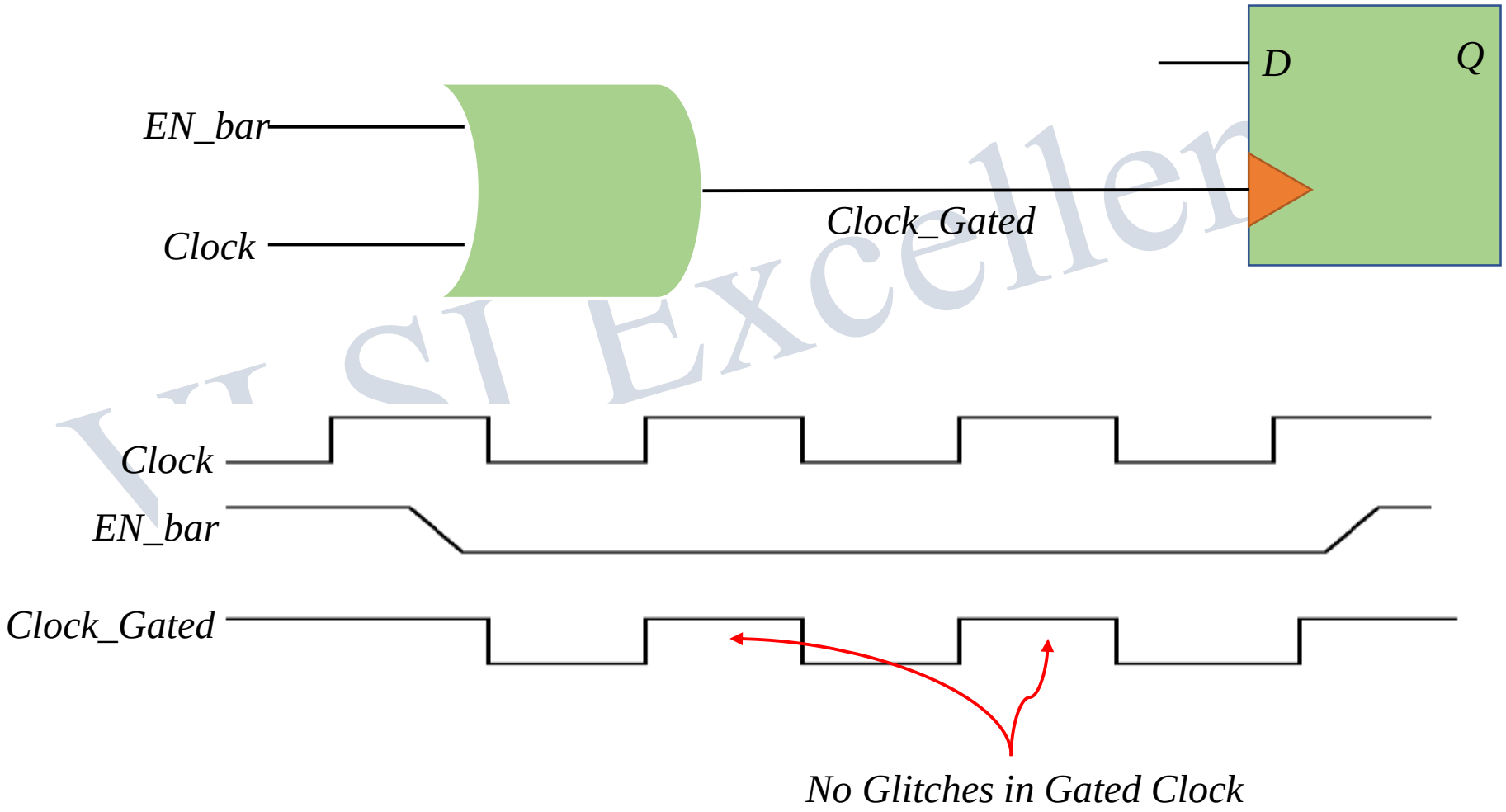
Solution: Flip –Flop Based Clock Gater

Make sure the enable signal changes only when the Clock Signal is LOW !!!

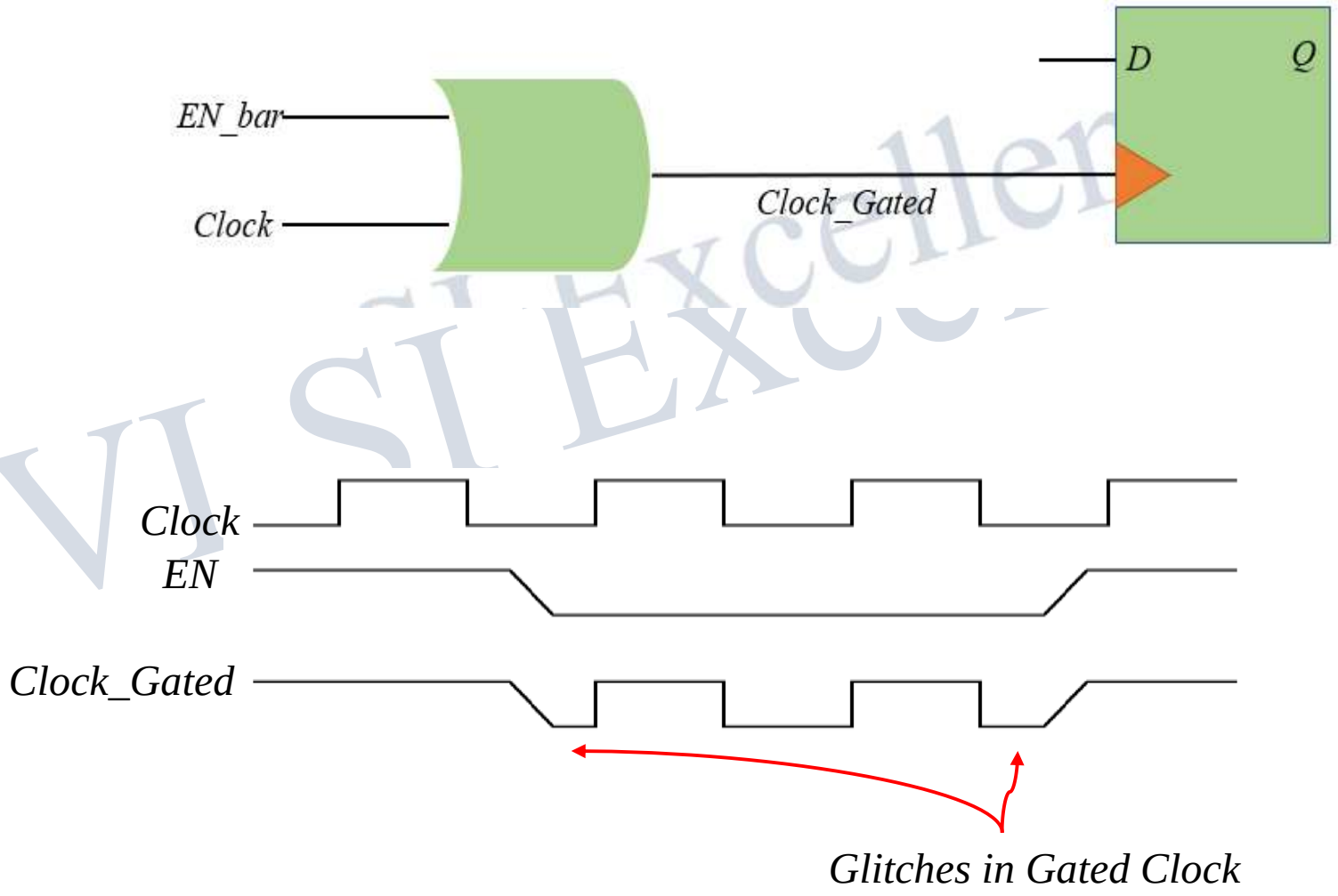
- Use a Negative Edge Triggered Flip- Flop



OR Gate Based Clock Gating Circuit



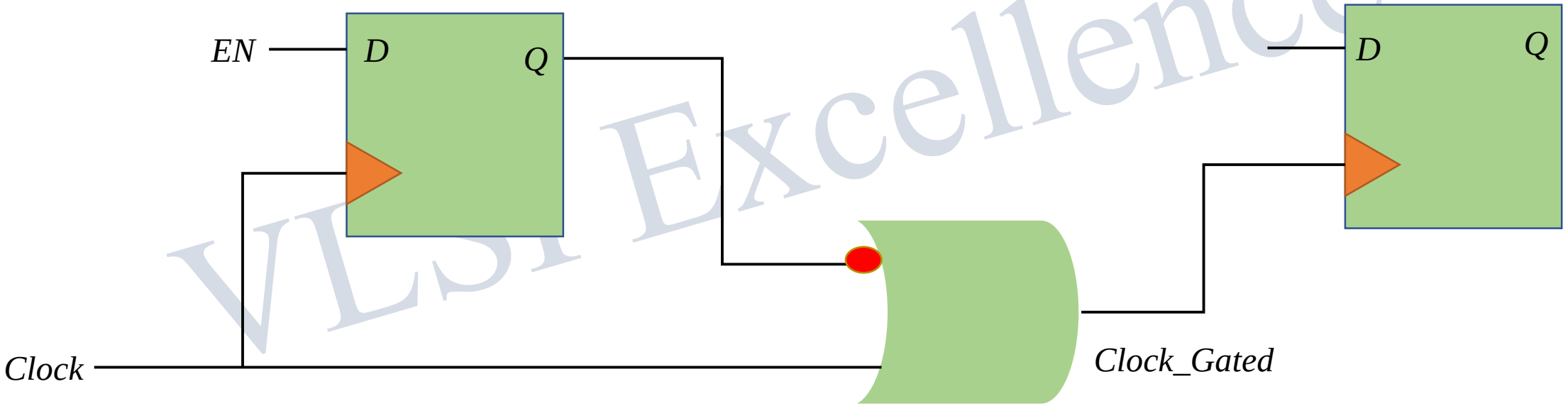
OR Gate Based Clock Gating Circuit



Solution: Flip - Flop Based Clock Gater

Make sure the enable signal changes only when the Clock Signal is HIGH !!!

- Use a Positive Edge Triggered Flip- Flop



Summary

AND/NAND Gate Based Clock Gating is Referred as Active High Clock Gating

OR/NOR Gate Based Clock Gating is Referred as Active Low Clock Gating

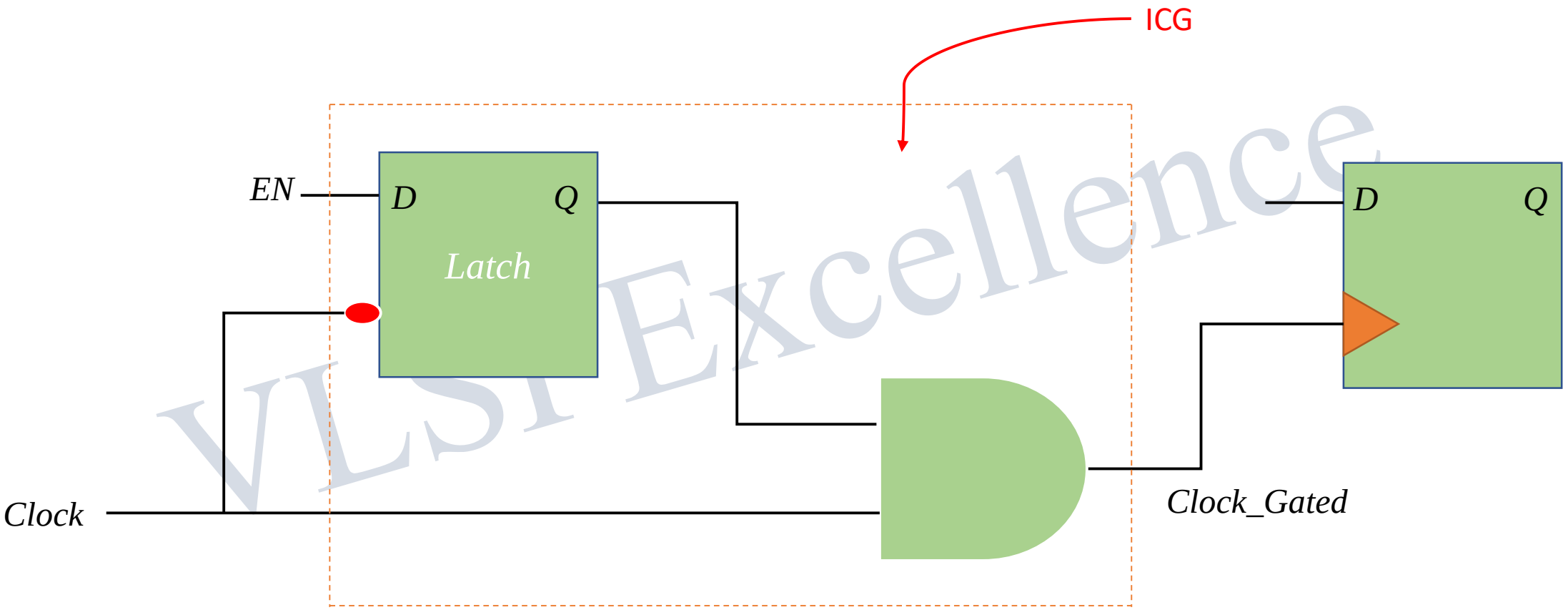
Clock Gating is an efficient way to save Dynamic Power Consumption in a Design !!!

Problems with Flip Flop Based Clock Gating Circuit

1. **Area** : An extra flip-flop (with an area of equal to 2 Latches)
2. **Power** Consumption (Adding extra flip flop will consume more power)
3. Timing : Due to introduced half cycle path, it becomes more difficult to meet the timing

Solution : Latch Based Clock Gating Circuit (Integrated Clock Gating [ICG] Circuit)

Latch Based Integrated Clock Gating Circuit



Note : Most ASIC library vendors now supply a standard ICG cell where the timings have already been sorted out internally, and it's safe just to instantiate it.

Best Free VLSI Content

1. Verilog HDL Crash Course – Link
2. Static Timing Analysis (STA) – Theory Concepts – Link
3. Static Timing Analysis (STA) – Practice/Interview Questions – Link
4. Low Power VLSI Design – Theory Concepts – Link
5. Low Power VLSI Design (LPVLSI) – Practice/Interview Questions – Link
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Thanks !!