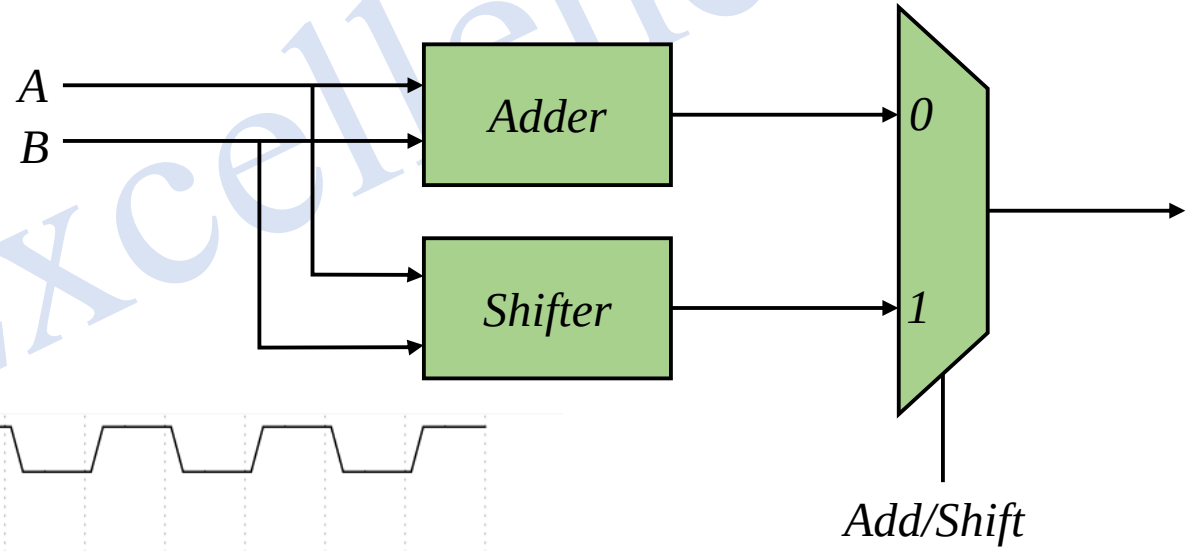
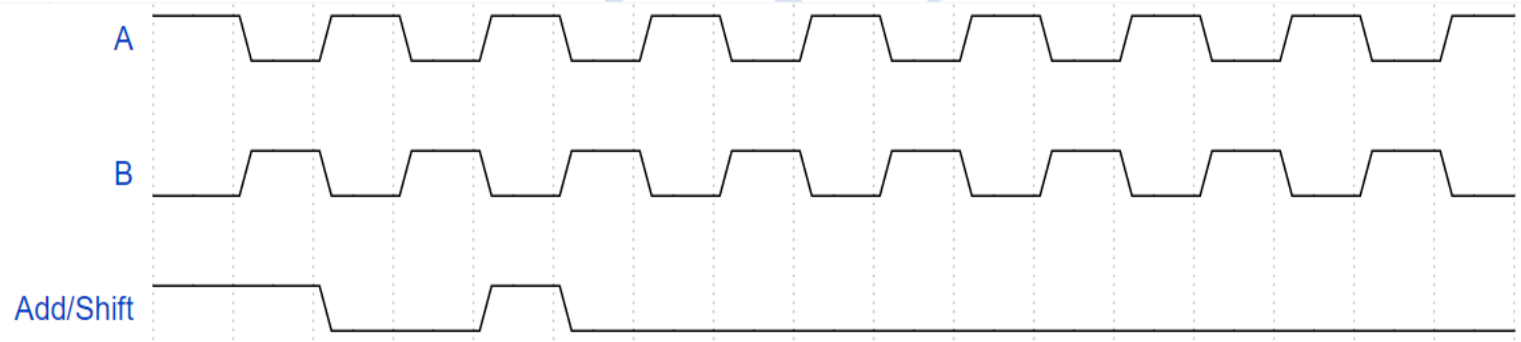
VLSI Low Power Design : Interview Question #02

Video Lecture Link

VLSI Low Power Design : Interview Question #02

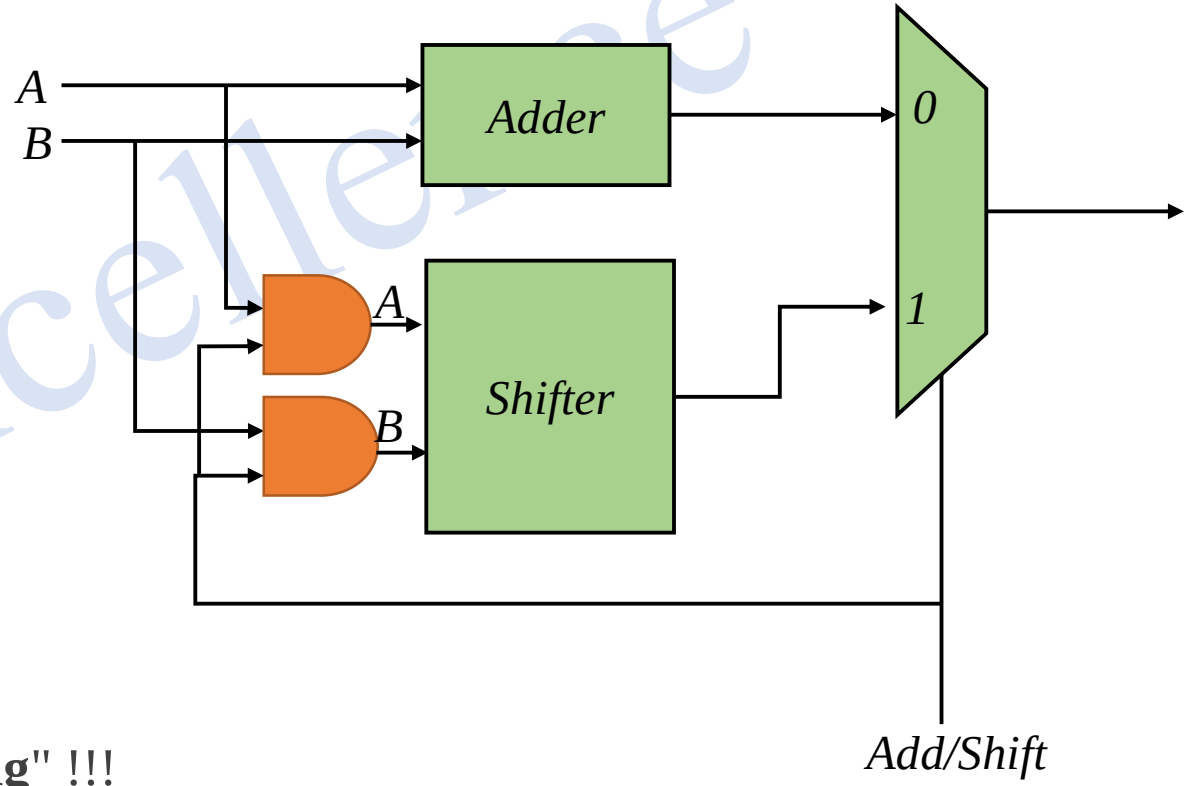
Modify the given circuit for dynamic power optimization if the adder is functional more frequently than shifter





VLSI Low Power Design : Interview Question #02 - Solution

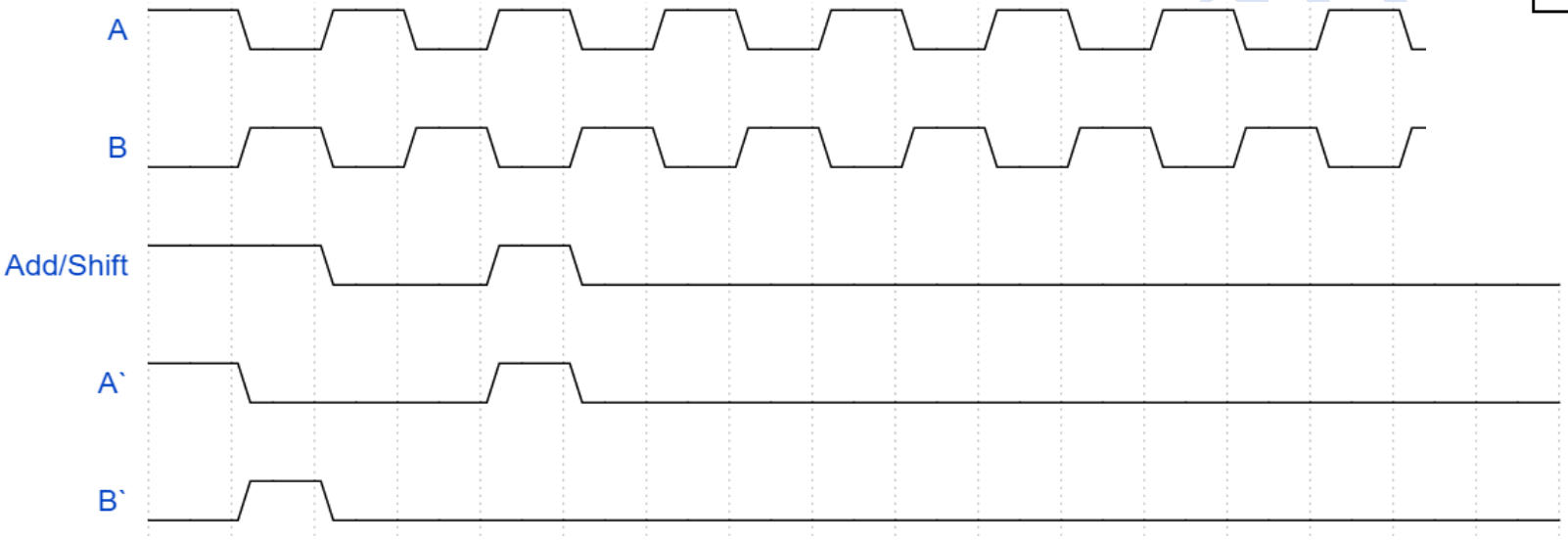
Since the shifter here is used infrequently, is it possible that we can just Gate the data going into it ? and only let the data pass to the shifter when the shifter is functional ?

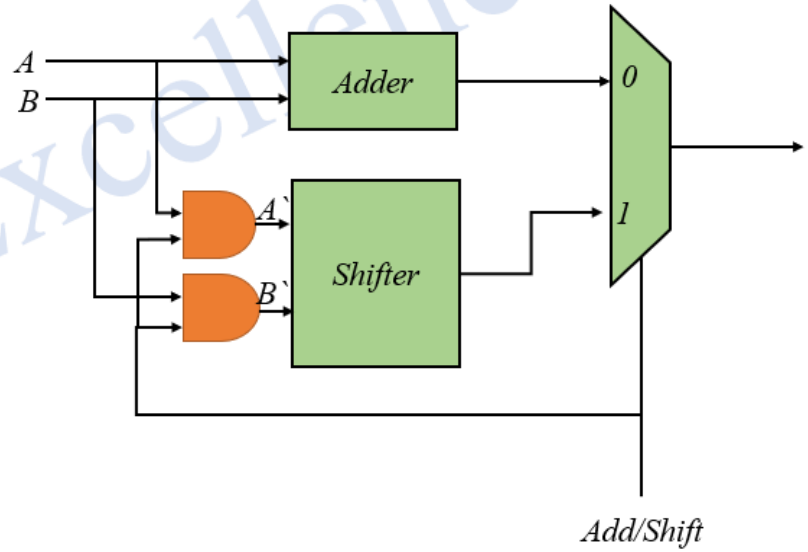


Hence, there will be minimal switching activity inside the Shifter and results in the minimum Power Consumption !!!

We can call this Low Power Technique as "**Data Gating**" !!!

VLSI Low Power Design : Interview Question #02





VLSI Low Power Design : Interview Question #02- Trade-Off

1. **Area Impact –** Two Additional AND Gates
2. **Timing Impact** – Additional Delay Caused by two AND Gates
3. **Availability of Data at MUX input**

Best Free VLSI Content

1. Verilog HDL Crash Course – Link
2. Static Timing Analysis (STA) – Theory Concepts – Link
3. Static Timing Analysis (STA) – Practice/Interview Questions – Link
4. Low Power VLSI Design – Theory Concepts – Link
5. Low Power VLSI Design (LPVLSI) – Practice/Interview Questions – Link
6. Digital ASIC Design Verilog Projects – Link

Please Like, Comment, Share & Subscribe My Channel in Order to Reach Out the Content to a Larger Audience.

Thanks !!