

Static Timing Analysis (STA)

Lecture #04: Wire Load Model (WLM) – Net Delay Calculation

Video Lecture [Link](#)

Static Timing Analysis (STA) – Wire Load Model

Net Delay - Wire Load Model :

- WLM is an estimation of delay, based on **area and fanout**.
- The net resistance (R) and the net capacitance (C) are used to calculate the delay of the net.
- The net delay is then calculated as **$(\text{Delay})_{\text{net}} = (R)_{\text{net}} * (C)_{\text{net}}$**
- Wire – Load Models (WLMs) provides synthesis tools with an estimation of net resistance and capacitance based on the length and fanout that represent 90% of the nets.
- Generally, a number of wire-load models are present in the technology library (Ex – Synopsys), each representing a particular size block of the logic. These models define the capacitance, resistance, and area factor of the net.

Static Timing Analysis (STA) – Wire Load Model

How STA Calculates Net Delay from a WLM:

- Determine the area that a net fits in.
- Select the WLM with a Block area that just encloses the area of the net
- STA uses the WLM to estimate the wire length based on the fanout of the net, or uses the wire-load table to model capacitance and resistance more accurately
- The capacitance multiplier (CM) and resistance multiplier(RM) are used to determine the actual RCs of the net.
- Hence, $(C)_{net}$ will be $CM * Length$
- $(R)_{net}$ will be $RM * Length$
- Note : For the same fanout, the bigger the block size, the bigger the estimate of average net length, and hence the value of the capacitance.

Static Timing Analysis (STA) – Wire Load Model

Example : Consider an enclosed Wire – Load Model. The Net fanout is 4 and the area of the block that the net is in is 200 units. The area of top design is 800 units. Determine the delay of the net using the below WLM

```
wire_load ("20X20"){
```

```
    resistance = 0.5;  
    capacitance = 0.15;  
    area = 400;  
    slope 0.12;  
    fanout_length (1, 0.15);  
    fanout_length (2, 0.30);  
    fanout_length (3, 0.47);  
    fanout_length (4, 0.70);  
    fanout_length (5, 1.05);  
    fanout_length (6, 1.25);  
}
```

```
wire_load ("30X30"){
```

```
    resistance = 0.5;  
    capacitance = 0.15;  
    area = 900;  
    slope 0.15;  
    fanout_length (1, 0.25);  
    fanout_length (2, 0.40);  
    fanout_length (3, 0.57);  
    fanout_length (4, 0.80);  
    fanout_length (5, 1.25);  
    fanout_length (6, 1.45);  
}
```

Static Timing Analysis (STA) – Wire Load Model

Example : Consider an enclosed Wire – Load Model. The Net fanout is 4 and the area of the block that the net is in is 200 units. The area of top design is 800 units. Determine the delay of the net using the below WLM

```
wire_load ("20X20"){
```

```
    resistance = 0.5;  
    capacitance = 0.15;  
    area = 400;  
    slope 0.12;  
    fanout_length (1, 0.15);  
    fanout_length (2, 0.30);  
    fanout_length (3, 0.47);  
    fanout_length (4, 0.70);  
    fanout_length (5, 1.05);  
    fanout_length (6, 1.25);  
}
```

```
wire_load ("30X30"){
```

```
    resistance = 0.5;  
    capacitance = 0.15;  
    area = 900;  
    slope 0.15;  
    fanout_length (1, 0.25);  
    fanout_length (2, 0.40);  
    fanout_length (3, 0.57);  
    fanout_length (4, 0.80);  
    fanout_length (5, 1.25);  
    fanout_length (6, 1.45);  
}
```

Solution :

RM = 0.5;
CM = 0.15;
Fanout = 4;
Block Area = 200 Units and
Hence, will select the first
WLM
Fanout Length = 0.70;

$(\text{Delay})_{\text{net}} = (0.70 \times 0.5) * (0.70 * 0.15) = 0.03675 \text{ unit}$

Best Free VLSI Content

1. Verilog HDL Crash Course – [Link](#)
2. Static Timing Analysis (STA) – Theory Concepts – [Link](#)
3. Static Timing Analysis (STA) – Practice/Interview Questions – [Link](#)
4. Low Power VLSI Design – Theory Concepts – [Link](#)
5. Low Power VLSI Design (LPVLSI) – Practice/Interview Questions – [Link](#)
6. Digital ASIC Design Verilog Projects – [Link](#)

Please Like, Comment, Share & Subscribe [My Channel](#) in Order to Reach Out the Content to a Larger Audience.

Thanks !!