# Static Timing Analysis (STA)

***Lecture #07: Clock, Clock Latency, Clock Slew, Clock Skew, Clock Jitter***

***Video Lecture Link***

# Static Timing Analysis (STA)

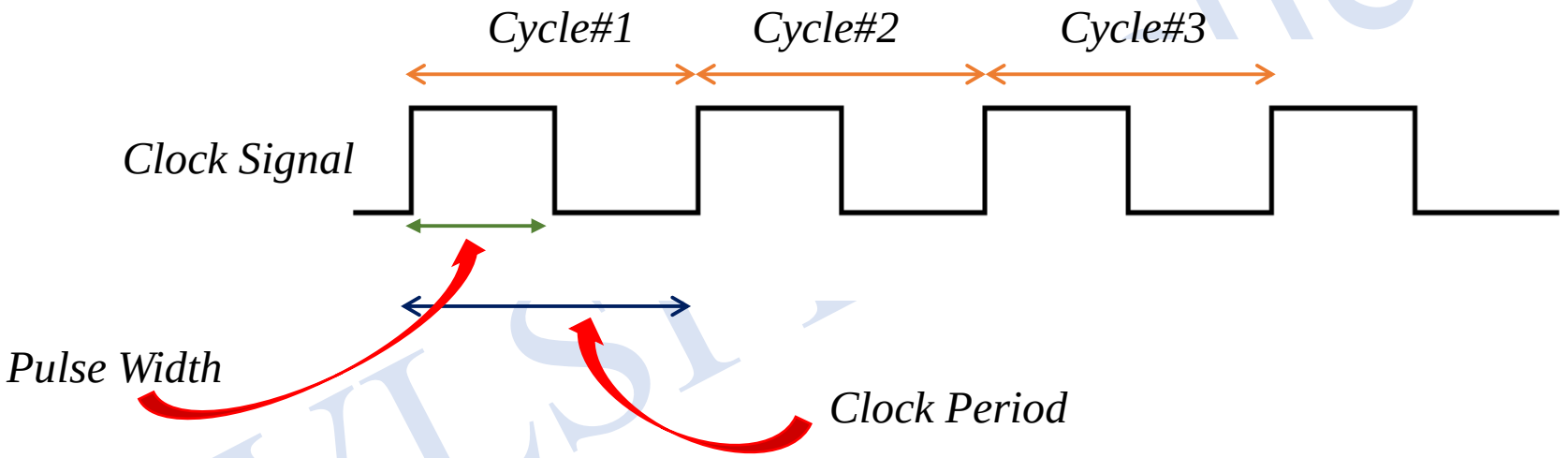
In the last Chapters of Static Timing Analysis, we have covered –

- **Types of Timing Paths**
- **Timing Arc**
- **Characteristics of Timing Arc**

In this Lecture, we are going to cover everything about Clocks.

# Static Timing Analysis (STA) - Clocks

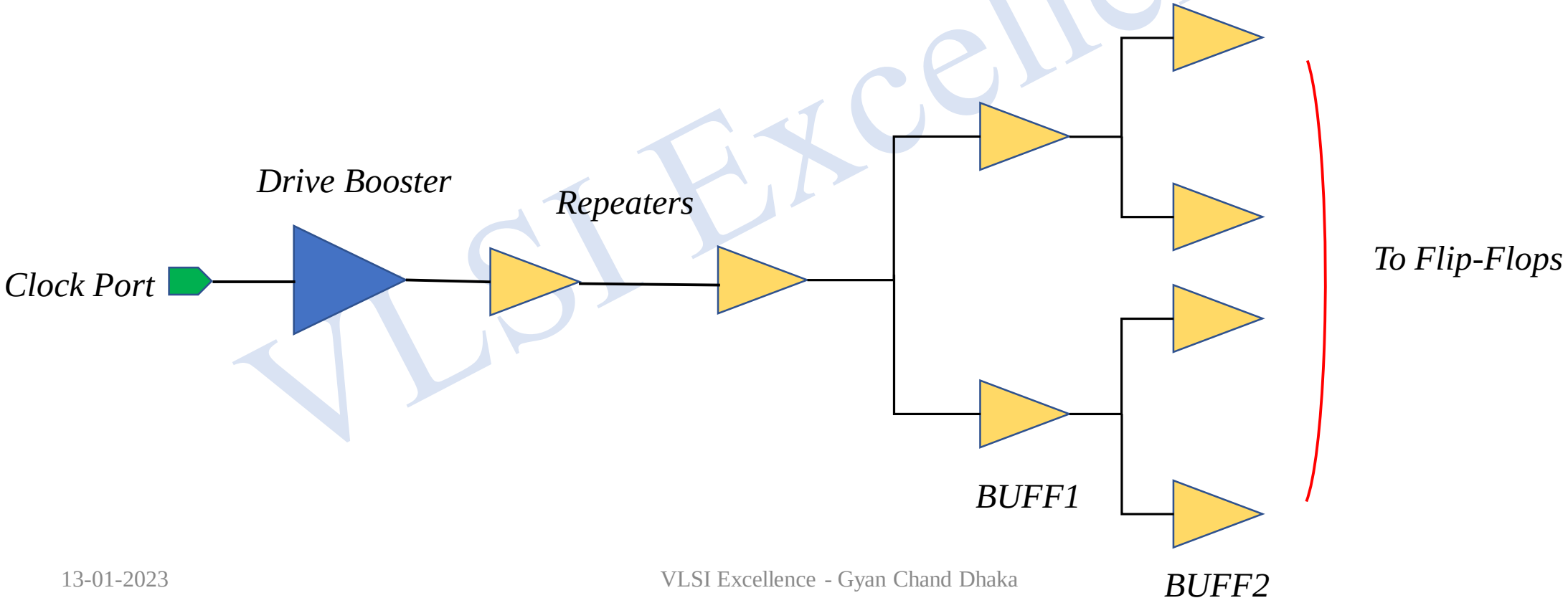
**Clock :** A Periodic signal used in sequential circuits to synchronize data transfer between sequential elements (Flip-Flops)
Clocks are generated by an external crystal oscillator outside of chip or by internal RC oscillator/PLL




***Note:*** The STA tool times the timing paths in relation to a clock and the goal is to meet the timing of each path within one clock cycle/period

# Static Timing Analysis (STA) - Clocks

**Clock Propagation :** Clock has to traverse through the entire design in order to reach to every sequential element in the design (FF/Latches) and hence there is a need to buffer that signal to keep its integrity and this structure is called **clock tree**.



# Static Timing Analysis (STA) - Clocks

There are two mode of Clock Propagation :

**1) Ideal Mode** – When there are no clock buffers in the design and hence we model the effect of these buffers in Static Timing Analysis.

**2) Propagated Mode** : When buffers are physically present in the design, then the STA tool replaces the modeled clock information with the actual clock information.

# Static Timing Analysis (STA) - Clocks

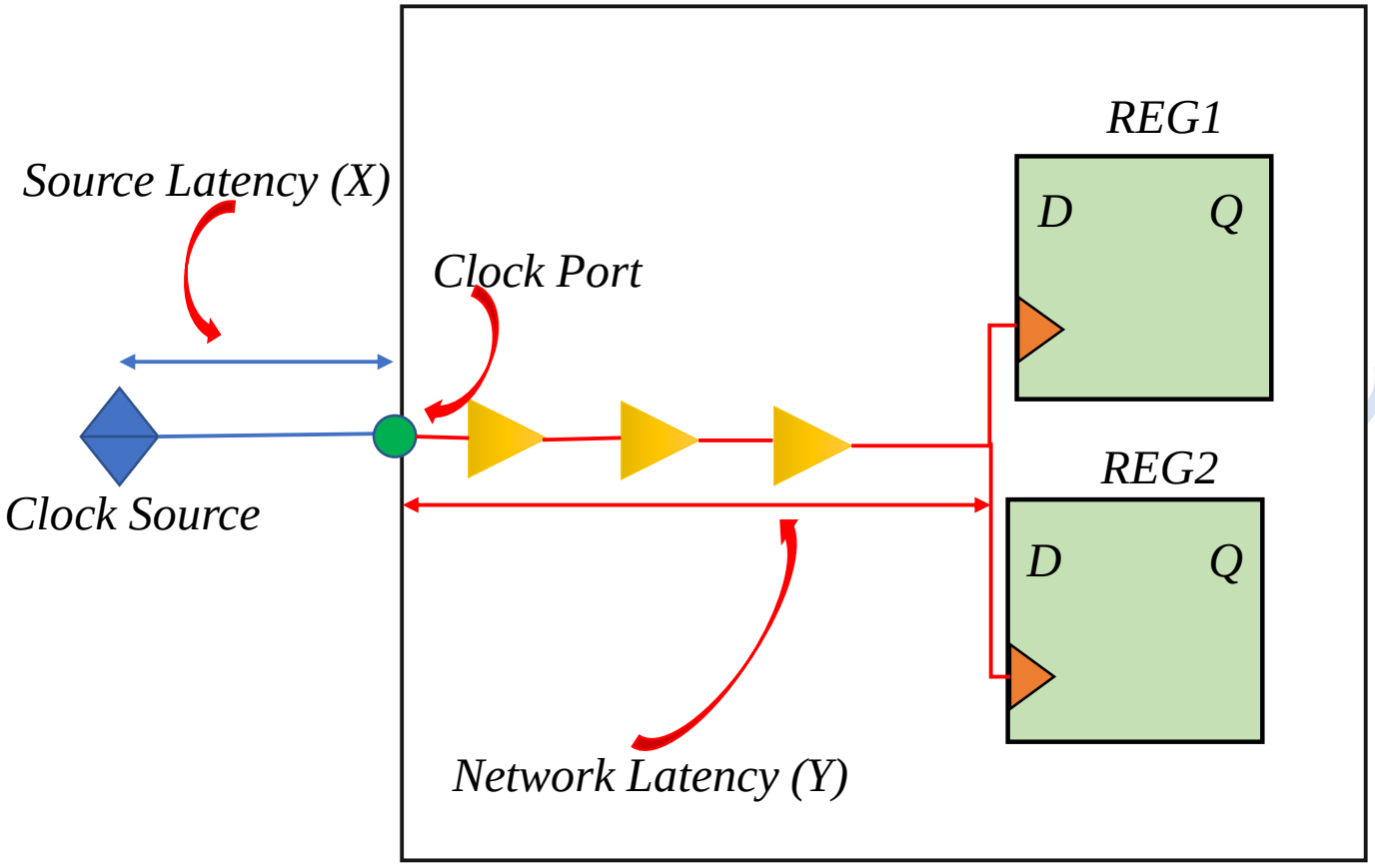
**Clock Latency** – It is a time taken by a clock signal to propagate from the clock definition point to a flip-flop clock pin. It is also known as insertion delay .

Latency is of two types –

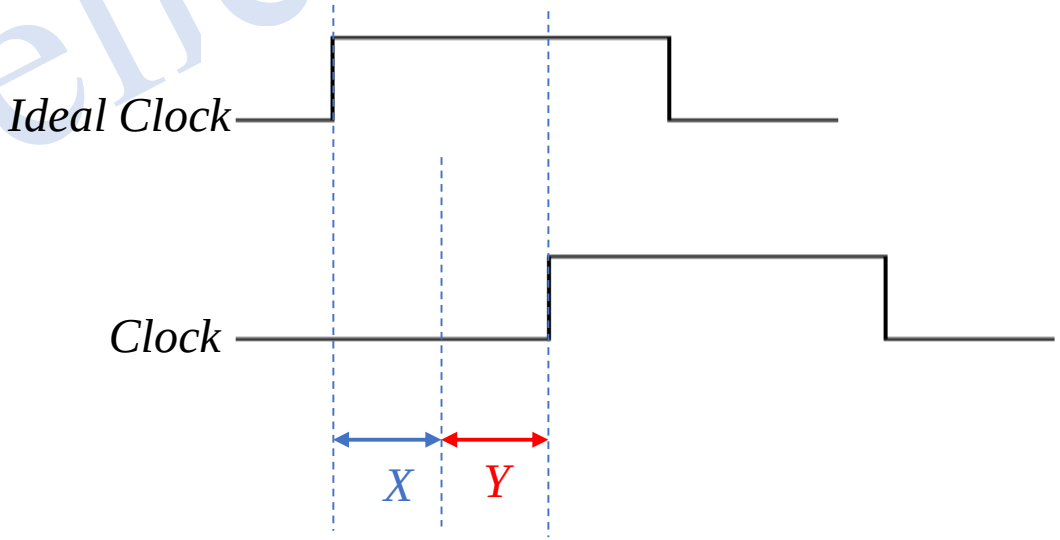
1) **Source Latency** – Latency between Clock source to the clock port in a given design
2) **Network Latency** – Clock port to the flip-flop (register) clock pin ( Clock Tree Delay)

# Static Timing Analysis (STA) - Clocks

**Clock Latency –**




***Total Latency @ FF Pin = Clock Source Latency + Clock Network Latency***



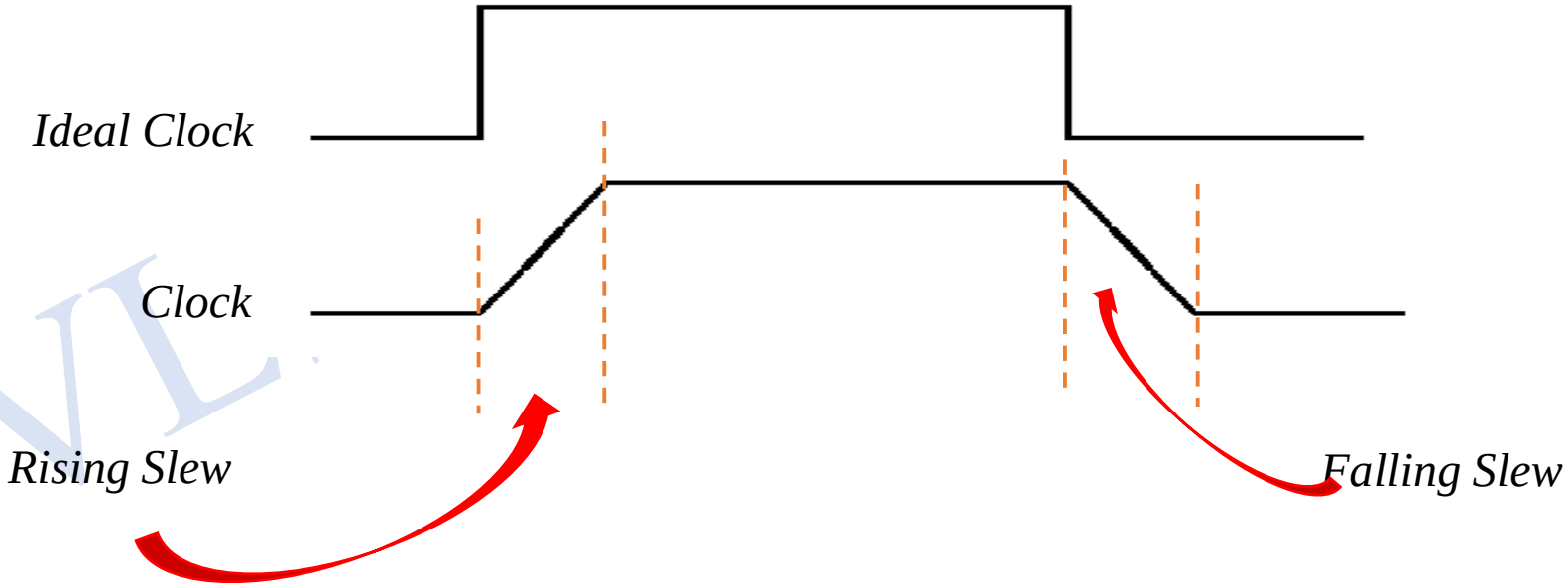

*Total Latency = X + Y*

# Static Timing Analysis (STA) - Clocks

**Clock Slew (Transition Time)** – It is the time taken by the clock signal to change its state from LOW to HIGH or HIGH to LOW

In Ideal Mode, we need to set the clock slew to be read by the STA tool

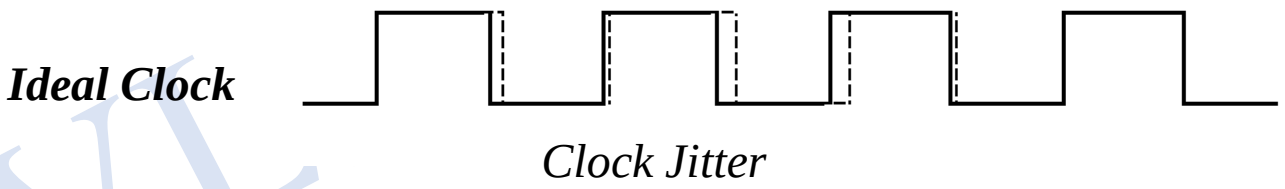
In Propagated Mode, clock slew is automatically calculated by the STA tool after clock buffers are inserted to the design during place and route.



# Static Timing Analysis (STA) - Clocks

## Clock Uncertainty – {Clock Jitter + Clock Skew}

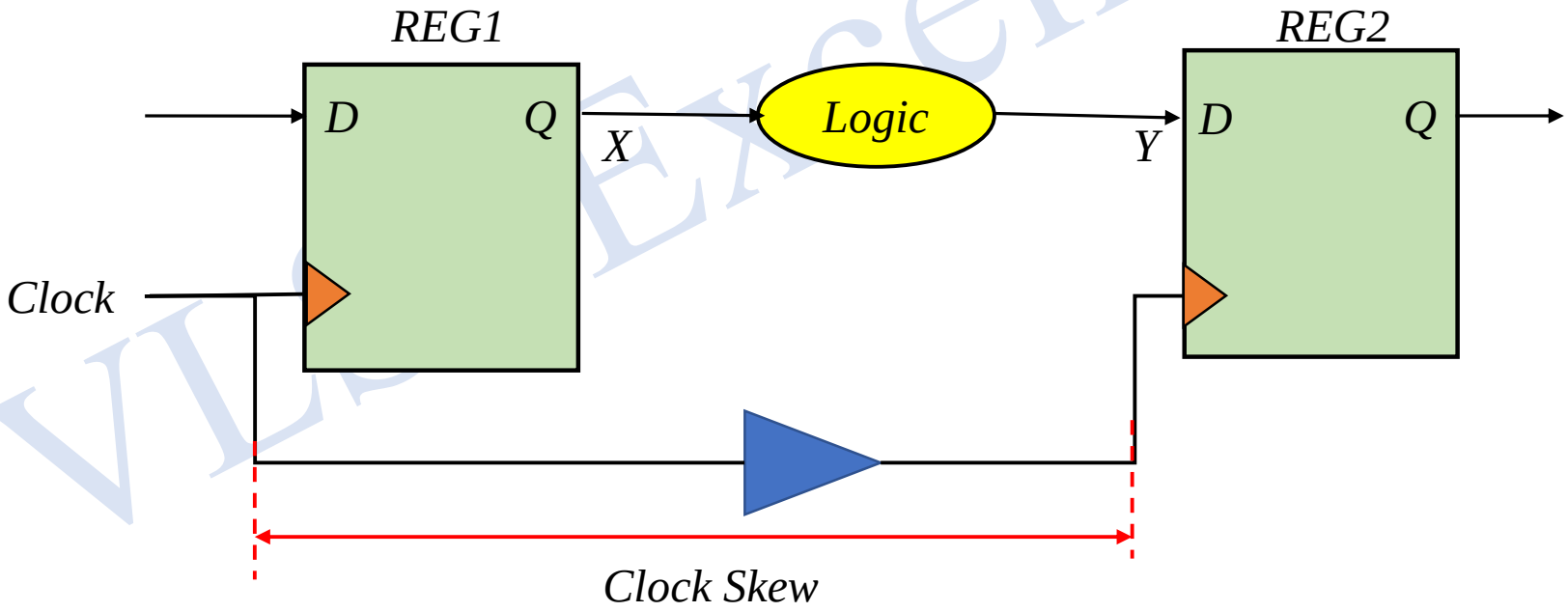
***Clock Jitter*** : The **clock period and duty cycle** of the clock can change cycle by cycle slightly due to clock generation circuitry. This is called Clock Jitter



# Static Timing Analysis (STA) - Clocks

## Clock Uncertainty – {Clock Jitter + Clock Skew}

***Clock Skew*** : When clock signal reaches at different point of times at different sequential components Clock pin because of clock tree and clock buffers, then this difference in clock arrival times is called Clock Skew.



# Static Timing Analysis (STA) - Clocks

## Clock Uncertainty – {Clock Jitter + Clock Skew}

**Note** : Uncertainty in the arrival of clock edges adds pessimism in the design requirements. Combination of Clock Jitter and Clock Skew is used as a value for clock uncertainty.

Hence, ***Clock Uncertainty = Clock Jitter + Clock Skew***

For Setup Timing Check,

***Clock Uncertainty = Clock Jitter + Worst Clock Skew***

For Hold Timing Check,

***Clock Uncertainty = 0 + Best Clock Skew***

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