Static Timing Analysis (STA)

Lecture #03: Characteristics of Timing Arc (Part #01) - Delay

Video Lecture Link

Static Timing Analysis (STA) – Characteristics of Timing Arc

Characteristics of Timing Arc :

1) ***Delay***
2) *Unateness*
3) *Slew*

Note : All the above information of timing arc are derived from Timing Library

Static Timing Analysis (STA) – Characteristics of Timing Arc

1) Delay:

A) Cell Delay

B) Net Delay

A) Cell Delay :

The delay through a cell is determined by -

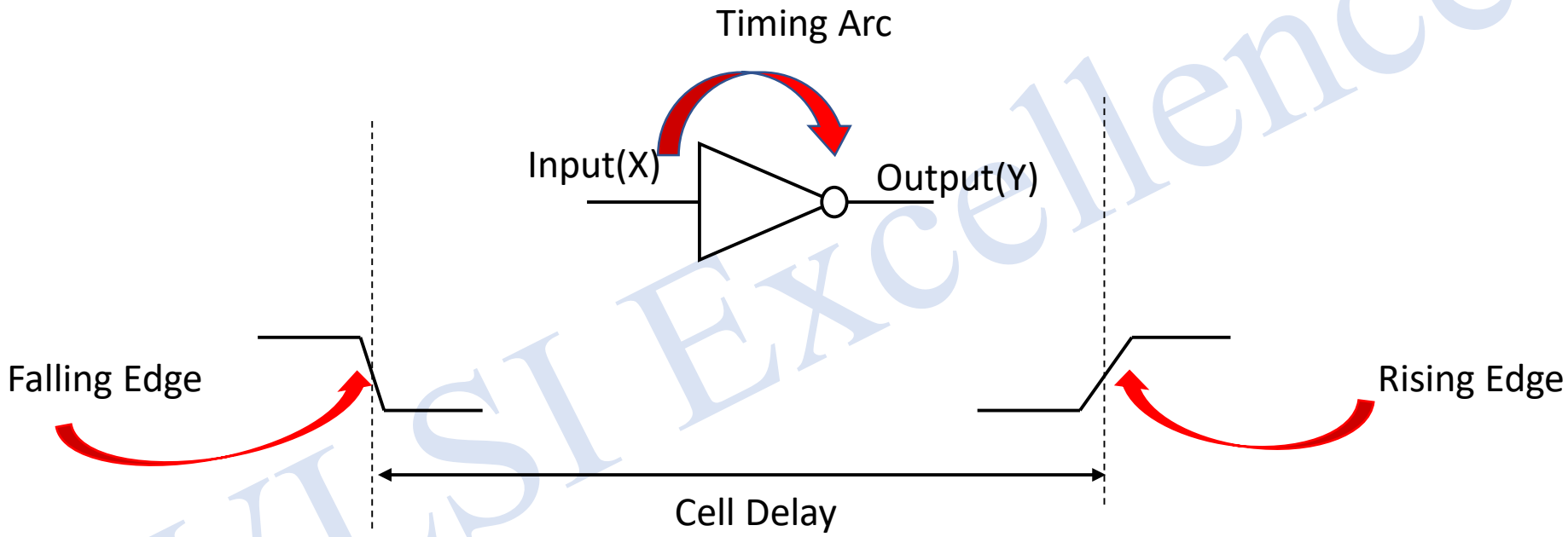
i) The intrinsic delay

ii) The load that it is driving and

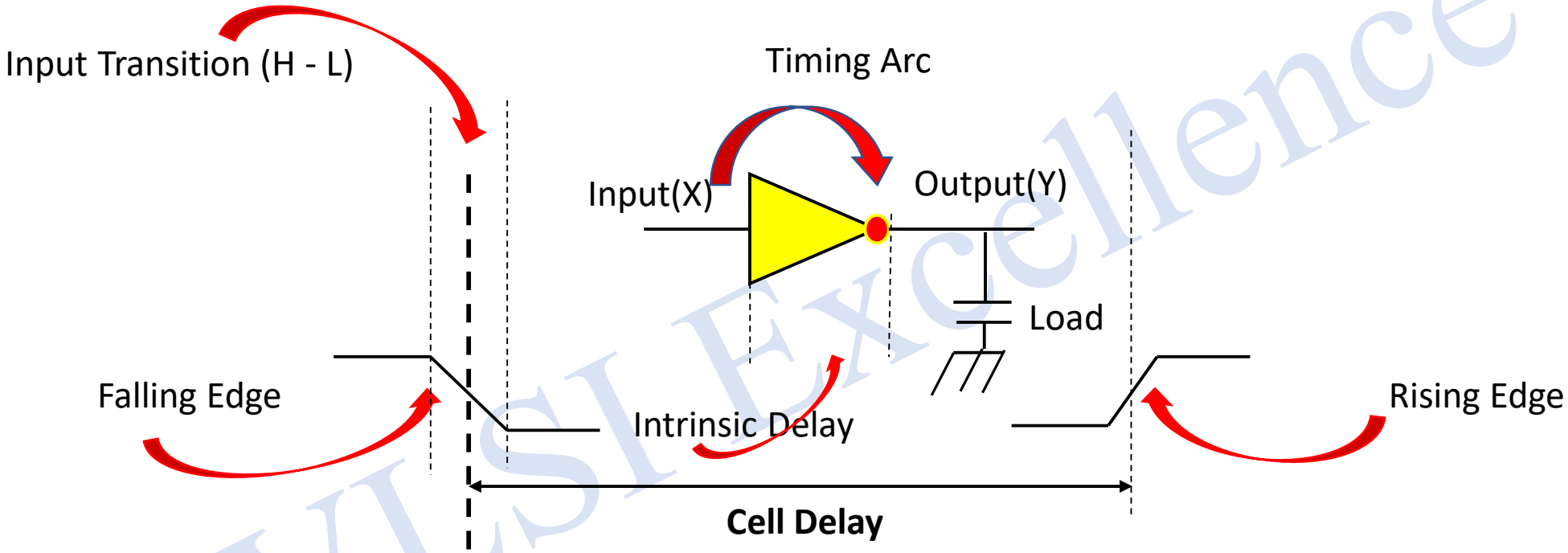
iii) The input transition, also known as input slew

Static Timing Analysis (STA) – Characteristics of Timing Arc

Lets have a look at below pictures for an inverter cell -



Static Timing Analysis (STA) – Characteristics of Timing Arc



Cell Delay = Transition Delay + Intrinsic Delay

Static Timing Analysis (STA) – Characteristics of Timing Arc

Transition Delay : The time it takes for the pin to change state from LOW to HIGH or HIGH to LOW

Intrinsic Delay : Cell Delay when a signal with a zero transition time is applied to the input pin and the output pin does not have any load

By default, STA tools measure the cell delay from 50% of the input signal to 50% of the output signal

Static Timing Analysis (STA) – Characteristics of Timing Arc

B) Net Delay :

- It appears because of the resistance and the capacitance of inter-connect
- ***Wire-Load Models[WLM]*** are used to calculate the net delay
- The delay is calculated based on the block area specification in WL Model
- Next Lecture explains WLM Model with example

Note: Timing information for all the cells is available in liberty (.lib) files

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