Static Timing Analysis (STA)

Lecture #10: Derivation of Setup & Hold Timing Equations, Maximum Operating Frequency

Video Lecture Link

Static Timing Analysis (STA) – Setup & Hold Equations

Something about Clock with respect to Timing Path – They (Timing Paths) are relative/synchronous to a clock

Note:

- Data arrives at a start point relative to a clock
- Data gets captured at a end point relative to a clock
- Starting a new cycle, the clock signal resets the time at the register
- STA tool breaks all the timing paths at registers, so that each timing path has ***one clock cycle*** or ***one clock period*** as the timing goal (**Required Time**)

Static Timing Analysis (STA) – Setup & Hold Equations

Slack :

Slack = Required Time – Arrival Time (***For Setup***)

Slack = Arrival Time – Required Time (***For Hold***)

Required Time : Defined by the timing constraints like Clock Period

Arrival Time : When the signal actually arrives at a end point

Note:

Positive Slack indicates that path Met timing constraint requirement, Negative Slack indicates that path did not Met timing requirements.

Static Timing Analysis (STA) – Setup & Hold Equations

Setup Requirement for Register-to-Register Path:

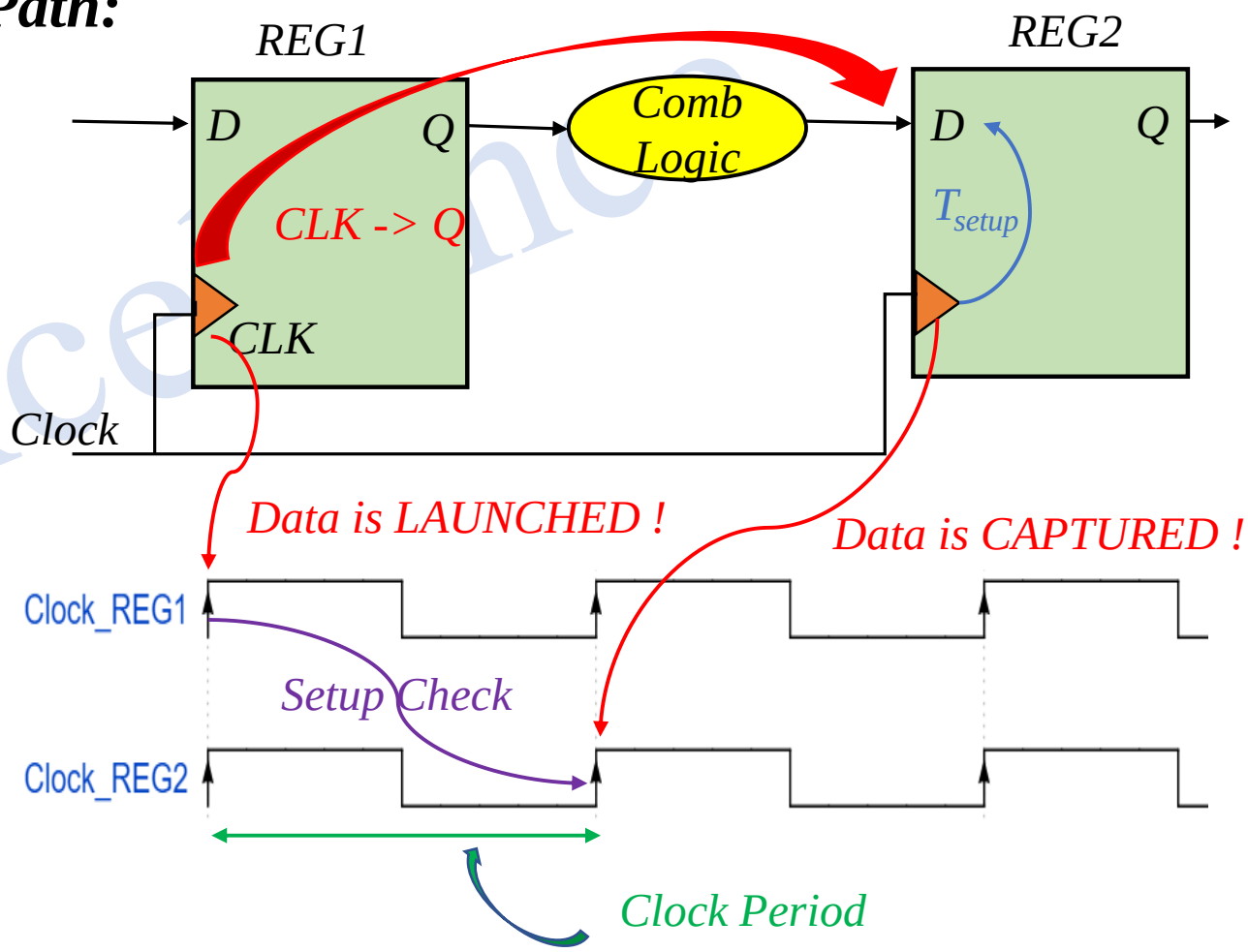
Clk_to_Q [REG1] + Comb Delay <= Clock Period

– T_{setup}[REG2]

Here, Required Time = Clock Period – T_{setup}[REG2]

Arrival Time = Clk_to_Q [REG1] + Comb Delay

Hence, Setup Slack = Required Time – Arrival Time



Static Timing Analysis (STA) – Setup & Hold Equations

Hold Requirement for Register-to-Register Path:

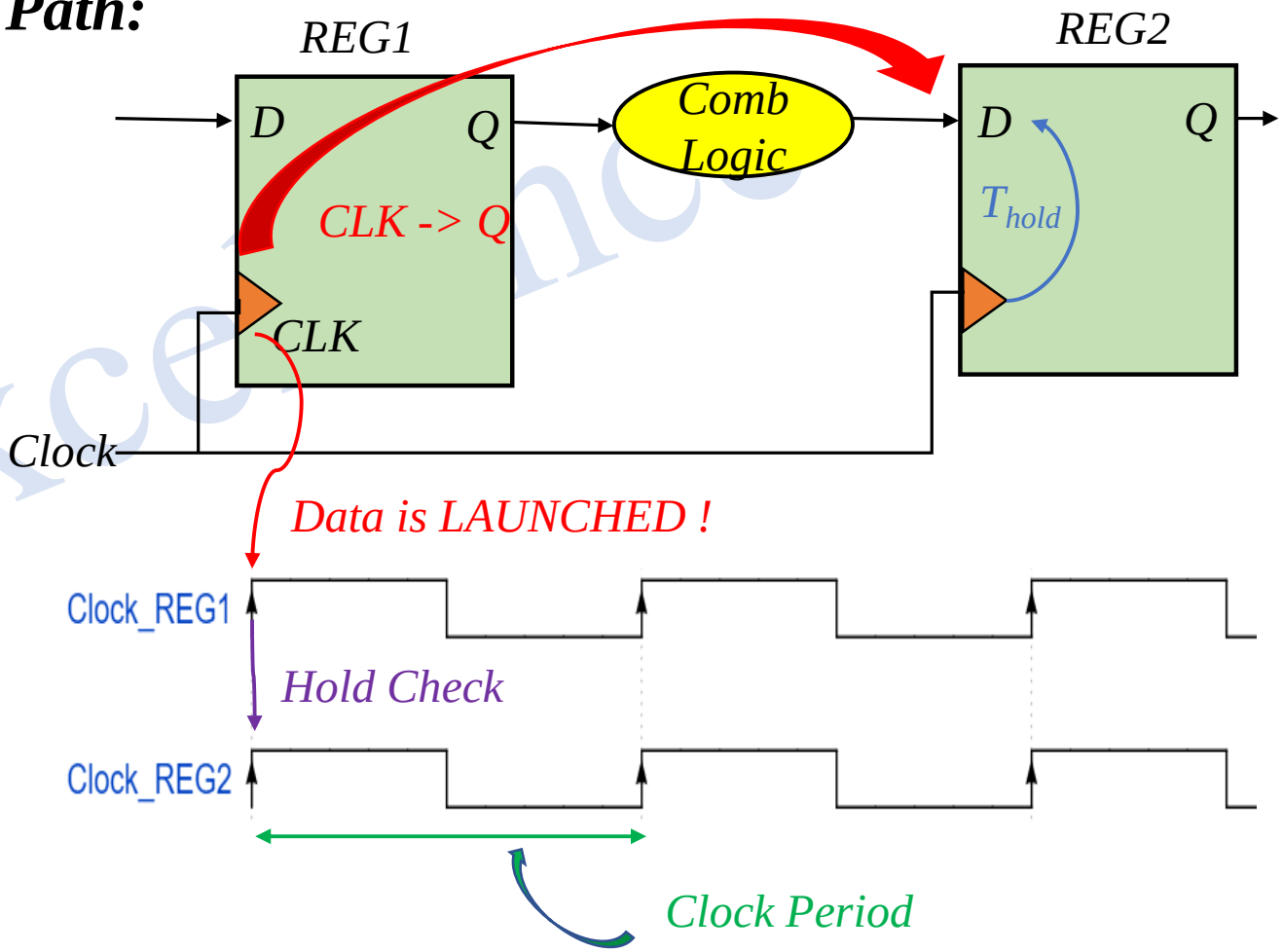
Clk_to_Q [REG1] + Comb Delay >= Hold_Check[0]
+ T_{hold} [REG2]

Here, Required Time = Hold_Check[0] + T_{hold} [REG2]

Arrival Time = Clk_to_Q [REG1] + Comb Delay

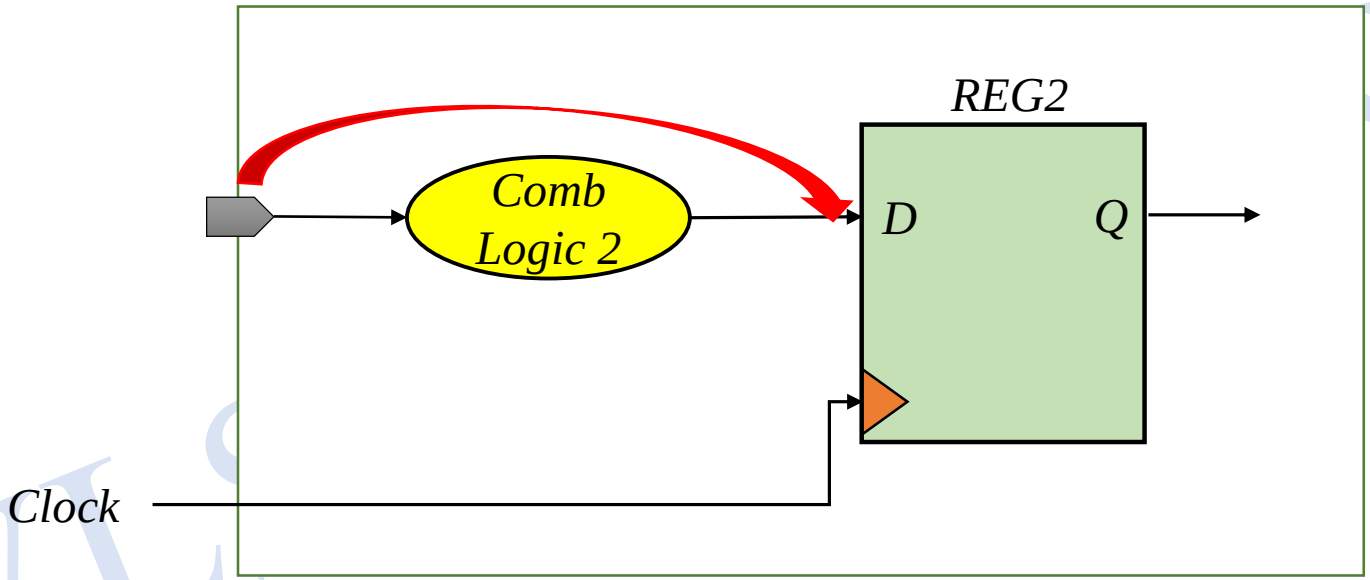
Hence, Hold Slack = Arrival Time – Required Time

Note: Default Hold Check is at 0



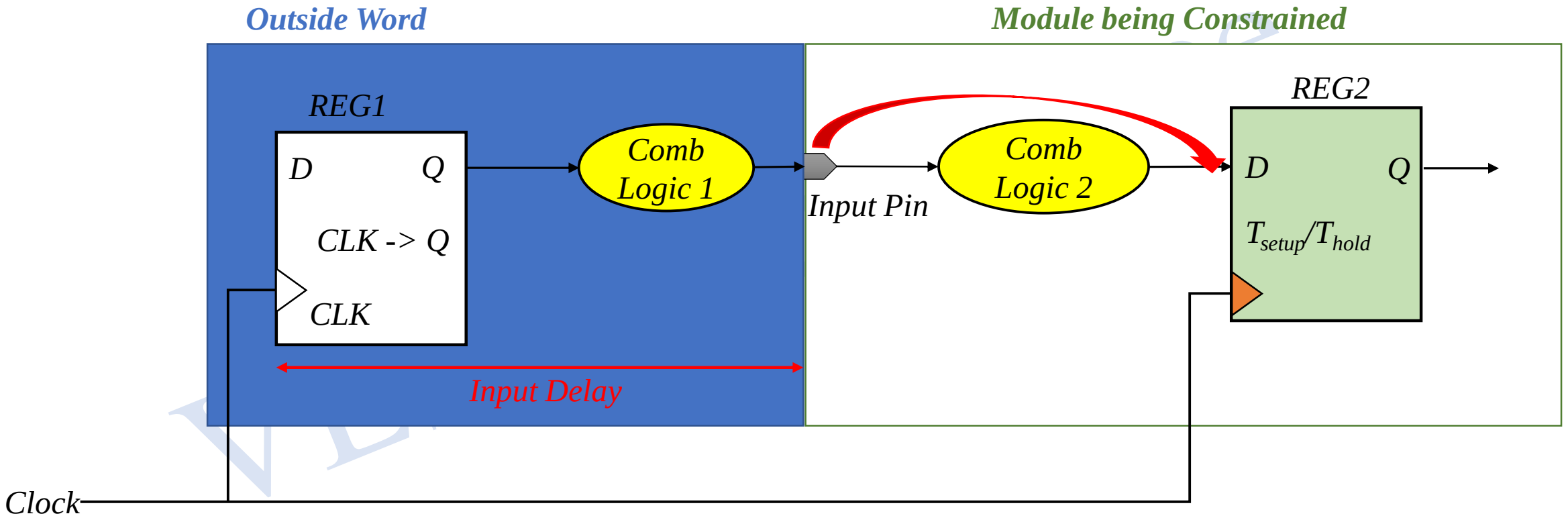
Static Timing Analysis (STA) – Setup & Hold Equations

Input-to-Register Path:

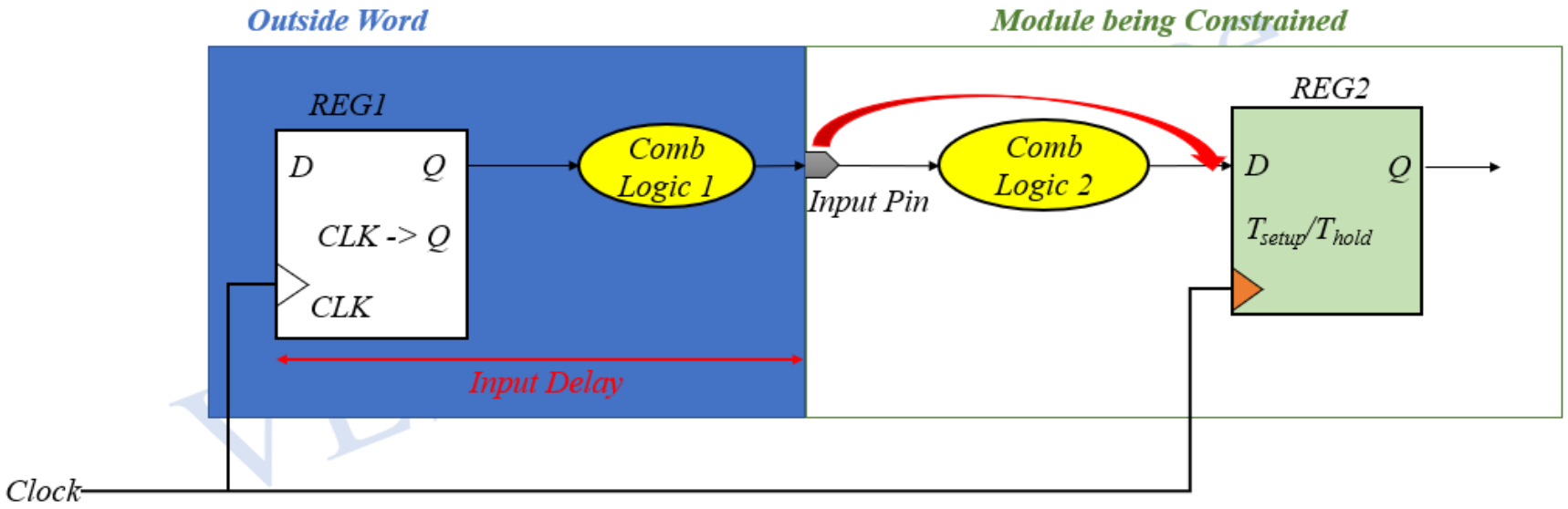


Static Timing Analysis (STA) – Setup & Hold Equations

Setup Requirement for Input-to-Register Path:



Static Timing Analysis (STA) – Setup & Hold Equations



Required Time = Clock Period – T_{setup} [REG2]

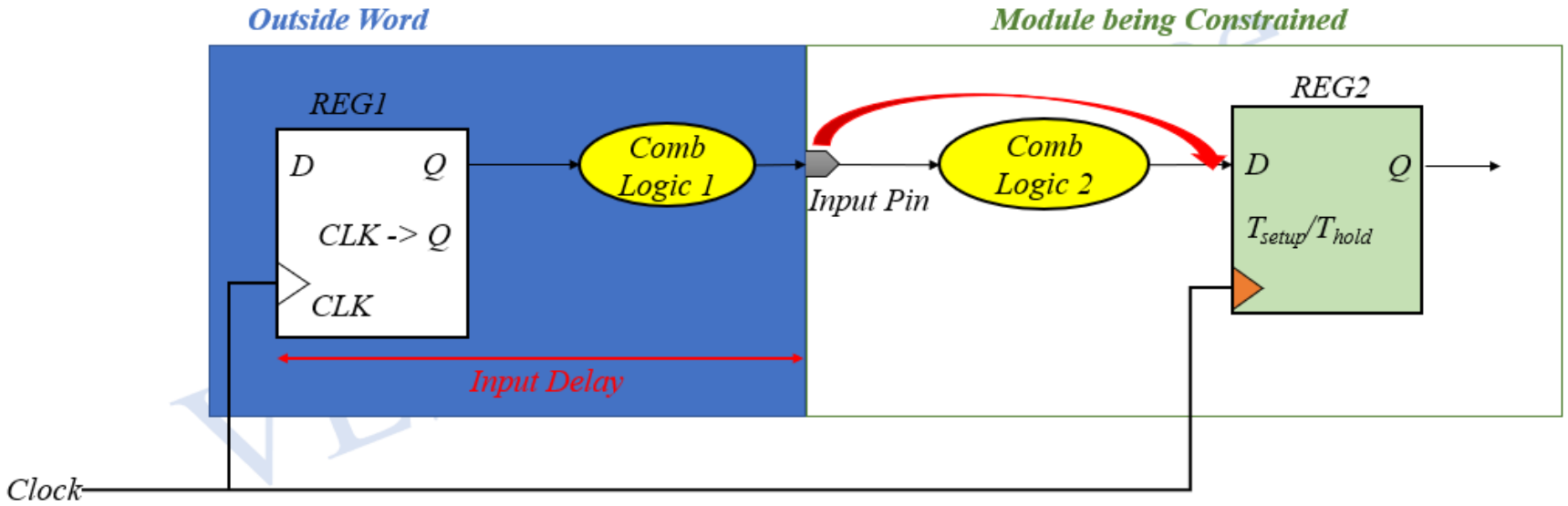
Arrival Time = {Clk_to_Q[REG1] + Comb Logic 1 Delay} + Comb Logic 2 Delay

Arrival Time = Input Delay + Comb Logic 2 Delay

Setup Slack = Required Time – Arrival Time

Static Timing Analysis (STA) – Setup & Hold Equations

Hold Requirement for Input-to-Register Path:



Required Time = Hold_Check[0] + T_{hold} [REG2]

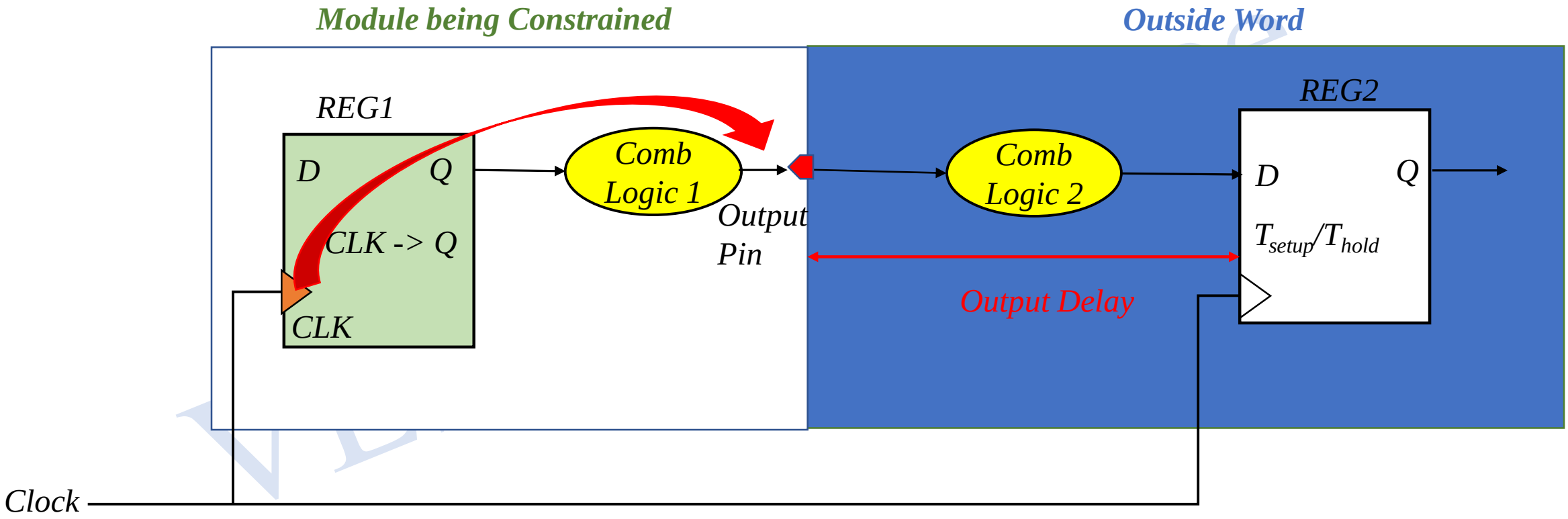
Arrival Time = {Clk_to_Q[REG1] + Comb Logic 1 Delay} + Comb Logic 2 Delay

Arrival Time = Input Delay + Comb Logic 2 Delay

Hold Slack = Arrival Time – Required Time

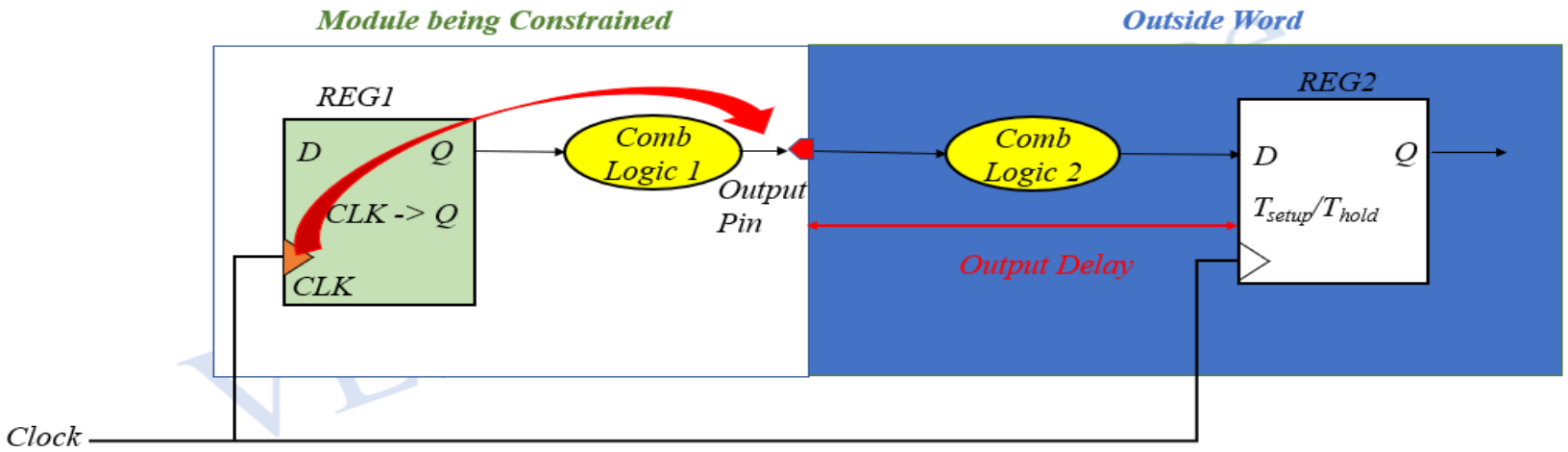
Static Timing Analysis (STA) – Setup & Hold Equations

Setup Requirement for Register-to-Output Path:



Static Timing Analysis (STA) – Setup & Hold Equations

Setup Requirement for Register-to-Output Path:



Required Time = Clock Period – T_{setup} [REG2]

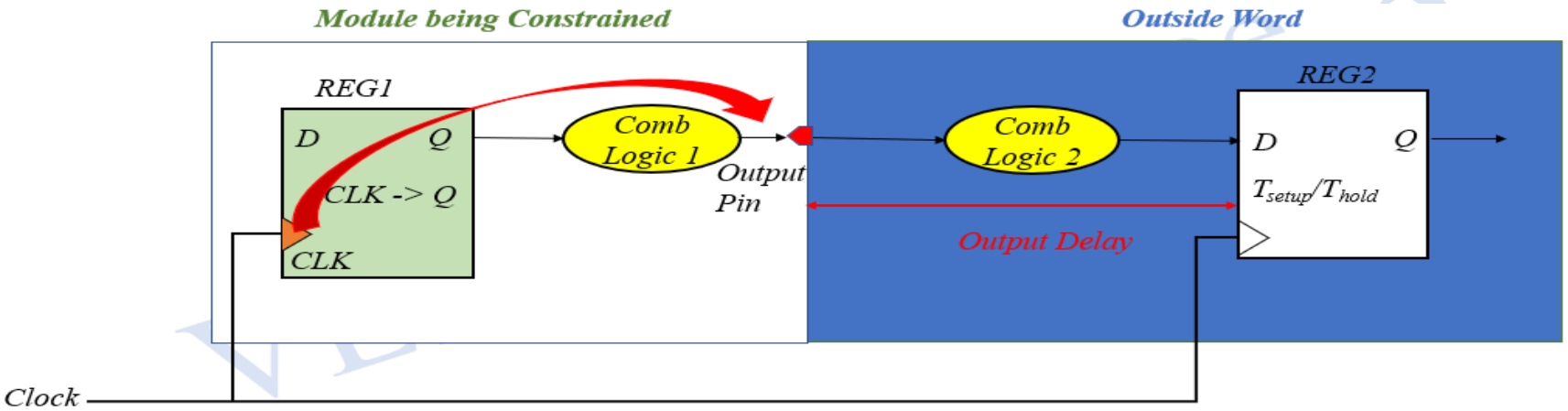
Arrival Time = Clk_to_Q [REG1] + Comb Logic 1 Delay + Comb Logic 2 Delay

Arrival Time = Clk_to_Q [REG1] + Comb Logic 1 Delay + **Output Delay**

Setup Slack = Required Time – Arrival Time

Static Timing Analysis (STA) – Setup & Hold Equations

Hold Requirement for Register-to-Output Path:



Required Time = Hold_Check[0] + T_{hold} [REG2]

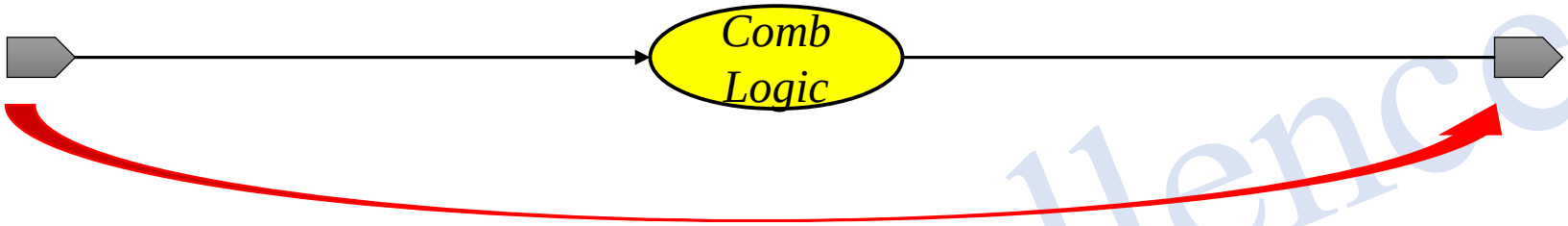
Arrival Time = Clk_to_Q [REG1] + Comb Logic 1 Delay + Comb Logic 2 Delay

Arrival Time = Clk_to_Q [REG1] + Comb Logic 1 Delay + **Output Delay**

Setup Slack = Arrival Time – Required Time

Static Timing Analysis (STA) – Setup & Hold Equations

Input – to – Output Path Timing Requirements:



There is no clock defined for combinational paths. So, we need to use either a virtual clock or set path delays to Constrain input to output paths

Using Virtual Clock or Dummy Clock –

Slack = Clock Period – Input Delay – Output Delay – Comb Logic Delay

Note: Input Delay and Output Delay are set with respect to a Clock

Static Timing Analysis (STA) – Setup & Hold (Summary)

1) For setup constraints, the data has to be propagate fast enough to be captured by the next clock edge.

- *This sets our maximum frequency*

- *If we have setup failures, we can always just slow down the clock*

2) For Hold constraints the data path delay has to be long enough so it is not accidently captured by the same clock edge

- *This is independent of the clock period*

- *If there is hold failure, you can throw your chip away!!!*

Static Timing Analysis (STA) – Maximum Operating Frequency

Maximum Operating Frequency:

Clk_to_Q [REG1] + Comb Delay <= Clock Period $- T_{setup}$[REG2] {Setup Equation}

Clock Period (T) >= Clk_to_Q[REG1] + Comb Delay + T_{setup}(REG2)

So, Minimum Clock Period (T) = Clk_to_Q[REG1] + Comb Delay + T_{setup}(REG2)

Hence, Maximum Clock Frequency = 1/T

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