Static Timing Analysis (STA)

Lecture #05: Characteristics of Timing Arc (Part #02) - Unatenes

Video Lecture Link

Static Timing Analysis (STA) – Characteristics of Timing Arc

Characteristics of Timing Arc :

1) *Delay*

2) Unateness

3) Slew

Static Timing Analysis (STA) – Characteristics of Timing Arc - Unateness

2) Unateness:

How the output (of a cell) changes for different types of transition on input

Specifies how the output is responding for a particular input and how much time it will take

A timing arc can have 3 types of unateness

A) Positive unate:

- When rising input results in rising output OR falling input results in falling output
- Example : Buffer, AND , OR

Static Timing Analysis (STA) – Characteristics of Timing Arc - Unateness

B) Negative unate:

- When rising transition on input results in falling transition on output OR falling transition in input results in rising transition on output

- Example : Inverter, NAND

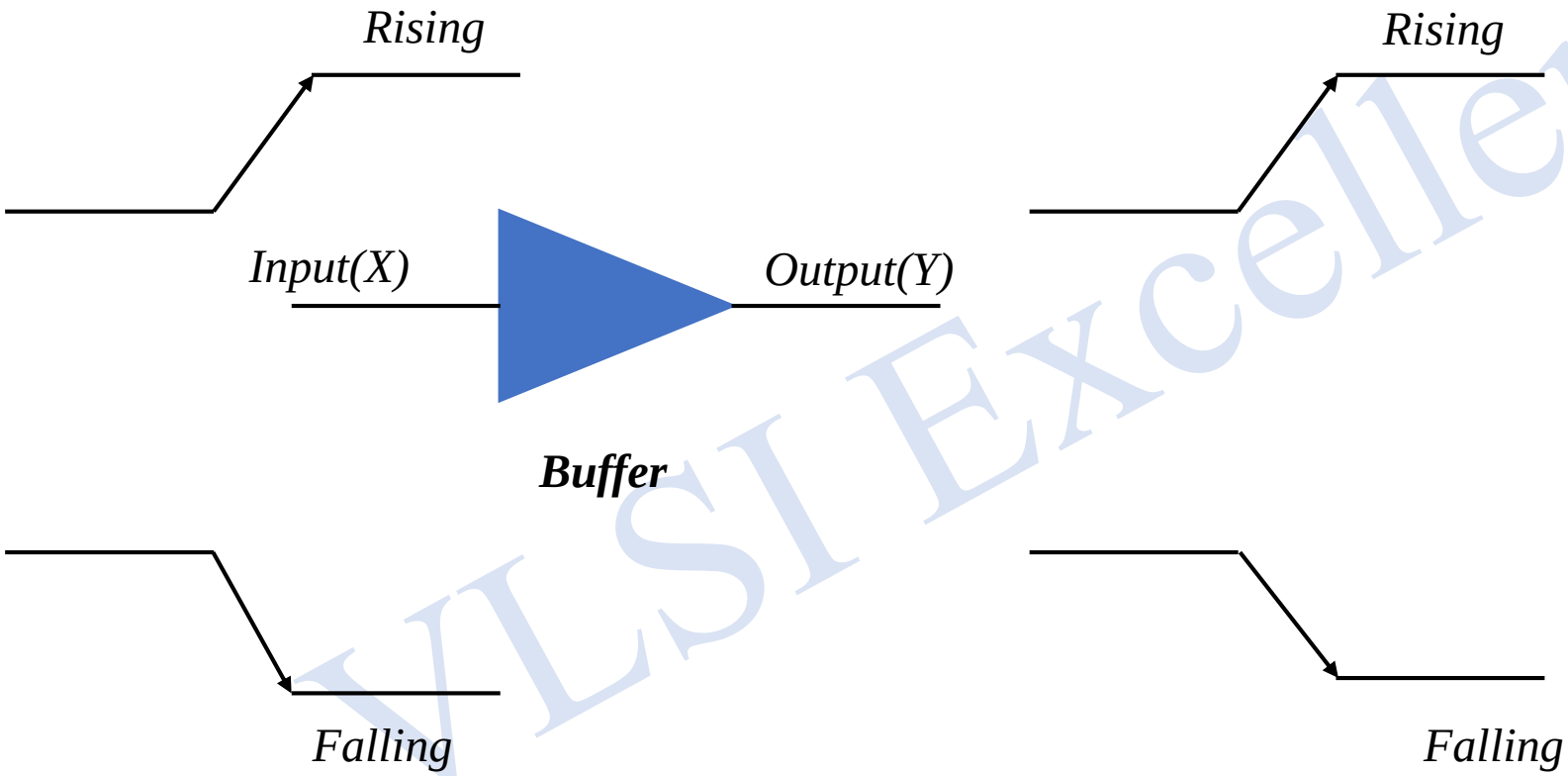
C) Non-unate:

- No relationship between input (source) and output (sink) pin

- Example : XOR, XNOR

Static Timing Analysis (STA) – Characteristics of Timing Arc - Unateness

Example: Buffer

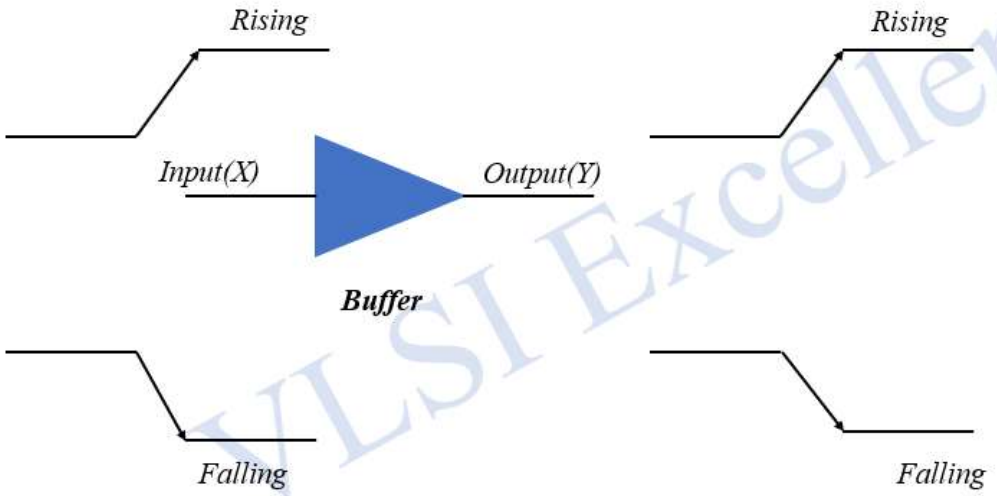


Note : Output Exactly Follows Input

=> Positive Unate

Static Timing Analysis (STA) – Characteristics of Timing Arc - Unateness

Example: Buffer



Note : Output Exactly Follows Input

=> Positive Unate

```
pin(X) {
   direction : input;
   -
   -
 }
 pin(Y) {
   direction : output;
   power_down_function : "!VDD + VSS";
   function : "X";
   timing () {
    related_pin : "X";
    timing_sense : positive_unate;
    timing_type : combinational;
```

Example: Buffer Liberty File

Static Timing Analysis (STA) – Characteristics of Timing Arc - Unateness

Example: AND Gate

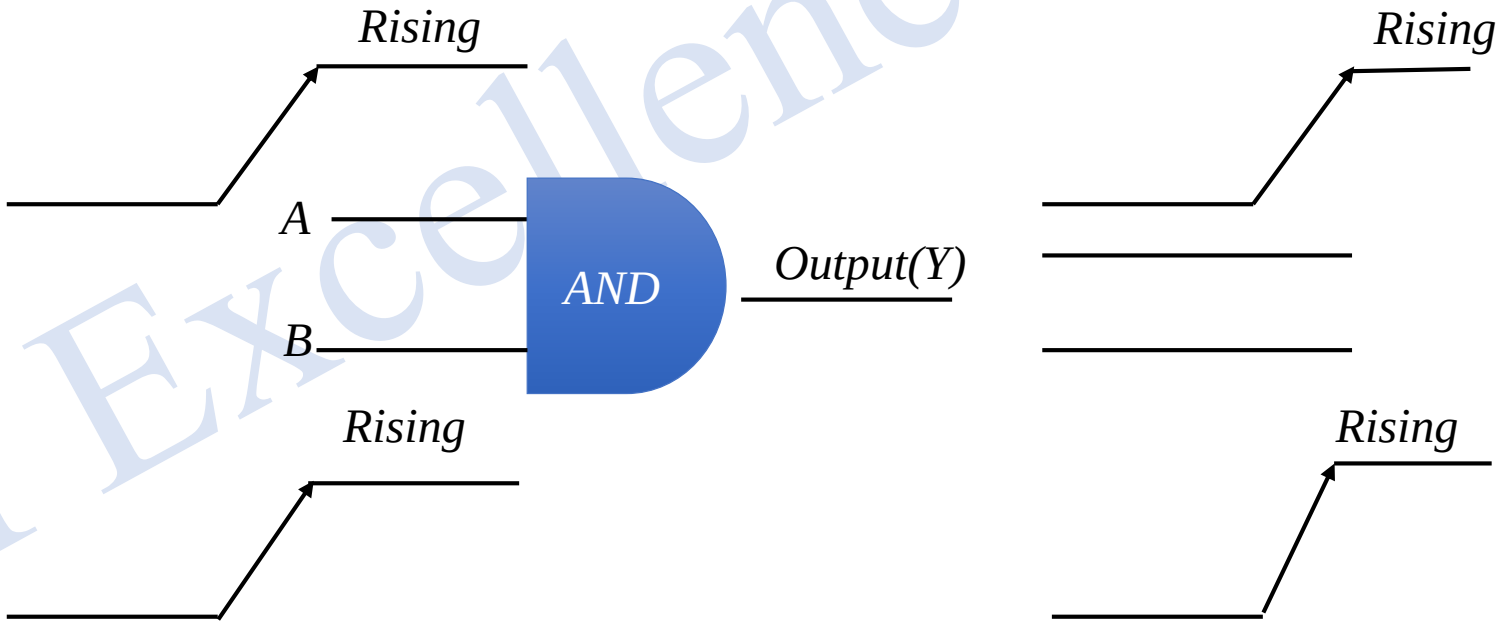
1) For rising edge –

A = 0; B (0 -> 1) => Y = 0
(No Change, Constant)

A = 1; B (0 -> 1) => Y (0 -> 1)
(Change and follows B)

A (0 -> 1) ; B = 0 => Y = 0
(No Change)

A(0 -> 1) ; B = 1 => Y (0 -> 1)
(Change and follows A)



Static Timing Analysis (STA) – Characteristics of Timing Arc - Unateness

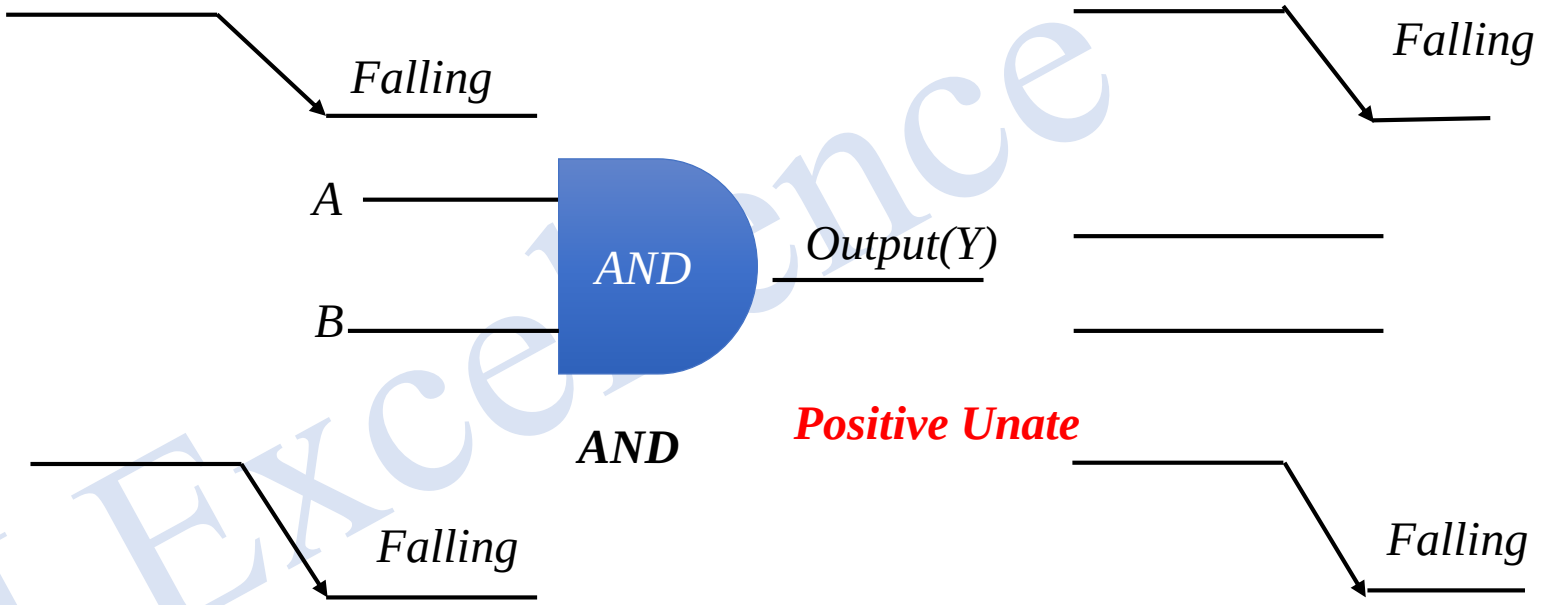
2) For falling edge -

A = 0; B (1 -> 0) => Y = 0
(No Change, Constant)

A = 1; B (1 -> 0) => Y (1 -> 0)
(Change and follows B)

A (1 -> 0) ; B = 0 => Y = 0
(No Change)

A(1 -> 0) ; B = 1 => Y (1 -> 0)
(Change and follows A)



Note: *Rising input results in rising output and falling input results in falling output*

=> Positive Unate

Static Timing Analysis (STA) – Characteristics of Timing Arc - Unateness

Example: Inverter

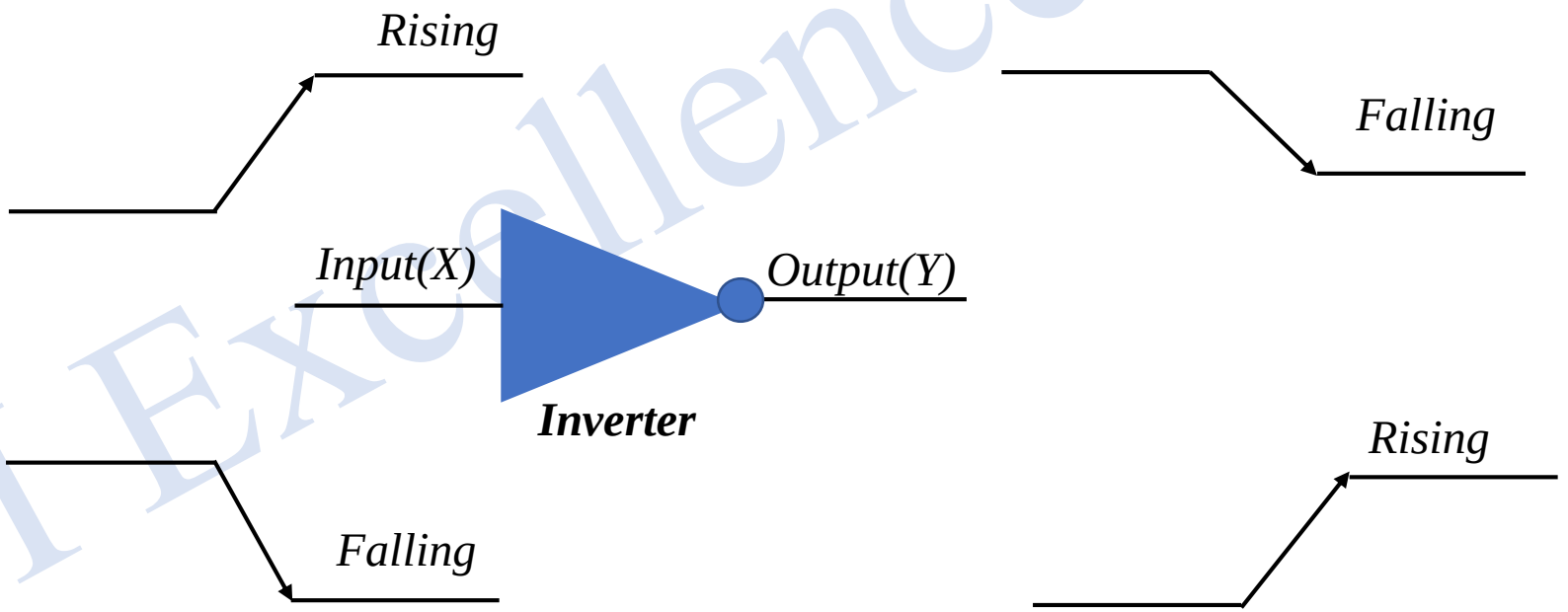
There are two timing arcs in inverter -

A) Rising input A to Y (Falling output Y)

B) Falling input A to Y (Rising output Y)

Note : Output is inversely proportional to the input edge

- Negative Unate



Static Timing Analysis (STA) – Characteristics of Timing Arc - Unateness

Example: X-OR Gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

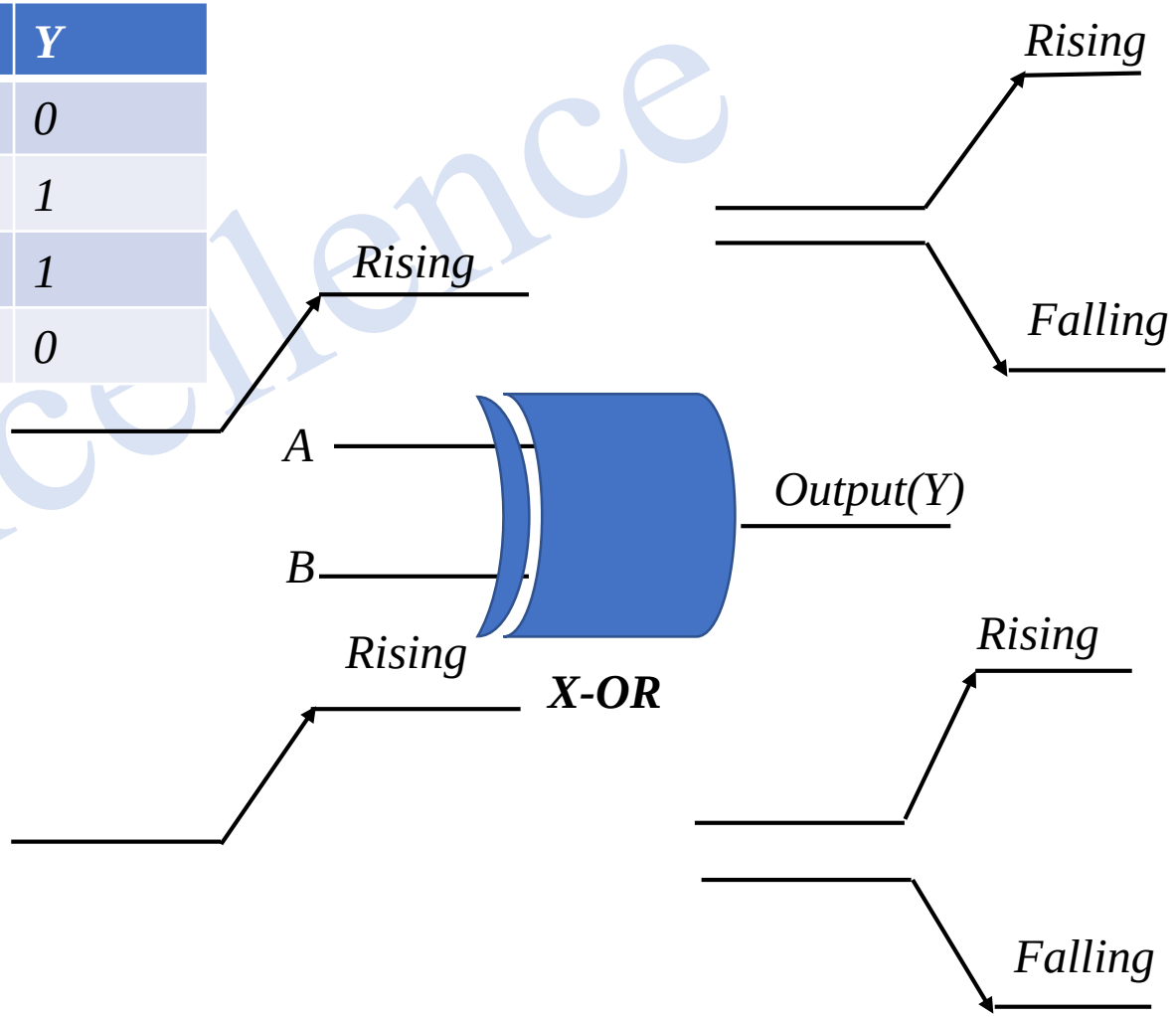
1) For rising edge -

A = 0; B (0 -> 1) => Y (0 -> 1)
(Change and follows B)

A = 1; B (0 -> 1) => Y (1 -> 0)
(Change and follows B with inverted edge)

A (0 -> 1) ; B = 0 => Y (0 -> 1)
(Change and follows A)

A(0 -> 1) ; B = 1 => Y (1 -> 0)
(Change and follows A with inverted edge)



Static Timing Analysis (STA) – Characteristics of Timing Arc - Unateness

2) For Falling edge -

A = 0; B (1 -> 0) => Y (1 -> 0)
(Change and follows B)

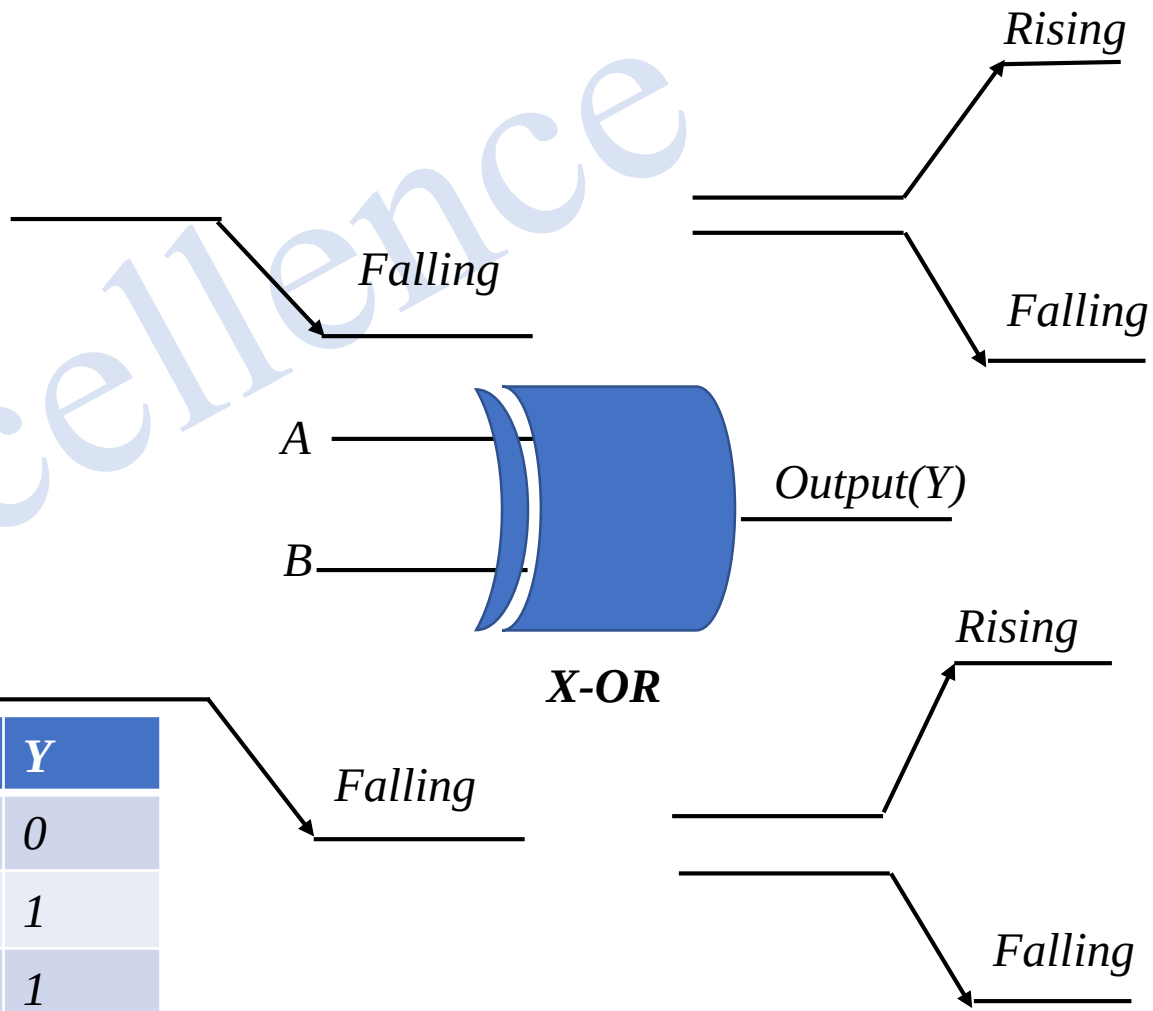
A = 1; B (1 -> 0) => Y (0 -> 1)
(Change and follows B with inverted edge)

A (1 -> 0) ; B = 0 => Y (1 -> 0)
(Change and follows A)

A(1 -> 0) ; B = 1 => Y (0 -> 1)
(Change and follows A with inverted edge)

Note : The output transition can not be determined by the direction of an input and it also depends on the state of other inputs

- Non-unate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Static Timing Analysis (STA) – Characteristics of Timing Arc - Unateness

Exercise #1 : Find out the Unateness of NOR Gate

Best Free VLSI Content

1. Verilog HDL Crash Course – Link
2. Static Timing Analysis (STA) – Theory Concepts – Link
3. Static Timing Analysis (STA) – Practice/Interview Questions – Link
4. Low Power VLSI Design – Theory Concepts – Link
5. Low Power VLSI Design (LPVLSI) – Practice/Interview Questions – Link
6. Digital ASIC Design Verilog Projects – Link

Please Like, Comment, Share & Subscribe My Channel in Order to Reach Out the Content to a Larger Audience.

Thanks !!