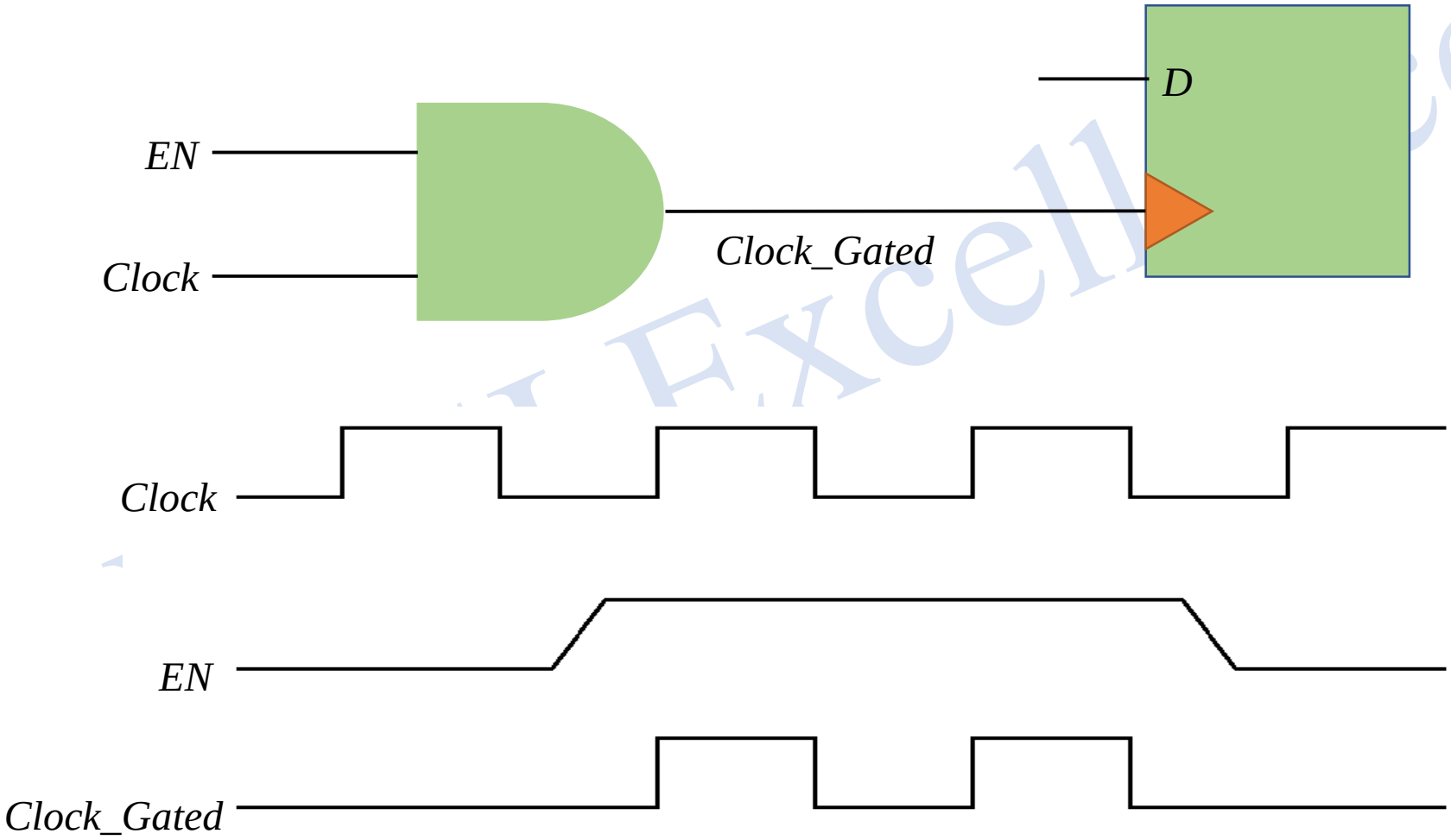
Static Timing Analysis (STA)

Lecture #16: Clock Gating Timing Checks

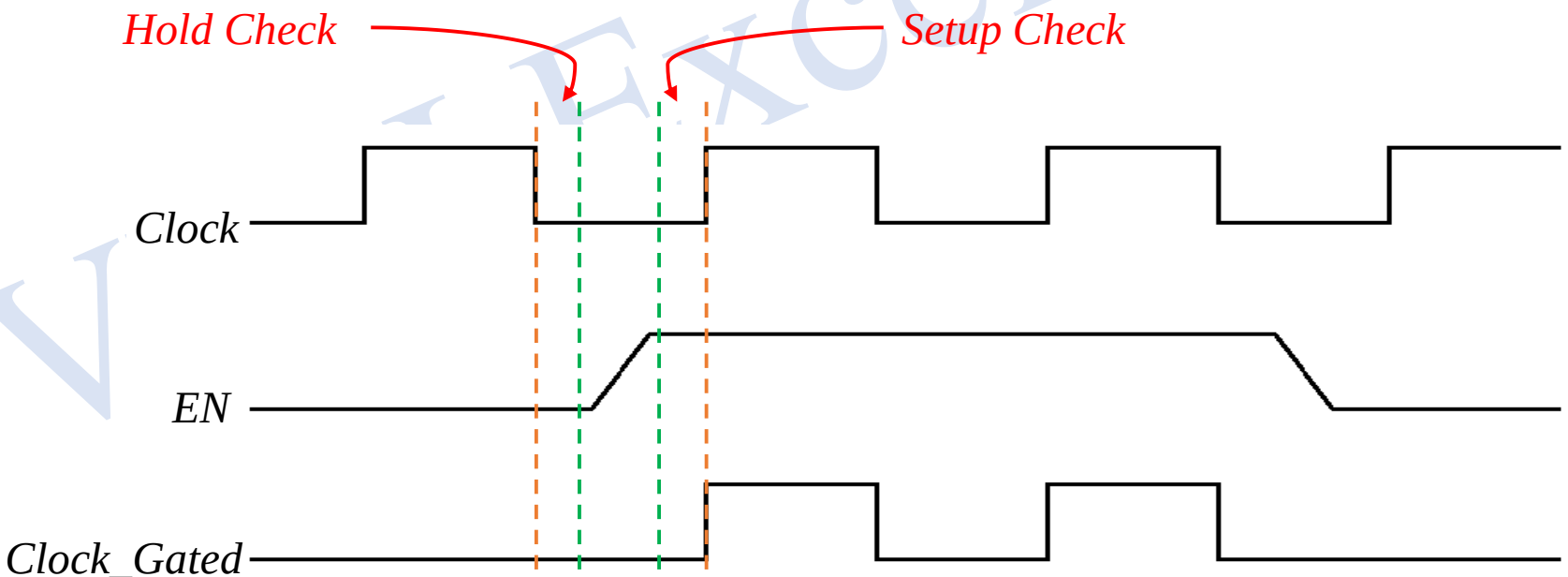
Video Lecture Link

AND Gate Based Clock Gating Circuit

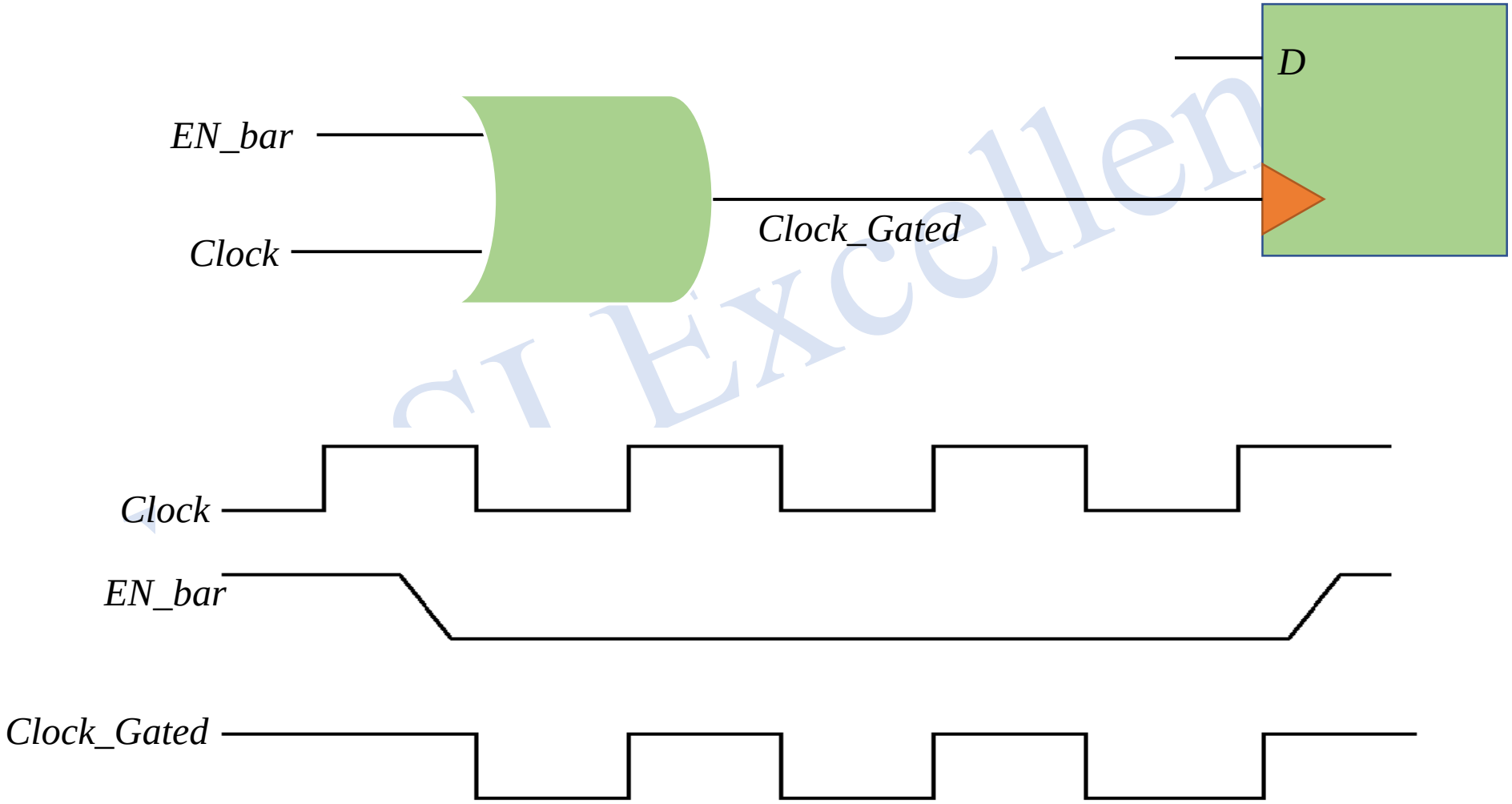


AND Gate Based Clock Gating Circuit

To prevent any glitch being propagated to the output of AND gate based clock gating, the enable should toggle only when the clock is LOW !!!

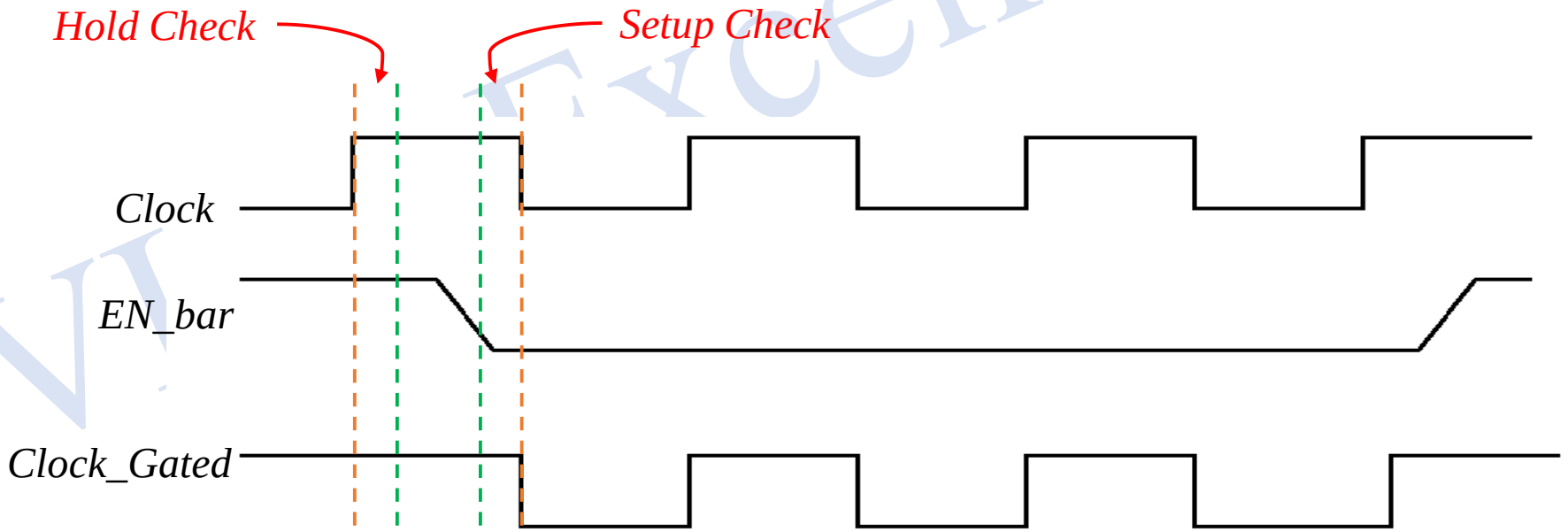


OR Gate Based Clock Gating Circuit

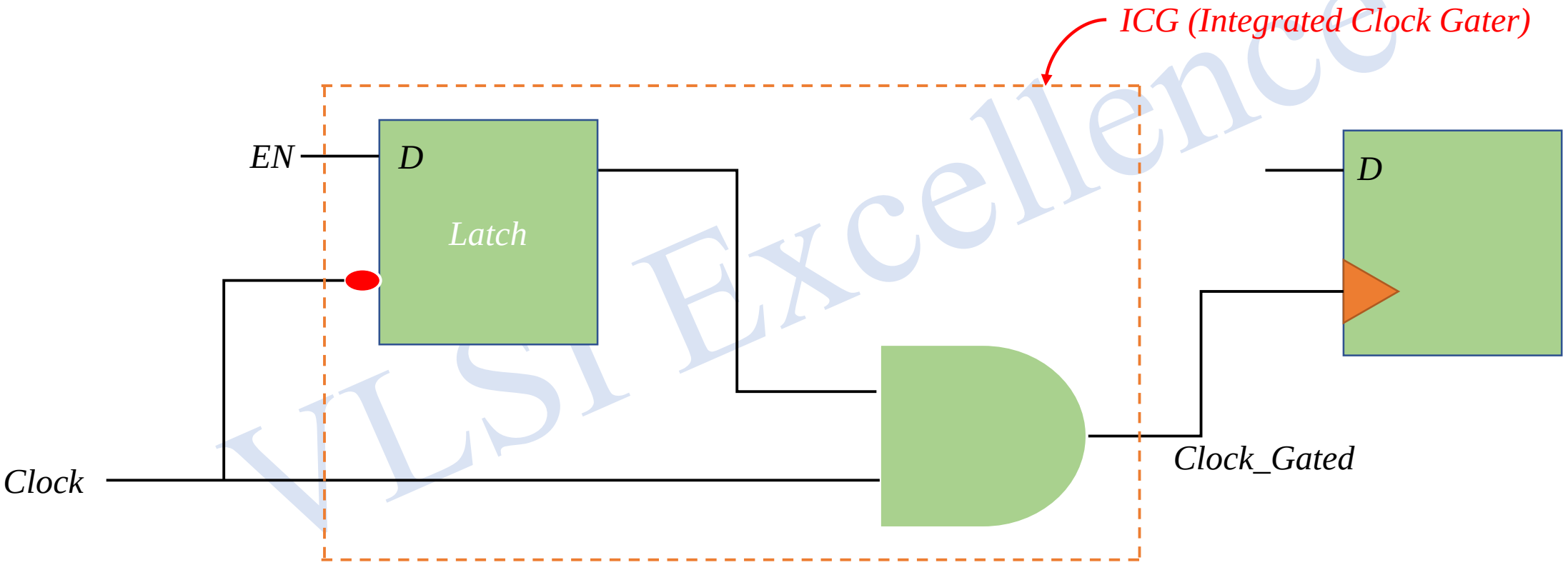


OR Gate Based Clock Gating Circuit

To prevent any glitch being propagated to the output of OR gate based clock gating, the enable should toggle only when the clock is HIGH !!!

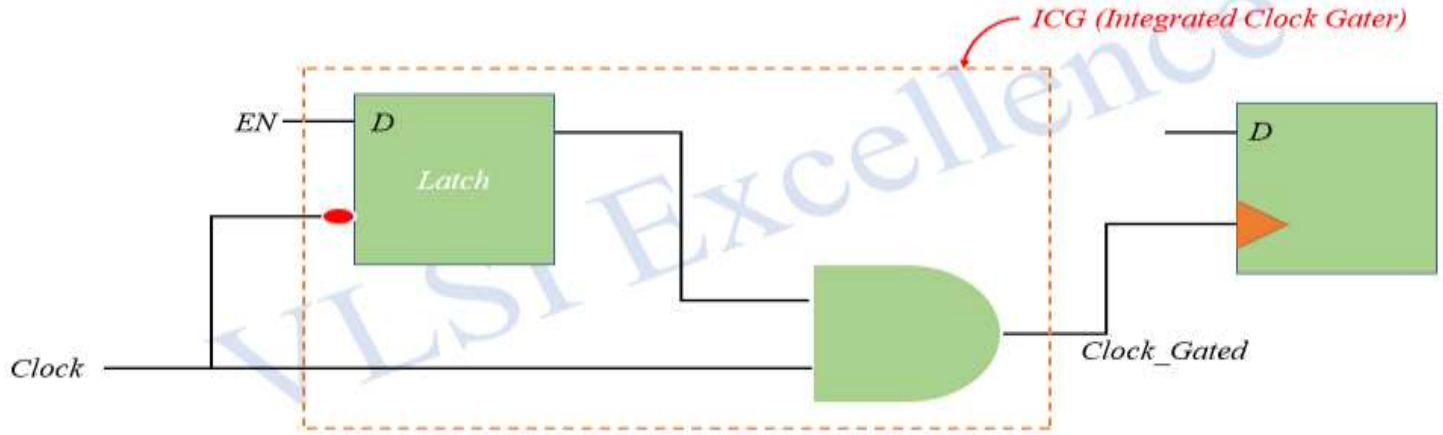


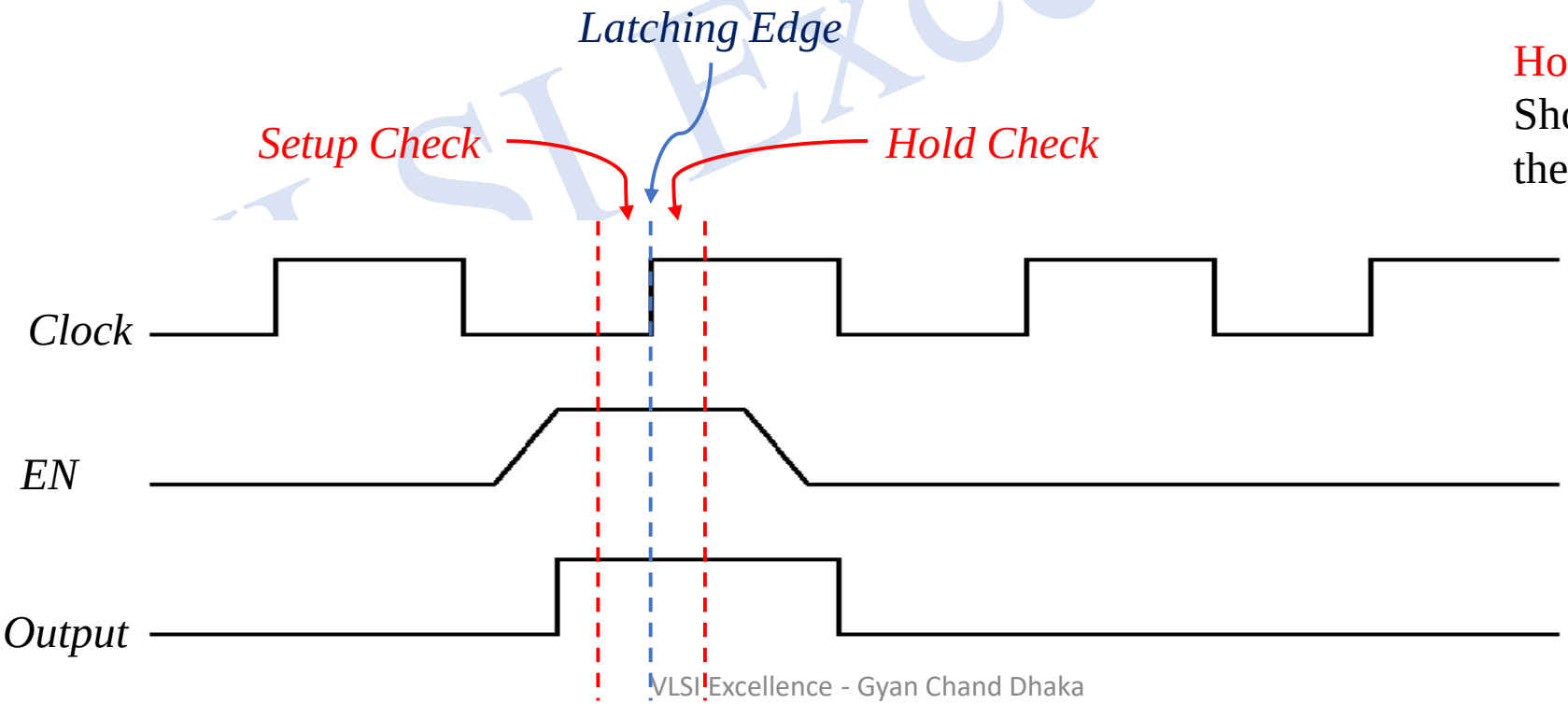
Latch Based Integrated Clock Gating Circuit



Latch Based Integrated Clock Gating Circuit

Setup : Minimum Time EN Should be Stable before the Latching Edge !!!





Hold : Minimum Time EN Should be Stable after the Latching Edge !!!

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Thanks !!