Static Timing Analysis (STA)

Lecture #02: Standard Cells & Timing Arcs

Video Lecture Link

Static Timing Analysis (STA) – Standard Cells

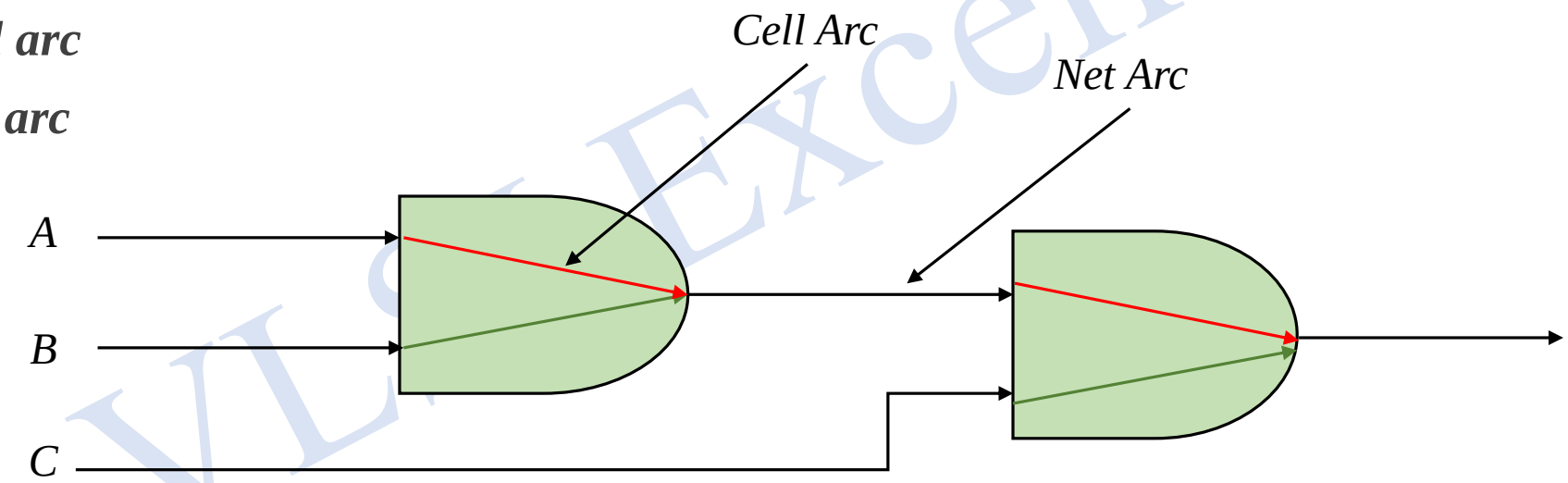
- The functionality of a chip is designed using the basic blocks of combinational logic gates (AND, OR, NAND, NOR, AOI, OAI) and sequential elements (Flip-Flops, Latches).
- These blocks are predesigned and called standard cells
- The timing information and functionality of these standard cells is available to the user in the form of nothing but called standard cell libraries. (Will be covering the Standard Cell Library in Incoming STA Chapter)

Static Timing Analysis (STA) – Timing Arc

- A path from each input pin to the each output pin of a cell
- Timing Arc provide a simple understanding of the structure and the functionality of a Gate
- Timing arcs are of two types -

1) *Cell arc*

2) Net arc

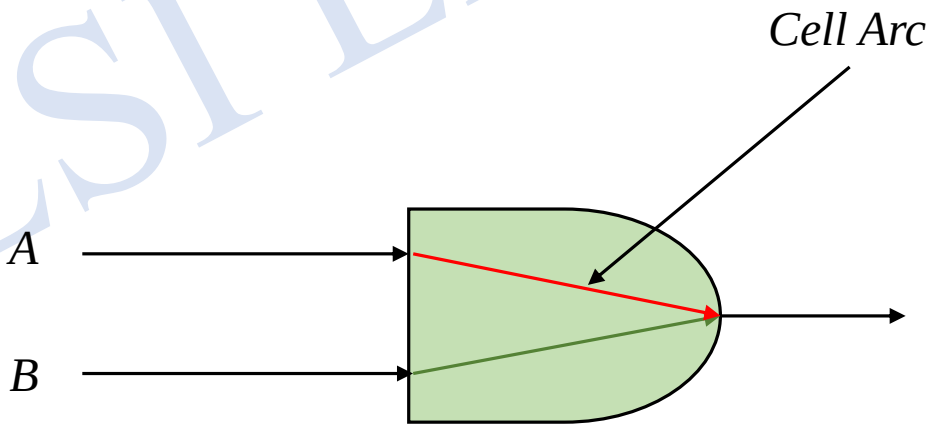


Static Timing Analysis (STA) – Timing Arc

1) Cell Arc:

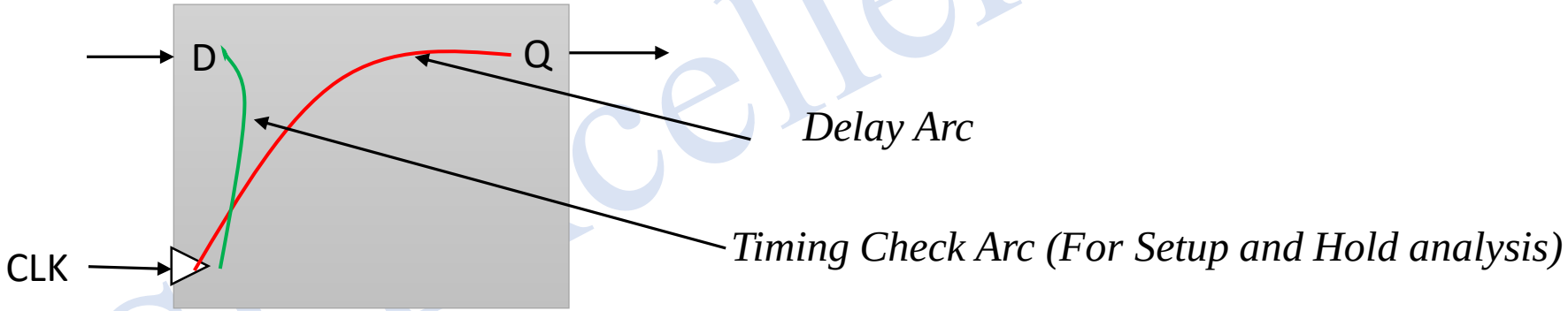
- Between an input pin and output pin of cell
- Cell arcs are of two types -
  - *A) Combinational Cell Arc*
  - *B) Sequential Cell Arc*

A) Combinational Cell Arc : Between input and output of a combinational cell



Static Timing Analysis (STA) – Timing Arc

B) Sequential Cell Arc :

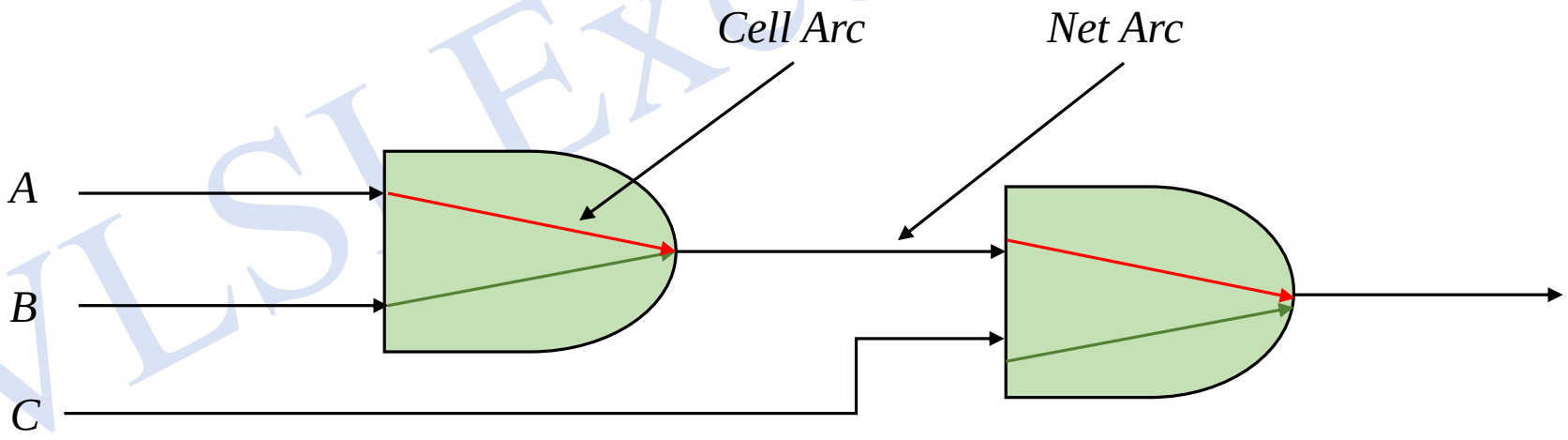


- Arc between the clock pin and the input data pin are known as timing check arcs (**Setup and hold timing arcs**)
- The arc between the clock pin and the flip-flop output pin is sequential delay arc (**Clock to Q Delay**)

Static Timing Analysis (STA) – Timing Arc

2) Net Arc :

- The arc between **source pin** (output pin of a cell) and the **sink pin** (input pin of an another cell)
- These arcs are always a delay timing arcs



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