Static Timing Analysis (STA)

Lecture #08: Flip-Flop Timing Parameters

Video Lecture Link

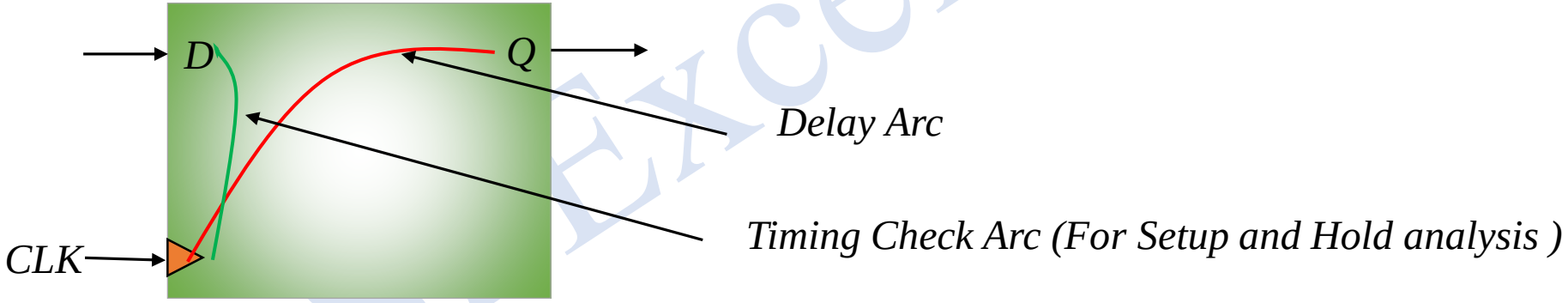
Static Timing Analysis (STA) – Flip-Flop Timing Parameters

The important timing parameters of a flip-flop are –

1) Clock-to-Q Delay
2) Setup Time
3) Hold Time

Static Timing Analysis (STA) – Flip-Flop Timing Parameters – Clock-to-Q Delay

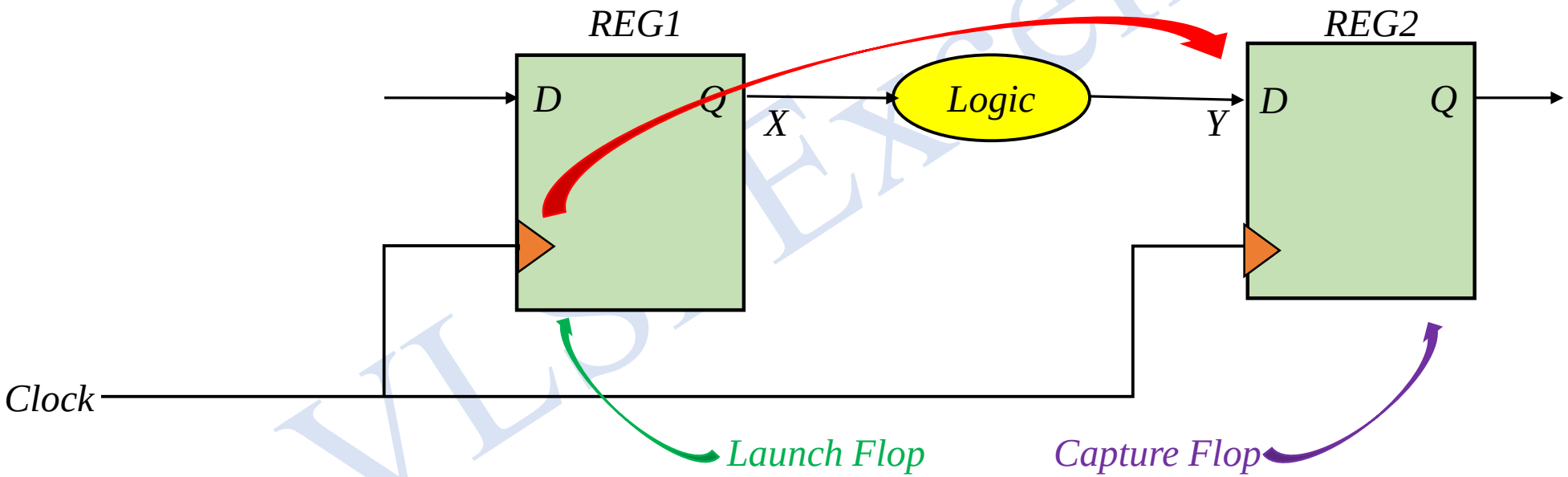
1) **Clock-to-Q Delay :** The Active Clock "Edge" triggers the input to the output in a flip-flop and hence flop timing is calculated from the clock edge, and Clock-to-Q Delay is used for the flop timing.



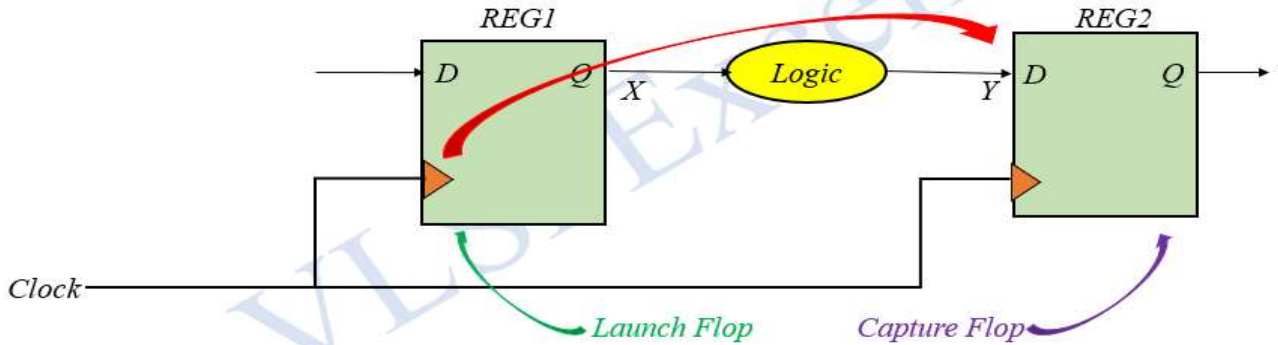
Static Timing Analysis (STA) – Flip-Flop Timing Parameters – Setup Time

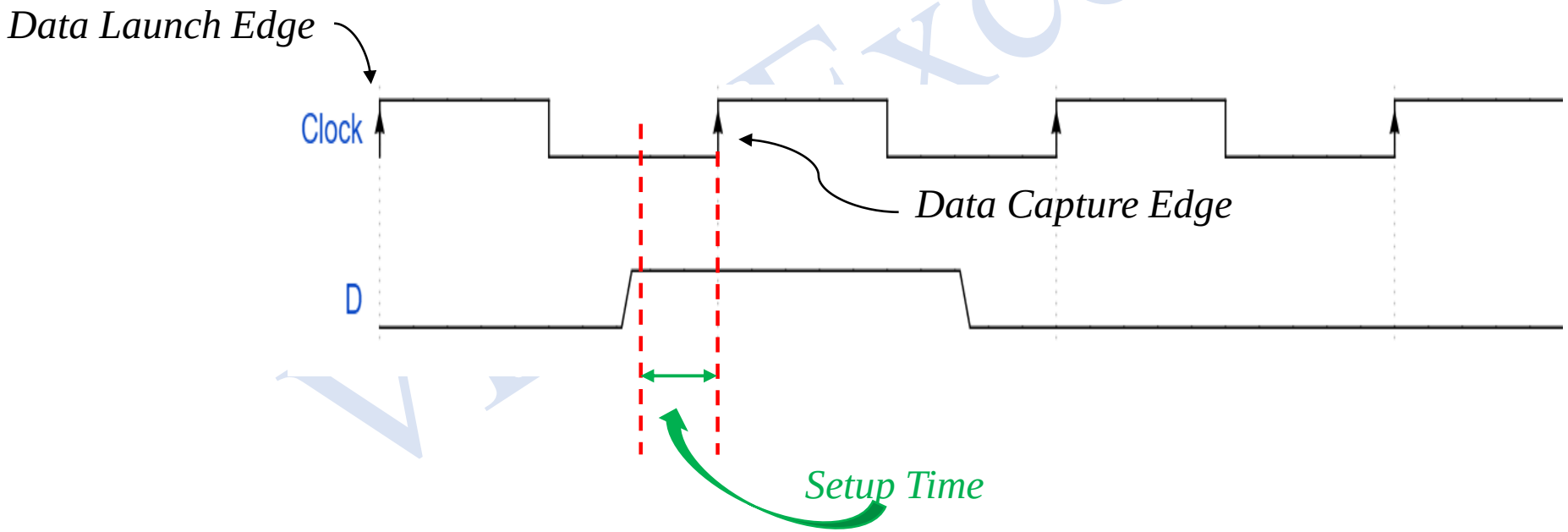
2) Setup Time –

is the duration of time, the synchronous input data must be stable ***before*** the triggering edge of the clock (Either Positive OR Negative Edge Triggered Flip-Flop)

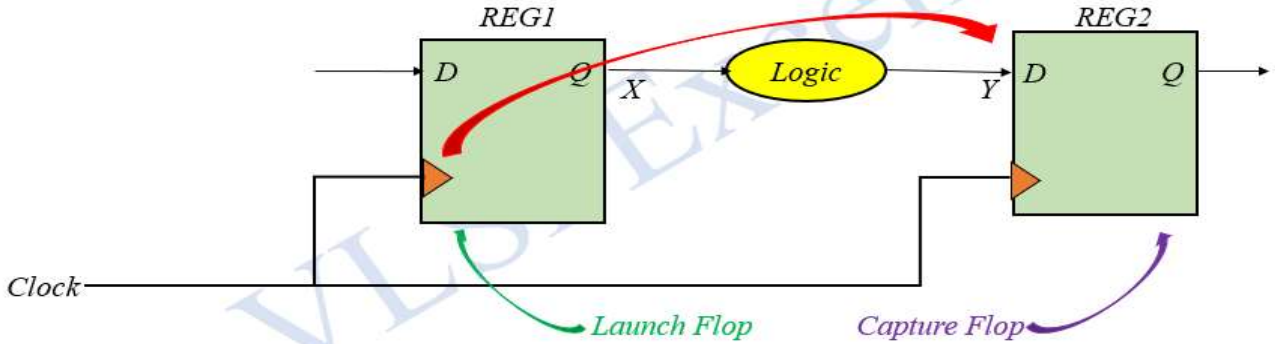


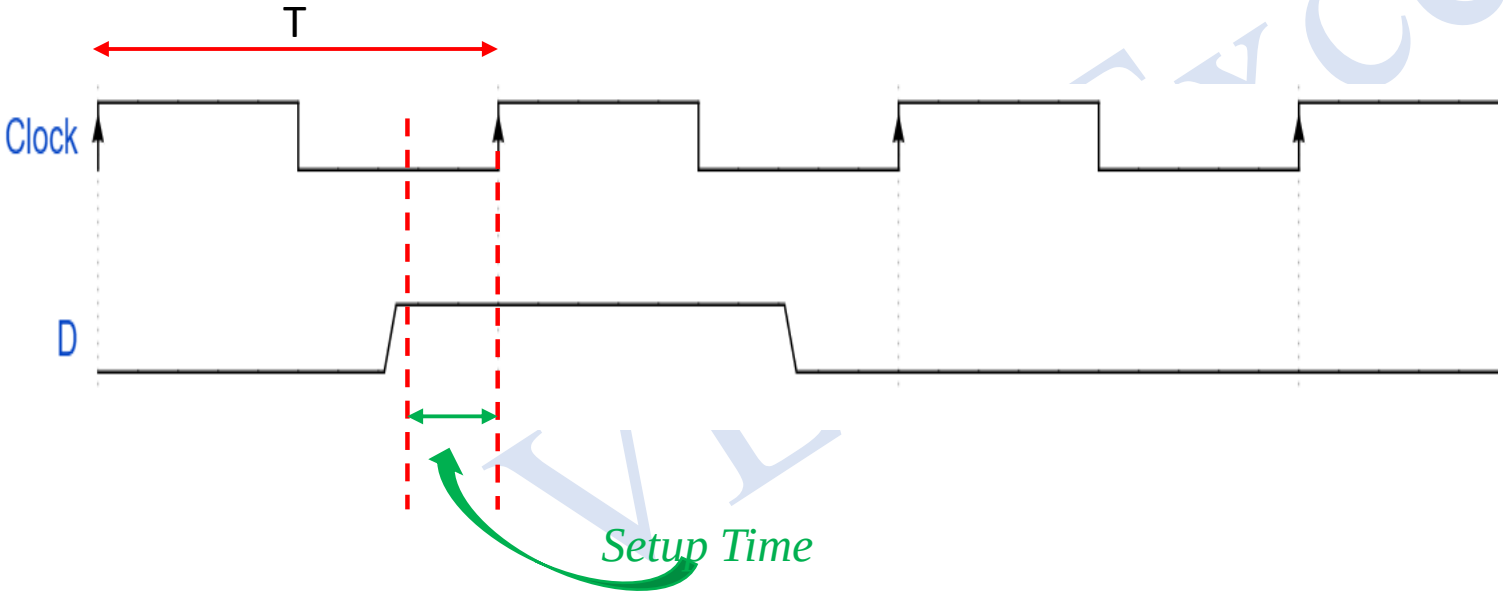
Static Timing Analysis (STA) – Flip-Flop Timing Parameters – Setup Time





Static Timing Analysis (STA) – Flip-Flop Timing Parameters – Setup Time





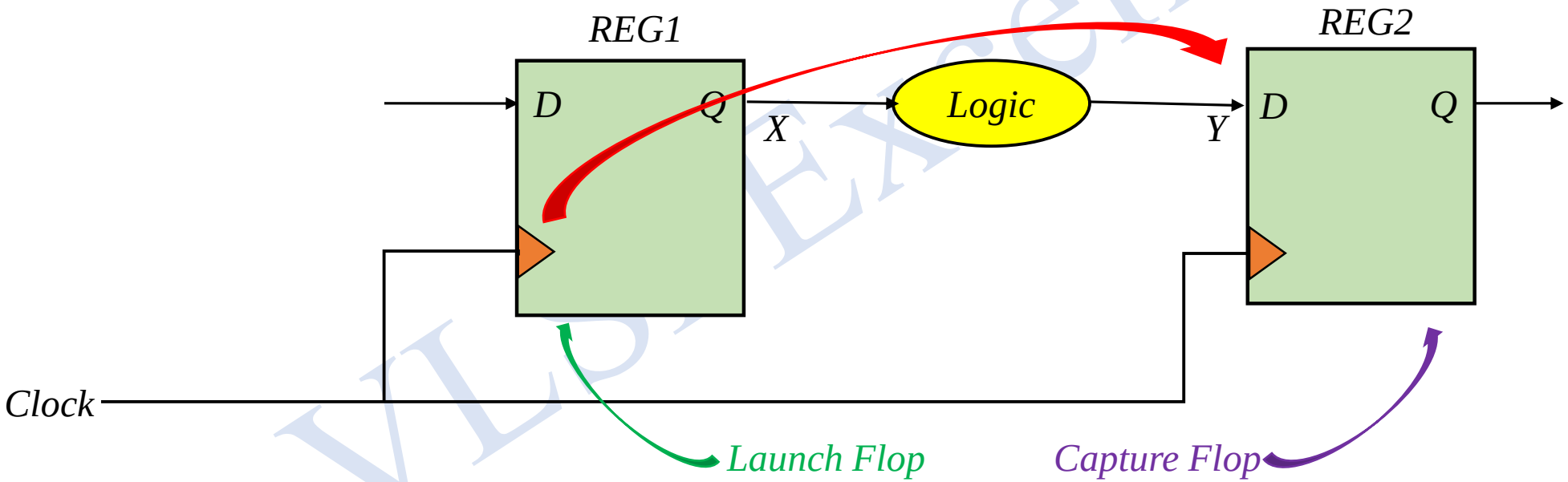
Note :

1) *If Setup time is not met, data is not stored in the Flip-Flop*
2) *If **Data is Slow**, Setup Time will be violated, Data Lost !!*
3) *If Clock is **Speed UP,** Setup Time will be violated, Data Lost !!*

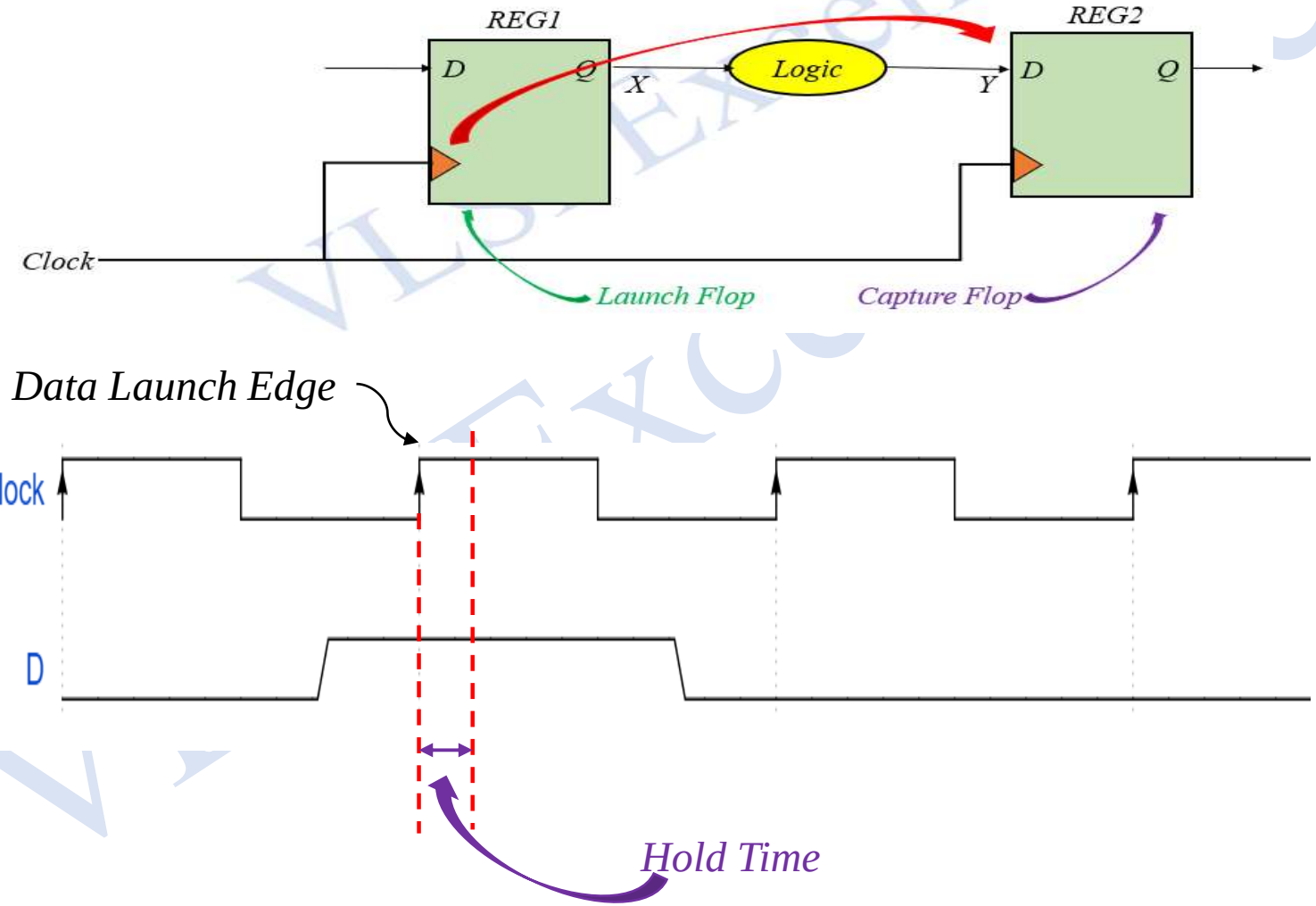
Static Timing Analysis (STA) – Flip-Flop Timing Parameters – Setup Time

3) Hold Time –

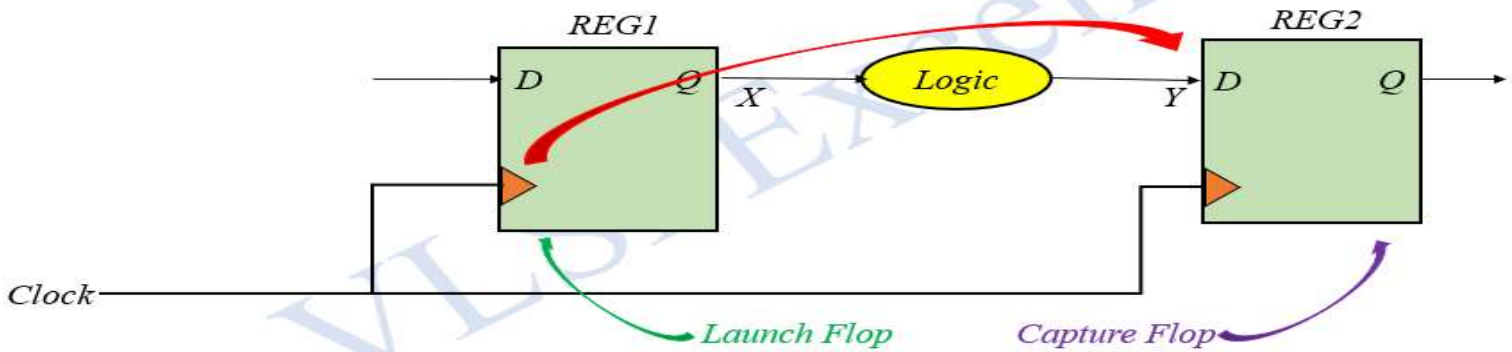
is the duration of time, the synchronous input data must be stable ***after*** the triggering edge of the clock (Either Positive OR Negative Edge Triggered Flip-Flop)

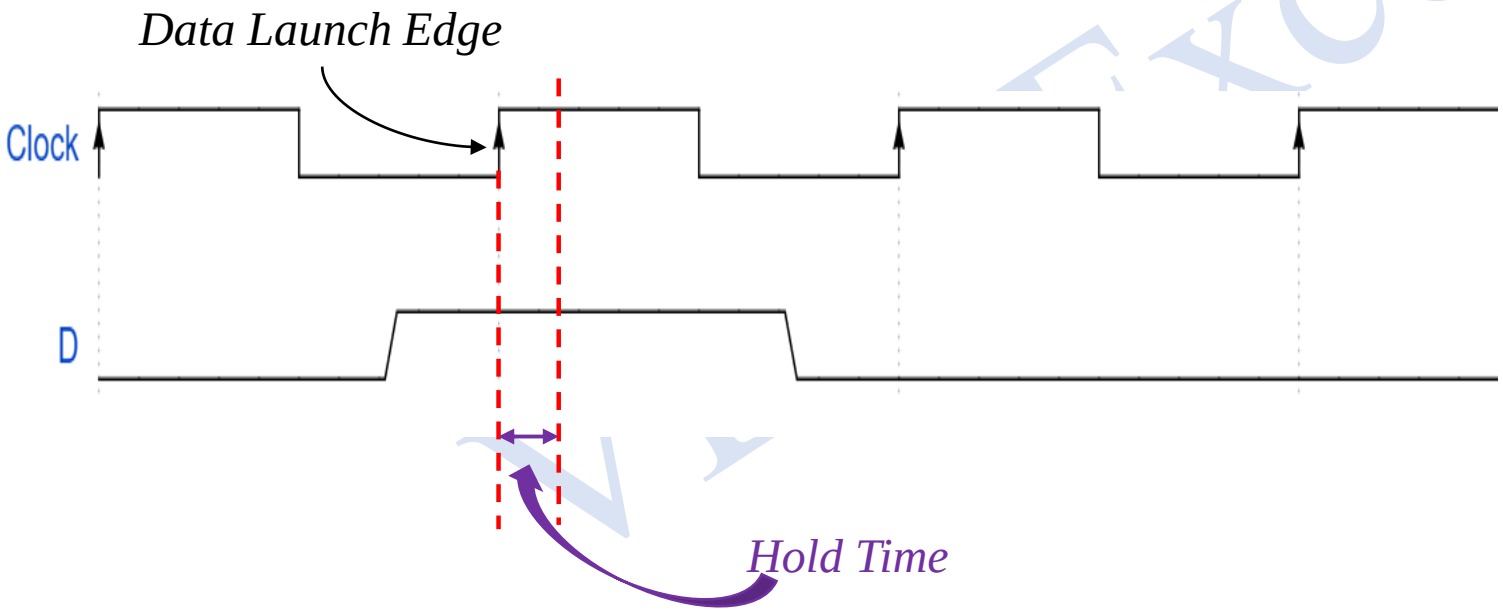


Static Timing Analysis (STA) – Flip-Flop Timing Parameters – Hold Time



Static Timing Analysis (STA) – Flip-Flop Timing Parameters – Hold Time





Note :

1) The Data Delay must be Greater than the Hold time of the Capture Flop for the Data to be safely stored in the Capture Flip-Flop

2) If the data starts changing immediately after the clock edge, Hold Time is Violated and Hence, Data Lost !!

Static Timing Analysis (STA) – Flip-Flop Timing Parameters – Setup and Hold in Timing Library

Example:

```
cell(DFF){
  . . .
 pin(D){
  direction : input;
  . . .
  timing(){
   related_pin : "CLK";
   timing_type : setup_rising;
   rise_constraint(setup_template_3x3){
    index_1("0.012, 0.020, 0.125");
    index_2("0.012, 0.020, 0.215");
    values ("0.04562, 0.06753, 0.1234",/
          "0.1234, 0.09876, 0.08967",/
          "0.4321, 0.03456, 0.7865");}

}
```

```
. . .
timing(){
   related_pin : "CLK";
   timing_type : hold_rising;
   rise_constraint(hold_template_3x3){
    index_1("0.012, 0.020, 0.125");
    index_2("0.012, 0.020, 0.215");
    values ("-0.04562, -0.06753, -0.1234",/
          "-0.1234, -0.09876, -0.08967",/
          "-0.4321, -0.03456, -0.7865");}

}
}
}
```

Note:
index_1 *= Data Transition*
Index_2 *= Clock Transition*

Static Timing Analysis (STA) – Flip-Flop Timing Parameters – Setup and Hold in Timing Library

The setup and hold timing constraints for the synchronous pin of a sequential cell can be described in terms of two-dimensional table as shown in the previous slide.

The setup and hold timing constraints are on the input pin D with respect to the rising (active) edge of clock pin of the Flip-Flop.

The two-dimensional models are in terms of data and clock transition time at the **constrained_pin** (Data Pin D) and the **related_pin** (clock pin CK) respectively. Index 1 is showing data transition (D) at the rising edge and index 2 is showing the clock transition (CK) at the rising edge.

Example : With data D pin rise transition of 0.012ns and clock CK pin rise transition of 0.215ns so the setup constraint for the rising edge of the D pin is 0.1234ns (this value is read from the rise_constraint table).

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