Static Timing Analysis (STA)

Lecture #09: Flip-Flop Timing Constraints – Setup & Hold

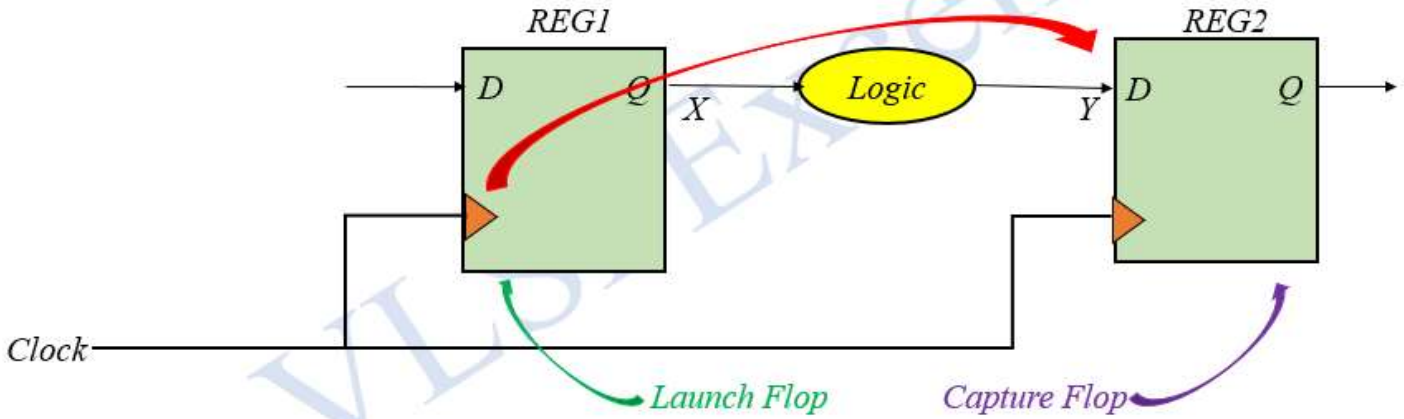
Video Lecture Link

Static Timing Analysis (STA) – Flip-Flop Timing Constraints

There are two main problems which can arise in synchronous logic designs -

1) Max Delay: The data does not have enough time to pass from one register to the next register before the next clock edge

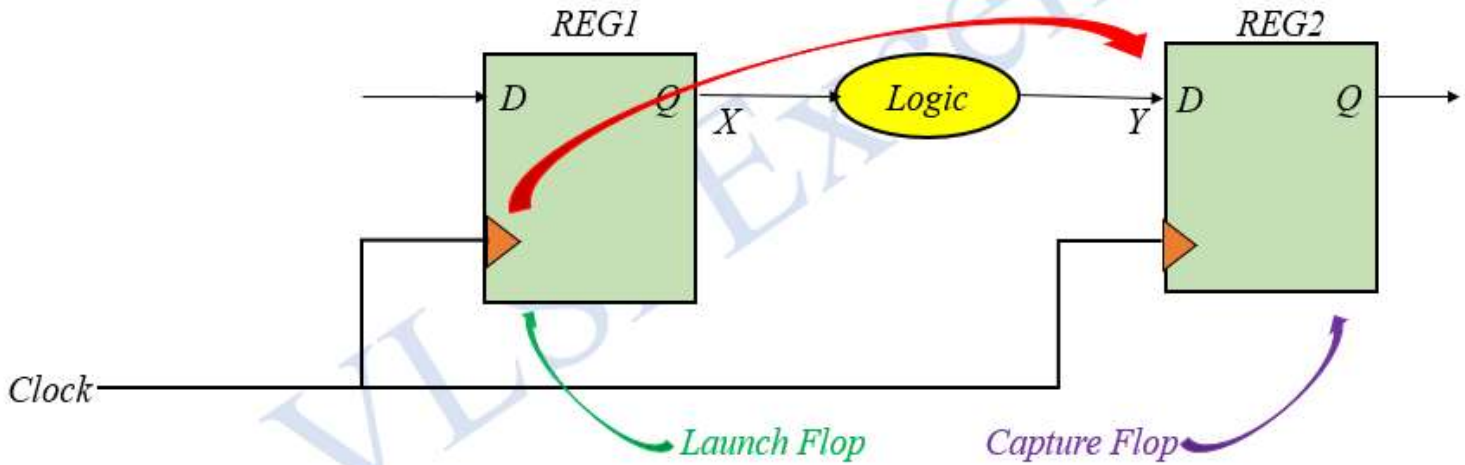
- Max delay violations are the result of slow data path, including the register's Tsetup time, therefore it is often called **Setup Path/Setup Constraint**
- A setup constraint specifies how much time is necessary for data to be available at the input if a sequential device before the clock edge that captures the data in the device.



Static Timing Analysis (STA) – Flip-Flop Timing Constraints

2) Min Delay: The data path is so short that it passes through several registers during the same clock cycle

- Min delay violations are the result of sort data path, causing the data to change before the register's Thold time has passed, therefore it is often called the **Hold Path/Hold Constraint**
- A hold constraint specifies how much time is necessary for data to be stable at the input of a sequential device after the clock edge that captures the data in the device



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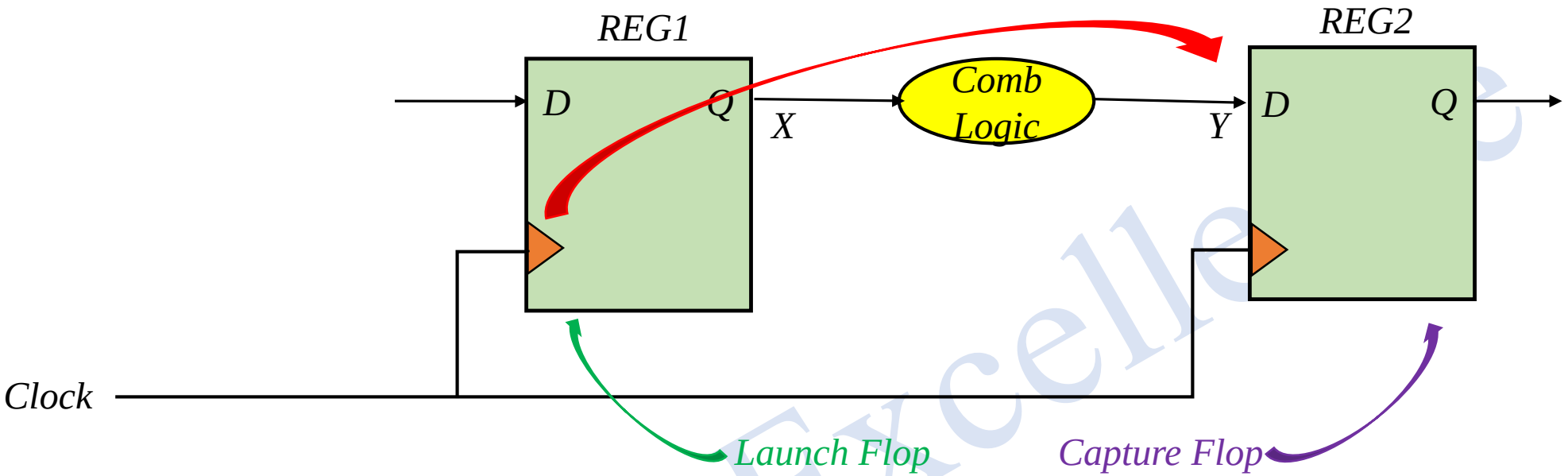
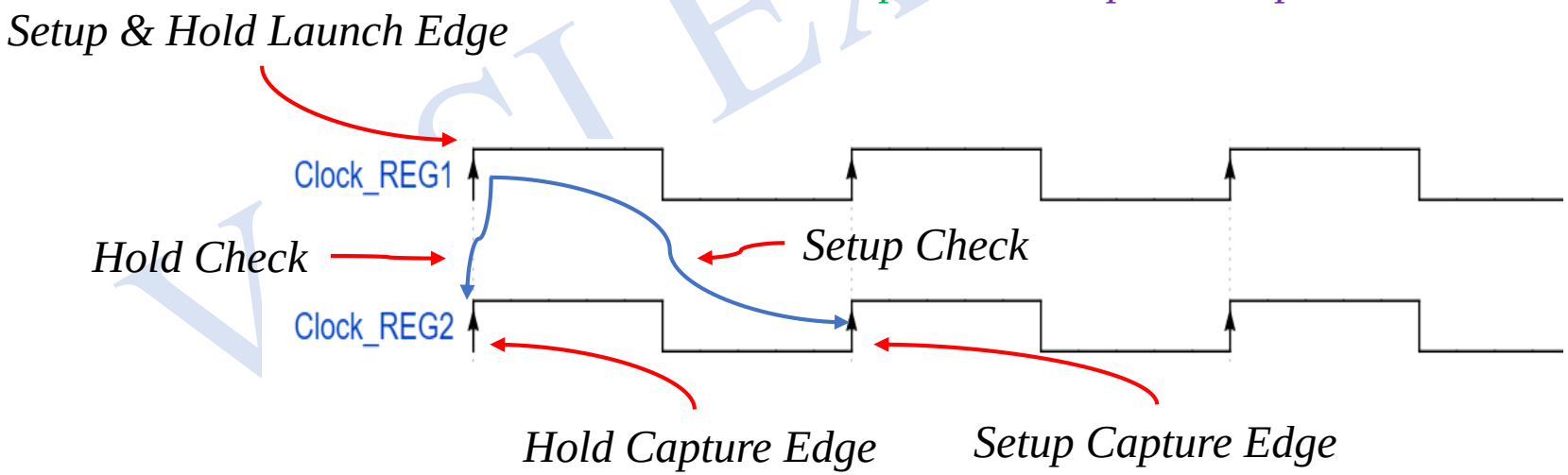
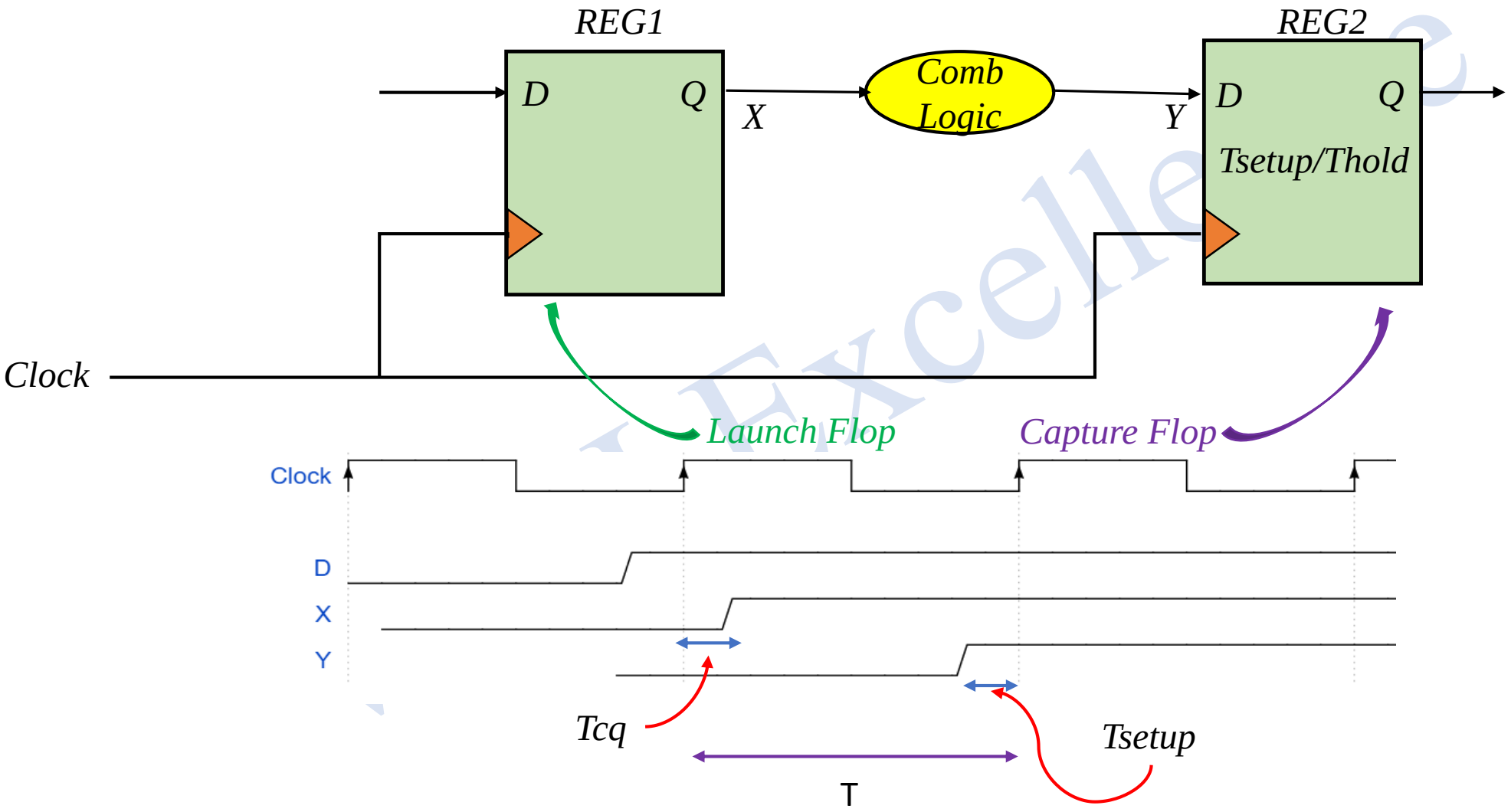




Static Timing Analysis (STA) – Flip-Flop Timing Constraints – Max Delay/Setup



Static Timing Analysis (STA)-Flip-Flop Timing Constraints – Max Delay/Setup

*1) After the clock rises, it takes **Tcq** for the data to propagate to point X.*

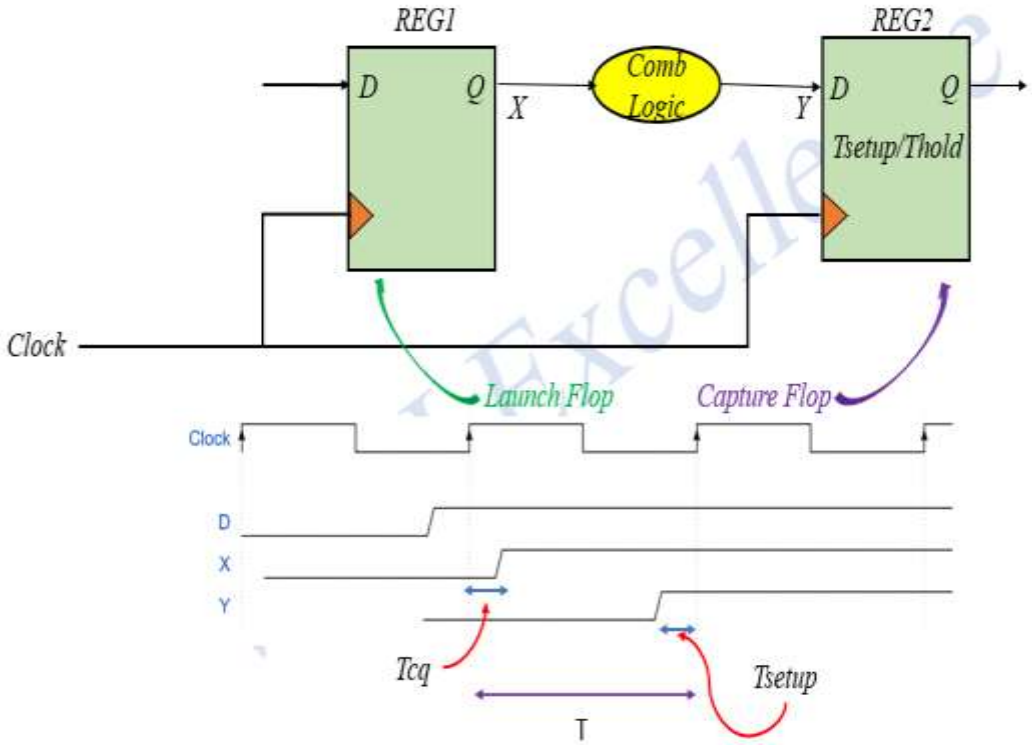
2) Then the data goes through the delay of the logic to get to point Y

3) The data has to arrive at point Y, Tsetup before the next clock edge

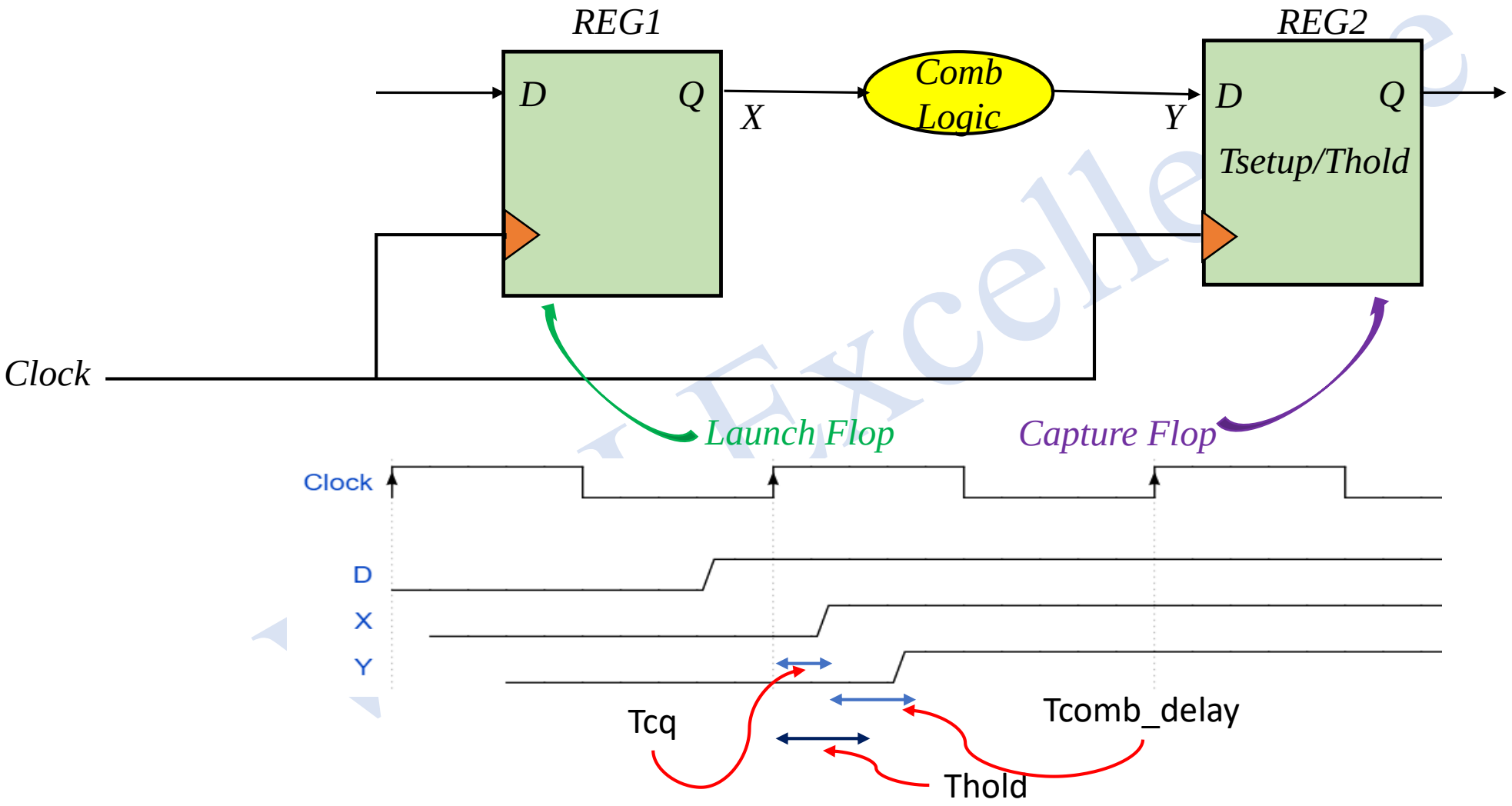
In general, out timing path is a race –

1) Between the data arrival, starting with the launching clock edge and

2) The data capture, one clock period later



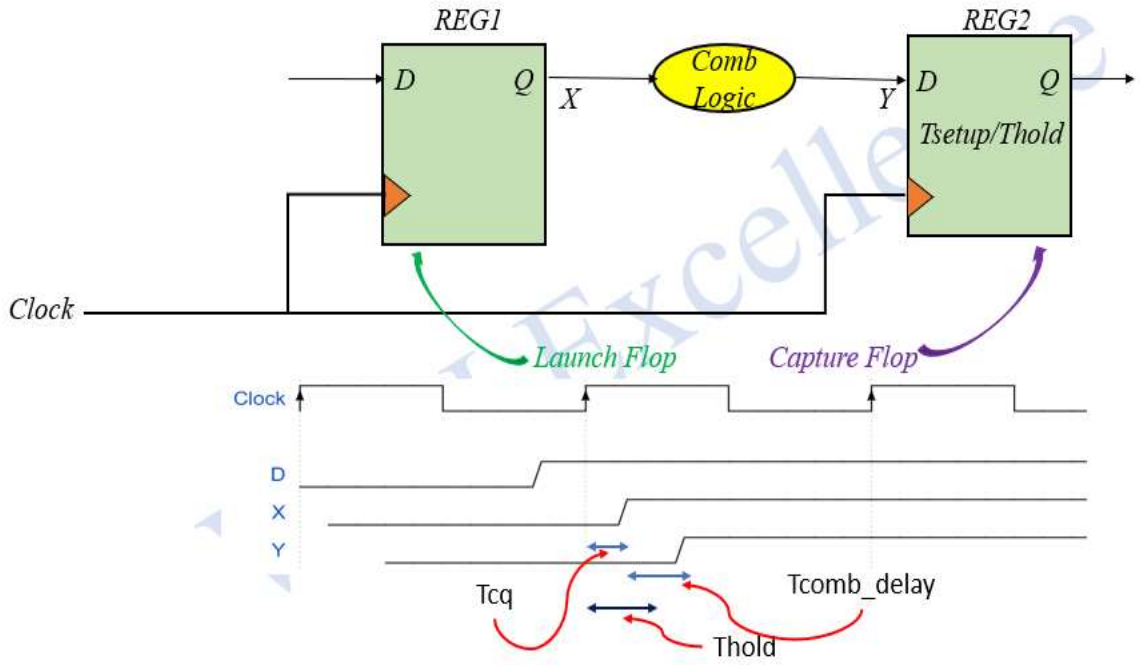
Static Timing Analysis (STA) – Flip-Flop Timing Constraints – Min Delay/Hold



Static Timing Analysis (STA) – Flip-Flop Timing Constraints – Min Delay/Hold

1) Hold problems occur due to the logic changing before ***Thold*** *has passed*

2) This is not a function of a cycle time – it is relative to a single clock edge



In general,
1) The clock rises and the data at X changes after ***Tcq***

2) The data at Y changes after comb logic delay later

3) Since the data at Y has to stay stable for Thold after the clock edge (for the second register).
The change at Y has to be at least Thold after the clock edge

- Hold time is the amount of time that REG1's old data must persist at the D input of REG2 after the clock edge

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