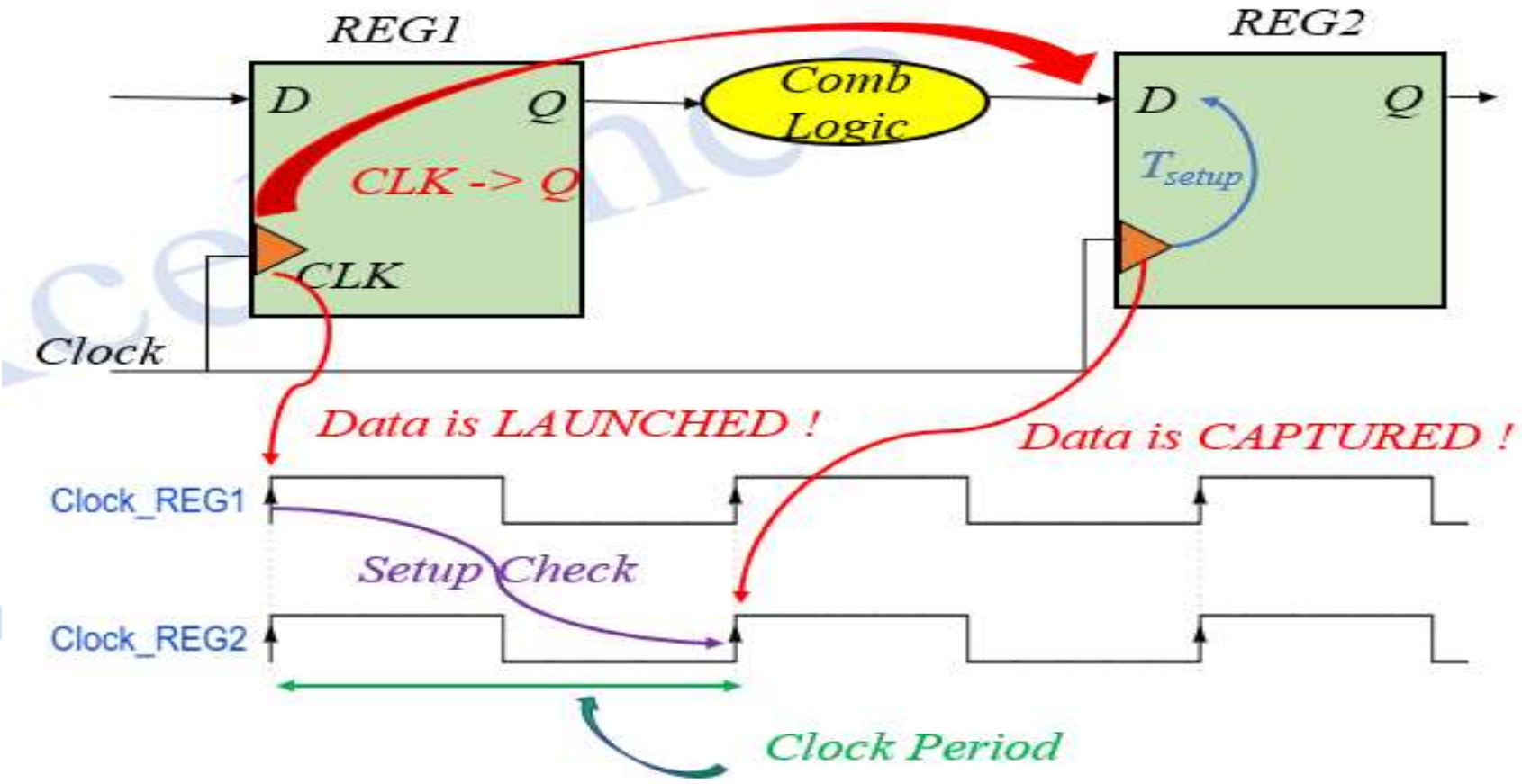
Static Timing Analysis (STA)

Lecture #11: Setup & Hold Timing Equations Summary & Maximum Operating Frequency

Video Lecture Link

Static Timing Analysis (STA) – Setup & Hold (Summary)



Static Timing Analysis (STA) – Setup & Hold (Summary)

1) For setup constraints, the data has to be propagate fast enough to be captured by the next clock edge.

- *This sets our maximum frequency*

- *If we have setup failures, we can always just slow down the clock*

2) For Hold constraints the data path delay has to be long enough so it is not accidently captured by the same clock edge

- *This is independent of the clock period*

- *If there is hold failure, you can throw your chip away!!!*

Static Timing Analysis (STA) – Maximum Operating Frequency

Maximum Operating Frequency:

Clk_to_Q [REG1] + Comb Delay <= Clock Period $- T_{setup}$[REG2] {Setup Equation}

Clock Period (T) >= Clk_to_Q[REG1] + Comb Delay + T_{setup}(REG2)

So, Minimum Clock Period (T) = Clk_to_Q[REG1] + Comb Delay + T_{setup}(REG2)

Hence, Maximum Clock Frequency = 1/T

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