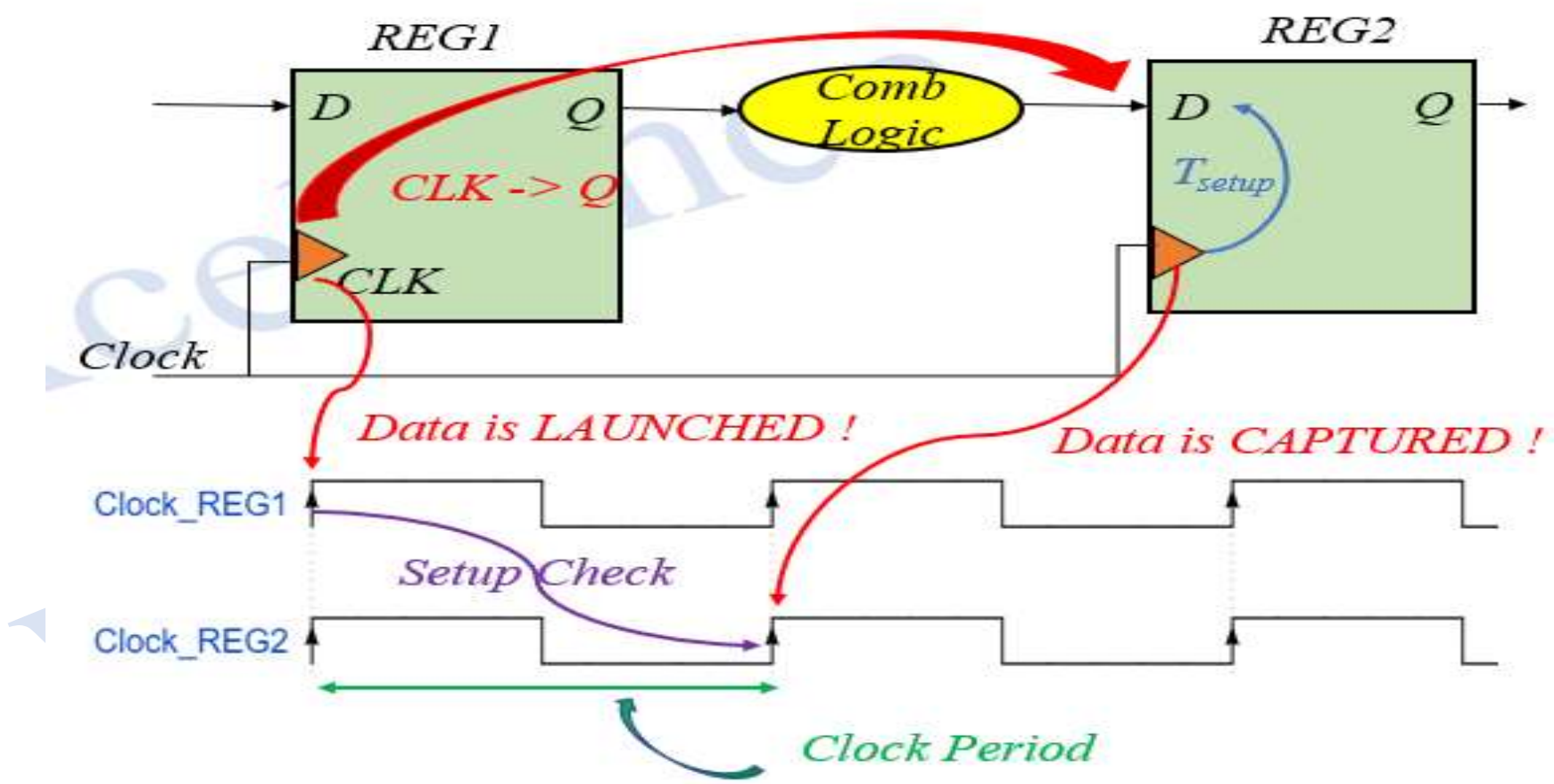


# Static Timing Analysis (STA)

*Lecture #11: Maximum Operating Frequency & Minimum  
Clock Period of a Digital Design*

*Video Lecture [Link](#)*

# Static Timing Analysis (STA) – Setup & Hold (Summary)



# Static Timing Analysis (STA) – Maximum Operating Frequency

## Maximum Operating Frequency:

$$\text{Clk\_to\_Q [REG1]} + \text{Comb Delay} \leq \text{Clock Period} - T_{\text{setup}}[\text{REG2}] \quad \{\text{Setup Equation}\}$$

$$\text{Clock Period (T)} \geq \text{Clk\_to\_Q[REG1]} + \text{Comb Delay} + T_{\text{setup}}(\text{REG2})$$

$$\text{So, Minimum Clock Period (T)} = \text{Clk\_to\_Q[REG1]} + \text{Comb Delay} + T_{\text{setup}}(\text{REG2})$$

$$\text{Hence, Maximum Clock Frequency} = 1/T$$

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