# Static Timing Analysis (STA)

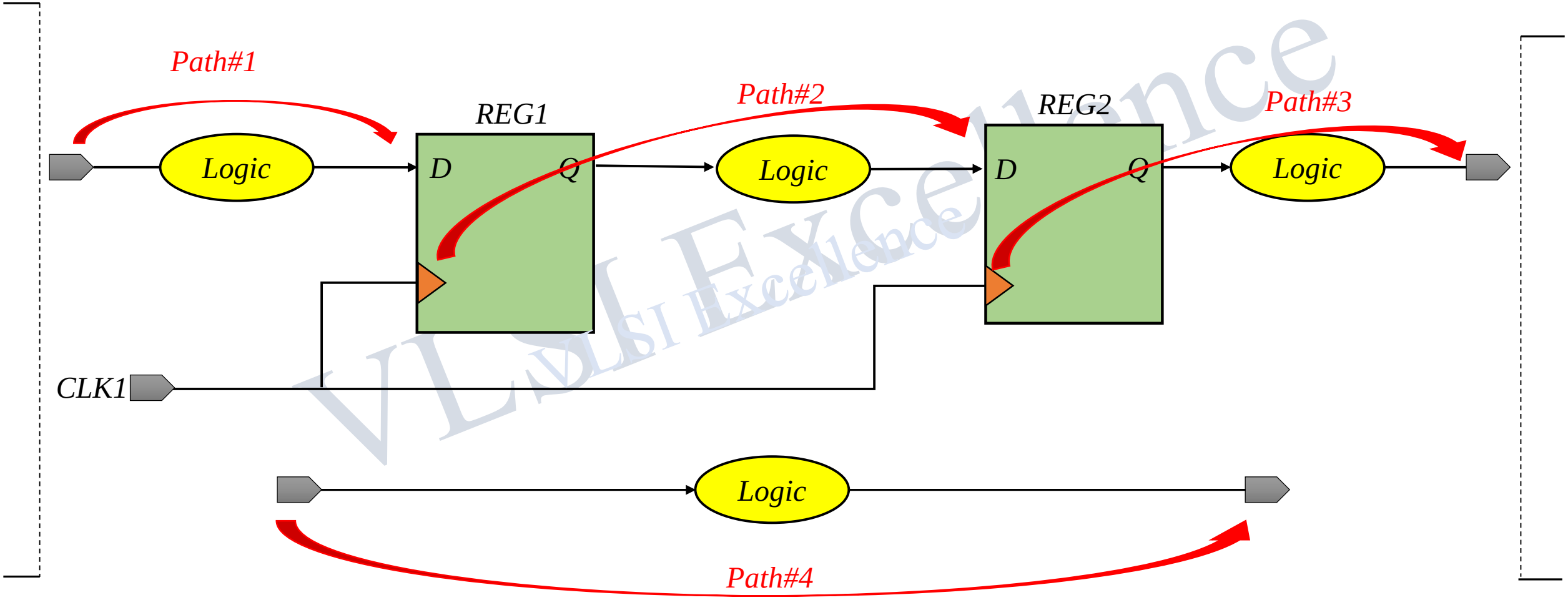
***Lecture #01: Introduction to STA + Timing Paths***

***Video Lecture Link***

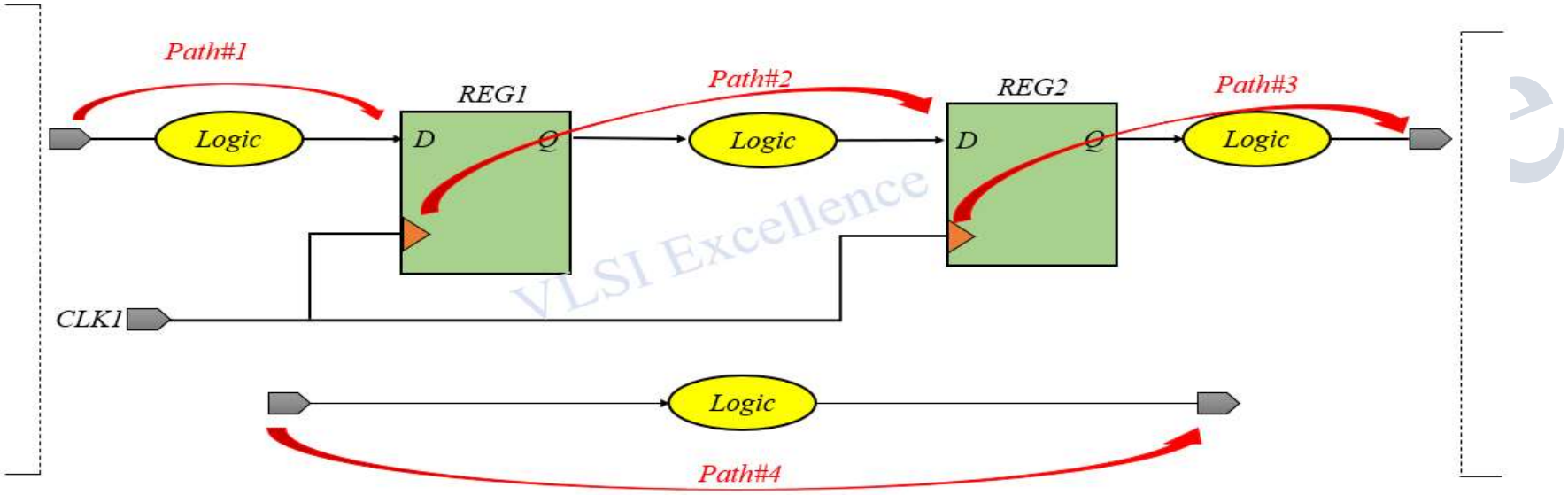
# Static Timing Analysis (STA)

- Method of validating the timing performance of a circuit by checking all the possible timing paths for violation of **timing constraints (Setup & Hold).**
- STA breaks the design into timing paths and calculated delay for each signal path and checks for the violations of timing constraints inside the design and at the input/output interface.
- The total delay of the path is sum of all the cell delays and net delays in the path.
- Lets discuss all the Timing Paths which STA tool considers in the design to validate the timing performance in this Lecture #01
- Popular STA Tool : Synopsys - **Prime Time**

# Static Timing Analysis (STA) - Timing Paths



# Static Timing Analysis (STA) - Timing Paths

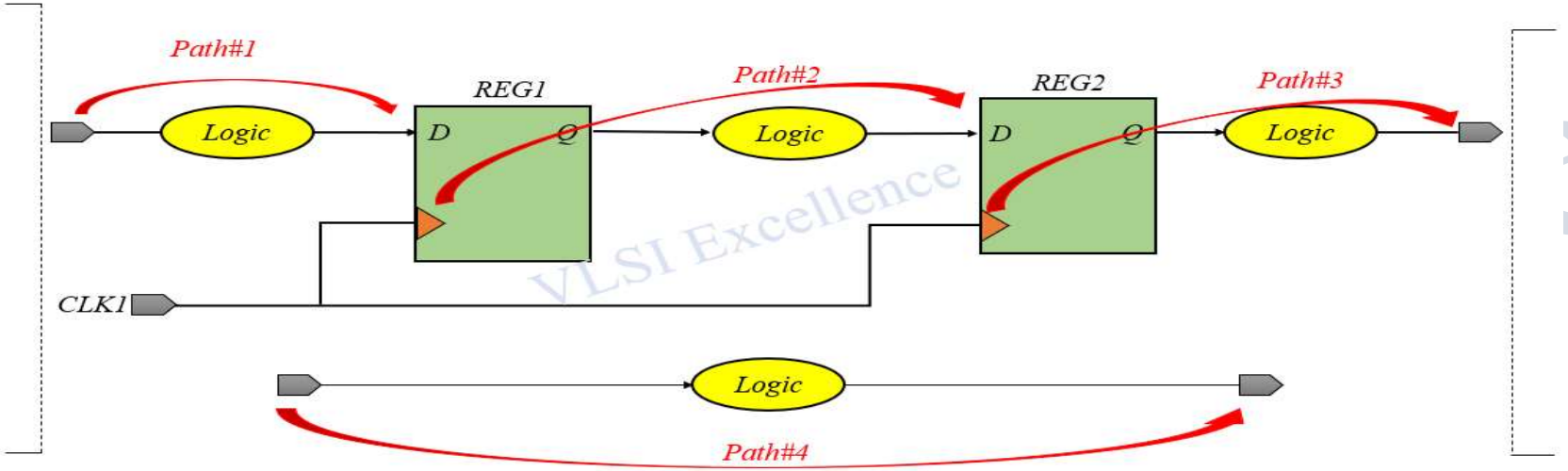



Each Timing Path consists of the following elements –

**Start Point** : Data Launch Clock Edge or where the data must be available at a specific time

**End Point** : Where the data is captured by a clock edge or where the data must be available at a specific time

# Static Timing Analysis (STA) - Timing Paths




Path#1, #2, #3, #4 are called as Data Path and their respective start point and end points are as below :

**Path#1** : **(in2reg )** Start Point - Input port of design ; End Point - Data input pin of Flip-Flop/Latch

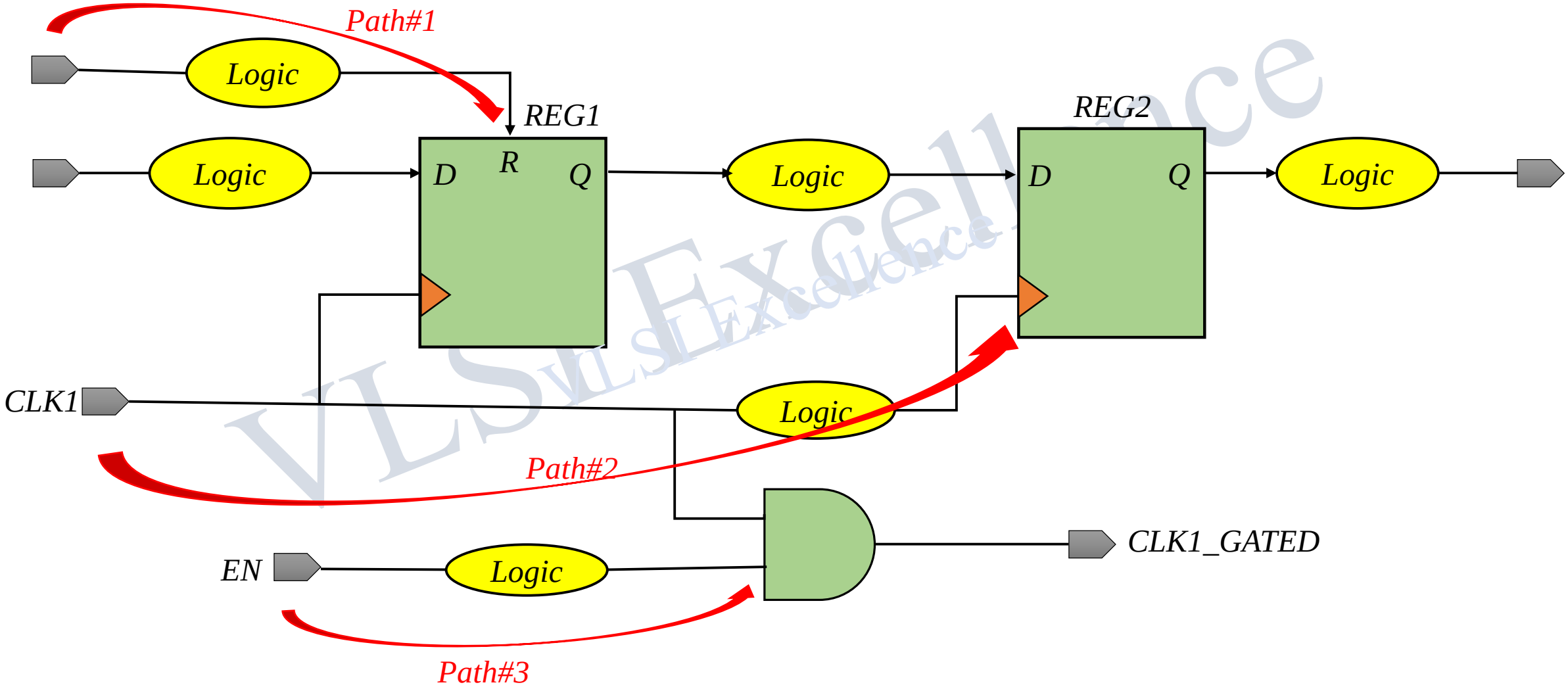
**Path#2 : (reg2reg)** Start Point - Clock pin of Flip-Flop/Latch ; End Point - Data input pin of Flip/Flop/Latch

**Path#3** : **(reg2out)** Start Point - Clock pin of Flip-Flop/Latch; End Point - Output port of design

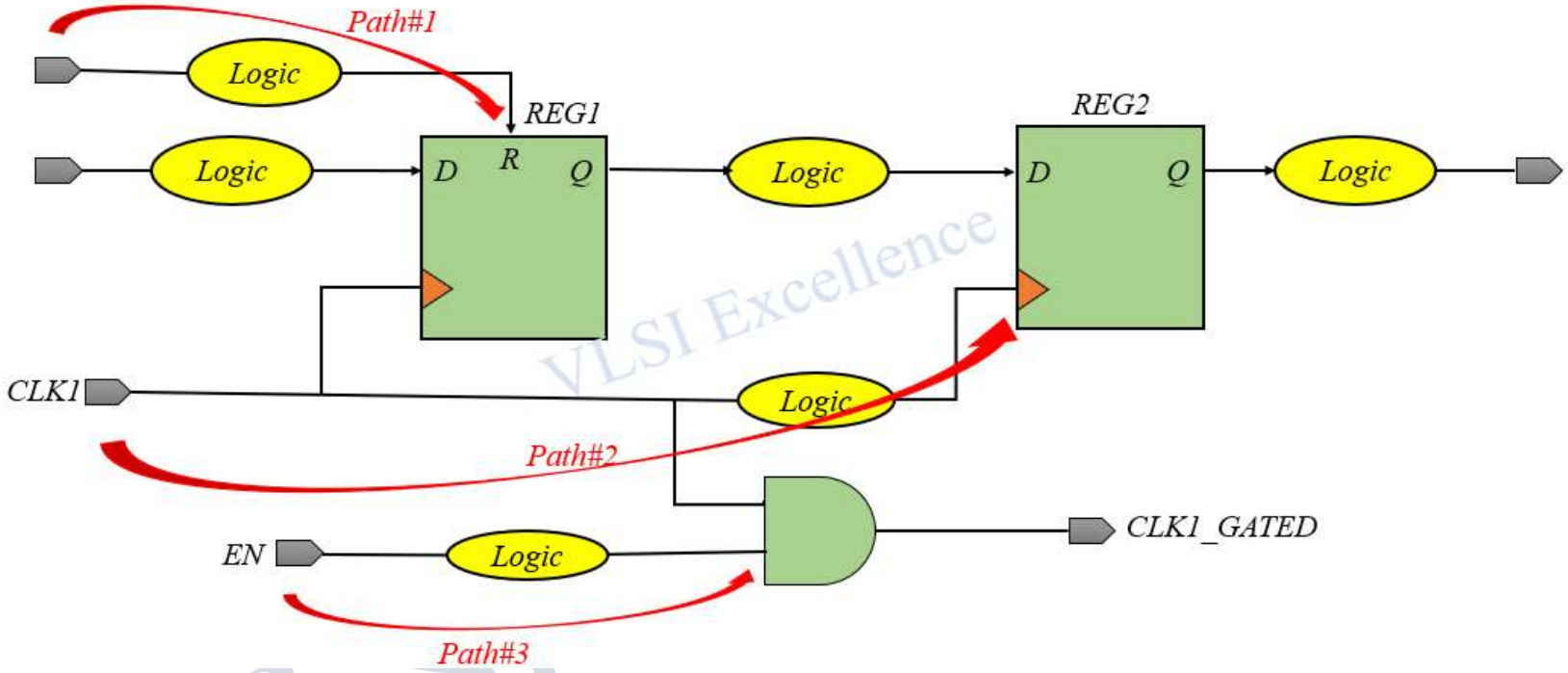
**Path#4** : **(in2out)** Start Point - Input port of design; End Point - Output port of design

# Static Timing Analysis (STA) – Timing Paths

*STA Also considers below path for timing analysis !!*



# Static Timing Analysis (STA) – Timing Paths

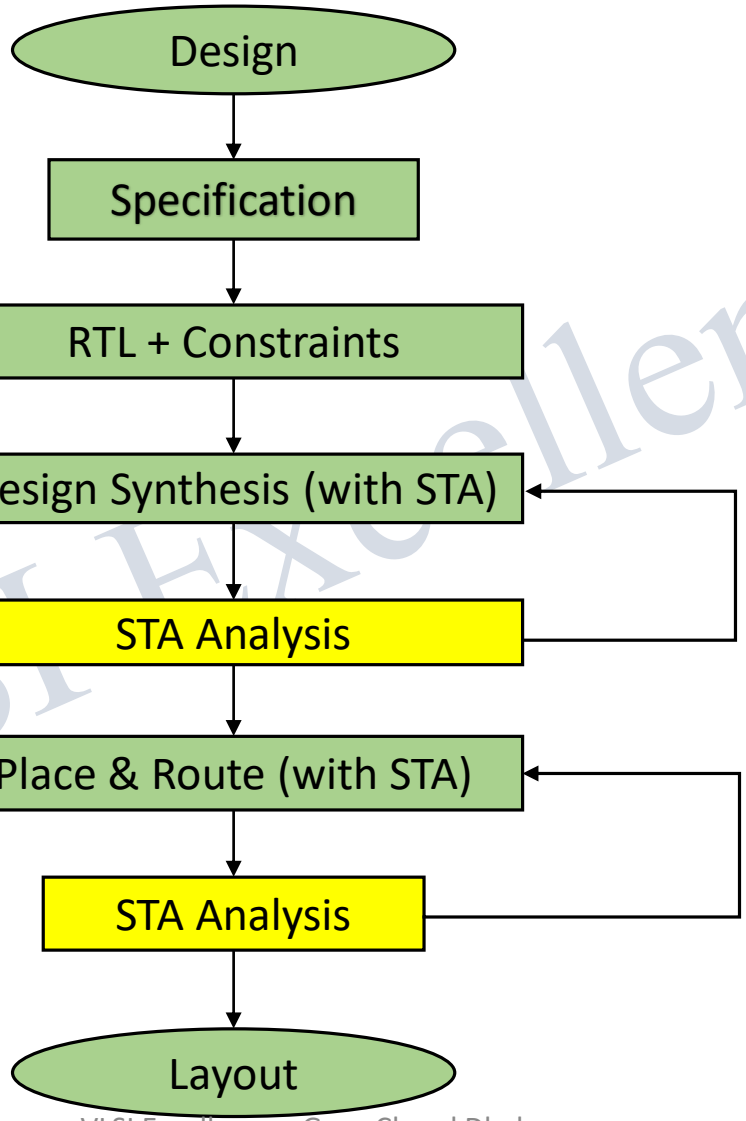



These paths are also considered by STA tool for timing analysis –

**Asynchronous Path** : Path from an input port to an asynchronous set or clear pin of a sequential element. For Recovery and Removal Checks (**Path#1**)
**Clock Path** : Need for Setup and Hold Timing Constraints (**Path#2**)
**Clock Gating Path** : For Clock Gater Setup and Hold Check (**Path#3**)

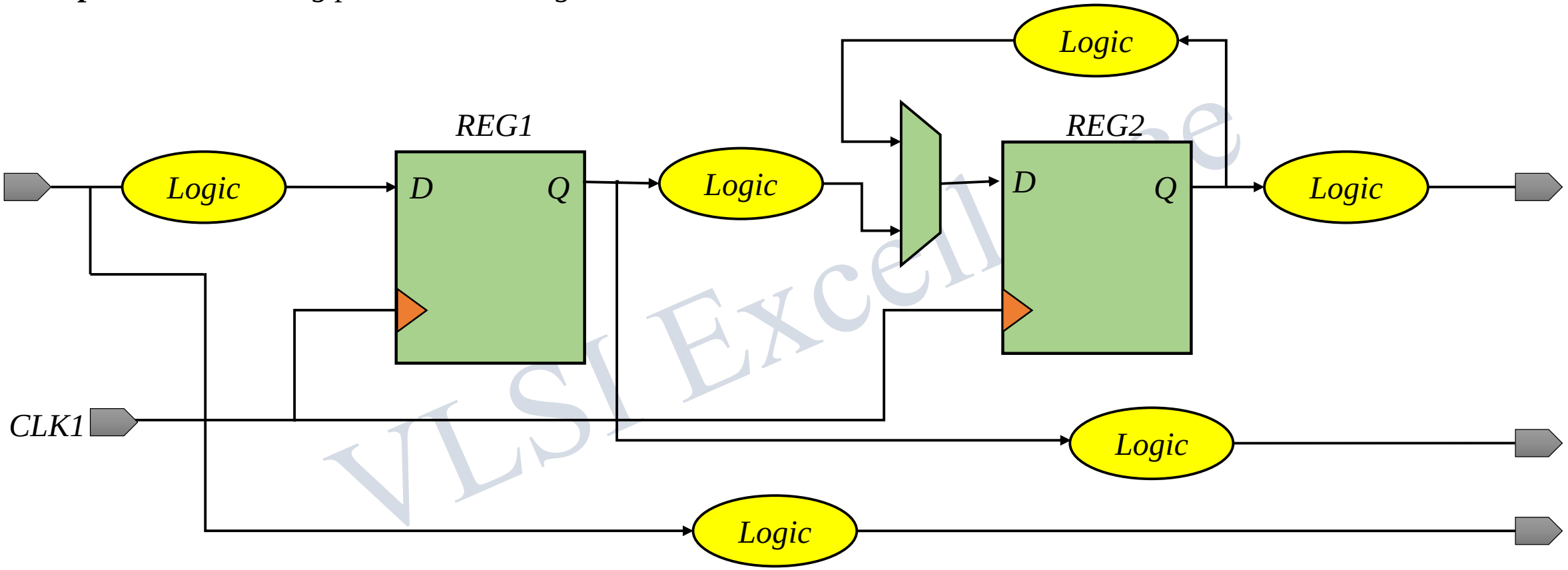
# Static Timing Analysis (STA)

***How does STA fit into a design flow ? Lets have a look at this flow chart -***



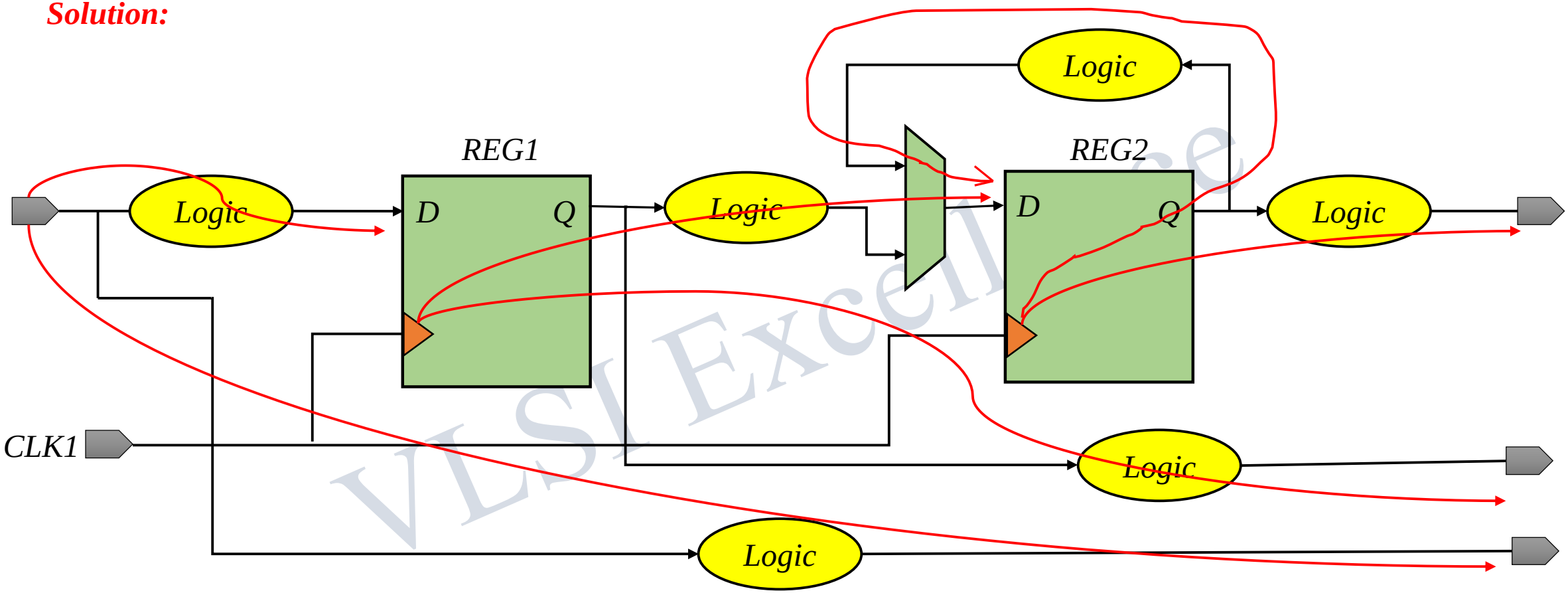
# Static Timing Analysis (STA) – Timing Paths

***Example:*** *Find all timing paths in below digital circuit?*



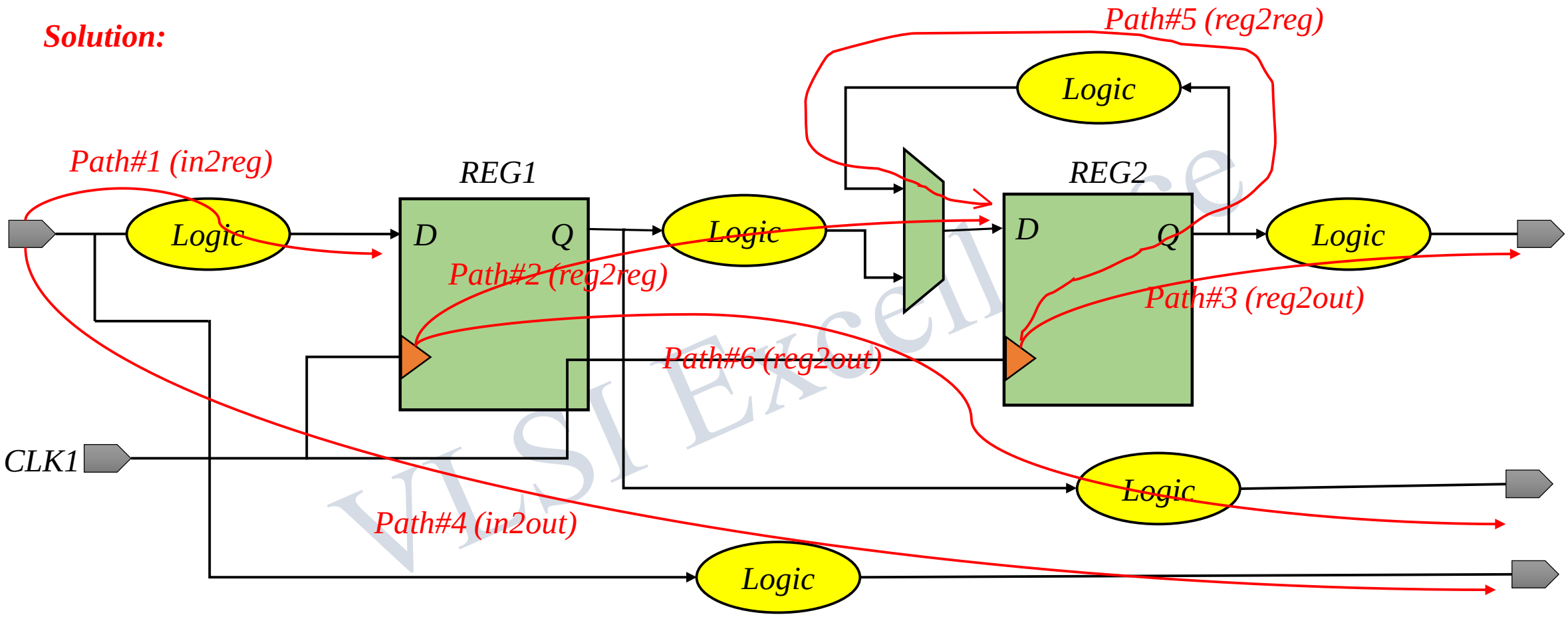
# Static Timing Analysis (STA) – Timing Paths

***Solution:***



# Static Timing Analysis (STA) – Timing Paths

***Solution:***



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