Static Timing Analysis (STA)

Interview/Practice Questions

Full Video Solution Playlist

Q#01 : How many timing Arc does the 2-input OR gate have ?

A) 1
B) 2
C) 3
D) 4

Ans : B

Q#02 : How many positive unate arcs does the 2-input NOR gate have ?

A) 0
B) 2
C) 3
D) 4

Ans : A

Q#03 : From the below timing library snippet, determine the output rise transition for an input transition of 1.2 and an output load of 0.250 ?

```
-------------------------------------------------------------
   timing_type: setup_rising;
      rise_transition(setup_template_3x3){
         index_1 (“0.01, 0.11, 0.12”);
         index_2 (“0.150, 0.250, 0.350”);
         values (/
                     “0.1234, 0.2341, 0.8076”,
                      “0.6790, 0.4563, 0.5687”,
                       “0.8767, 0.7056, 0.4567”);
}
-------------------------------------------------------------
```

A) 0.1234
B) 0.7056
C) 0.5687
D) 0.8767

Ans : B

Q#04 : What is the total clock latency given maximum clock tree delay is 100ps and maximum clock delay From the clock source to the clock port is 150ps ?

A) 100ps
B) 200ps
C) 250ps
D) 300ps

Ans : C

Q#05 : Which of the following are considered as start point of a timing path ? Select all that apply

A) D input of a register/flop
B) Clock pin of a register
C) Output port of a design
D) input port of a design excluding clock port

Ans : B, D

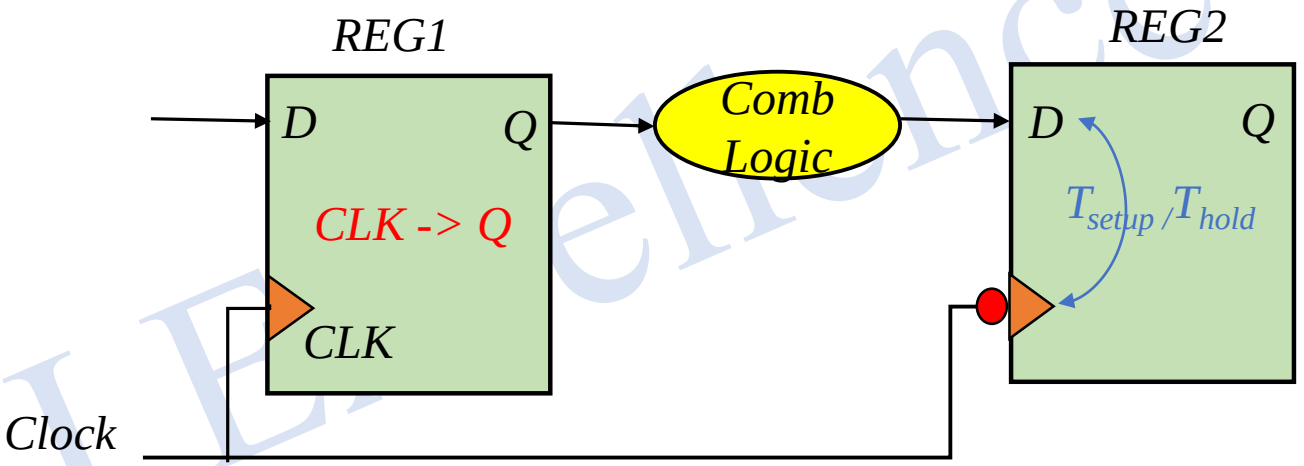
Q#06 : What is the setup slack of a path if the given required time is 1.5 ns and arrival time is 1.8 ns ?

A) 0.3 ns
B) 0.03 ns
C) 3.3 ns
D) -0.3 ns

Ans : D

Q#07 : What is the setup slack of given register –to–register path if the clock period is 2 ns , clock-to-Q delay is 0.5 ns , setup and hold time of capture flop are 0.5 ns each and the combination delay is 0.3 ns ?

A) 0.3 ns
B) 0.03 ns
C) 3.3 ns
D) -0.3 ns



Ans : D

Q#08 : Considering a single clock design with a clock period of 50ps and setup time of all flip flops in design is 100ps. Is there any timing problem with this design ?

Ans : Yes

Q#09: Setup time violation can be mitigated by –

A) Speeding up the clock
B) Speeding up data and clock
C) Increasing the Data Delay
D) Speeding up the data OR increase the clock period

Ans : D

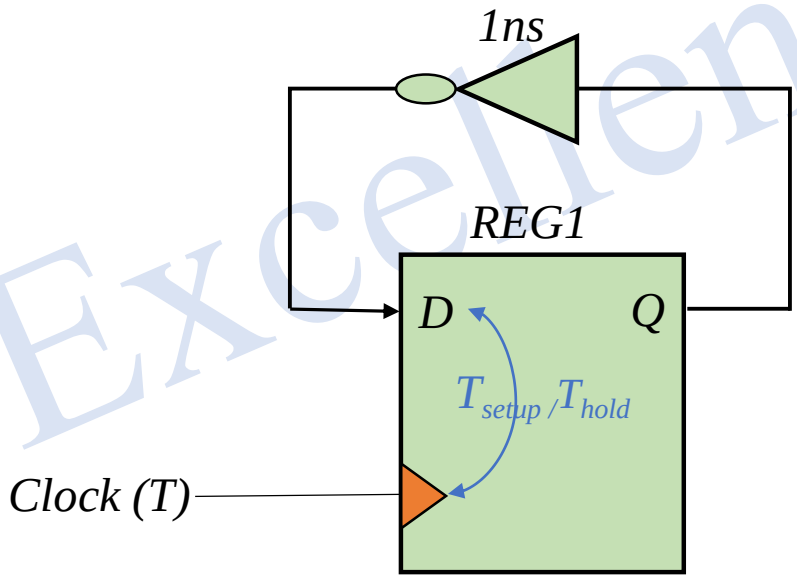
Q#10 : Hold time violation can be mitigated by –

A) Speeding up the clock
B) Speeding up data
C) Increasing the Data Delay
D) Reducing Clock Skew or Uncertainty

Ans : C, D

Q#11 : For the below given digital circuit, calculate the minimum clock period required for proper functioning of the circuit. Given the data setup time of flip flop is 5ns, hold time of flip flop is 1ns and clock to Q delay is given as 8ns. Also, through some light on the hold constraint of this circuit with proper explanation.

$T_{cq} = 8ns$
$T_{su} = 5ns$
$T_h = 1ns$
T_{min} ?



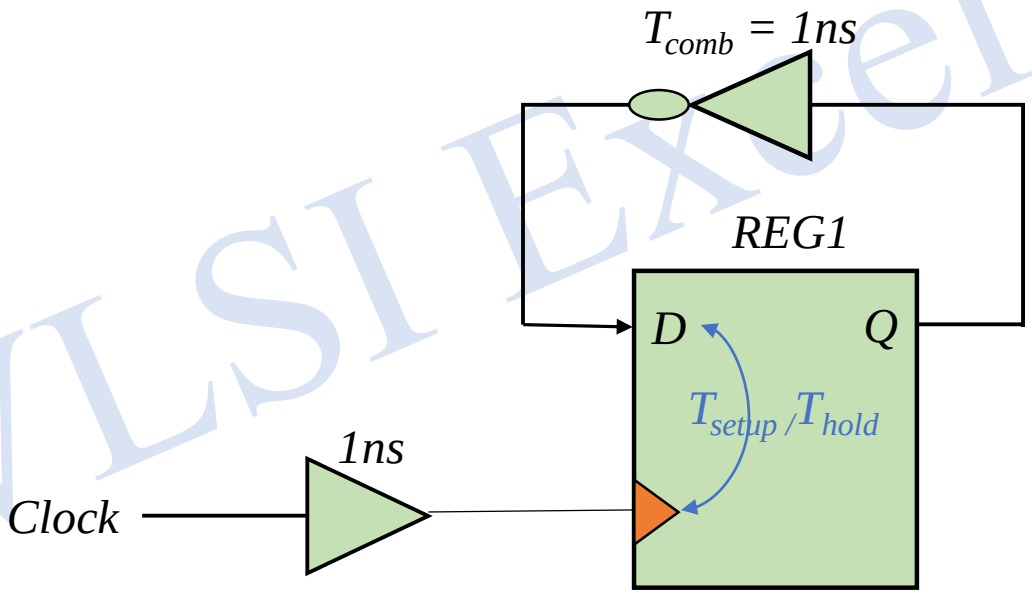
Q#12 : A clock buffer is added in the clock path. Find out any violation with the below given timing parameters –

Setup time of Flip - flop = 3 ns

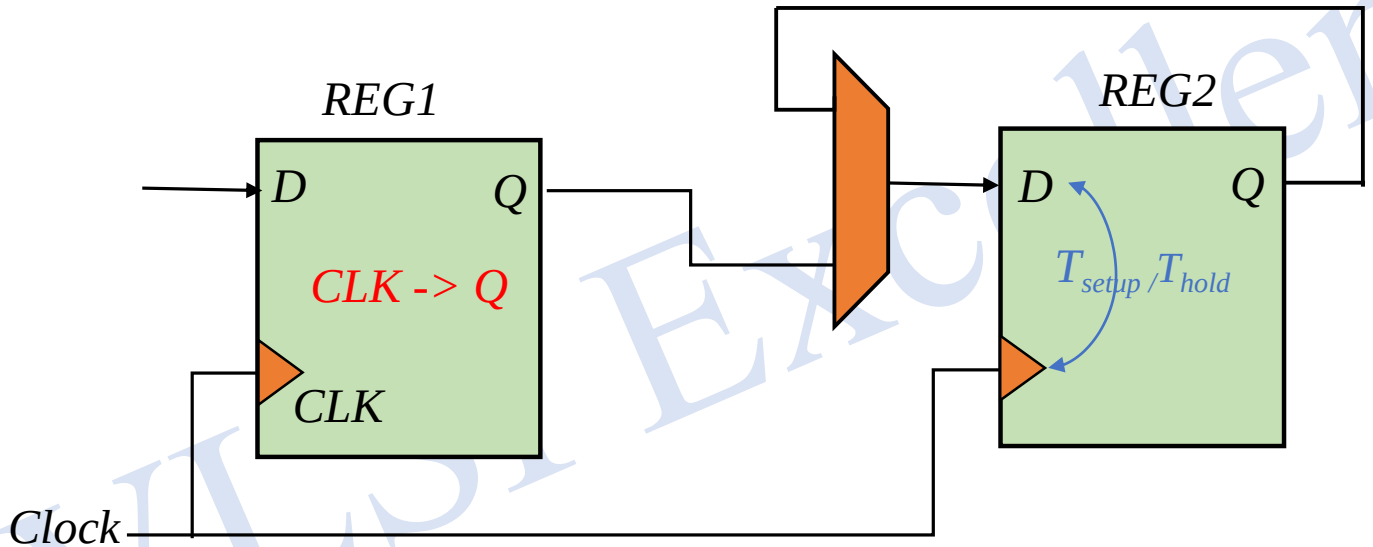
Hold time of Flip – flop = 4ns

Clock to Q Delay of Flip-flop = 2ns

What is the effect of clock buffer on Maximum clock frequency of circuit ?

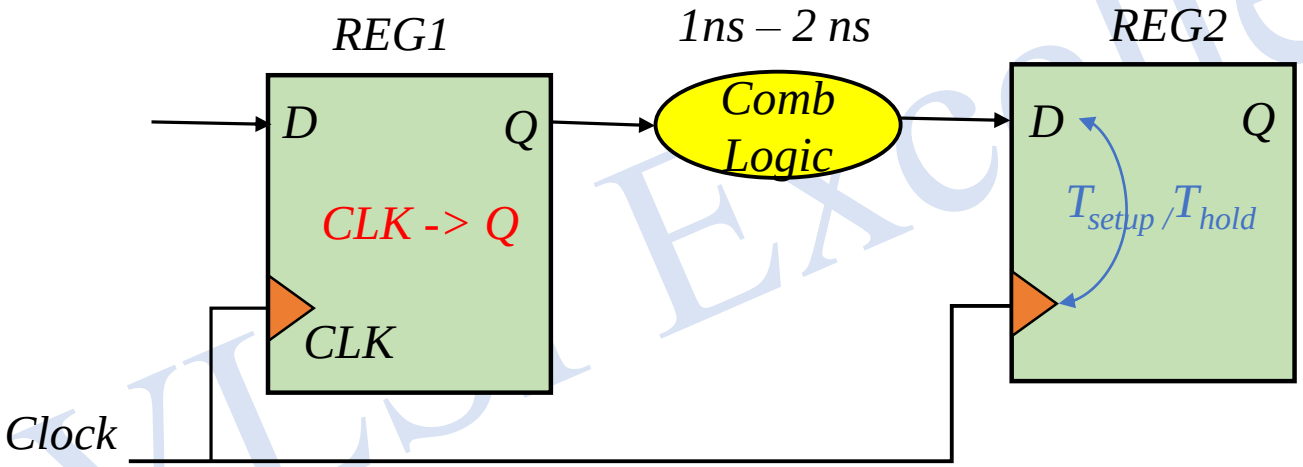


Q#13 : Find the maximum clock frequency of the below circuit if Clock to Q delay of both Flip-Flops is 2ns , setup and hold time for REG1 flip flops is 2ns, for REG2 flip flop 3 ns and the Mux delay is 0.5ns

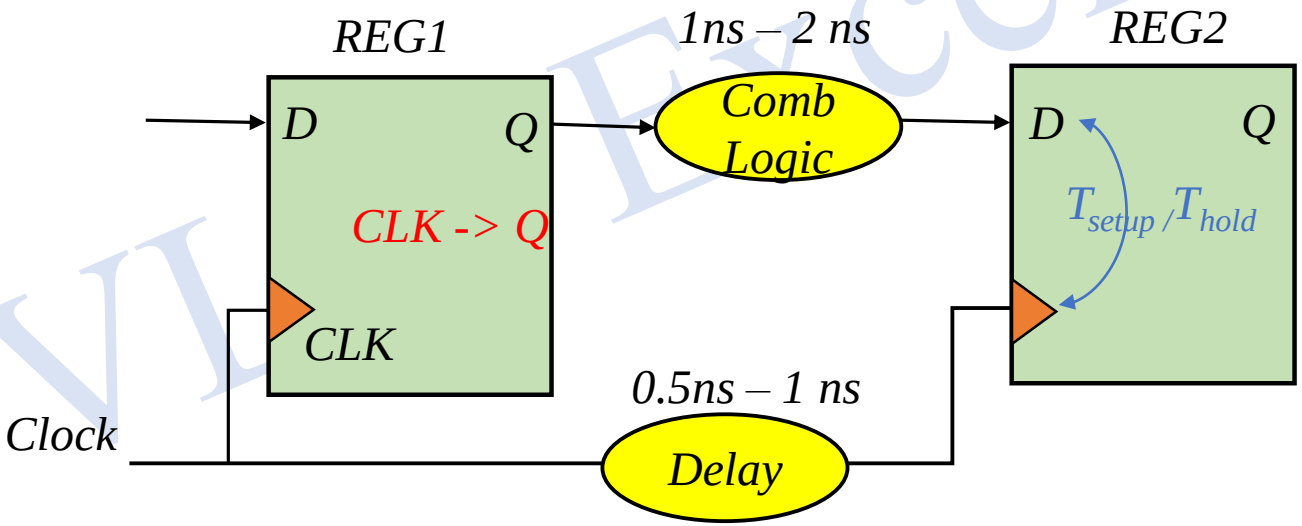


Q#14 : Find minimum Setup and Hold Slack for the Register – to – Register timing path as given in the below digital circuit.

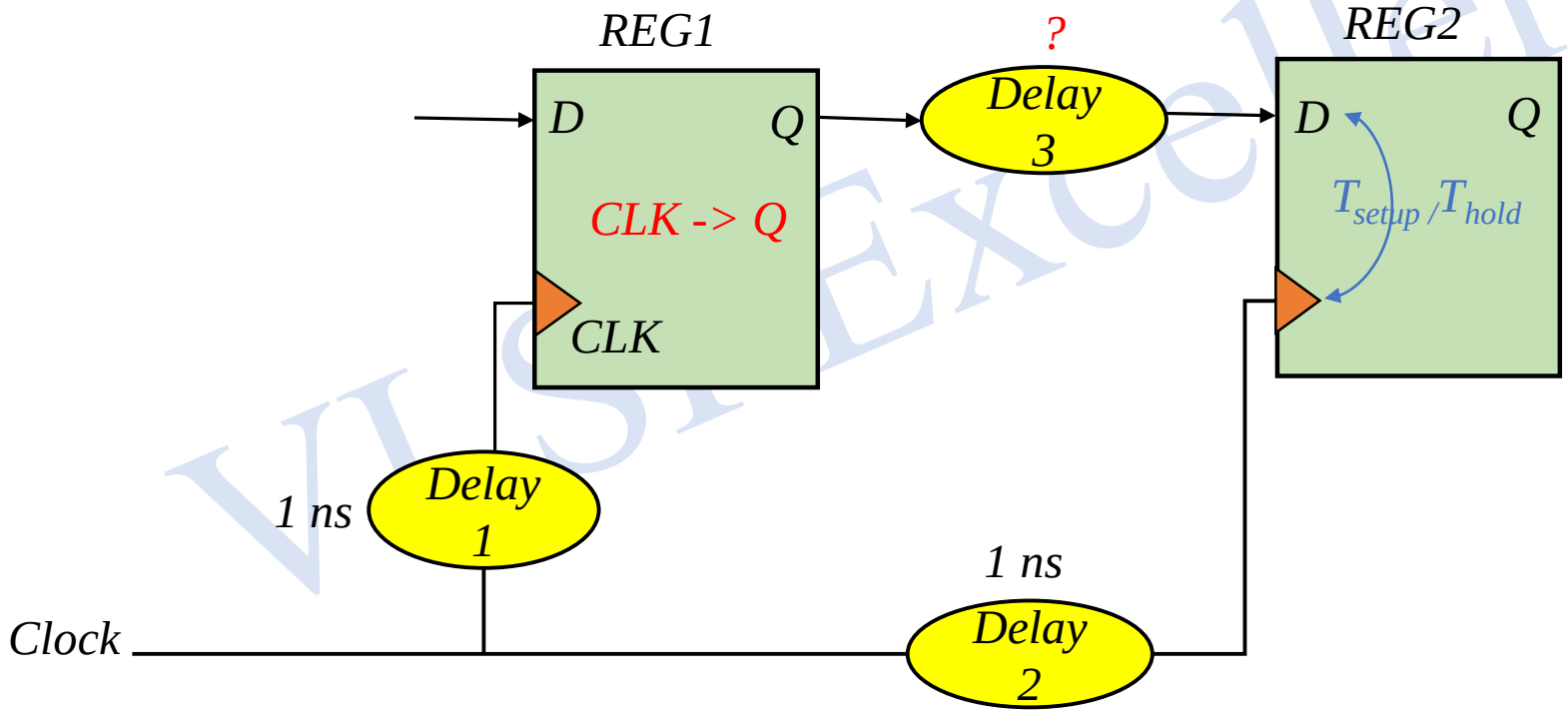
Consider , Clock – to – Q Delay of both the flip flops is 2ns and setup and hold data time for both the flip flops is 1.2ns.



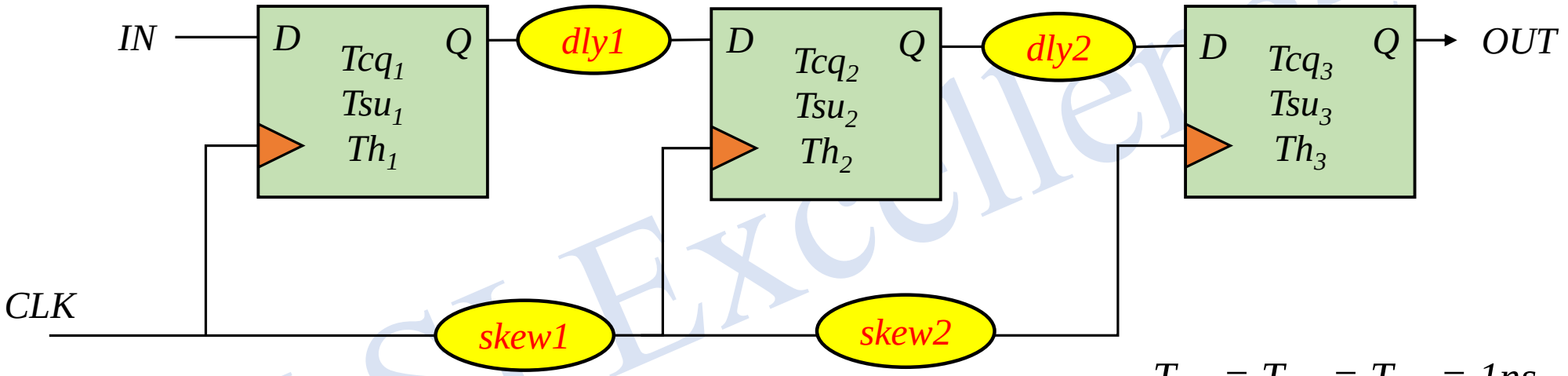
Q#15 : Find minimum Setup and Hold Slack for the Register – to – Register timing path as given in the below digital circuit. Consider , Clock – to – Q Delay of both the flip flops is 2ns and setup and hold data time for both the flip flops is 1.2ns.
Clock Period is 6ns.



Q#16 : Find value of Delay 3 in the below digital circuit such that there is no setup and hold violation. Also, find the maximum operating clock frequency of the circuit
Consider , Clock – to – Q Delay of both the flip flops is 2ns and setup and hold data time for both the flip flops is 2.2ns.



Q#17: Find maximum frequency of operation for the below digital design ?



Setup Equation:

Clock Period (T) + T_{skew} – T_{setup} >= Tcq + Comb Delay

Hold Equation:

T_{hold} + T_{skew} <= T_{cq} + Comb Delay

$T_{cq1} = T_{cq2} = T_{cq3} = 1ns$
$T_{su1} = T_{su2} = T_{su3} = 2ns$
$T_{h1} = T_{h2} = T_{h3} = 1ns$
$dly1 = 0.8ns$
$dly2 = 1ns$
$skew1 = 0.5ns$
$skew2 = 0.5ns$

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