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Verilog in 10 Minutes – Verilog Coding Styles

Video Lecture Link

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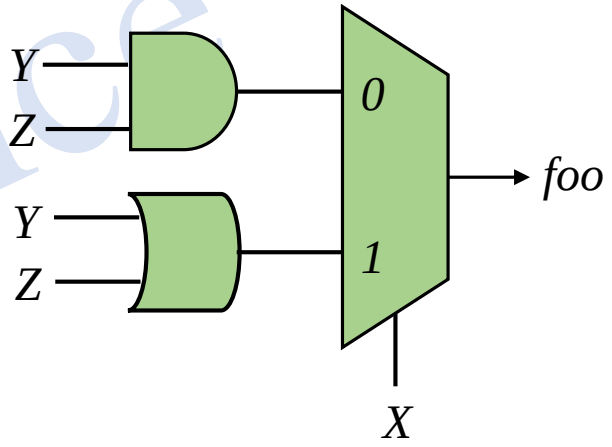
Verilog Combinational Logic (CL)

How would you describe the behavior of this function in words ?

If X = 1, then foo = Y or Z,
else foo = Y and Z



How would you describe the behavior of this function in Verilog Code ?

```
always @ (X or Y or Z)
 if(X) foo = Y | Z;
 else foo = Y & Z;
```

foo can change when any of X, Y or Z changes
So, code must be rerun whenever any of these changes

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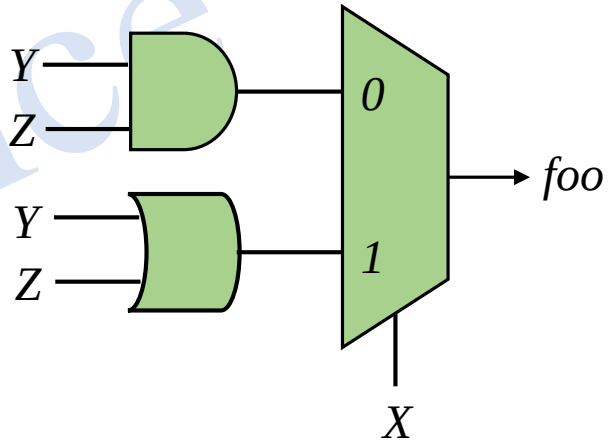
Alternative Coding Style for CL

Verilog has a short hand way to capture Combinational Logic
Called “Continuous Assignment”

```
assign foo = X ? Y | Z : Y & Z;
```



LHS Re-evaluated whenever anything in RSH changes

```
assign f = a ? b : c
```

Is same as
if(a) f = b;
else f = c;

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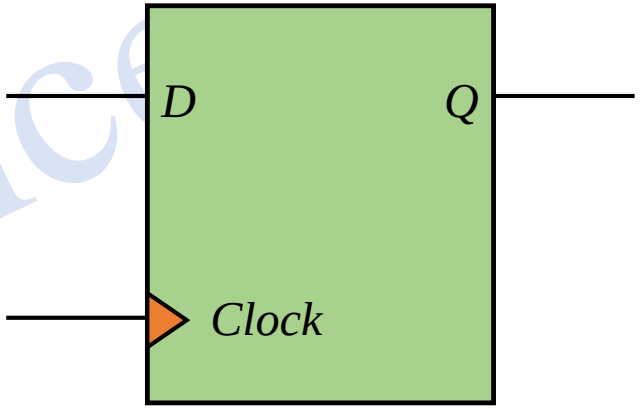
Flip-Flop

Flip Flop Behavior -

For every positive edge of the clock Q changes to become equal to D



Flip Flop Behavior as Verilog Code -

```
always @ (posedge clock)
  Q <= D;
```

always @ ()
- Triggers execution of the following code block
- () is called 'Sensitivity List'
  -- Describe when execution triggered

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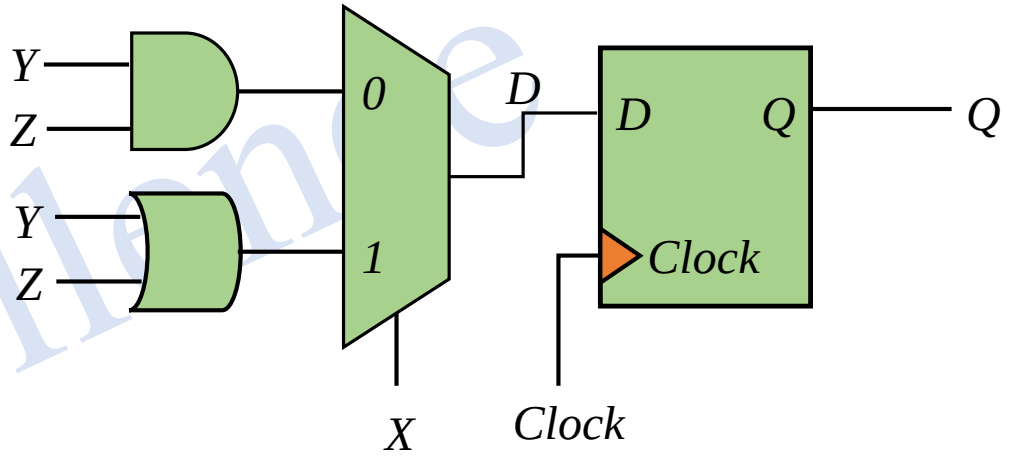
Verilog Module for Flip Flop

```
module flipflop (Clock, X, Y, Z, Q);

    input Clock, X, Y, Z;
    output Q;
    reg Q;
    wire D;
assign D = X ? Y | Z : Y & Z;

always @ (posedge Clock)
   begin
       Q <= D;
    end
endmodule
```



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Verilog Module for Flip Flop

```
module flipflop (Clock, X, Y, Z, Q);

    input Clock, X, Y, Z;
    output Q;
    reg Q;
    wire D;
assign D = X ? Y | Z : Y & Z;

always @ (posedge Clock)
   begin
       Q <= D;
    end
endmodule
```

Module Name

Connected Ports

Port Declarations

Local Variables Declarations

Code Segments

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RTL Coding Styles

Three Coding Styles -

- always @(???edge Clock) -> Flip Flops and Input Logic
- always @(*) -> Combinational Logic (CL) specified by its behavior
- assign a = . . . -> Combinational Logic (CL) specified as structure

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Thanks !!