Finite State Machine (FSM) Design Techniques in Verilog HDL

Video Lecture Link1

Video Lecture Link2

Video Lecture Link3

Finite State Machine (FSM) Design Techniques

- What is FSM ?
- Moore and Mealy FSM Block Diagram
- FSM Design Techniques
- Verilog HDL Design
- Synthesizing the Design
- Test Bench Design
- Analysing Simulation Waveforms

Finite State Machine (FSM) Design Techniques

In Digital VLSI design, Finite State Machines play a very important role in implementing the correct behaviour of the system during different operating modes.

The FSM enables the system to go through different operating modes as per the user requirements or during the self booting process

Finite State Machine (FSM) Design Techniques

Moore and Mealy FSM

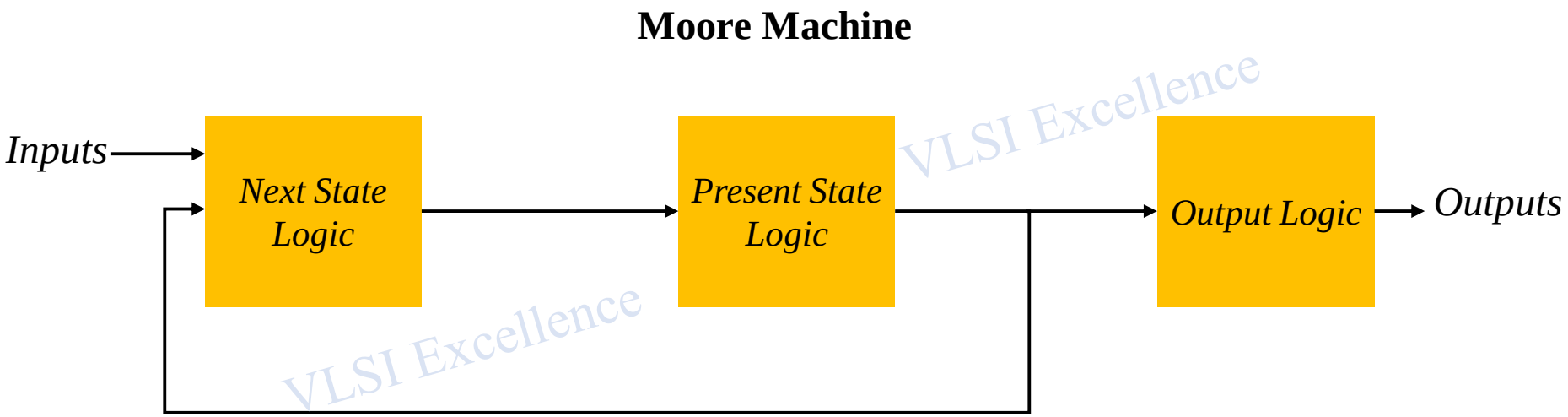

Figure #01: Moore Finite State Machine Block Diagram

Finite State Machine (FSM) Design Techniques

Moore and Mealy FSM

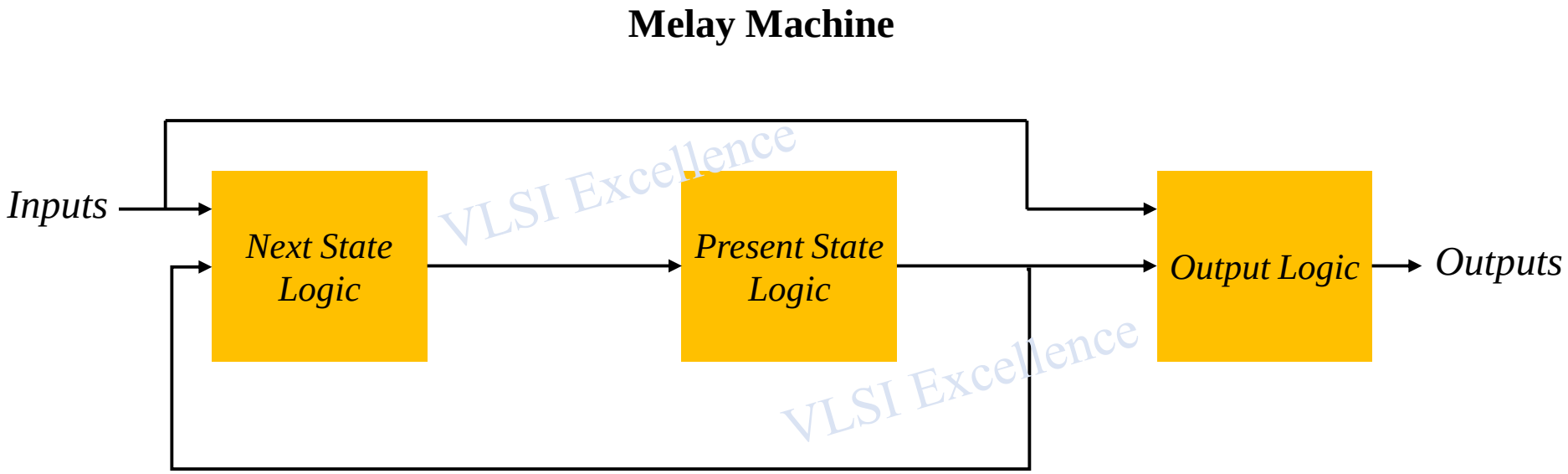

Figure #02: Melay Finite State Machine Block Diagram

Finite State Machine (FSM) Design Techniques

Different Techniques to Design Finite State Machines are as below –

1) Using a Single Process (Procedural Block) to Code Present State, Next State and Output Logic

2) Using Two Process, One to code Present State and Next State logic and another to code Output Logic,

3) Using Three Process each to code Present State, Next State and Output Logic

Finite State Machine (FSM) Design Techniques

Verilog HDL Design and Test-Bench Simulation:

We will be using **EDA Playground (https://www.edaplayground.com)** to design Fixed Priority Round Robin Arbiter in Verilog HDL.

Synthesis using Open Source Synthesis Tool : **Yosys** (Available in EDA Playgound)

Simulation using Open Source Simulation Tool : **Riviera** (Available in EDA Playground)

Verilog Project Link1

Verilog Project Link2

Verilog Project Link3

Finite State Machine (FSM) Design Techniques

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Thank You !!!