Module #15 : Verilog HDL Compiler Directives

15.1: Compiler Directives:

- Compiler directives are special commands, beginning with `, that affect the operation of the Verilog simulator.
- A compiler directive is a statement that causes the compiler to take a specific action during compilation.
- *Examples :*
    1) Time Scale
    2) Macro Definitions
    3) Include Directive

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15.2: Time Scale:

- **`timescale** specifies the time unit and time precision. A time unit of 10 ns means a time expressed as say #2.3 will have a delay of 23.0 ns.
- Time precision specifies how delay values are to be rounded off during simulation.
- Valid time units include s, ms, us (µs), ns, ps, fs.
- Only 1, 10 or 100 are valid integers for specifying time units or precision.
- It also determines the displayed time units in display commands like $display.

Syntax:

`timescale *time_unit/time_precision;*

Example 14 .1:

`timescale *1 ns/1 ps // unit =1ns, precision=1/1000ns*

`timescale *1 ns /100 ps // time unit = 1ns; precision = 0.1ns;*

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Example 15 .2:

`timescale 100ps/10ps shall have a #1 delay of 100ps while you can give #0.1 as the smallest delay i.e. of 10ps.

`timescale 1ns/1ps shall have `#1` as 1ns and `#0.001ns` as 1ps as the smallest delay.

`timescale 10ps/1fs shall represent a #1 of 10ps delay and #0.001ps is the smallest measurable delay.

`timescale 1ns/1ns ; #0.49 , which is less than half a time unit. However the time precision is specified as 1ns and hence the simulator can not go smaller than 1ns which makes it to round to 0ns
#0.51; will get rounded to 1ns

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15.3: Macro Definitions:

- A macro is an identifier that represents a string of text. Macros are defined with the directive `define, and are invoked with the quoted macro name as shown in the example.
- Verilog compilers will substitute the string for the macro name before starting compilation.
- The `define statement must appear in the file before the statement using the string. If they are in separate files, the file containing the definition must be compiled first.

Syntax:

`define *macro_name text_string;*

. . . `macro_name . .

Example 14 .3:

`define *add_lsb a[7:0] + b[7:0]*

`define *N 8 // Word length*

wire [`N -1:0] S;

assign S = `add_lsb; // assign S = a[7:0] + b[7:0];

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15.4: Include Directive:

- Include is used to include the contents of a text file at the point in the current file where the include directive is.
- The include directive is similar to the C/C++ include directive.

Syntax:

`include *file_name;*

Example 14 .4:

```
module x;
`include "dclr.v"; // contents of file "dclr,v" are put here
```