Course Content

1. Introduction to Verilog ----------

Verilog HDL Brief Description, Level of Abstraction

2. Verilog Lexical Tokens ----------

White Space, Comments, Numbers, Identifiers, Operators, Verilog Keywords

3. Verilog Data Types ----------

Value Set, Wire, Reg, Input, Output, Inout, Integer, Supply0, Supply1, Time, Parameter

4. Operators ----------

Arithmetic Operators, Relational Operators, Bit-wise Operators, Logical Operators, Reduction Operators, Shift Operators, Concatenation Operator, Conditional Operator, Operator Precedence

5. Operands ----------

Literals, Wires, Regs, and Parameters, Bit-Selects “x[3]” and Part-Selects “x[5:3]”, Function Calls

Course Content

6. Modules----------

Module Declaration, Module Instantiations, Parameterized Modules, Continuous Assignment

7. Behavioral Modeling ----------

Procedural Assignments, Delay in Assignment, Blocking and Nonblocking Assignments, begin ... end, for Loops, while Loops, forever Loops, repeat, disable, if ... else if ... else case, casex, casez

8. Timing Controls----------

Delay Control, Event Control, @, Wait Statement, Intra-Assignment Delay

9. Procedures: Always and Initial Blocks ----------

Always Block, Initial Block

10. Functions ----------

Function Declaration, Function Return Value, Function Call, Function Rules, Example

Course Content

11. Tasks----------

12. Component Inference ----------

Registers, Latches, Flip-flops, Counters, Multiplexers, Adders/Subtracters, Tri-State Buffers Other Component Inferences

13. Finite State Machines ----------

Counters, Shift Registers

14. Memories ----------

Two-dimensional arrays, Initializing memory from a file

15. Compiler Directives----------

Time Scale, Macro Definitions, Include Directive

Course Content

16. System Tasks and Functions ----------

$display, $strobe, $monitor; $time, $stime, $realtime; $reset, $stop, $finish; $deposit; $scope, $showscope; $list; $random; $dumpfile, $dumpvar, $dumpon, $dumpoff, $dumpall; $shm_probe, $shm_open, $fopen, $fdisplay, $fstrobe, $fmonitor.

17. Test Benches ----------

Test Benches, Synchronous Test Benches

18. Verilog HDL Interview Questions – Asked in Top Semiconductor MNCs----------

19. Frequently Asked Interview Questions List----------

20. Verilog HDL Practice Question Bank ----------

Course Content

Crash Course Duration : 200 Minutes

(Average 10 Minutes Per Module * 20 = 200 Minutes)