	October 4th, 2021	October 5th, 2021	October 6th, 2021	October 7th, 2021	October 8th, 2021
CET time GMT + 2	**Monday**	**Tuesday**	**Wednesday**	**Thursday**	**Friday**
08:15 am 09:00 am	*Opening: VLSI SoC 40th anniversary*				
09:00 am 10:00 am	Keynote 1 Kurt Keutzer	Industrial Talk 1 Kanisha Bhaduri	Industrial Talk 2 Sunil Cheruvu	Industrial Talk 3 Peter Debacker	Keynote 3 Damien Querlioz
10:00 am 10:15 am	Break				
10:15 am 11:45 am	Oral session 1	Oral session 2	Oral session 3	Special session 2	Special session 3
11:45 am 12:00 pm	Break				
12:00 pm 01:00 pm		Special session 1	Oral session 4	PhD Forum	*Closing session and Awards*
01:00 pm 02:00 pm	Poster session 1	Poster session 2			
02:00 pm 03:00 pm			Keynote 2 Ruby Lee		

Keynotes:

1. **The Deep Learning Software Stack: What Every NN Accelerator Architect Should Know,**
   Kurt Keutzer, UC Berkeley

2. **Preventing Secret leaks from Edge Devices,**
   Ruby Lee, Princeton University, USA

3. **Memory-Centric Artificial Intelligence**,
   Damien Querlioz, CNRS, Université Paris-Saclay, France

Industrial Talks:

1. **Running Privacy-aware Machine Learning Applications on Edge Devices,**
   Kaniskha Bhaduri, Apple, USA

2. **Intelligent Edge security challenges and HW based technologies to the rescue,**
   Sunil Cheruvu, Intel, USA

3. **Optimizing memory device technology for energy efficient AI hardware,**
   Peter Debacker, IMEC, Belgium

Special Sessions

1. **Secure Hardware Architectures**
   Organizers: *Nele Mentens, KU Leuven and University of Leiden*

   This session concentrates on the design and evaluation of hardware and system-on-chip solutions for data security. Three important aspects of secure hardware architectures are covered in the session. The first talk will be on trusted execution environments for system-on-chip platforms. The second talk will be on novel countermeasures for physical security. The third talk will be on secure hardware architectures for post-quantum cryptography.

   Talk 1: In Hardware We Trust? From TPMs to Enclave Computing on RISC-V,
   Speaker: *Ahmad-Reza Sadeghi*, TU Darmstadt, Germany

   Talk 2: Physical security evaluation of rotation-based countermeasures,
   Speaker: *Lejla Batina*, Radboud University, The Netherlands

   Talk 3: Secure Post-Quantum Crypto in MPSoC Environments,
   Speaker: *Johanna Sepulveda*, Airbus, Germany

2. **Towards Reliable In-Memory Computing: From Emerging Devices to Post-von-Neumann Architectures**
   Organizers: Hussam Amrouch and Ilia Polian

   This special session aims at providing a comprehensive cross-layer overview on how post-von-Neumann architectures can be realized using three interesting different emerging technologies: logic-in-memory architectures based on Ferroelectric FETs; memristive computation-in memory architectures; and brain inspired approaches powered by novel memristive devices. Various abstraction layers will be covered starting from semiconductor device physics to circuit and microarchitecture levels all the way up to the system level. Special attention is put on reliability aspects.

   Talk 1: Reliable Computing Beyond von-Neumann on Unreliable Ferroelectric Transistors,
   Speaker: *Hussam Amrouch*, University of Stuttgart, Germany

   Talk 2: Emerging Memristive Devices for Unconventional Brain-Inspired Computing,
   Speaker: *Nan Du*, Fraunhofer Institute for Electronic Nano Systems, Research Fab Microelectronics Germany

   Talk 3: Ultra-low Power Memristor based Computation-in-Memory for Edge AI,
   Speaker: *Said Hamdioui*, TU Delf, Netherland.

3. **Intelligent, Secure, Efficient Cyber-Physical Systems on Heterogeneous System on Chips**
   Organizers: Apostolos P. Fournaris, Aris Lalos

   The special session is providing insight in one of the latest trend of System on Chip design, which is the SoCs heterogeneity. Latest SoCs, provide CPUs, GPUs as well as FPGA fabrics within the SoC structure and this opens the potentials for a broad range of intelligent and secure applications that can be implemented in a highly efficient manner.

   Talk 1: Title: Enabling Cooperative CAV awareness in heterogeneous SOC Devices,
   Speaker: *Nousias Stavros*, University of Patras

   Talk 2: Evaluating and accelerating Number Theoretic Transform for Postquantum Cryptography Algorithms in System-on-chip FPGAs
   Speaker: *Alexander El-Kandy*, University of Patras

   Talk 3: A Modular Approach to Introduce Fixed-Logic FPGA accelerators to PoCL,
   Speaker: *Georgios Keramidas*, University of Thessaloniki.

Oral sessions

1. **Emerging Technologies and Analog/Mixed-signal Circuits**

[60] A 13.56 MHz Active Rectifier with PMOS AC-DC Interface for Wireless Powered Medical Implants, *Jianming Zhao and Yuan Gao*
[67] Design of Fully Differential Energy-Efficient Inverter-Based Low-Noise Amplifier for Ultrasound Imaging, *Zhaoyang Cao, Tan-Tan Zhang, Yuan Gao and Wang Ling Goh*
[03] A Reconfigurable Nanophotonic Architecture based on Phase Change Material, *Parya Zolfaghari and Sébastien Le Beux*
[21] Metastability with Emerging Reconfigurable Transistors: Exploiting Ambipolarity for Throughput, *Abhiroop Bhattacharjee, Shubham Rai, Ansh Rupani, Michael Raitza and Akash Kumar*
[28] A Self-referenced and regulated sensing solution for PCM with OTS selector*, Julien Gasquez, Bastien Giraud, Philippe Boivin, Yohann Moustapha-Rabault, Vincenzo Della-Marca, Jean-Pierre Walder and Jean-Michel Portal*

2. **VLSI and Embedded System Design**

[09] Processor Architecture Optimization for Spatially Dynamic Neural Networks, *Steven Colleman, Thomas Verelst, Linyan Mei, Tinne Tuytelaars and Marian Verhelst*
[43] Hardware-In-The Loop Emulation for Agile Co-Design of Parallel Ultra-Low Power IoT Processors, *Luca Valente, Davide Rossi and Luca Benini*
[53] AdapTTA: Adaptive Test-Time Augmentation for Reliable Embedded ConvNets, *Luca Mocerino, Roberto Giorgio Rizzo, Valentino Peluso, Andrea Calimera and Enrico Macii*

[66] Adaptive Random Forests for Energy-Efficient Inference on Microcontrollers, *Francesco Daghero, Alessio Burrello, Chen Xie, Luca Benini, Andrea Calimera, Enrico Macii, Massimo Poncino and Daniele Jahier Pagliari*

[62] A 25 TOPS/W High Power Efficiency Deterministic and Split Stochastic MAC (SC-MAC) Design, *Ming Ming Wong, Lu Chen and Anh Tuan Do*

3. Testing and Verification

[18] System-level bug explanation through program slicing and instruction clusterization, *Moreno Bragaglio, Samuele Germiniani, Graziano Pravadelli and Nicola Donatelli*

[29] Metamorphic Testing for Processor Verification: A RISC-V Case Study at the Instruction Level, *Frank Riese, Vladimir Herdt, Daniel Große and Rolf Drechsler*

[38] On Antagonism Between Side-Channel Security and Soft-Error Reliability in BNN Inference Engines, *Xinhui Lai, Thomas Lange, Aneesh Balakrishnan, Dan Alexandrescu and Maksim Jenihhin*

[47] Cross-layer Approach to Assess FMEA on Critical Systems and Evaluate High-Level Model Realism, *Julie Roux, Katell Morin-Allory, Vincent Beroulle, Régis Leveugle, Gilles Genevrier, Frédéric Cézilly, Lilian Bossuet and François Cerisier*

[52] On the Evaluation of SEEs on Open-Source Embedded Static RAMs, *Luca Sterpone, Sarah Azimi and Corrado De Sio*

4. Computer-Aided Design and Design for Security

[01] Security Assessment of Heterogeneous SoC-FPGA: On the Practicality of Cache Timing Attacks, *Lilian Bossuet and El Mehdi Benhani*

[02] Logic Locking at the Frontiers of Machine Learning: A Survey on Developments and Opportunities, *Dominik Sisejkovic, Lennart M. Reimann, Elmira Moussavi, Farhad Merchant and Rainer Leupers*

[23] Aspect-Oriented Design Automation with Model Transformation, *Zhao Han, Deyan Wang, Gabriel Rutsch, Bowen Li, Sebastian Siegfried Prebeck, Daniela Sanchez Lopera, Keerthikumara Devarajegowda and Wolfgang Ecker*

[45] A High-Level Design Flow for Locally Body-Biased Asynchronous Circuits, *Yoan Decoudu, Katell Morin-Allory and Laurent Fesquet*

Poster session 1

[04] Efficient Implementation of Activation Functions for LSTM accelerators, *Yi Sheng Chong, Wang Ling Goh, Yew Soon Ong, Vishnu P. Nambiar and Anh Tuan Do*

[11] An Efficient Light-weight Configurable Approximate Adder Design, *Hongwei Li, Xuemei Fan, Qiang Li and Hao Liu*

[71] Algebraic Techniques for Rectification of Finite Field Circuits, *Vikas Rao, Haden Ondricek, Priyank Kalla and Florian Enescu*

[41] Evaluating a DFT Strategy's Capability to Detect Emerging Faults in RRAMs, *Thiago Santos Copetti and Leticia Maria Bolzani Poehls*

[55] Using Monte Carlo Tree Search for CAD – A Case-study with Designing Cross-layer Reliability for Heterogeneous Embedded Systems, *Siva Satyendra Sahoo and Akash Kumar*

Poster session 2

[25] A 12 pA Sigma Delta ADC Topology for Chemiresistive Sensor-Based Application, *Matthieu Couriol, Edouard Giacomin and Pierre-Emmanuel Gaillardon*

[24] A Novel High-Gain Amplifier Circuit Using Super-Steep-Subthreshold-Slope Field-Effect Transistors, *Matthieu Couriol, Patsy Cadareanu, Edouard Giacomin and Pierre-Emmanuel Gaillardon*

[27] Energy Efficient and Multiplierless Approximate Integer DCT Implementation for HEVC, *Skandha Deepsita Sarvepalli, Divya K and Noor Mahammad Sk*

[69] Reducing Breakdown Voltage in a Bipolar Impact Ionization MOSFET (BI-MOS) using Gate–Source Underlap, *Akshay Balaji and Sneh Saurabh*

[56] CLEO-CoDe: Exploiting Constrained Decoding for Cross-Layer Energy Optimization in Heterogeneous Embedded Systems, *Siva Satyendra Sahoo and Akash Kumar*

PhD Forum

[74] Trustworthy Hardware Design with Logic Locking, *Dominik Sisejkovic and Rainer Leupers*

[75] Ph.D. Forum: Hardware Trojans in Reconfigurable Computing, *Qazi Arbab Ahmed*

[76] Exploring a New Tool for Automatic Layout Synthesis for FDSOI 28 nm, *Vitor Hugo Fuerstenau Maciel, Germano Girondi, Elias de Almeida Ramos and Ricardo Augusto da Luz Reis*

[77] Classical and Physical Security of Symmetric Key Cryptographic Algorithms, *Anubhab Baksi*

[79] Practical Side-Channel and Fault Attacks on Lattice-Based Cryptography, *Prasanna Ravi*

[80] In Quest for Fast and Secure SoC, *Naina Gupta and Anupam Chattopadhyay*

[81] Formal Analysis of Physically Unclonable Functions, *Durba Chatterjee, Debdeep Mukhopadhyay and Aritra Hazra*

[82] Design and Analysis of Logic Locking Techniques, *Akashdeep Saha, Debdeep Mukhopadhyay and Rajat Subhra Chakraborty*