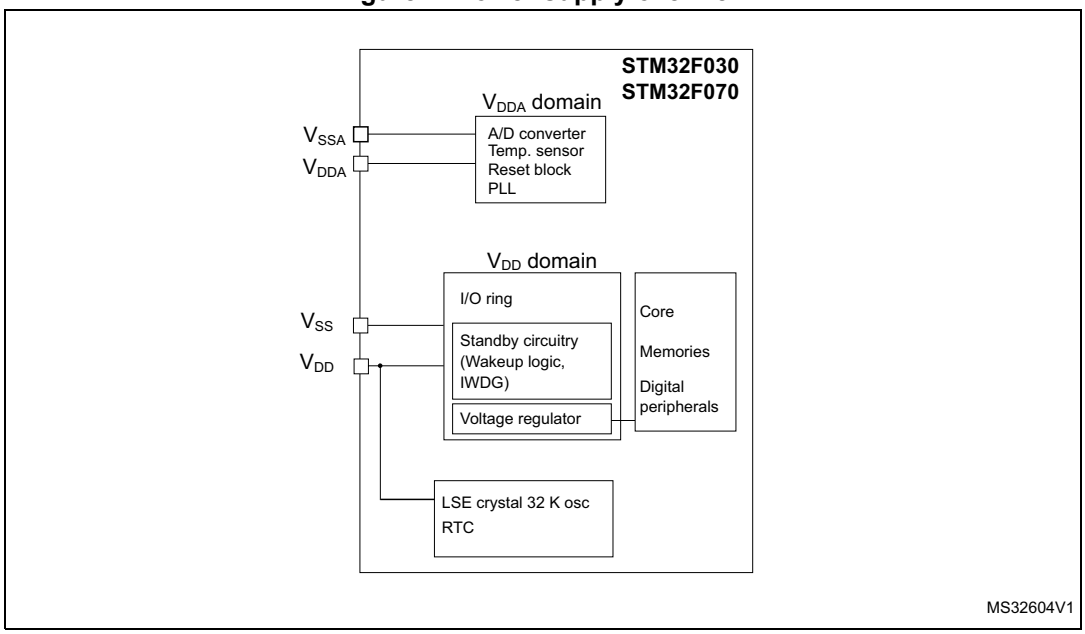
6 Power control (PWR)

6.1 Power supplies

The STM32F030/STM32F070 subfamily embeds a voltage regulator in order to supply the internal 1.8 V digital power domain.

- The STM32F030/STM32F070 devices require a 2.4 V - 3.6 V operating supply voltage (V_{DD}) and a 2.4 V - 3.6 V analog supply voltage (V_{DDA}).

Figure 7. Power supply overview



6.1.1 Independent A/D converter supply and reference voltage

To improve conversion accuracy and to extend the supply flexibility, the ADC has an independent power supply which can be separately filtered and shielded from noise on the PCB.

- The ADC voltage supply input is available on a separate V_{DDA} pin.
- An isolated supply ground connection is provided on pin V_{SSA}.

The V_{DDA} supply/reference voltage must be equal or higher than V_{DD}.

When a single supply is used, V_{DDA} can be externally connected to V_{DD}, through the external filtering circuit in order to ensure a noise free V_{DDA} reference voltage.

When V_{DDA} is different from V_{DD}, V_{DDA} must always be higher or equal to V_{DD}. To keep safe potential difference in between V_{DDA} and V_{DD} during power-up/power-down, an external Shottky diode may be used between V_{DD} and V_{DDA}. Refer to the datasheet for the maximum allowed difference.

6.1.2 Voltage regulator

The voltage regulator is always enabled after Reset. It works in three different modes depending on the application modes.

- In Run mode, the regulator supplies full power to the 1.8 V domain (core, memories and digital peripherals).
- In Stop mode the regulator supplies low-power to the 1.8 V domain, preserving contents of registers and SRAM
- In Standby Mode, the regulator is powered off. The contents of the registers and SRAM are lost except for the Standby circuitry.

6.2 Power supply supervisor

6.2.1 Power on reset (POR) / power down reset (PDR)

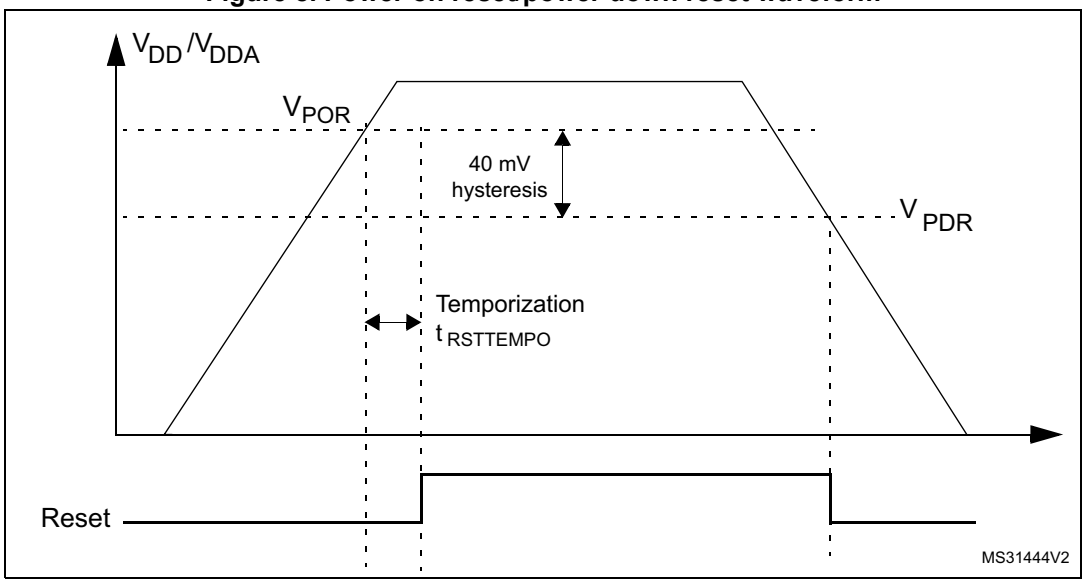
The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits which are always active and ensure proper operation above a threshold of 2 V.

The device remains in Reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase V_{DDA} must arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages. However, the V_{DDA} power supply supervisor can be disabled (by programming a dedicated option bit $V_{DDA\_MONITOR}$) to reduce the power consumption if the application is designed to make sure that V_{DDA} is higher than or equal to V_{DD}.

For more details on the power on / power down reset threshold, refer to the electrical characteristics section in the datasheet.

Figure 8. Power on reset/power down reset waveform



6.3 Low-power modes

By default, the microcontroller is in Run mode after a system or a power Reset. Several low-power modes are available to save power when the CPU does not need to be kept running, for example when waiting for an external event. It is up to the user to select the mode that gives the best compromise between low-power consumption, short startup time and available wakeup sources.

The device features three low-power modes:

- Sleep mode (CPU clock off, all peripherals including ARM® Cortex®-M0 core peripherals like NVIC, SysTick, etc. are kept running)
- Stop mode (all clocks are stopped)
- Standby mode (1.8V domain powered-off)

In addition, the power consumption in Run mode can be reduce by one of the following means:

- Slowing down the system clocks
- Gating the clocks to the APB and AHB peripherals when they are unused.

Table 15. Low-power mode summary

Mode name	Entry	wakeup	Effect on 1.8V domain clocks	Effect on V_{DD} domain clocks	Voltage regulator
Sleep (Sleep now or Sleep-on - exit)	WFI	Any interrupt	CPU clock OFF no effect on other clocks or analog clock sources	None	ON
	WFE	Wakeup event			
Stop	PDDS and LPDS bits + SLEEPDEEP bit + WFI or WFE	Any EXTI line (configured in the EXTI registers)	All 1.8V domain clocks OFF	HSI and HSE oscillators OFF	ON or in low-power mode (depends on *Power control register (PWR_CR)*)
Standby	PDDS bit + SLEEPDEEP bit + WFI or WFE	WKUP pin rising edge, RTC alarm, external reset in NRST pin, IWDG reset			OFF

6.3.1 Slowing down system clocks

In Run mode the speed of the system clocks (SYSCLK, HCLK, PCLK) can be reduced by programming the prescaler registers. These prescalers can also be used to slow down peripherals before entering Sleep mode.

For more details refer to *Section 7.4.2: Clock configuration register (RCC_CFGR)*.

6.3.2 Peripheral clock gating

In Run mode, the AHB clock (HCLK) and the APB clock (PCLK) for individual peripherals and memories can be stopped at any time to reduce power consumption.

To further reduce power consumption in Sleep mode the peripheral clocks can be disabled prior to executing the WFI or WFE instructions.

Peripheral clock gating is controlled by the *AHB peripheral clock enable register (RCC_AHBENR)*, the *APB peripheral clock enable register 2 (RCC_APB2ENR)* and the *APB peripheral clock enable register 1 (RCC_APB1ENR)*.

6.3.3 Sleep mode

Entering Sleep mode

The Sleep mode is entered by executing the WFI (Wait For Interrupt) or WFE (Wait for Event) instructions. Two options are available to select the Sleep mode entry mechanism, depending on the SLEEPONEXIT bit in the ARM® Cortex®-M0 System Control register:

- Sleep-now: if the SLEEPONEXIT bit is cleared, the MCU enters Sleep mode as soon as WFI or WFE instruction is executed.
- Sleep-on-exit: if the SLEEPONEXIT bit is set, the MCU enters Sleep mode as soon as it exits the lowest priority ISR.

In the Sleep mode, all I/O pins keep the same state as in the Run mode.

Refer to *Table 16* and *Table 17* for details on how to enter Sleep mode.

Exiting Sleep mode

If the WFI instruction is used to enter Sleep mode, any peripheral interrupt acknowledged by the nested vectored interrupt controller (NVIC) can wake up the device from Sleep mode.

If the WFE instruction is used to enter Sleep mode, the MCU exits Sleep mode as soon as an event occurs. The wakeup event can be generated either by:

- enabling an interrupt in the peripheral control register but not in the NVIC, and enabling the SEVONPEND bit in the ARM® Cortex®-M0 System Control register. When the MCU resumes from WFE, the peripheral interrupt pending bit and the peripheral NVIC IRQ channel pending bit (in the NVIC interrupt clear pending register) have to be cleared.
- or configuring an external or internal EXTI line in event mode. When the CPU resumes from WFE, it is not necessary to clear the peripheral interrupt pending bit or the NVIC IRQ channel pending bit as the pending bit corresponding to the event line is not set.

This mode offers the lowest wakeup time as no time is wasted in interrupt entry/exit.

Refer to *Table 16* and *Table 17* for more details on how to exit Sleep mode.

Table 16. Sleep-now

Sleep-now mode	Description
Mode entry	WFI (Wait for Interrupt) or WFE (Wait for Event) while: – SLEEPDEEP = 0 and – SLEEPONEXIT = 0 Refer to the ARM® Cortex®-M0 System Control register.
Mode exit	If WFI was used for entry: Interrupt: Refer to *Table 32: Vector table* If WFE was used for entry Wakeup event: Refer to *Section 11.2.3: Event management*
Wakeup latency	None

Table 17. Sleep-on-exit

Sleep-on-exit	Description
Mode entry	WFI (wait for interrupt) while: – SLEEPDEEP = 0 and – SLEEPONEXIT = 1 Refer to the ARM® Cortex®-M0 System Control register.
Mode exit	Interrupt: Refer to *Table 32: Vector table*.
Wakeup latency	None

6.3.4 Stop mode

The Stop mode is based on the ARM® Cortex®-M0 deep sleep mode combined with peripheral clock gating. The voltage regulator can be configured either in normal or low-power mode. In Stop mode, all clocks in the 1.8 V domain are stopped, the PLL, the HSI and the HSE oscillators are disabled. SRAM and register contents are preserved.

In the Stop mode, all I/O pins keep the same state as in the Run mode.

Entering Stop mode

Refer to *Table 18* for details on how to enter the Stop mode.

To further reduce power consumption in Stop mode, the internal voltage regulator can be put in low-power mode. This is configured by the LPDS bit of the *Power control register (PWR_CR)*.

If Flash memory programming is ongoing, the Stop mode entry is delayed until the memory access is finished.

If an access to the APB domain is ongoing, The Stop mode entry is delayed until the APB access is finished.

In Stop mode, the following features can be selected by programming individual control bits:

- Independent watchdog (IWDG): the IWDG is started by writing to its Key register or by hardware option. Once started it cannot be stopped except by a Reset. See *Section 19.3: IWDG functional description* in *Section 19: Independent watchdog (IWDG)*.

- real-time clock (RTC): this is configured by the RTCEN bit in the *RTC domain control register (RCC_BDCR)*
- Internal RC oscillator (LSI): this is configured by the LSION bit in the *Control/status register (RCC_CSR)*.
- External 32.768 kHz oscillator (LSE): this is configured by the LSEON bit in the *RTC domain control register (RCC_BDCR)*.

The ADC can also consume power during Stop mode, unless it is disabled before entering this mode. Refer to *ADC control register (ADC_CR)* for details on how to disable it.

Exiting Stop mode

Refer to *Table 18* for more details on how to exit Stop mode.

When exiting Stop mode by issuing an interrupt or a wakeup event, the HSI oscillator is selected as system clock.

When the voltage regulator operates in low-power mode, an additional startup delay is incurred when waking up from Stop mode. By keeping the internal regulator ON during Stop mode, the consumption is higher although the startup time is reduced.

Table 18. Stop mode

Stop mode	Description
Mode entry	WFI (Wait for Interrupt) or WFE (Wait for Event) while: – Set SLEEPDEEP bit in ARM® Cortex®-M0 System Control register – Clear PDDS bit in Power Control register (PWR_CR) – Select the voltage regulator mode by configuring LPDS bit in PWR_CR **Note:** To enter Stop mode, all EXTI Line pending bits (in *Pending register (EXTI_PR)*), all peripherals interrupt pending bits and RTC Alarm flag must be reset. Otherwise, the Stop mode entry procedure is ignored and program execution continues. If the application needs to disable the external oscillator (external clock) before entering Stop mode, the system clock source must be first switched to HSI and then clear the HSEON bit. Otherwise, if before entering Stop mode the HSEON bit is kept at 1, the security system (CSS) feature must be enabled to detect any external oscillator (external clock) failure and avoid a malfunction when entering Stop mode.
Mode exit	If WFI was used for entry: – Any EXTI Line configured in Interrupt mode (the corresponding EXTI Interrupt vector must be enabled in the NVIC). Refer to *Table 32: Vector table*. If WFE was used for entry: Any EXTI Line configured in event mode. Refer to *Section 11.2.3: Event management on page 173*
Wakeup latency	HSI wakeup time + regulator wakeup time from Low-power mode

6.3.5 Standby mode

The Standby mode allows to achieve the lowest power consumption. It is based on the ARM® Cortex®-M0 deepsleep mode, with the voltage regulator disabled. The 1.8 V domain is consequently powered off. The PLL, the HSI oscillator and the HSE oscillator are also switched off. SRAM and register contents are lost except for registers in the Standby circuitry (see *Figure 7*).

Entering Standby mode

Refer to *Table 19* for more details on how to enter Standby mode.

In Standby mode, the following features can be selected by programming individual control bits:

- Independent watchdog (IWDG): the IWDG is started by writing to its Key register or by hardware option. Once started it cannot be stopped except by a reset. See *Section 19.3: IWDG functional description* in *Section 19: Independent watchdog (IWDG)*.
- Real-time clock (RTC): this is configured by the RTCEN bit in the *RTC domain control register (RCC_BDCR)*.
- Internal RC oscillator (LSI): this is configured by the LSION bit in the *Control/status register (RCC_CSR)*.
- External 32.768 kHz oscillator (LSE): this is configured by the LSEON bit in the *RTC domain control register (RCC_BDCR)*.

Exiting Standby mode

The microcontroller exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on one of the enabled WKUPx pins or an RTC event occurs. All registers are reset after wakeup from Standby except for *Power control/status register (PWR_CSR)*.

After waking up from Standby mode, program execution restarts in the same way as after a Reset (boot pin sampling, option bytes loading, reset vector is fetched, etc.). The SBF status flag in the *Power control/status register (PWR_CSR)* indicates that the MCU was in Standby mode.

Refer to *Table 19* for more details on how to exit Standby mode.

Table 19. Standby mode

Standby mode	Description
Mode entry	WFI (Wait for Interrupt) or WFE (Wait for Event) while: – Set SLEEPDEEP in ARM® Cortex®-M0 System Control register – Set PDDS bit in Power Control register (PWR_CR) – Clear WUF bit in Power Control/Status register (PWR_CSR)
Mode exit	WKUP pin rising edge, RTC alarm event's rising edge, external Reset in NRST pin, IWDG Reset.
Wakeup latency	Reset phase

I/O states in Standby mode

In Standby mode, all I/O pins are high impedance except:

- Reset pad (still available)
- PC13, PC14 and PC15 if configured by RTC or LSE
- WKUPx pins

Debug mode

By default, the debug connection is lost if the application puts the MCU in Stop or Standby mode while the debug features are used. This is due to the fact that the ARM® Cortex®-M0 core is no longer clocked.

However, by setting some configuration bits in the DBGMCU_CR register, the software can be debugged even when using the low-power modes extensively.

6.3.6 RTC wakeup from low-power mode

The RTC can be used to wakeup the MCU from low-power mode by means of the RTC alarm. For this purpose, two of the three alternative RTC clock sources can be selected by programming the RTCSEL[1:0] bits in the *RTC domain control register (RCC_BDCR)*:

- Low-power 32.768 kHz external crystal oscillator (LSE OSC)
  This clock source provides a precise time base with very low-power consumption (less than 1µA added consumption in typical conditions)
- Low-power internal RC Oscillator (LSI)
  This clock source has the advantage of saving the cost of the 32.768 kHz crystal. This internal RC Oscillator is designed to add minimum power consumption.

To wakeup from Stop mode with an RTC alarm event, it is necessary to:

- Configure the EXTI Line 17 to be sensitive to rising edge
- Configure the RTC to generate the RTC alarm

To wakeup from Standby mode, there is no need to configure the EXTI Line 17.

6.4 Power control registers

The peripheral registers can be accessed by half-words (16-bit) or words (32-bit).

6.4.1 Power control register (PWR_CR)

Address offset: 0x00

Reset value: 0x0000 0000 (reset by wakeup from Standby mode)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	Res	Res	Res	DBP	Res	Res	Res	Res	CSBF	CWUF	PDDS	LPDS
							rw					rc_w1	rc_w1	rw	rw

Bits 31:9 Reserved, must be kept at reset value.

Bit 8 **DBP**: Disable RTC domain write protection.
In reset state, the RTC registers are protected against parasitic write access. This bit must be set to enable write access to these registers.
0: Access to RTC disabled
1: Access to RTC enabled

Bits 7:4 Reserved, must be kept at reset value

Bit 3 **CSBF**: Clear standby flag.
This bit is always read as 0.
0: No effect
1: Clear the SBF Standby Flag (write).

Bit 2 **CWUF:** Clear wakeup flag.
This bit is always read as 0.
0: No effect
1: Clear the WUF Wakeup Flag **after 2 System clock cycles**. (write)

Bit 1 **PDDS**: Power down deepsleep.
This bit is set and cleared by software. It works together with the LPDS bit.
0: Enter Stop mode when the CPU enters Deepsleep. The regulator status depends on the LPDS bit.
1: Enter Standby mode when the CPU enters Deepsleep.

Bit 0 **LPDS:** Low-power deepsleep.
This bit is set and cleared by software. It works together with the PDDS bit.
0: Voltage regulator on during Stop mode
1: Voltage regulator in low-power mode during Stop mode

Note: When a peripheral that can work in STOP mode requires a clock, the Power controller automatically switch the voltage regulator from Low-power mode to Normal mode and remains in this mode until the request disappears.

6.4.2 Power control/status register (PWR_CSR)

Address offset: 0x04

Reset value: 0x0000 000X (not reset by wakeup from Standby mode)

Additional APB cycles are needed to read this register versus a standard APB read.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	EWUP 7	EWUP 6	EWUP 5	EWUP 4	Res.	EWUP 2	EWUP 1	Res	Res	Res	Res	Res	Res	SBF	WUF
	rw	rw	rw	rw		rw	rw							r	r

Bits 31:15 Reserved, must be kept at reset value.

Bits 14:11 **EWUPx:** Enable WKUPx pin (available only on STM32F070xB and STM32F030xC devices)

These bits are set and cleared by software.

0: WKUPx pin is used for general purpose I/O. An event on the WKUPx pin does not wakeup the device from Standby mode.

1: WKUPx pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUPx pin wakes-up the system from Standby mode).

Note: These bits are reset by a system Reset.

Bit 10 Reserved, must be kept at reset value.

Bits 9:8 **EWUPx:** Enable WKUPx pin

These bits are set and cleared by software.

0: WKUPx pin is used for general purpose I/O. An event on the WKUPx pin does not wakeup the device from Standby mode.

1: WKUPx pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUPx pin wakes-up the system from Standby mode).

Note: These bits are reset by a system Reset.

Bits 7:2 Reserved, must be kept at reset value.

Bit 1 **SBF:** Standby flag

This bit is set by hardware when the device enters Standby mode and it is cleared only by a POR/PDR (power on reset/power down reset) or by setting the CSBF bit in the *Power control register (PWR_CR)*

0: Device has not been in Standby mode

1: Device has been in Standby mode

Bit 0 **WUF:** Wakeup flag

This bit is set by hardware to indicate that the device received a wakeup event. It is cleared by a system reset or by setting the CWUF bit in the *Power control register (PWR_CR)*

0: No wakeup event occurred

1: A wakeup event was received from one of the enabled WKUPx pins or from the RTC alarm.

Note: An additional wakeup event is detected if one WKUPx pin is enabled (by setting the EWUPx bit) when its pin level is already high.

6.4.3 PWR register map

The following table summarizes the PWR register map and reset values.

Table 20. PWR register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	PWR_CR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DBP	Res.	Res.	Res.	Res.	CSBF	CWUF	PDDS	LPDS
	Reset value																								0					0	0	0	0
0x004	PWR_CSR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	EWUP7(1)	EWUP6(1)	EWUP5(1)	EWUP4(1)	Res.	EWUP2	EWUP1	Res.	Res.	Res.	Res.	Res.	Res.	SBF	WUF
	Reset value																		0	0	0	0		0	0							0	0

1. Available on STM32F070xB and STM32F030xC devices only.

Refer to *Section 2.2.2 on page 37* for the register boundary addresses.