Lakshmi Sowjanya Vendra

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SUMMARY:

Passionate Computer Engineering (EE) graduate student with strong expertise in digital and mixed-signal design, verification, and system integration. Actively seeking internship opportunities for Summer 2025.

EDUCATION

Masters of Science in Computer Engineering (Electrical Engineering) Expected Graduation: May 2026
Arizona State University, Tempe, AZ GPA - 3.32

Bachelor of Technology in Electronics and Communication Engineering June 2024
Amrita Vishwa Vidyapeetham Bengaluru GPA - 3.34

TECHNICAL SKILLS AND RELEVANT COURSES

EDA& Simulation Tools: Cadence (Virtuoso, Innovus, Spectre), Synopsys (Design Compiler, HSPICE | Calibre, StarRC, IC Validator), Mentor Graphics (Modelsim, Questasim), Xilinx (Vivado), MATLAB, Questa Sim, TCAD, Ansys HFSS, Cisco Packet Tracer, Dsch2, AutoCAD, LTspice, Lingua Franca, Simulink, VMware
Embedded & Hardware Platforms: Raspberry Pi, Arduino Uno, Pololu 3pi+ 2040 Robot, RTL Design, ARM Cortex
Programming/Scripting Languages: C, C++, Python, Verilog, VHDL, System Verilog
Coursework: Analog & RF IC Design, Digital Verification and Testing, Transistor Design, VLSI Design, Computer Architecture
Hands-on Skills: Physical Design Implementation (Netlist to GDSII), Physical Verification (DRC/LVS/ERC), Layout Issues, ASIC Design, Digital Circuit Design.

PROFESSIONAL EXPERIENCE

Systems Engineering Intern, Ingersoll Rand, Bengaluru, India January 2024 - June 2024

- Tested Small and Microunit Controllers for air compressors using PuTTY for remote access and OmniMBT for automated testing, employing oscilloscopes, spectrum analyzers, and network analyzers for circuit validation and debugging.
- Conducted power analysis to ensure microcontroller efficiency and optimized PCB layouts using Altium Designer.
- Enhanced system integration through Modbus communication protocol testing over Ethernet.

Intern, Bharat Electronics Limited (BEL), Hyderabad, India July 2023 - August 2023

- Utilized the ZC706 evaluation board for the XC7Z045 SoC along with Xilinx Vivado FPGA and VHDL to design and implement complex digital systems for real-time signal processing.
- Evaluated and optimized VARUNA, a high-performance system, ship-borne Electronic Support Measures (ESM) system, specializing in the interception, detection, classification, and identification of conventional and advanced radar signals.

PROJECTS

RTL to GDSII ASIC Design: Graph Convolutional Neural Networks using Cadence Innovus 7nm PDK Spring 2025

- Developed Verilog for GCN Module for 6 node classification application and verified functionality in Modelsim
- Executed synthesis using design compiler and validated synthesized netlist, conducted automatic place and route (APR) using Innovus, conducted post-APR simulations, and optimized power measurements.

Comprehensive and High-Coverage Verification of ALU and State Machine in SystemVerilog Spring 2025

- Spearheaded the verification of ALU operations, Read/Write protocols, and state machine transitions, developing a comprehensive test plan aligned with chip specifications and ensuring robust validation of all functional scenarios.
- Utilized SystemVerilog testbenches within vi editor, achieving 100% code and functional coverage, ensuring design integrity and seamless state machine behavior across all defined operations.

RTL to GDSII ASIC Design: Two-bit adder using Cadence Innovus 7nm PDK Spring 2025

- Designed and verified a 2-bit adder RTL using Verilog and ModelSim, synthesized with Synopsys Design Compiler, and implemented floorplanning, power planning, CTS, and APR using Cadence Innovus.
- Performed post-layout extraction, timing and power analysis, imported GDSII into Cadence Virtuoso, and ensured design integrity through DRC and LVS checks.

Layout Design: Standard Gates Design and Development using 7nm FINFET and 32nm CMOS PDK Spring 2025

- Engineered schematic and layout of Inverter, NAND, NOR, and XOR using Cadence Virtuoso.
- Performed Transient and DC analysis using HSPICE and the waive viewer tool was used to view the simulations.
- Designed 3x3 layouts for NAND, NOR. Running DRC and LVS checks and debugging the errors. Parasitic extraction (PEX) of the layout using Xact 3D for post-layout simulations.

Autonomous Robot for Surveillance: Object Detection & Live Streaming Fall 2023

- Engineered an autonomous surveillance robot utilizing Raspberry Pi 4 Model B, YOLO v4 for real-time object detection, and L298n Motor Drivers for precise navigation and obstacle avoidance in complex environments.
- Integrated live streaming and alert functionality using Raspberry Pi Camera, LoRa communication for data transmission and Python-based image processing, ensuring continuous monitoring and instantaneous security alerts.

RESEARCH AND PUBLICATION

Enhanced Brain Tumor Classification using Feature Optimization IEEE Mysore Conference, August 2024
Pioneered an optimized deep learning model for brain tumor classification, achieving 94% accuracy. Utilized techniques like RFE and Random Forest to classify tumors efficiently.