LAKSHMI SOWJANYA VENDRA

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SUMMARY

Passionate Computer Engineering Graduate Student with strong expertise in digital and mixed-signal design, verification, and system integration. Proficient in essential hardware engineering tools and methodologies, including schematic capture, circuit layout, and prototype testing. Well-versed in advanced simulation and design tools like Cadence Virtuoso and MATLAB. Skilled in C, Python, VHDL and Verilog for effective design and troubleshooting. Committed to leveraging extensive knowledge in digital system architecture and semiconductor device physics to enhance project outcomes in complex, high technology environments. Actively seeking a internship for Summer 2025 in the field of Electrical Engineering.

EDUCATION

Masters of Science in Computer Engineering(Electrical Engineering) — Graduates by May 2026
Arizona State University, Tempe, AZ — GPA - 2.78

Bachelor of Technology in Electronics and Communication Engineering — June 2024
Amrita Vishwa Vidyapeetham Bengaluru — GPA - 3.34

TECHNICAL SKILLS

Embedded & Hardware Platforms	Raspberry Pi, Arduino Uno, Pololu 3pi+ 2040 Robot, RTL Design, ARM Cortex
Programming Languages	C, C++, Python, MATLAB, Simulink, Verilog ,VHDL, System Verilog
Design & Simulation Tools	Cadence Virtuoso, Questa Sim, TCAD, AutoCAD, LTspice, Lingua Franca, Linux Ansys HFSS, Cisco Packet Tracer, Dsch2, VMware, Microsoft Office (Excel, PowerPoint)
Technical Expertise	Analog and RF IC Design, CMOS Processes, Transistor Design, Wireless Communication, System-Level Simulation, Computer Architecture, SDN, ASIC Verification, RTL Design, Digital IC Design, Debugging, Hardware Validation & Verification, FPGA prototyping CPU Architecture, PCB Design, Embedded Systems, VLSI Design, DFT, DSP

PROFESSIONAL EXPERIENCE

Systems Engineering Intern, Ingersoll Rand, Bengaluru, India — January 2024 - June 2024

- Tested Small and Microunit Controllers for air compressors using PuTTY for remote access and OmniMBT for automated testing, employing oscilloscopes, spectrum analyzers, and network analyzers for circuit validation and debugging.
- Conducted power analysis to ensure microcontroller efficiency and optimized PCB layouts using Altium Designer.
- Enhanced system integration through Modbus communication protocol testing over Ethernet.

Intern, Bharat Electronics Limited (BEL), Hyderabad, India — July 2023 - August 2023

- Utilized the ZC706 evaluation board for the XC7Z045 SoC along with Xilinx Vivado FPGA and VHDL to design and implement complex digital systems for real-time signal processing.
- Gained deep insights into VARUNA, a high-performance, ship-borne Electronic Support Measures (ESM) system, specializing in the interception, detection, classification, and identification of conventional and advanced radar signals.

Trainee, Bharat Sanchar Nigam Limited (BSNL) — August 2022
CDOT NGN Switching , Broadband and FTTH Technologies

- Worked with CDOT NGN Switching to modernize telecommunication exchanges, gaining hands-on experience in broadband infrastructure and data transmission.
- Learned about Cellular (LTE, 5G) , WiFi (802.11n Standards) FTTH technologies, focusing on fiber-optic installations and network management.

Trainee, Teachnook — April 2022 - May 2022

- Completed an IoT/Robotics course certificate , programming IoT devices and developing robot control algorithms.
- Gained hands-on experience in data processing, cloud integration, and IoT security.

PROJECTS

Autonomous Robot for Surveillance — Fall 2023

- Developed an autonomous surveillance robot with object detection and avoidance capabilities, enabling real-time monitoring and navigation in complex environments.
- Integrated live streaming and alert functionality into the robot's system using Raspberry Pi.

Comparator and ADC Block — Spring 2023

- Designed an ultra low power dynamic comparator and ADC block for IoT devices, achieving significant power savings and reducing latency.
- Implemented sample and hold circuit, SAR block, and DAC conversion techniques, integrating a Phase-Locked Loop (PLL) for enhanced timing accuracy and system stability, reducing noise and optimizing signal integrity in the ADC block.

Charge Pump — Fall 2022

- Designed and implemented a high-speed CMOS charge pump circuit for PLL applications in 90nm CMOS technology, achieving low power consumption, high output voltage, and fast settling time using LTSpice.

Optimization Technique — Spring 2022

- Developed a Python-based algorithm to minimize equations using the Golden Section Search Method, enhancing computational efficiency by over 50% for mathematical optimization.

RESEARCH AND PUBLICATION

Enhanced Brain Tumor Classification using Feature Optimization — IEEE Mysore Conference, August 2024
Developed an optimized deep learning model for brain tumor classification, achieving 94% accuracy. Utilized techniques like RFE and Random Forest to classify tumors efficiently.