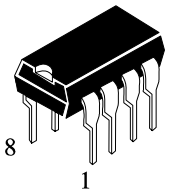
CMOS IC of Real Time Watch with Serial Interface, 56 X 8 RAM

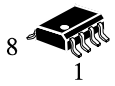
The IN1307 is a low power full BCD clock calendar plus 56 bytes of nonvolatile SRAM. Address and data are transferred serially via a 2-wire bi-directional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The IN1307 has a built-in power sense circuit which detects power failures and automatically switches to the battery supply.

Functions and Features

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100
- 56 byte nonvolatile RAM for data storage
- 2-wire serial interface
- Programmable square wave output signal
- Automatic power fail detect and switch circuitry
- Consumes less than 500 nA in battery backup mode
- Industrial temperature range -40°C to +85°C (IND)
- Available in 8-pin DIP or SOIC and chip form



N SUFFIX
PLASTIC



D SUFFIX
SOIC

ORDERING INFORMATION

IN1307N Plastic DIP
IL1307D SOIC
IZ1307 Chip

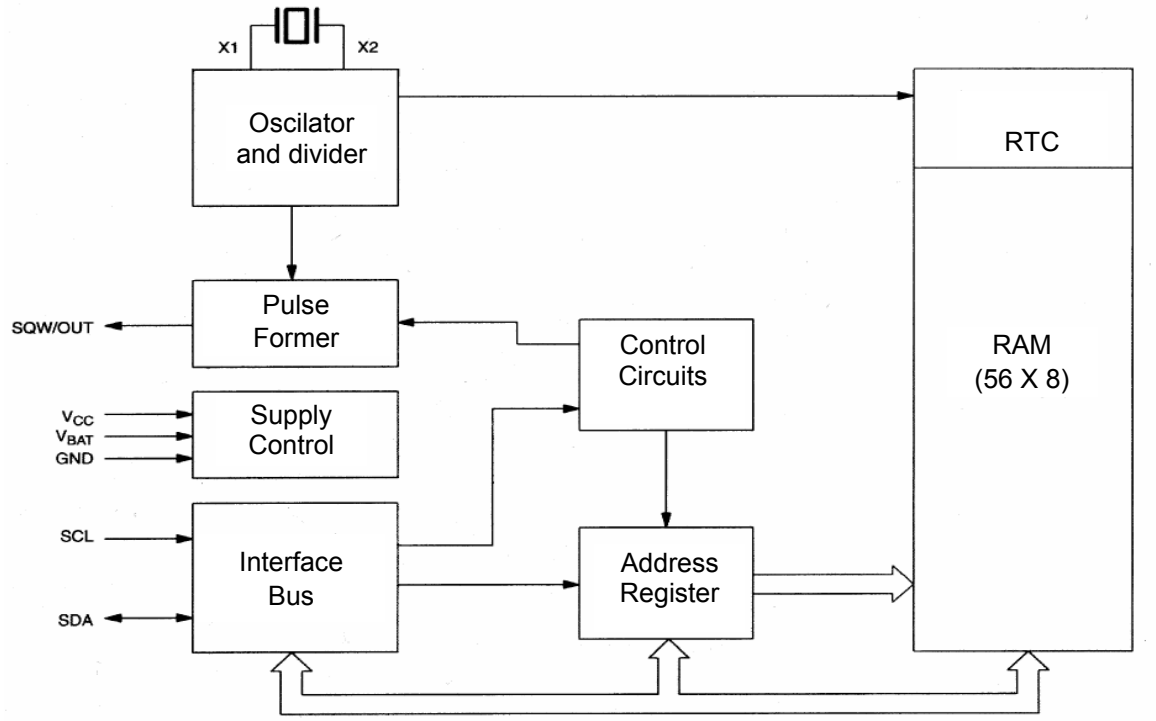


Fig.1 Structural Diagram IN1307

Table 1 Recommended operating mode and maximum ratings

Parameter, unit	Symbol	Norm			
		Recommended mode		Maximum ratings	
		min	max	min	max
Supply voltage, V	V_{CC}	4,5	5,5	-0,5	7,0
Battery voltage, V	V_{BAT}	2,0	3,5	-0,5	7,0
Low level input voltage, V	V_{IL}	-0,3	0,8	-0,5	7,0
High level input voltage, V	V_{IH}	2,2	V_{CC}+ 0,3	-0,5	7,0
Storage temperature, °C	T_S	-	-	-55	+125

All voltages are indicated relative to ground. Under influence of the maximum ratings serviceability of the microcircuits is not guaranteed. After measuring the limit mode serviceability is guaranteed in the limit permissible mode.

Table 2 Electric parameters

(T_A = –40...+ 85°C, V_{CC} = 4,5 – 5,5 V)

Parameter, unit	Symbol	Measurement Mode	Norm	
			min	max
Input leakage current, uA (SCL only)	I_{LI}	–	–	1
In / Out leakage current, uA (SDA and SQW/OUT)	I_{LO}	–	–	1
Low level output voltage, V	V_{OL} [1)]	V_{CC} = 4,5 V	–	0,4
Supply current in the data transfer mode, uA	I_{CCA}	f_{SCL} = 100 kHz	–	1500
Supply current in the static mode, uA	I_{CCS}	V_{CC} = 5 V and SDA, SCL = 5 V	–	200
Supply current in the battery mode (SQW/OUT OFF., 32 kHz – ON), uA	I_{BAT1}	V_{CC} = 0 V, V_{BAT} = 3 V	–	0,5
Supply current in the battery mode (SQW/OUT – ON, 32 kHz – ON), uA	I_{BAT2}	V_{CC} = 0 V, V_{BAT} = 3 V	–	0,8
Low level voltage is determined under the load current of 5 mA; V_{OL} = GND under the capacitance load				

Table 3 Dynamic parameters (T_A = –40...+ 85°C, V_{CC} = 4,5 – 5,5 V)

Parameter, unit	Symbol	Measurement Mode	Norm	
			Min	Max
Clock frequency SCL, kHz	f_{SCL}	–	0	100
Bus free time between the STOP and START conditions , usec	t_{BUF}	–	4,7	–
Hold time (repeated) of START condition, usec	$t_{HD:STA}$ [1)]	–	4,0	–
Low period of SCL clock, μs	t_{LOW}	–	4,7	–
High period of SCL clock, μs	t_{HIGH}	–	4,0	–
Setup time for the repeated START condition, usec	$t_{SU:STA}$	–	4,7	–
Data hold time, usec	$t_{HD:DAT}$ [2)]	–	0	–
Data setup time, nsec	$t_{SU:DAT}$	–	250	–
SDA and SCL signals rise time, nsec	t_R	–	–	1000
SDA and SCL signals fall time, nsec	t_F	–	–	300
Setup time for STOP condition, usec	$t_{SU:STO}$	–	4,7	–
Total capacitance load per each bus line, pF	C_B	–	–	400
IN / OUT capacitance, pF	$C_{I/O}$	–	10	10
Load capacitance of the quartz resonator, pF	C_{LX}	–	12,5	12,5

After this time interval the first time clock signal is formed;

Device should internally ensure the hold time, at least, 300 ns for the signal SDA (relative to V_{IHMIN} of signal SCL) in order to bridge undefined area of the fall signal of SCL.

Maximum value $t_{HD:DAT}$ should be definite in that case, if the device does not increase duration of the low status (t_{LOW}) of signal SCL.

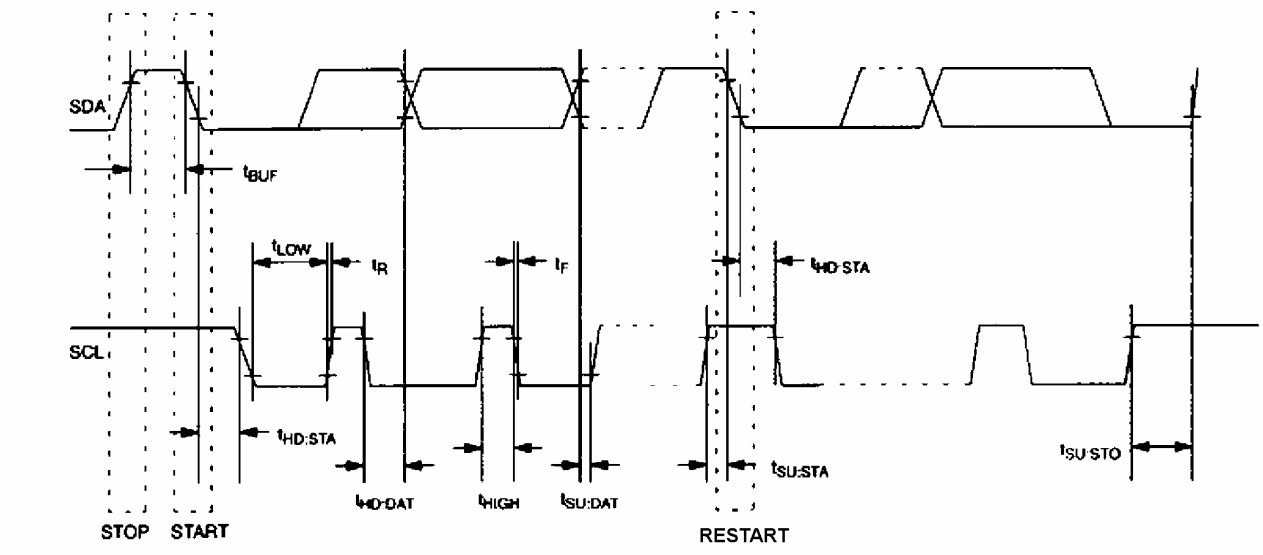


Fig.2 Timing diagramm

Operation description

IN1307 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by a register address. Subsequent registers can be accessed sequentially until a STOP condition is executed. When Vcc falls below 1.25 x V_{BAT} the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When Vcc falls below V_{BAT} the device switches into a low current battery backup mode. Upon power up, the device switches from battery to Vcc when Vcc is greater than V_{BAT}+0,2V and recognizes inputs when V_{CC} is greater than 1.25 x V_{BAT}.

RTC AND RAM ADDRESS MAP

The address map for the RTC and RAM registers of the IN1307 is shown in Fig. 3. The real time clock registers are located in address locations OOh to 07h. The RAM registers are located in address locations 08h to 3Fh. During a muitibyte access, when the address pointer reaches 3Fh, the end of RAM space, it wraps around to location OOh, the beginning of the clock space

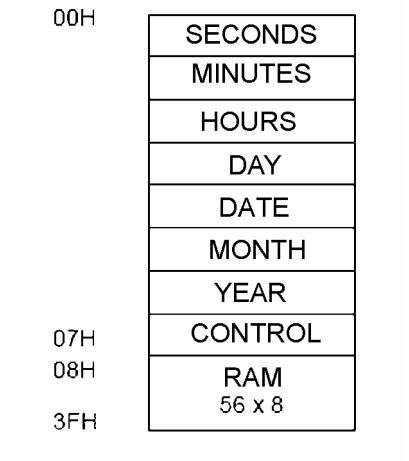


Fig.3 Memory map

CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. The real time clock registers are illustrated in Fig. 4. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the Binary-Coded Decimal (BCD) format. Bit 7 of Register 0 is the Clock Halt (CH) bit. When this bit is set to a one, the oscillator is disabled. When cleared to a zero, the oscillator is enabled.

IN1307 operates in the 12-hour or in the 24-hour format. Bit 6 of the hours register is defined as the 12-or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10 hour bit (20-23 hours).

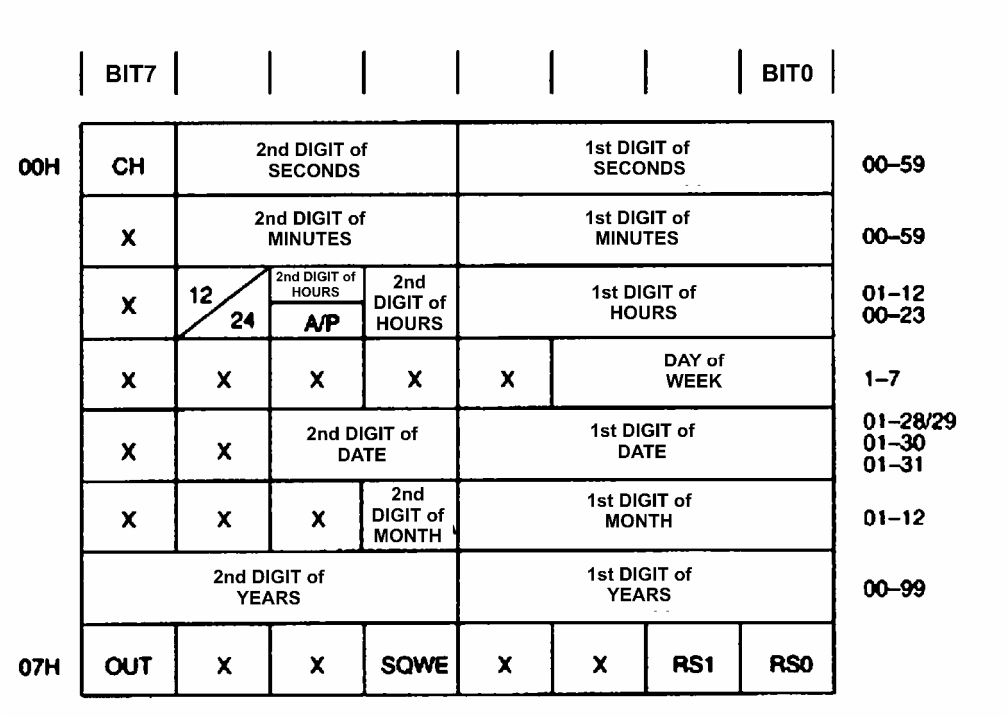


Fig.4 IN1307 timekeeper registers

Control Register

Control register is used for control of pin SQW/OUT.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT	X	X	SQWE	X	X	RS1	RS0

OUT (Output control): This bit controls the output level of the SQW/OUT pin when the square wave output is disabled. If SQWE = 0, the logic level on the SQW/OUT pin is 1 if OUT = 1 and is 0 if OUT = 0.

SQWE (Square wave Enable): This bit when set to a logic 1 will enable the oscillator output. The frequency of the square wave output depends on the value of the RS0 and RS1 bits.

RS (Rate Select): These bits control the frequency of the square wave output when the square wave output has been enabled.

Table 4 Square wave frequencies.

RS1	RS0	Frequency SQW/OUT
0	0	1 Hz
0	1	4,096 kHz
1	0	8,192 kHz
1	1	32,768 кГц

Two-wire Serial Data Bus

IN1307 supports the bi-directional two-wire bus and the protocol of the data exchange. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1307 operates as a slave on the 2-wire bus. Typical configuration of the bus with the two-wire protocol is indicated in Fig.5

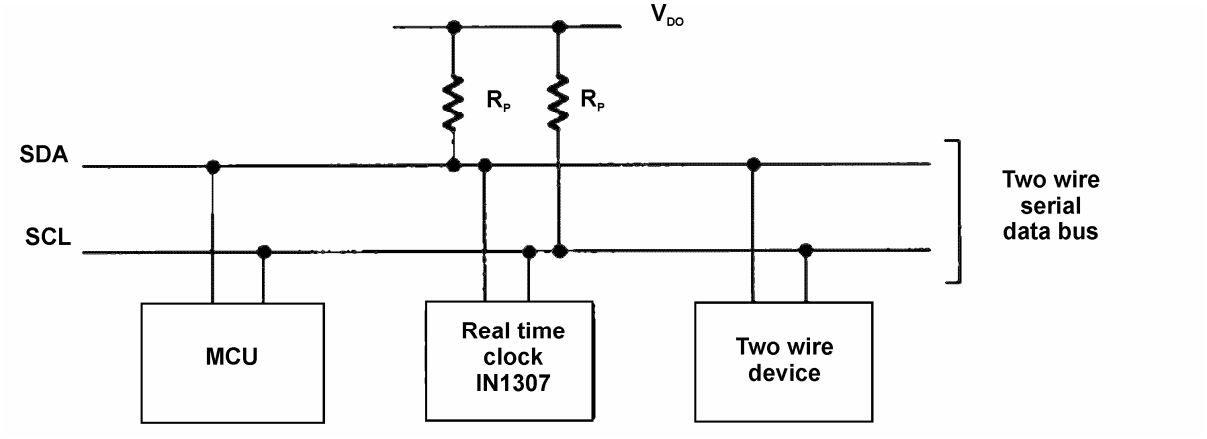


Fig.5 Typical 2-wire bus configuration

- Data transfer can be initiated only when the bus is not busy. In the process of the data transfer the data line should remain stable, while the clock line is HIGH. All changes in the data line while the clock line is high will be interpreted as control signals.

In compliance with this the following conditions are determined:

Bus not busy: both the data and clock line are HIGH.

Data transfer start: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

Data transfer stop: A change in the state of the data line from low to high, while the clock line is high defines the STOP condition.

Data valid: Data line status complies with the valid data, when after the status START the data line is stable during the HIGH status of the cycle signal. Data on the line should be altered at the time of the LOW status of the cycle signal. One cycle pulse per one data bit.

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the

acknowledge related clock pulse. Of course, setup and hold times must be taken into account. When receiving data from a slave a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

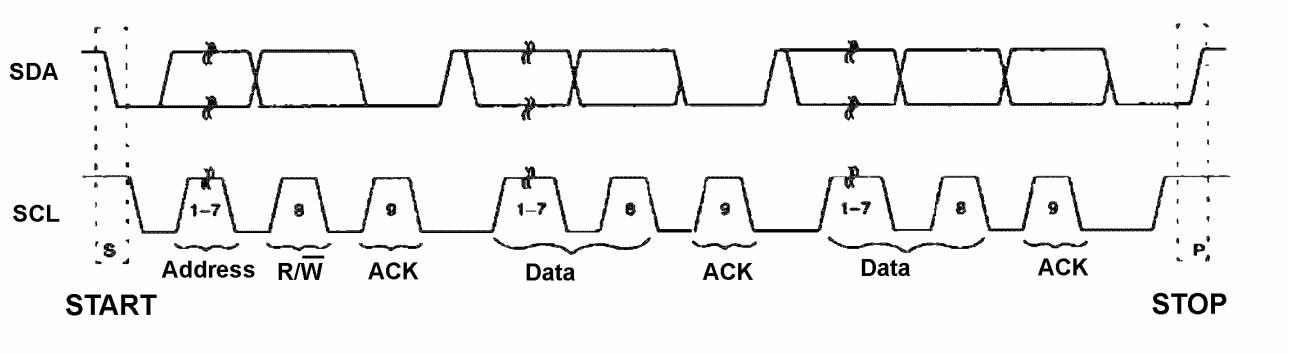


Fig.6 Data Transfer by the Serial Two-wire Bus

Depending on the status of bit $R/\overline{W}$, there are possible two types of transfer:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transfered with the most significant bit (MSB) first.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transfered with the most significant bit (MSB) first.

IN1307 can operate in the two following modes:

1. Slave receiver mode (write mode): Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (See Fig. 7). The address byte is the first byte received after the start condition is generated by the master. The address byte contains the 7 bit IN1307 address, which is 1101000, followed by the direction bit (R/W\) which for a write is a 0. After receiving and decoding the address byte the DS1307 outputs an acknowledge on the SDA line. After the IN1307 acknowledges the slave address + write bit, the master transmits a register address to the IN1307 This will set the register pointer on the IN1307. The master will then begin transmitting each byte of data with the IN1307 acknowledging each byte received. The master will generate a stop condition to terminate the data write.

2. Slave transmitter mode (read mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1307 while the serial clock is input on SCL. START and STOP conditions are recognized as the

beginning and end of a serial transfer (See Fig. 8). The address byte is the first byte received after the start condition is generated by the master. The address byte contains the 7 bit IN1307 address, which is 1101000, followed by the direction bit (RAM) which for a read is a 1. After receiving and decoding the address byte the IN1307 inputs an acknowledge on the SDA line. The IN1307 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The IN1307 must receive a Not Acknowledge to end a read

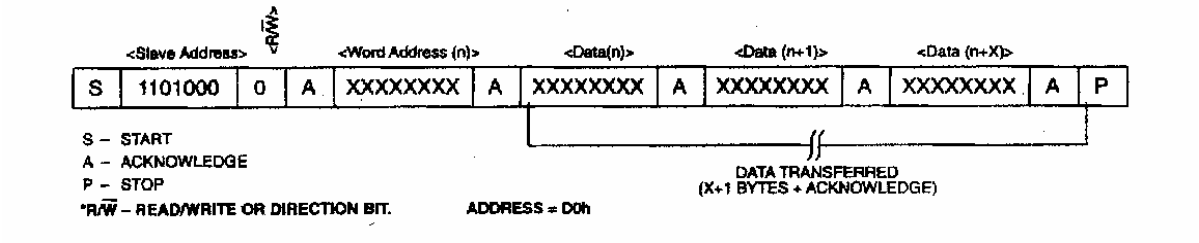


Fig.7 Data write – mode («slave» receiver)

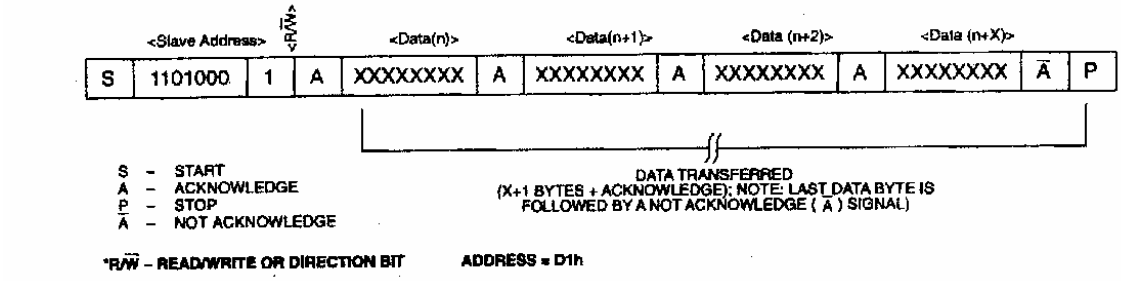


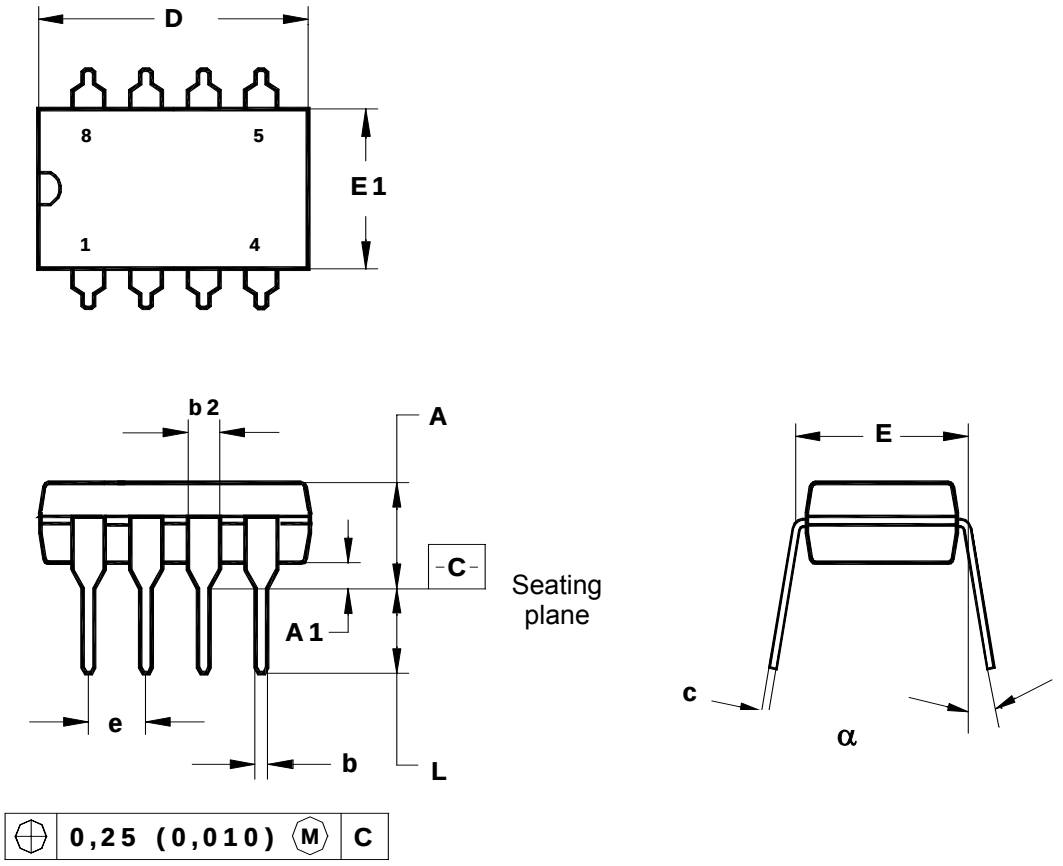
Fig.8 Data read– mode («slave» transmitter)

Table 5 Pin description table

Contact pad number	Pin number	Identification	Type	Pin Designation
1	1	X1	In	Pin for connection of the quartz resonator
2	2	X2	In	Pin for connection of the quartz resonator
3	3	VBAT	In	Pin for battery
4	4	GND	In	Ground pin
5	5	SDA	Bi	Input / output of serial data
6	6	SCL	In	Input of the consecutive cycle signal
7	7	SQW/OUT	Out	Output of rectangular signal
8	8	VCC	In	Power supply pin

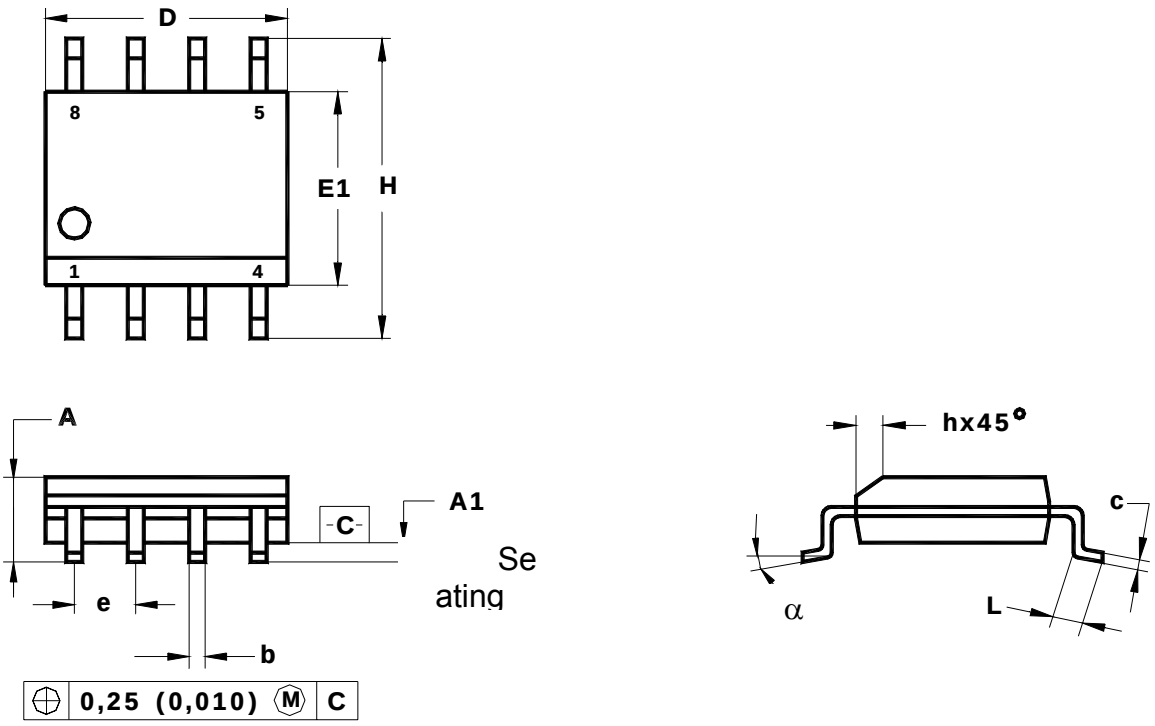
Package Overall Dimensions

N SUFFIX PLASTIC DIP (MS-001BA)

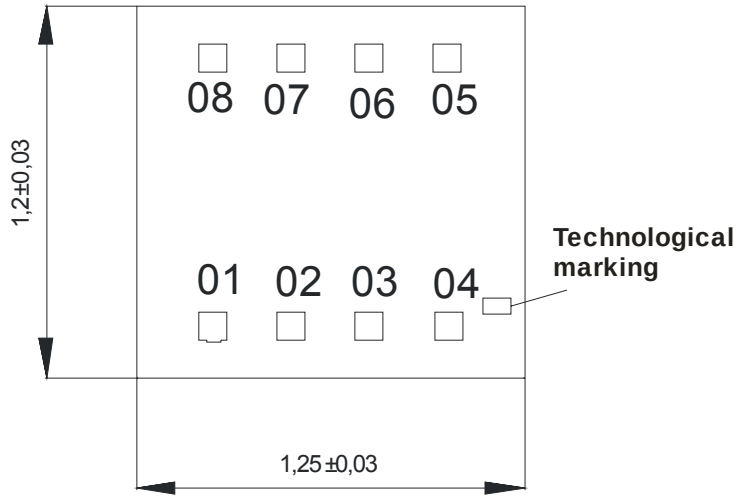


	D	E1	A	b	b2	e	α	L	E	c	A1
mm											
min	9.02	6.07	—	0.36	1.14		0°	2.93	7.62	0.20	0.38
max	10.16	7.11	5.33	0.56	1.78	2.54	15°	3.81	8.26	0.36	—
inches											
min	0.355	0.240	—	0.014	0.045		0°	0.115	0.300	0.008	0.015
max	0.400	0.280	0.210	0.022	0.070	0.1	15°	0.150	0.325	0.014	—

D SUFFIX PLASTIC SOP
(MS-012AA)



	D	E1	H	b	e	α	A	A1	c	L	h
mm											
min	4.80	3.80	5.80	0.33		0°	1.35	0.10	0.19	0.41	0.25
max	5.00	4.00	6.20	0.51	1.27	8°	1.75	0.25	0.25	1.27	0.50
inches											
min	0.1890	0.1497	0.2284	0.013		0°	0.0532	0.0040	0.0075	0.016	0.0099
max	0.1968	0.1574	0.2440	0.020	0.100	8°	0.0688	0.0090	0.0098	0.050	0.0196



Technological mark “1307” has coordinates (mm): left bottom corner x = 1.590, y = 0.150

Die thickness 0,46±0,02 mm.

Таблица 1 **Contact pad location table**

Pad number	Coordinates (Left bottom corner), mm	
	X	Y
01	0.271	0.144
02	1.010	0.144
03	1.435	0.144
04	1.832	0.144
05	1.857	1.547
06	1.379	1.547
07	1.046	1.547
08	0.273	1.547
Note: Contact pad coordinates and dimensions 0.100 x 0.100 mm are indicated under ”Passivation” layer		