CSE/EEE 120

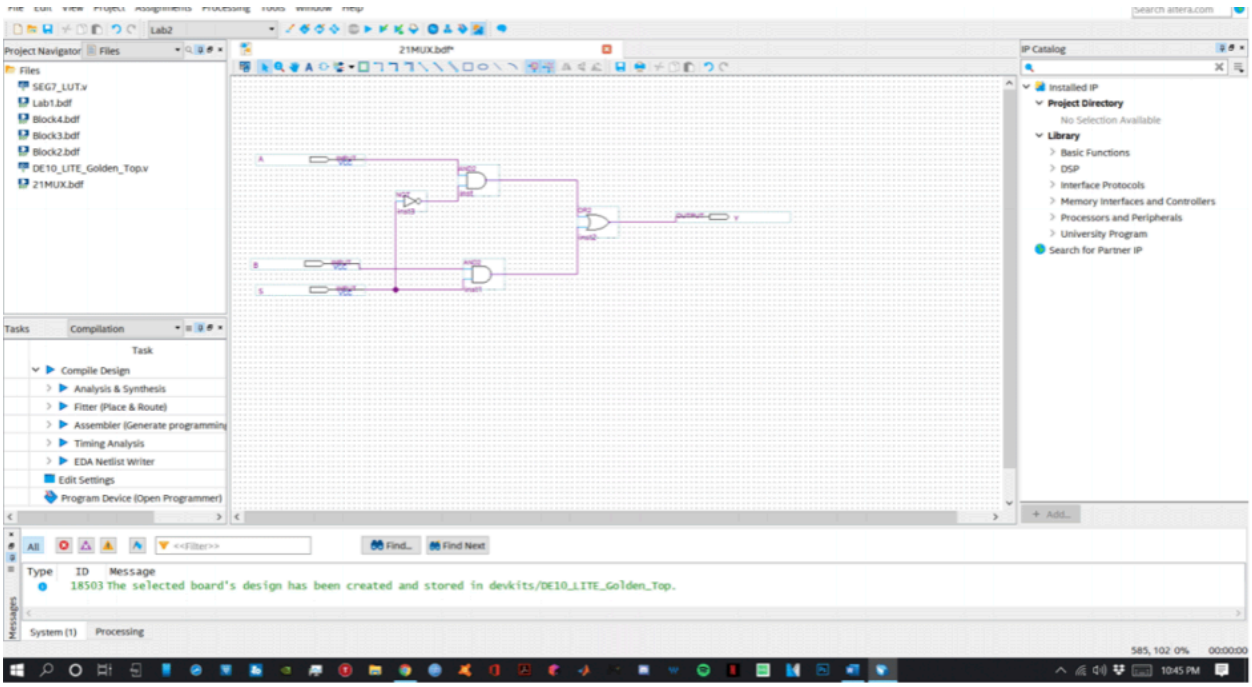
Lab 2 Answer Sheet
Multiplexers and Decoders

Name:Vishwas Mani Instructor/Time:_Matar, 3:00

Date: October 21, 2019

Task 2-1: Build and Test a 1-Bit 2:1 Multiplexer

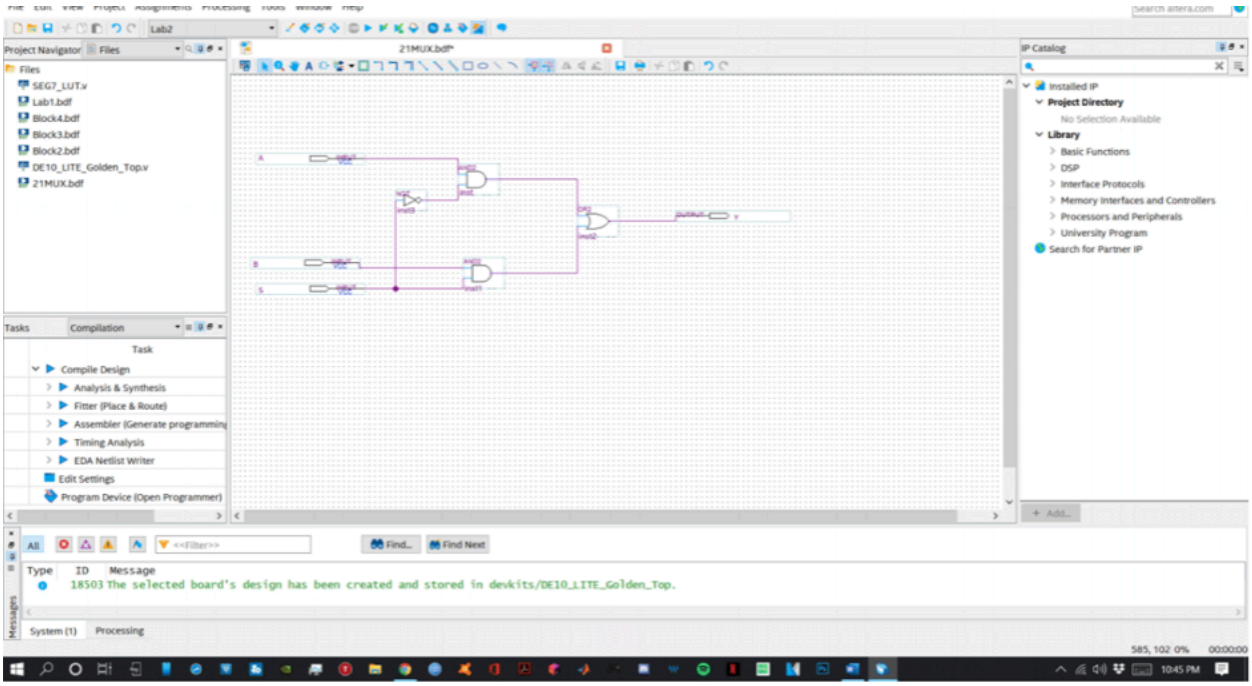
Include a picture of your Quartus circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

The single biggest issue I faced when designing this circuit

Include a picture of your Quartus simulation (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

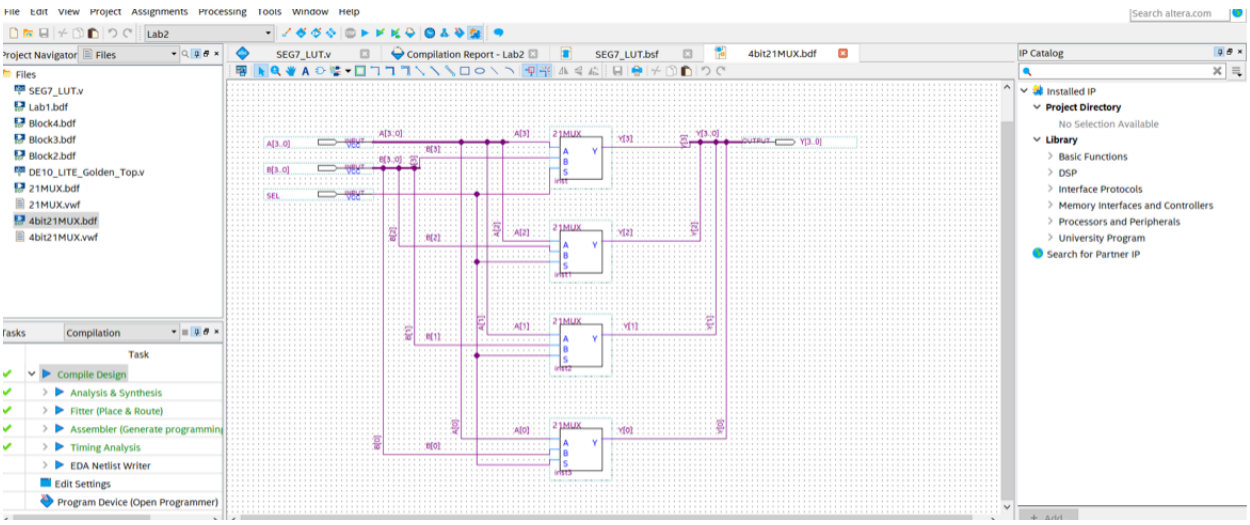
The circuit behaved as expected, and I had no bugs that I ran into.

Please comment on the single biggest issue you were facing when simulating the circuit.

The biggest issue I faced was figuring out what pins to use

Task 2-2: Build a 4-Bit 2:1 Multiplexer

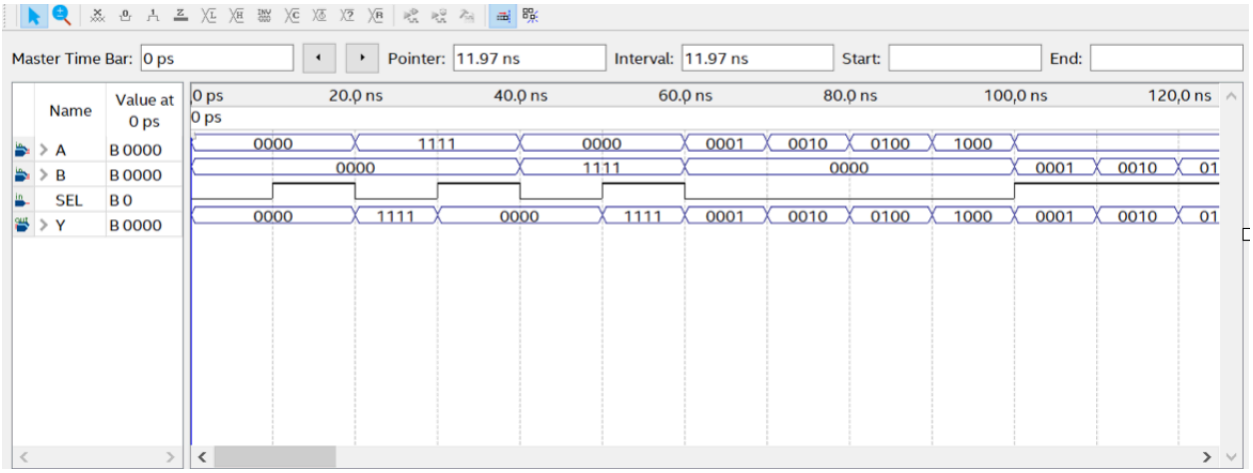
Include a picture of your Quartus circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I faced was connecting all the wires to the appropriate places

Include a picture of your Quartus simulation (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

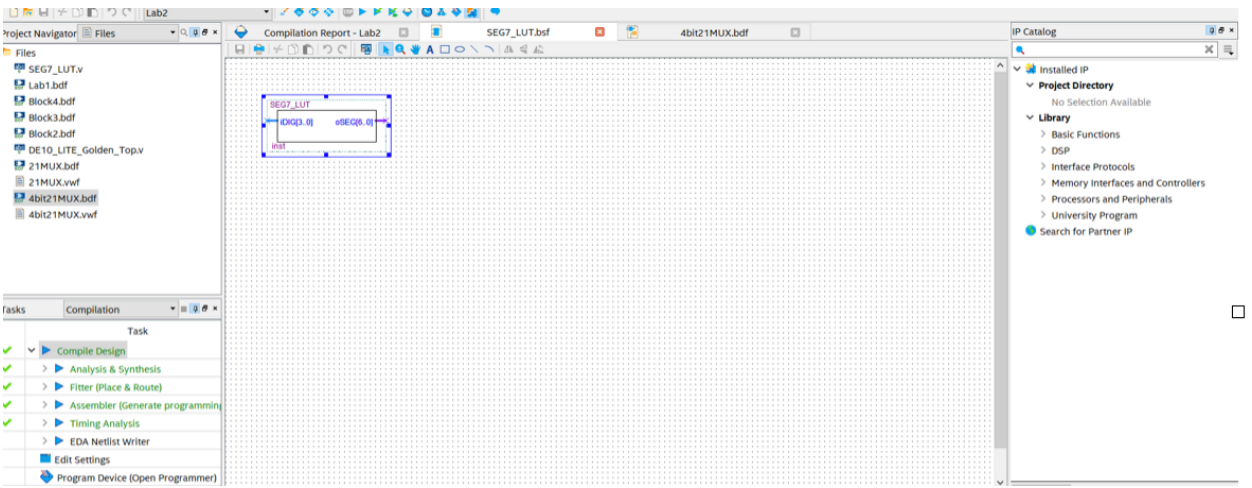
It behaved as expected

Please comment on the single biggest issue you were facing when simulating the circuit.

Finding out what test calls to use

Task 2-3: Create a 7-Segment Decoder Symbol File based on Verilog code

Include a picture of your Quartus Symbol File here:

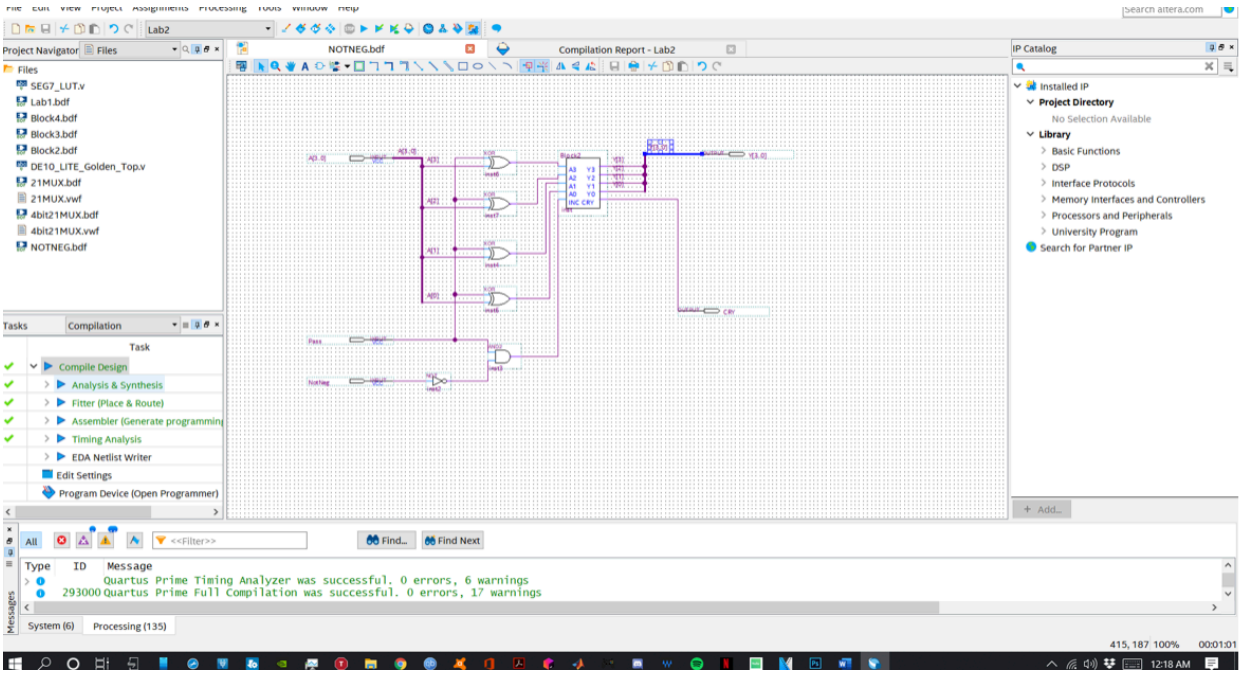


Please comment on the single biggest issue you were facing when creating the Symbol File.

Figuring out the procedures as to how to code this part

Task 2-4: Build the NOT/NEG Circuit

Include a picture of your Quartus circuit here:

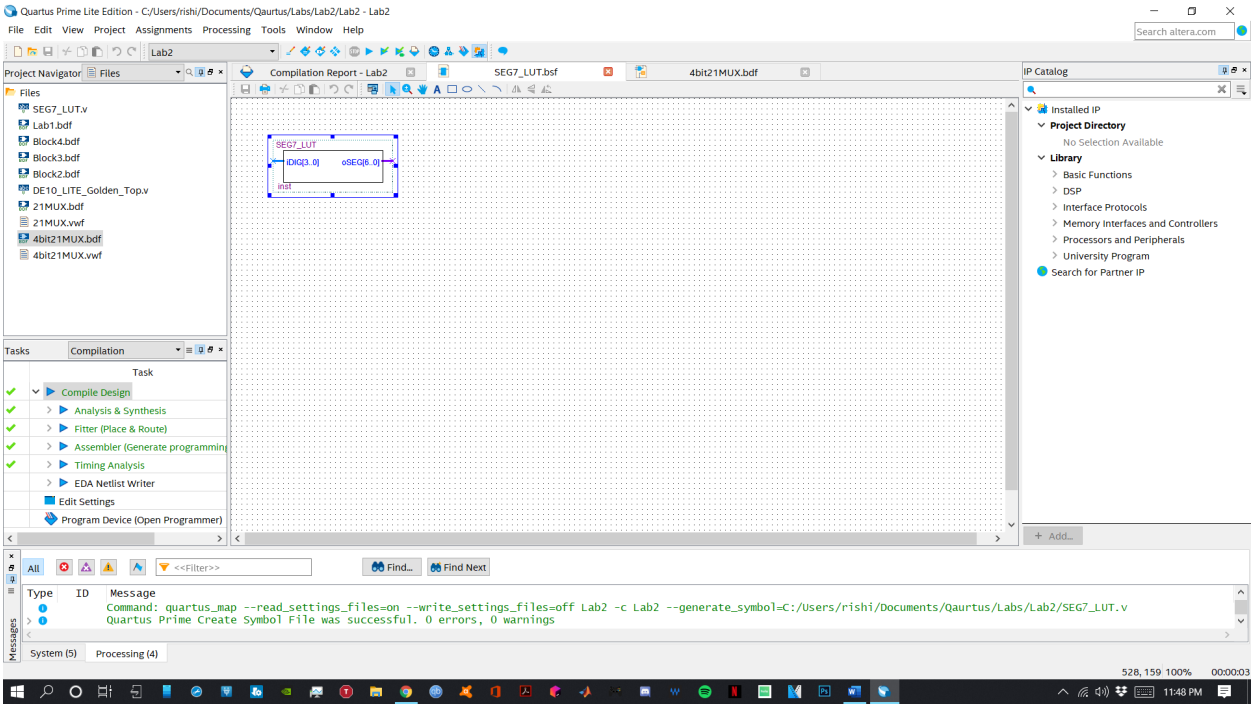


Please comment on the single biggest issue you were facing when designing the circuit.

Wiring everything appropriately

Task 2-5: Build the AND/ADD Circuit

Include a picture of your Quartus circuit here:

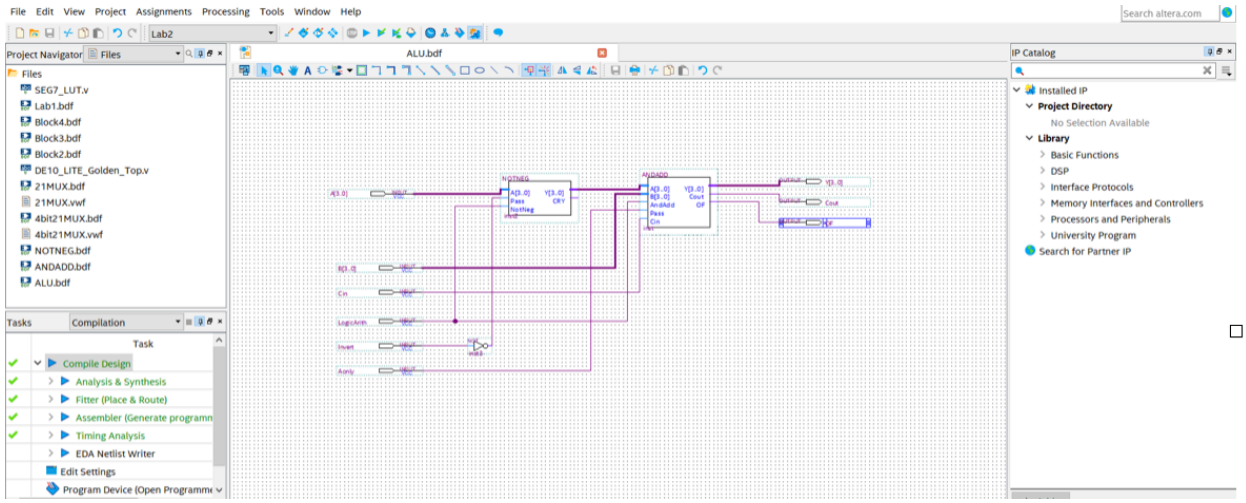


Please comment on the single biggest issue you were facing when designing the circuit

The biggest issue I was having was the wire rerouting

Task 2-6: Build and Test the ALU Circuit

Include a picture of your Quartus circuit here:

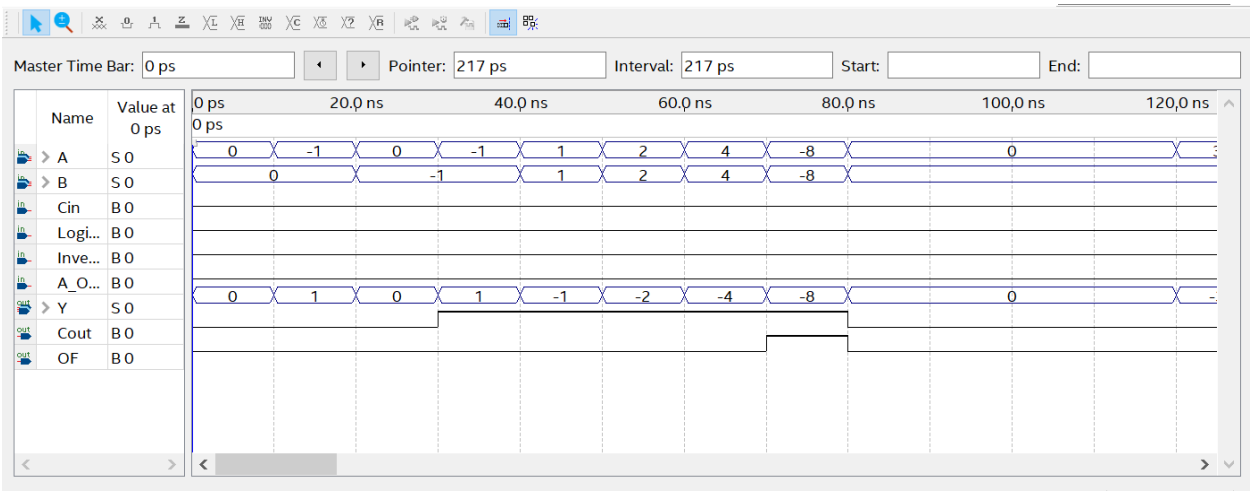


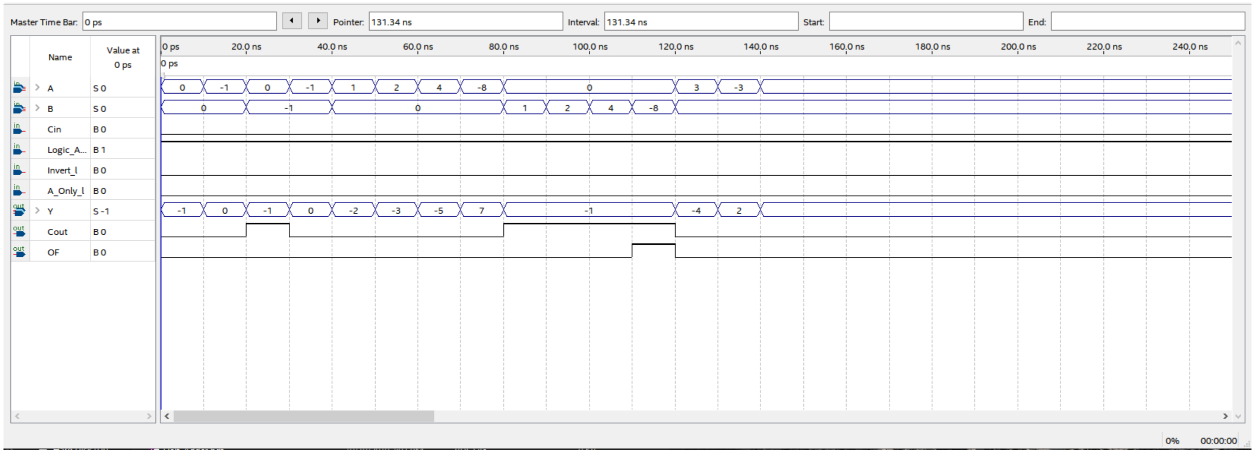
Please comment on the single biggest issue you were facing when designing the circuit.

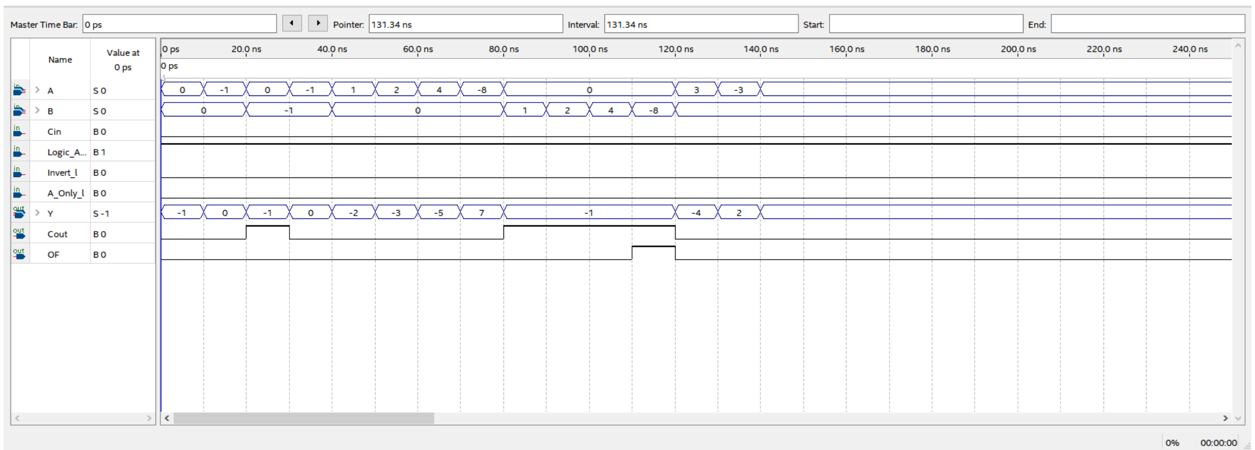
Please complete the ALU function definition table shown below:

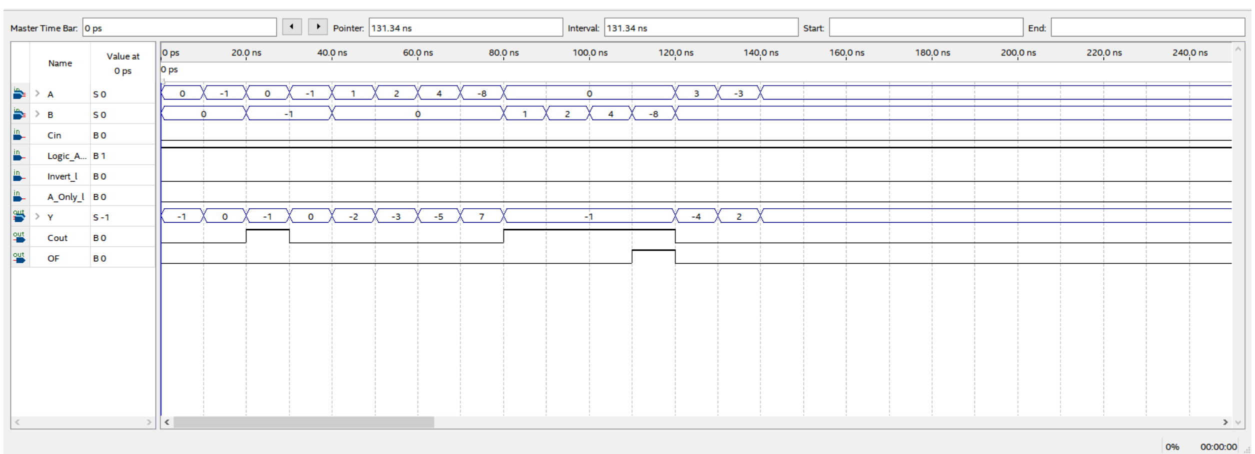
Logic_Arith_l	Invert_l	A_Only_l	Function
0	0	0	Arthimetic Sum, B-A
0	0	1	Pass through
0	1	0	(a+b) 1's compliment
0	1	1	Arithmetic Sum, A+B
1	0	0	A and B
1	0	1	Pass A Through
1	1	0	(a+b)
1	1	1	As 1s Compliment

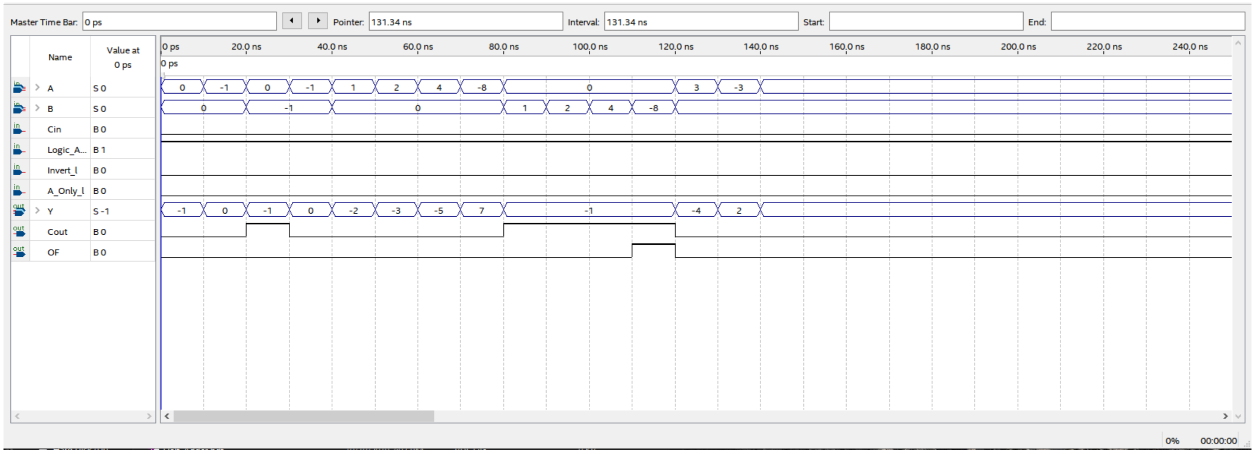
Include pictures of your Quartus simulations (timing diagrams) here:

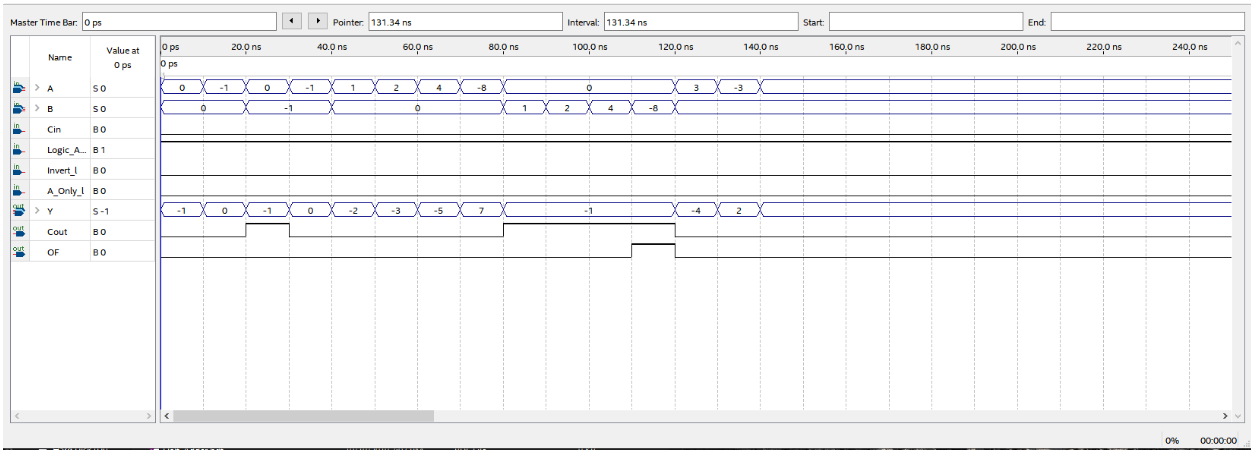


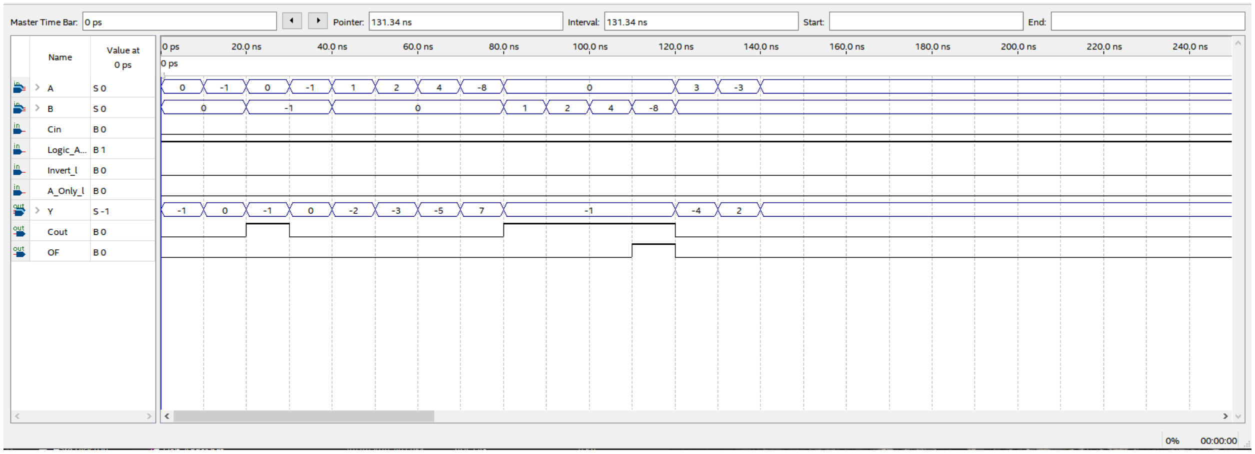

Master Time Bar: 0 ps
Pointer: 131.34 ns
Interval: 131.34 ns
Start:
End:
Name
Value at 0 ps
0 ps 20.0 ns 40.0 ns 60.0 ns 80.0 ns 100.0 ns 120.0 ns 140.0 ns 160.0 ns 180.0 ns 200.0 ns 220.0 ns 240.0 ns
A S 0
B S 0
Cin B 0
Logic_A... B 1
Invert_I B 0
A_Only_I B 0
Y S -1
Cout B 0
OF B 0

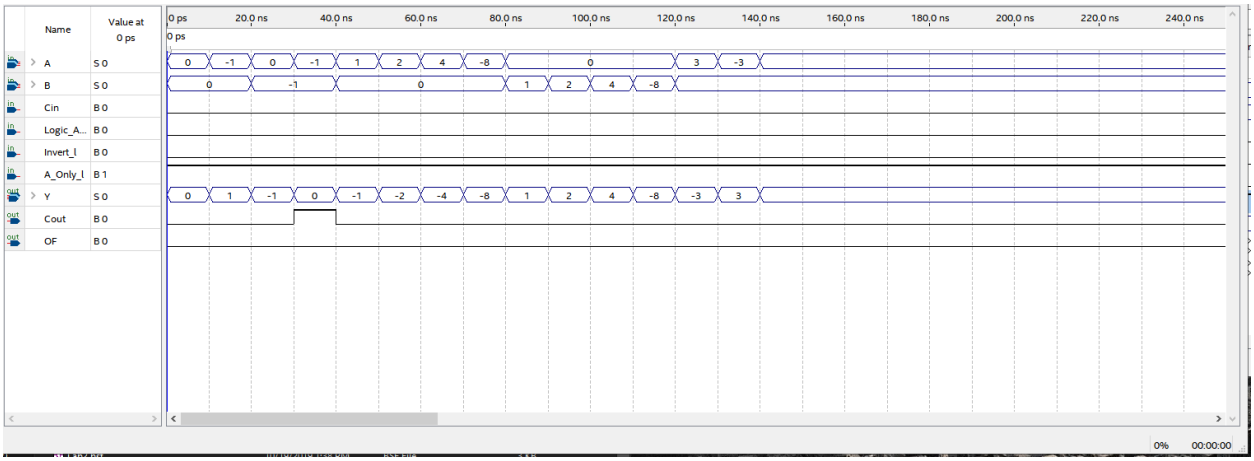

Master Time Bar: 0 ps
Pointer: 131.34 ns
Interval: 131.34 ns
Start:
End:
Name
Value at 0 ps
0 ps 20.0 ns 40.0 ns 60.0 ns 80.0 ns 100.0 ns 120.0 ns 140.0 ns 160.0 ns 180.0 ns 200.0 ns 220.0 ns 240.0 ns
A S 0
B S 0
Cin B 0
Logic_A... B 1
Invert_I B 0
A_Only_I B 0
Y S -1
Cout B 0
OF B 0


Master Time Bar: 0 ps
Pointer: 131.34 ns
Interval: 131.34 ns
Start:
End:
Name
Value at 0 ps
0 ps 20.0 ns 40.0 ns 60.0 ns 80.0 ns 100.0 ns 120.0 ns 140.0 ns 160.0 ns 180.0 ns 200.0 ns 220.0 ns 240.0 ns
A S 0
B S 0
Cin B 0
Logic_A... B 1
Invert_I B 0
A_Only_I B 0
Y S -1
Cout B 0
OF B 0


Master Time Bar: 0 ps
Pointer: 131.34 ns
Interval: 131.34 ns
Start:
End:
Name
Value at 0 ps
0 ps 20.0 ns 40.0 ns 60.0 ns 80.0 ns 100.0 ns 120.0 ns 140.0 ns 160.0 ns 180.0 ns 200.0 ns 220.0 ns 240.0 ns
A S 0 | 0 -1 0 -1 1 2 4 -8 0 3 -3
B S 0 | 0 -1 0 1 2 4 -8
Cin B 0
Logic_A... B 1
Invert_I B 0
A_Only_I B 0
Y S -1 | -1 0 -1 0 -2 -3 -5 7 -1 -4 2
Cout B 0
OF B 0
0% 00:00:00


Master Time Bar: 0 ps
Pointer: 131.34 ns
Interval: 131.34 ns
Start:
End:
Name
Value at 0 ps
0 ps 20.0 ns 40.0 ns 60.0 ns 80.0 ns 100.0 ns 120.0 ns 140.0 ns 160.0 ns 180.0 ns 200.0 ns 220.0 ns 240.0 ns
A S 0 | 0 -1 0 -1 1 2 4 -8 0 3 -3
B S 0 | 0 -1 0 1 2 4 -8
Cin B 0
Logic_A... B 1
Invert_I B 0
A_Only_I B 0
Y S -1 | -1 0 -1 0 -2 -3 -5 7 -1 -4 2
Cout B 0
OF B 0
0% 00:00:00


Master Time Bar: 0 ps
Pointer: 131.34 ns
Interval: 131.34 ns
Start:
End:
Name
Value at 0 ps
0 ps 20.0 ns 40.0 ns 60.0 ns 80.0 ns 100.0 ns 120.0 ns 140.0 ns 160.0 ns 180.0 ns 200.0 ns 220.0 ns 240.0 ns
A S 0 | 0 -1 0 -1 1 2 4 -8 0 3 -3
B S 0 | 0 -1 0 1 2 4 -8
Cin B 0
Logic_A... B 1
Invert_I B 0
A_Only_I B 0
Y S -1 | -1 0 -1 0 -2 -3 -5 7 -1 -4 2
Cout B 0
OF B 0
0% 00:00:00



Did the circuit behave as expected? If no, what was wrong?

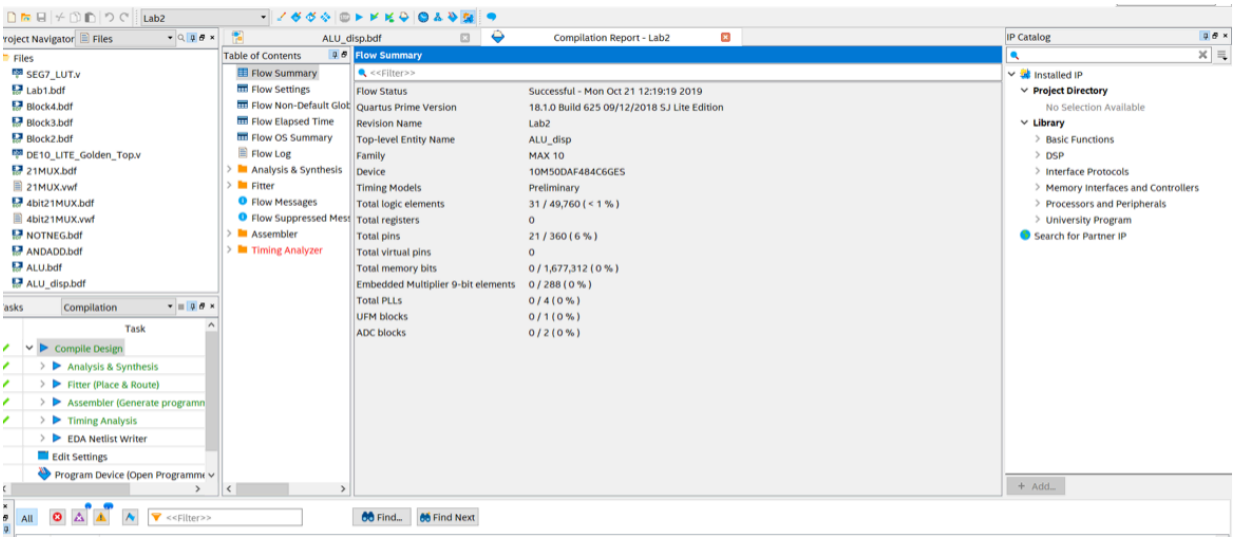
Yes it did

Please comment on the single biggest issue you were facing when simulating the circuit.

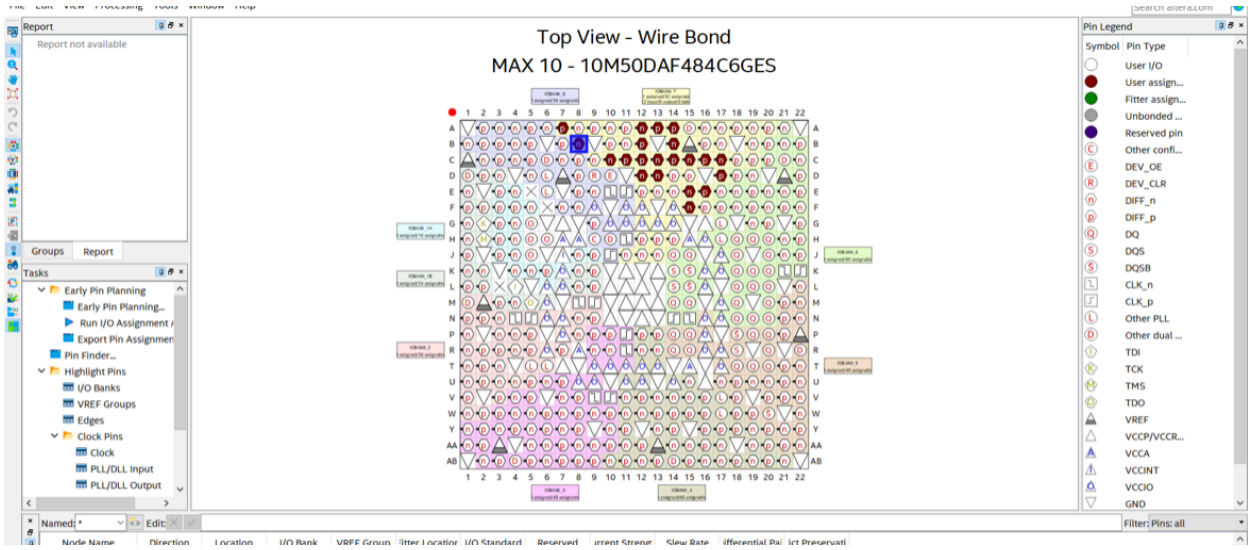
Figuring out the highs and lows

Task 2-7: Test the 4-Bit ALU Using a 7-Segment Display on the Hardware Board

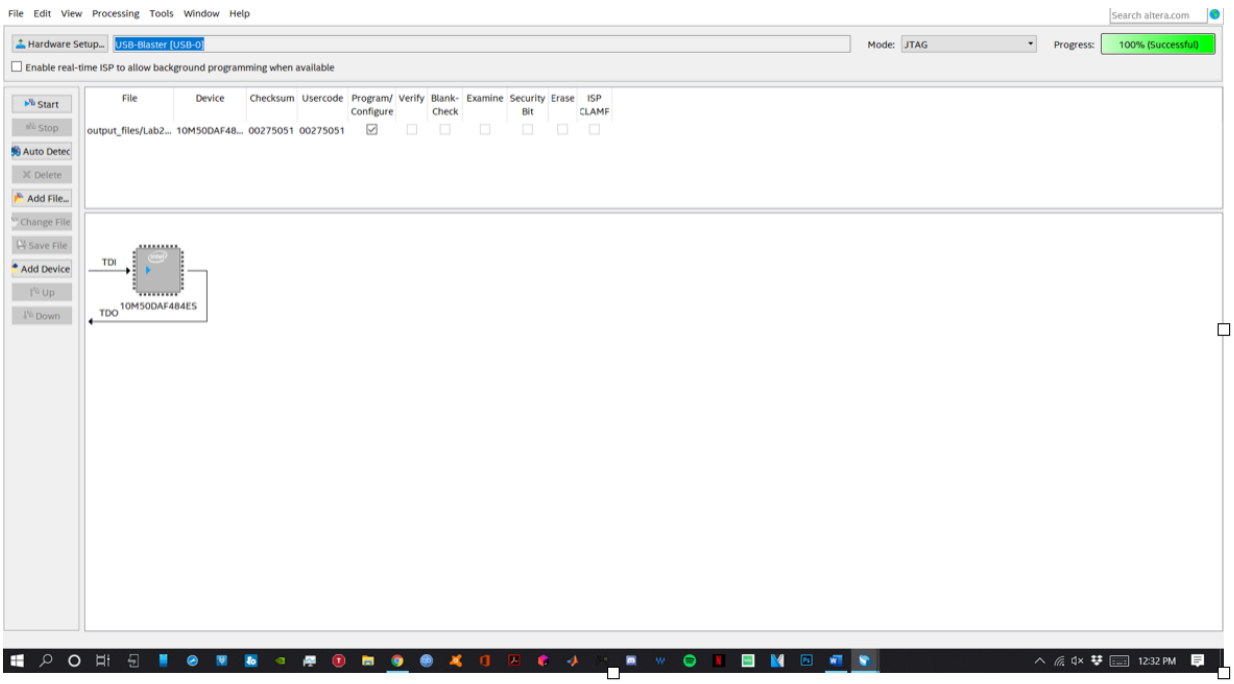
Include a picture of your Quartus System Message Window here:



Include a picture of your Pin Planner assignment window here:



Include a picture of your Programmer Window here:



Which ALU functions did you test?

Tested all the cases above

Was the test on the FPGA board successful?

Yes it was

What was the biggest issue you were facing when you prepared the design for hardware upload?

Fixing the USB Blaster

Please have the TA record your score for upload on Canvas !

LAB 2: LAB REPORT GRADE SHEET

Nam _____

Instructor Assessment

Grading Criteria	Max Points	Points Lost
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task 2-1: Build and Test a 1-bit 2:1 Multiplexer	5	
Task 2-2: Build a 4-Bit 2:1 Multiplexer	5	
Task 2-3: Create a 7-Segment Decoder Symbol File based on Verilog code (ROM-based Decoder)	5	
Task 2-4: Build the NOT/NEG Circuit	5	
Task 2-5: Build the AND/ADD Circuit	10	
Task 2-6: Build and Test the ALU Circuit	10	
Task 2-7: Test the 4-Bit ALU Using a 7-Segment Display on the Hardware Board	10	
Lab Score (50 points total)	**Points Lost**	
	Late Lab	
	Lab Score	