CSE/EEE 120

Lab 1 Answer Sheet

Half Adder, Full Adder, 4-bit Incrementer and Adder

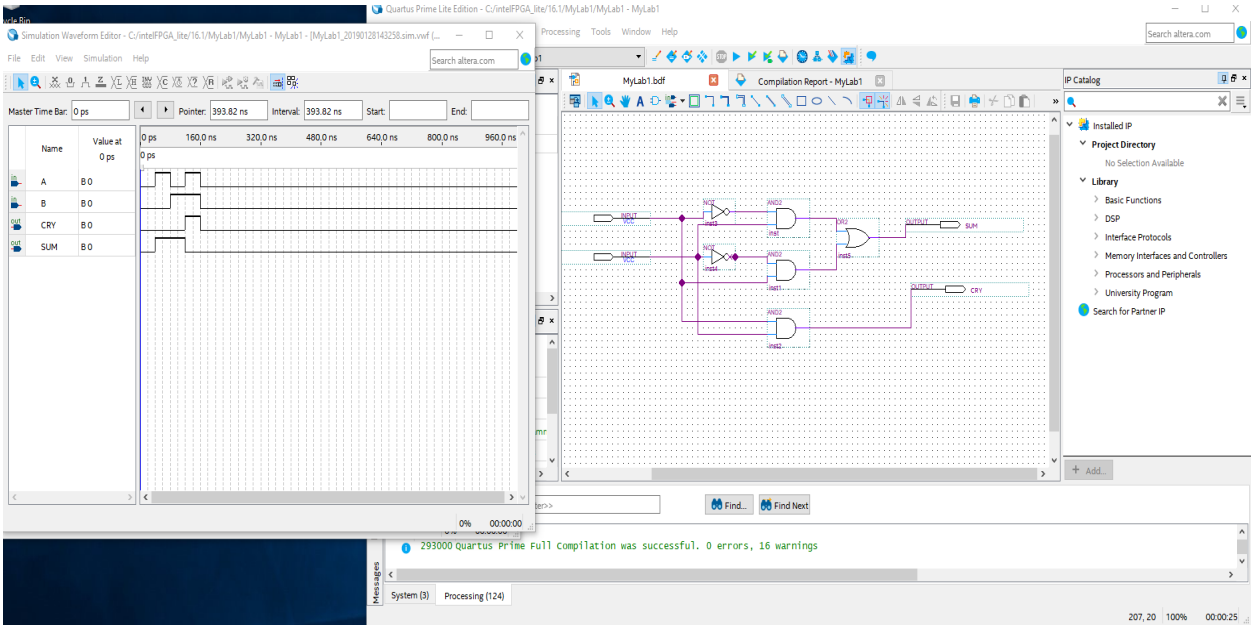
Name:Vishwas Mani

Instructor/Time: Matar/ 3:00 - 4:20

Date: 9/23/19

Task 1-1: Build and Test the 1-Bit Half-Adder

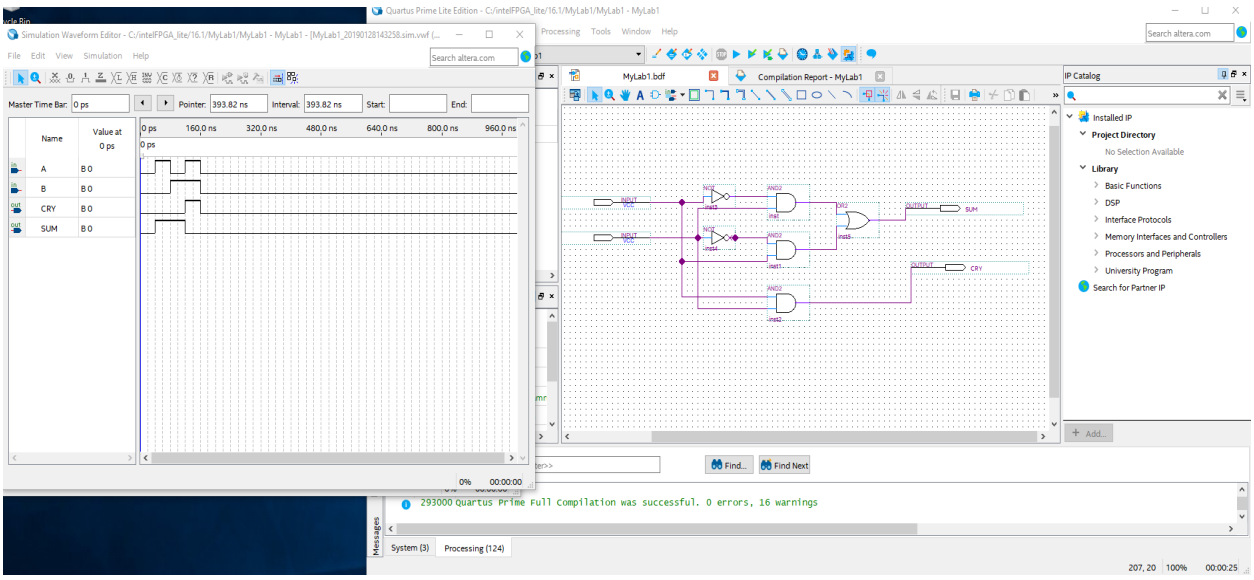
Include a picture of your Quartus circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

The single biggest issue I faced when designing the circuit was to make sure that all points were connected and sometimes the computer not recognize all the points when the program is not entirely compiled

Include a picture of your Quarus simulation (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

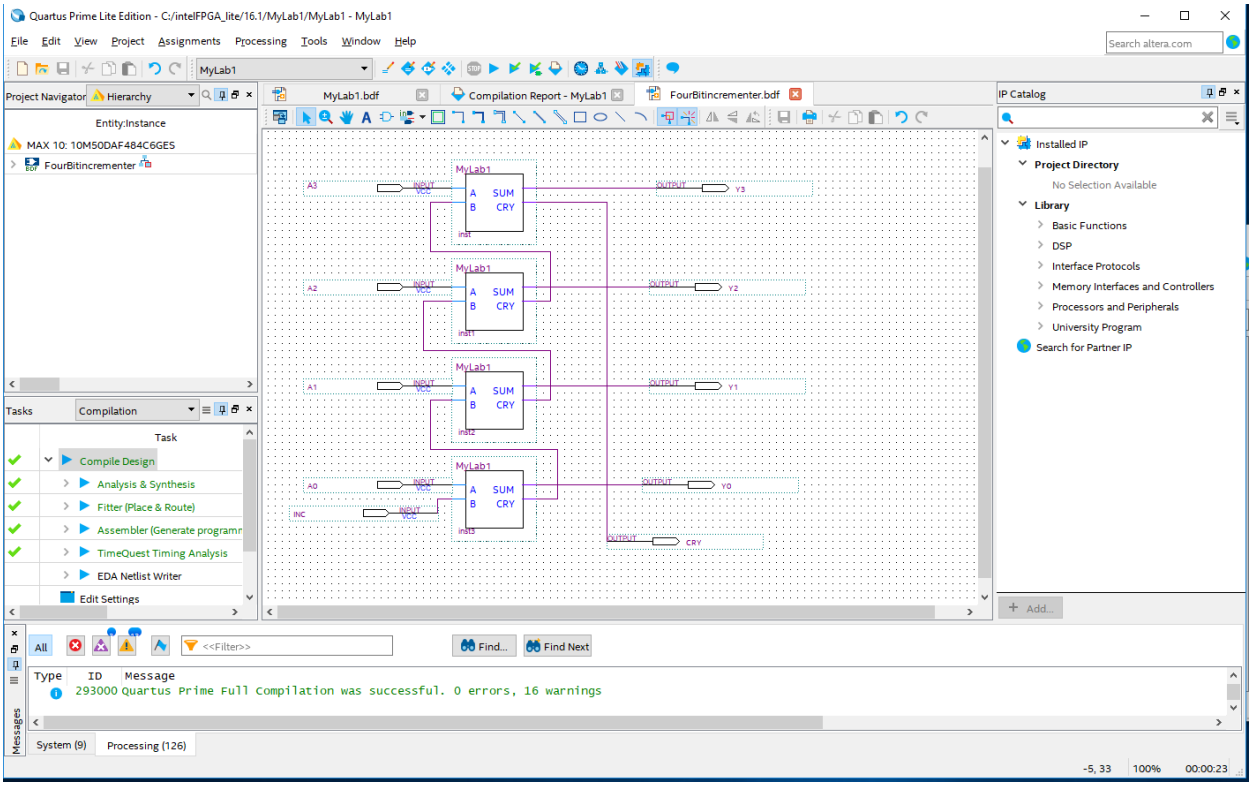
Yes the circuit behaved as we expected as we were expecting it to behave as a 4 bit ladder and it ended up fulfilling those requirements

Please comment on the single biggest issue you were facing when simulating the circuit.

Making sure we had different inputs to check if half adder worked properly

Task 1-2: Build and Test a 4-Bit Increment Circuit

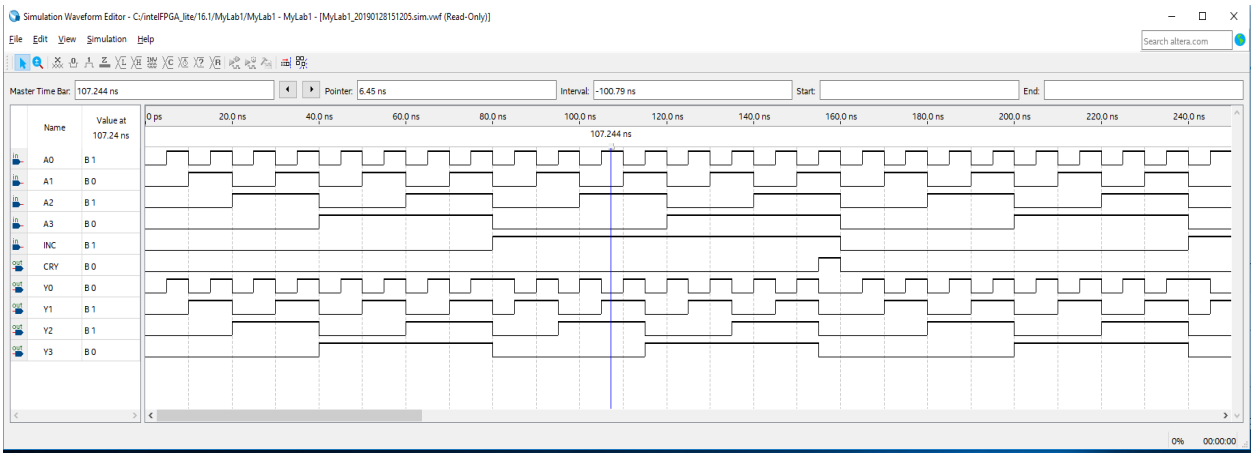
Include a picture of your Quartus circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

Making sure that the connection was present and making sure the “x” doesn’t show up

Include a picture of your Quartus simulation (timing diagram) here:



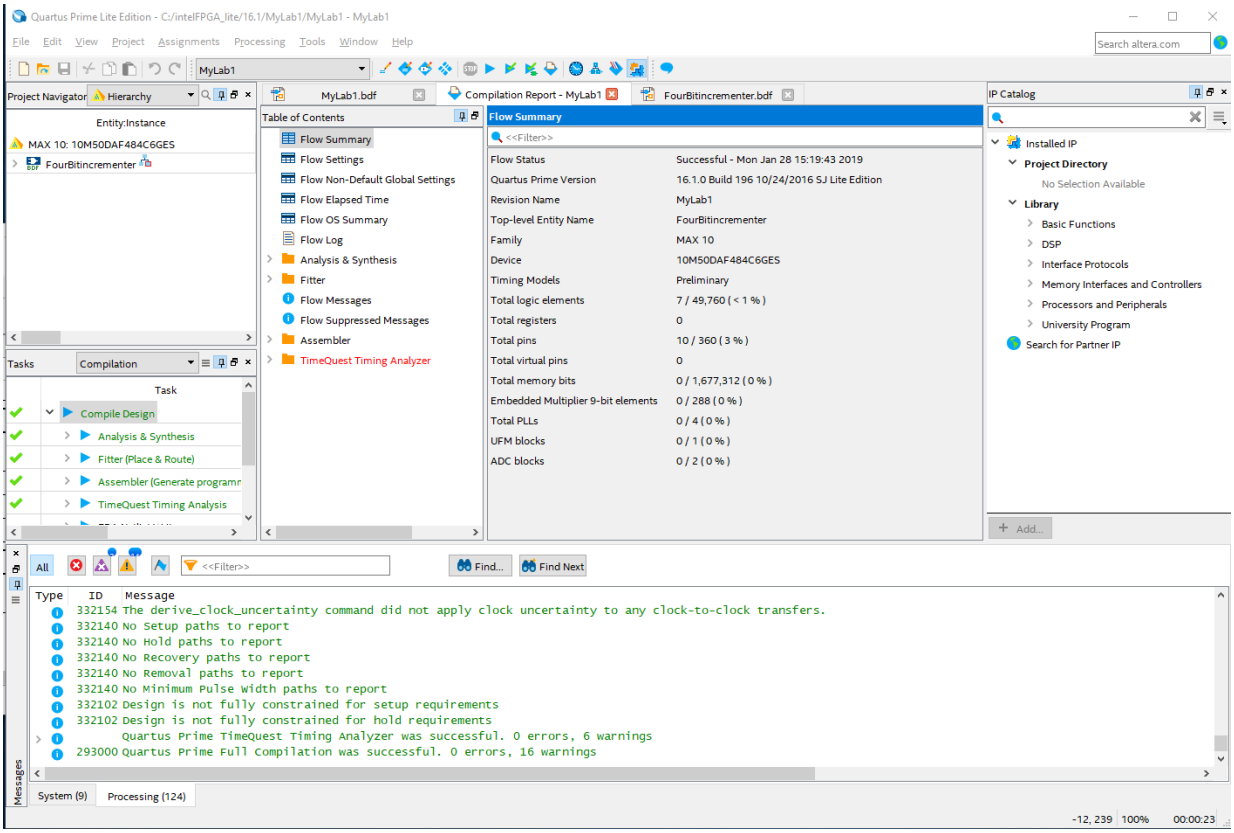
Did you test all input conditions? Were the results as you expected them to be? If you performed your own test sequence, which tests did you perform and why? The following table is an example of how to describe your test sequence:

Test stimulus	**Test motivation**	**Pass/Fail**
All inputs 0	Check for stuck-at-1 faults	Pass
All inputs 1	Check for correct CRY	Pass
A0 is 1 the rest are 0	Check for bit order error	Pass
A3 is 1 the rest are 0	Check for bit order error	Pass
A2 is 1 the rest are 0	Check for bit order error	Pass
A1 is 1 the rest are 0	Check for bit order error	Pass
A0 &A2 are 1 the rest are 0	Check for stuck at-0 faults	Pass

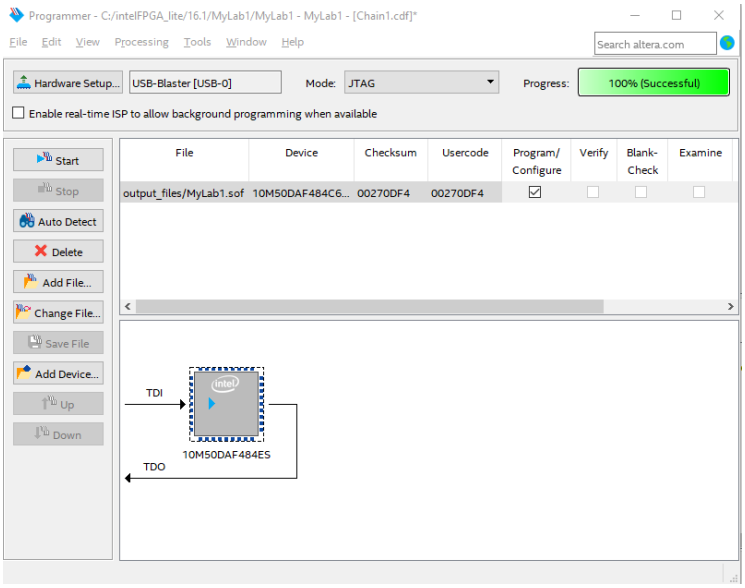
Please comment on the single biggest issue you were facing when simulating the circuit.

Task 1-3: Test the 4-bit Increment Circuit using LEDs on Hardware

Include a picture of your Quartus System Message Window here:



Include a picture of your Programmer Window here:



Was the test on the FPGA board successful?

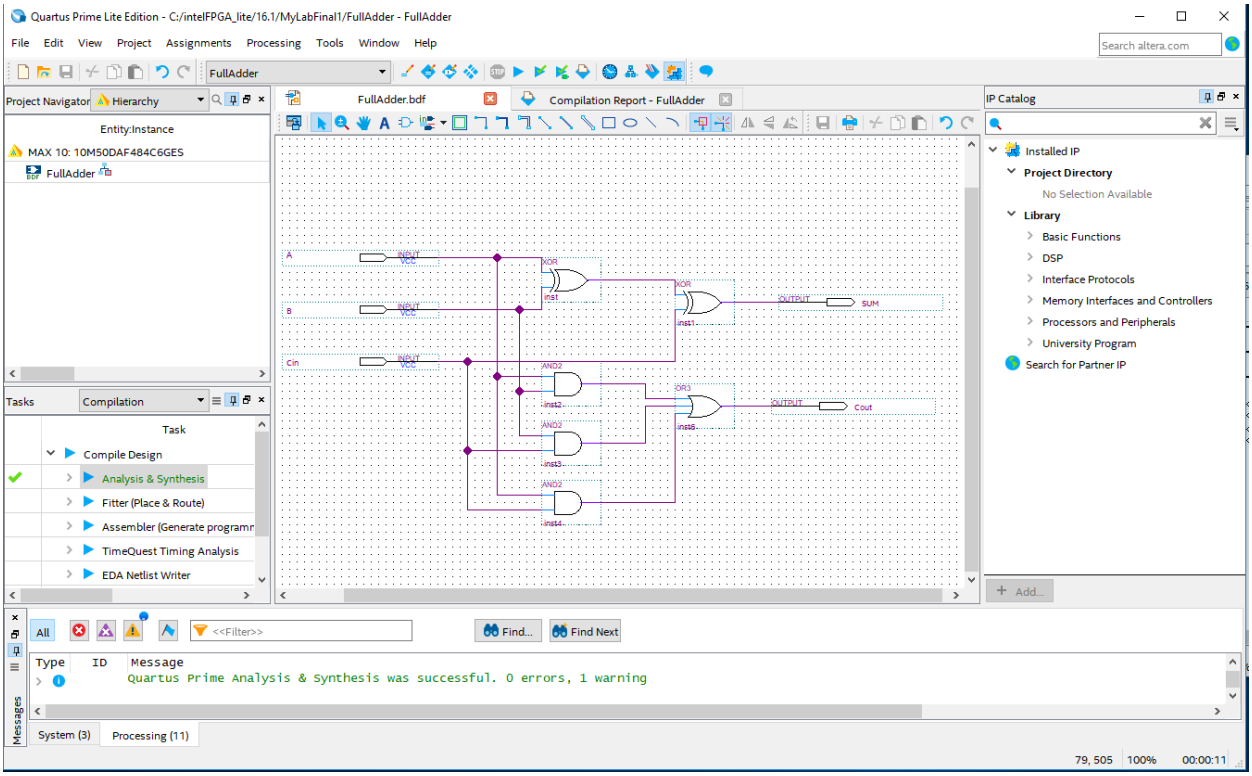
Yes

What was the biggest issue you were facing when you prepared the design for hardware upload?

Making sure that we new the different combination of pins and which switches they were paired

Task 1-4: Build and Test the 1-Bit Full Adder

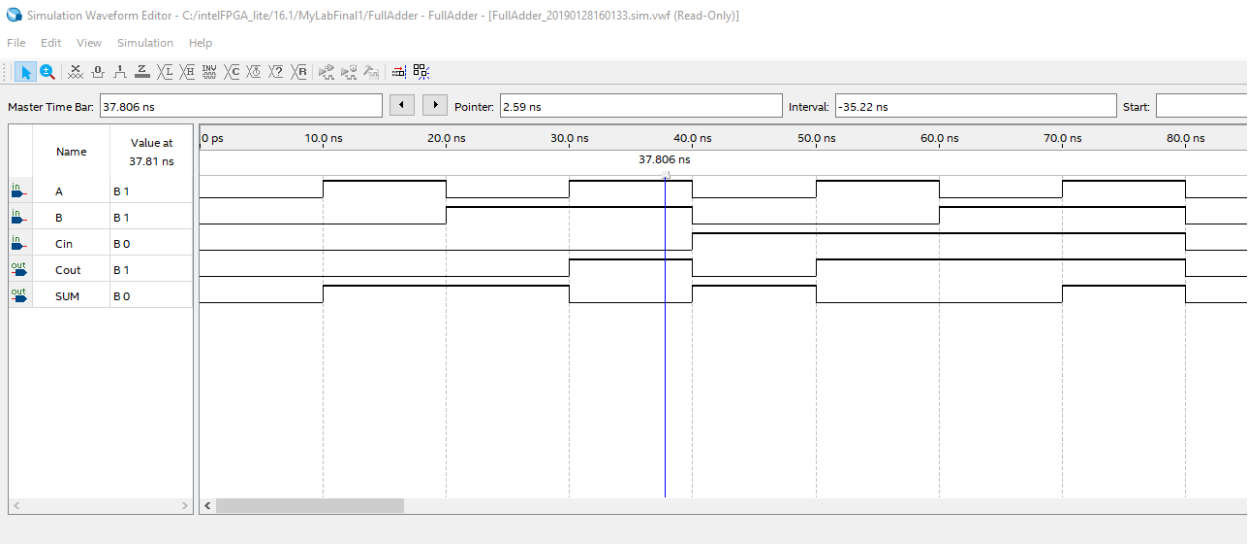
Include a picture of your Quartus circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

Making sure we had all the points connected because and x would show up indicating that the connection was not present

Include a picture of your Quartus simulation (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

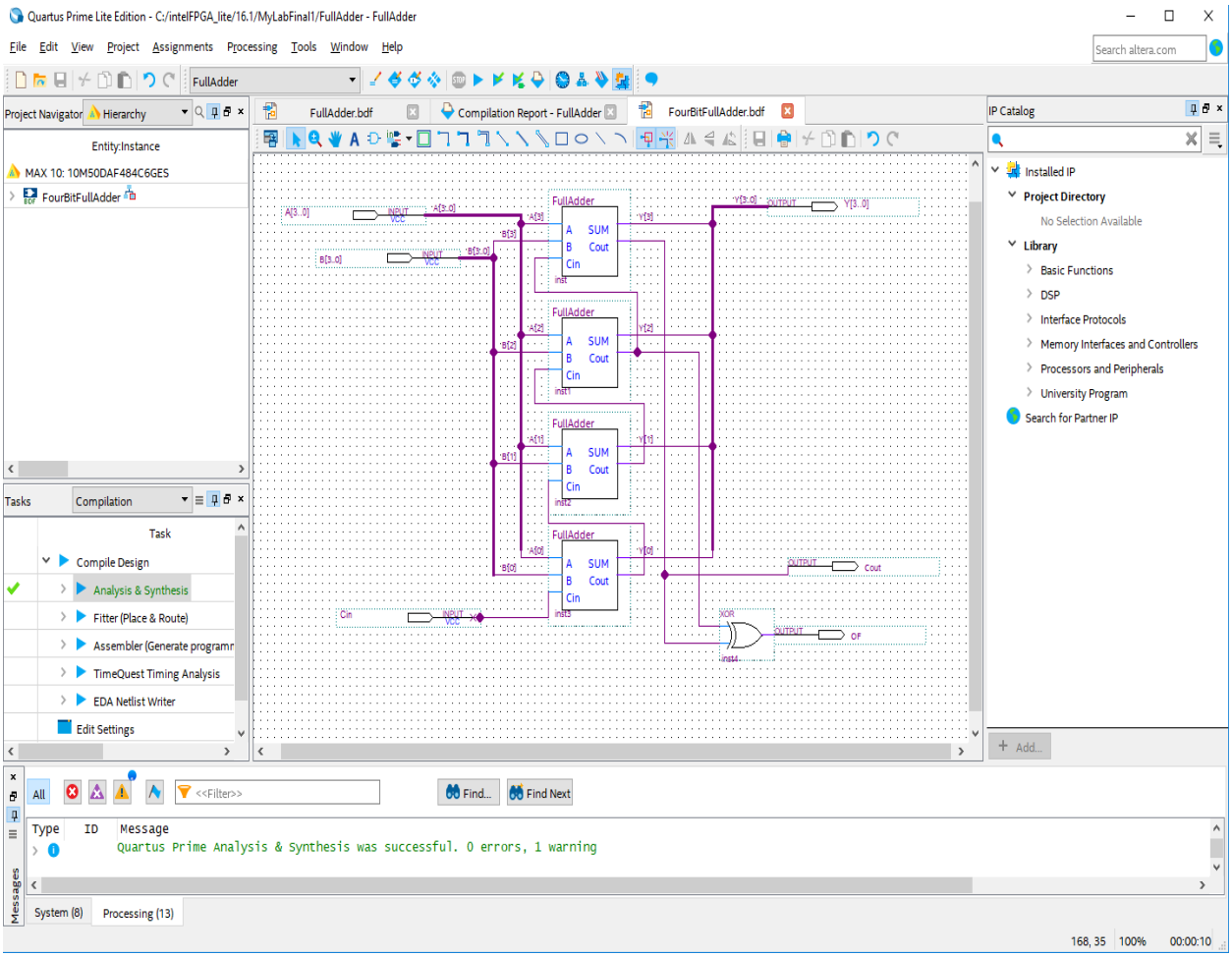
Yes it worked with a 4 bit incrementor.

Please comment on the single biggest issue you were facing when simulating the circuit.

We had to make sure we had different inputs to check if the half adder worked or not.

Task 1-5: Build and Test a 4-bit Full Adder

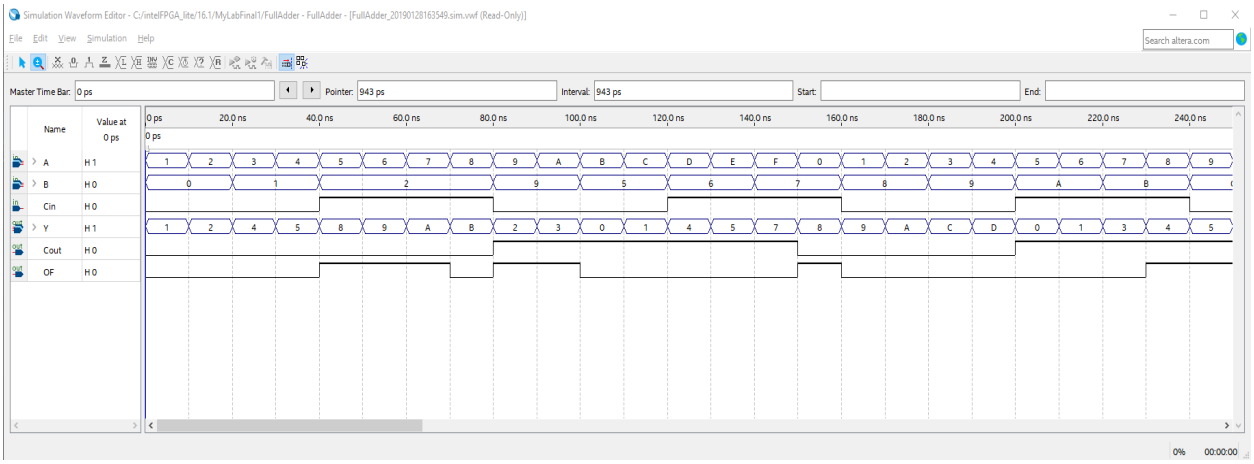
Include a picture of your Quartus circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

Making sure all points were connected to the right inputs so the “x” does not show up.

Include a picture of your Quartus simulation (timing diagram) here:



Which tests did you perform and why? The following table is an example of how to describe your test sequence. Please add additional columns if you performed more tests. You need to make sure to perform a sufficient number of tests to check the circuit for eventual faults.

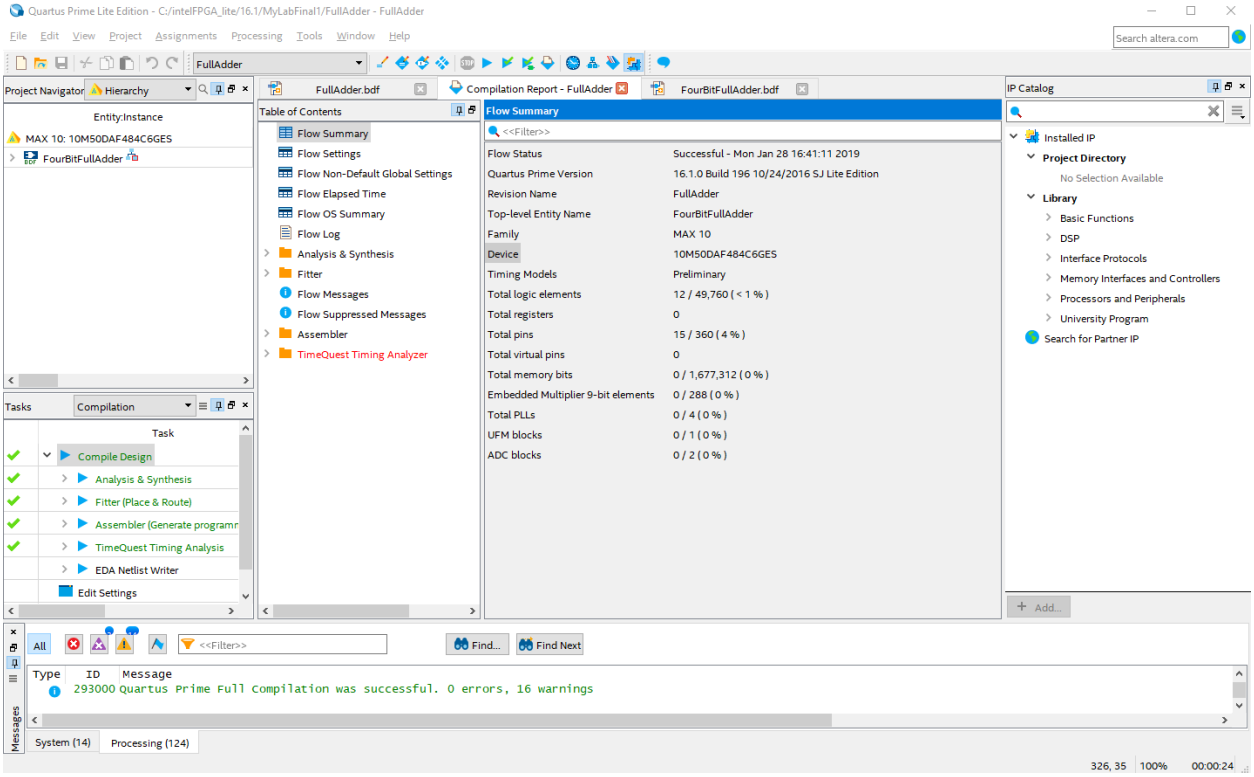
Test stimulus	**Test motivation**	**Pass/Fail**
All inputs 0	Check for stuck-at-1 faults	Pass
All inputs 1	Check for correct CRY	Pass
A0 is 1 the rest are 0	Check for bit order error	Pass
A3 is 1 the rest are 0	Check for bit order error	Pass
A2 is 1 the rest are 0	Check for bit order error	Pass
A1 is 1 the rest are 0	Check for bit order error	Pass
A0 &A2 are 1 the rest are 0	Check for stuck at-0 faults	Pass

Please comment on the single biggest issue you were facing when simulating the circuit.

Making sure we had different inputs to check if the half adder worked or not.

Task 1-6: Test the 4-bit Full Adder using LEDs on Hardware

Include a picture of your Quartus System Message Window here:



Was the test on the FPGA board successful?

Yes

What was the biggest issue you were facing when you prepared the design for hardware upload?

Knowing which switches are allocated to their respective the pins.

Don’t forget to ask the TA to record your score for upload onto Canvas!

LAB 1: LAB REPORT GRADE SHEET

Nam _____

Instructor Assessment

Grading Criteria	Max Points	Points Lost
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task 1-1: Build and Test a 1-Bit Half-Adder	10	
Task 1-2: Build and Test a 4-Bit Increment Circuit	10	
Task 1-3: Test the 4-Bit Increment Circuit Using LEDs on Hardware	5	
Task 1-4: Build and Test a 1-Bit Full Adder	10	
Task 1-5: Design, Build and Test a 4-Bit Full Adder	10	
Task 1-6: Test the 4-Bit Full Adder Circuit Using LEDs on Hardware	5	
Lab Score (50 points total)	**Points Lost**	
	Late Lab	
	Lab Score	