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CSE 230 Assignment 7

1. The CPI for a single cycle process model is 1.
2. The clock cycle for a single cycle implementation and a fixed length clock is 200ps
3. The clock cycle for a single cycle implementation and a fixed length clock is 450ps
4. The clock cycle for a single cycle implementation and a fixed length clock is 375ps
5. The clock cycle for a single cycle implementation and a fixed length clock is 200ps
6. The clock cycle for a single cycle implementation and a fixed length clock is 650ps

7.

Stack Control and Instruction	R Format	Lw	Sw	Beq
RegDst(0)	The path should selct register at [15-11] as the final destination. Therefore, this will not work	This works	This works	This works
ALUSrc(0)	This works	This will not work as lw has to pick an immediate value for ALU	This does not work as sw has to select an immediate value as for alu	This works
MemtoReg(0)	This works	This will not work as lw writes data from the memory to register, not the other way around	This works	This works
RegWrite(0)	This will not work as there is not point to writing data to register	This will not work as the load should not write data to register	This works	This works
MemRead(0)	This works	This will not work as it needs data	This works	This works

		from the memory		
MemWrite (0)	This works	This works	Will not work as data needs to be written in memory	This works
Branch(0)	This works	This works	This works	This will not work as it is needed by the and gate
ALUOp1 (0)	This will not work as it will only do addition	This works	This works	This works
ALUOp0 (0)	This works	This works	This works	Will not work as we should subtract the two values

8. In order to implement JR, we can add an additional command line

9. We would not have to change anything

Values include:

RegDst - 0

ALUSrc- 1

MemtoReg- 0

RegWrite- 1

MemRead - 0

MemWrite- 0

Branch- 0

OPCode- 0010000

ALUOp- 00(+)

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