

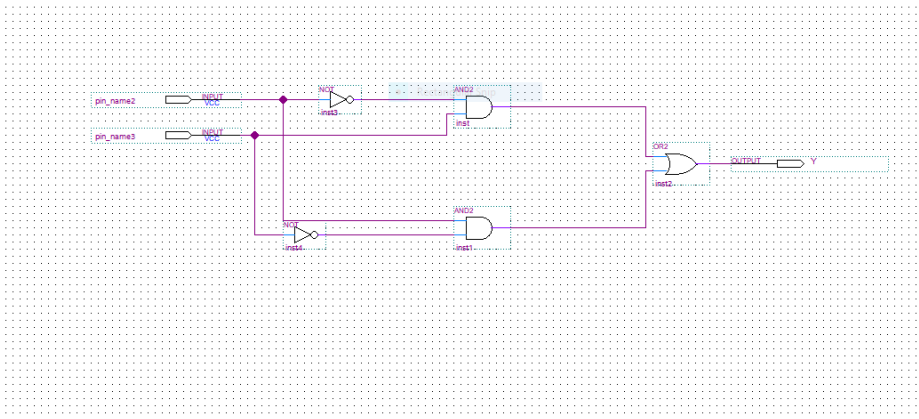
CSE/EEE 120
Lab 0 Answer Sheet
Tutorial: Using Quartus Prime Lite

Name: Vishwas Mani Instructor/Time: Matar / Tues-Thurs, 3:00 - 4:15

Date: September 9, 2019

Task 0-1: Build a 2-input XOR gate using AND/OR/NOT gates in Intel Quartus

Include a picture of your Quartus circuit here:

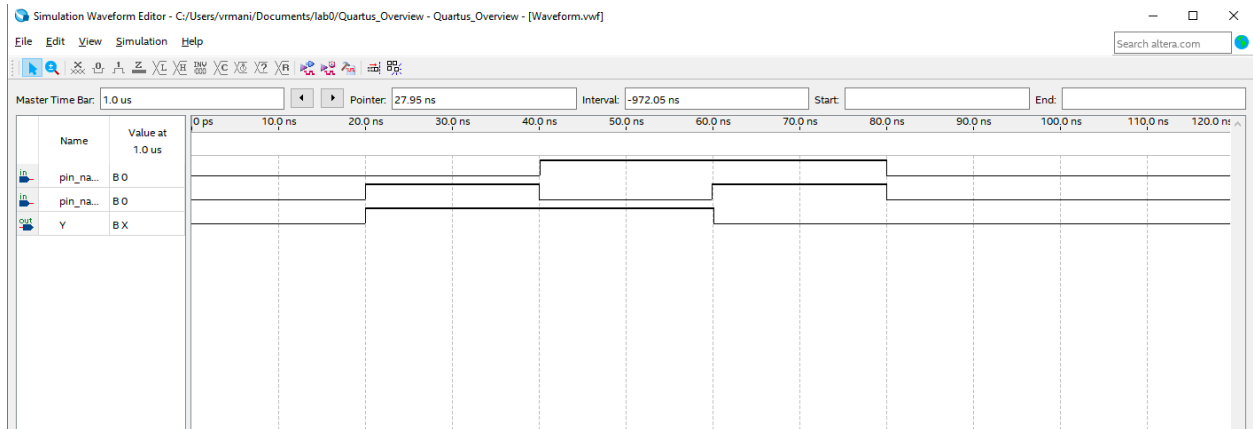


Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I faced when designing the circuit was getting a hang of using the various tools that we used during this portion of the lab. After I became comfortable with the location of all the tools, it was a lot easier to put the pieces together and make the circuit.

Task 0-2: Simulate the 2-input XOR gate using the University Waveform VWF and QSIM

Include a picture of your Quartus simulation (timing diagram) here:



Please answer the following questions:

1. How do you expect the output of a 2-input XOR gate to behave?
 - a. I expected the output of a 2 input XOR gate to act as I expected based on the truth table, and I had no surprises in the outcome during this Lab.
2. What tests did you perform to verify your logic circuit?
 - a. I performed 4 tests of each possible combinations of inputs(0 and 1). All the combinations ended up working
3. Did the circuit behave as expected? If no, what was wrong?
 - a. The circuit behaved as I expected to and passed all test cases

Task 0-3: Test the 2-input XOR gate Using LEDs on Hardware

Include a picture of your Quartus System Message Window here:

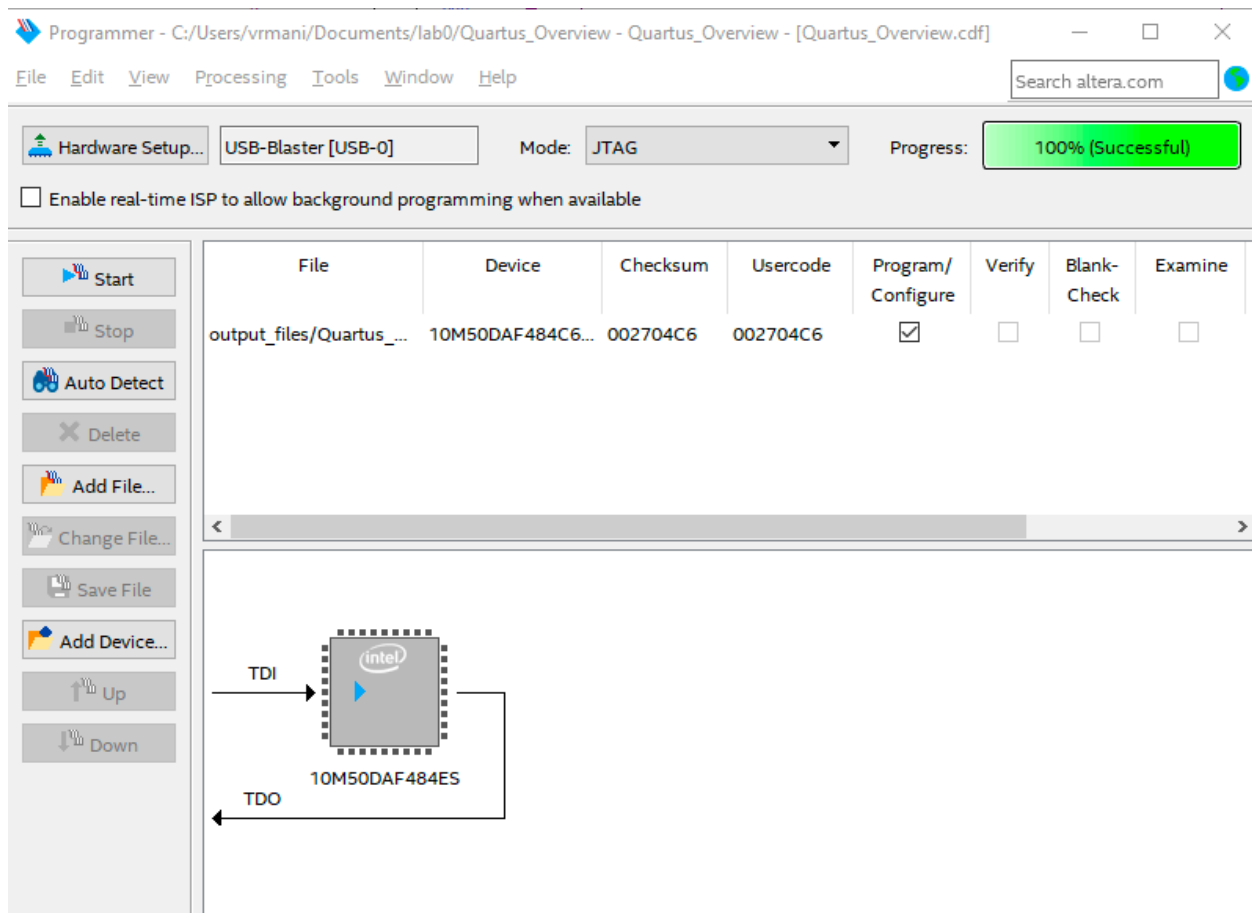
The screenshot displays the Quartus Prime Lite Edition software interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The main workspace is divided into several panes:

- Project Navigator:** Shows the project hierarchy with 'MAX 10: 10M50DAF484C6GES' and 'Quartus_Overview'.
- Table of Contents:** Lists various reports and settings, including Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, Flow OS Summary, Flow Log, Analysis & Synthesis, Fitter, Flow Messages, Flow Suppressed Messages, Assembler, and Timing Analyzer.
- Flow Summary:** The active window showing the compilation status and details.
- Tasks:** A list of tasks with checkboxes, including Compile Design, Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate programming), Timing Analysis, EDA Netlist Writer, Edit Settings, and Program Device (Open Programmer).

The **Flow Summary** window displays the following information:

<<Filter>>	
Flow Status	Successful - Mon Sep 09 16:11:33 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 5J Lite Edition
Revision Name	Quartus_Overview
Top-level Entity Name	Quartus_Overview
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	2 / 49,760 (< 1 %)
Total registers	0
Total pins	3 / 360 (< 1 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Include a picture of your Programmer Window here:



Was the test on the FPGA board successful?

The test on the FPGA board was successful and passed all the cases

What was the biggest issue you were facing when you prepared the design for hardware upload?

The Pin Assignments always kept changing when I compiled the program because I didn't them correctly, but after I changed the input to their respective names it ran properly.

Don't forget to ask the TA to record your score for upload onto Canvas!

Lab 0: Lab Report Grade Sheet

Nam Vishwas Mani

Instructor Assessment

Grading Criteria	Max Points	Points Lost
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task 0-1: Build a 2-input XOR gate using AND/OR/NOT gates in Intel Quartus	10	
Task 0-2: Simulate the 2-input XOR gate using the University Waveform VWF and QSIM	10	
Task 0-3: Test the 2-input XOR gate Using LEDs on Hardware	10	
Lab Score (30 points total)	Points Lost	
	Late Lab	
	Lab Score	