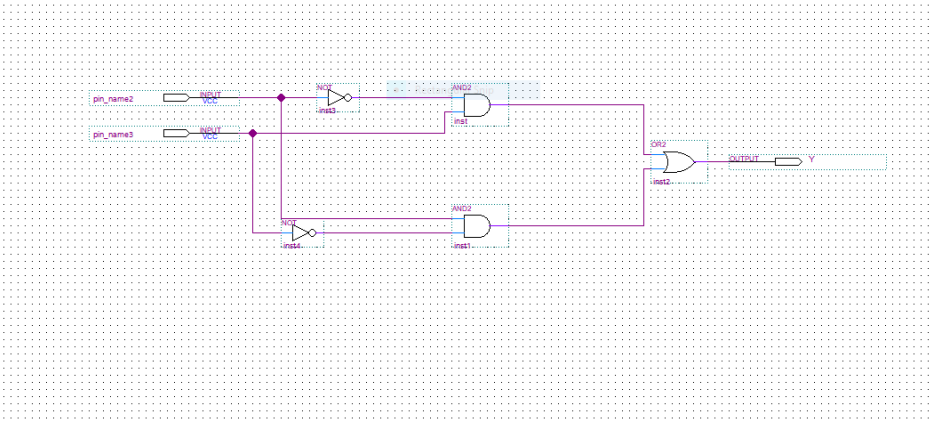
CSE/EEE 120
Lab 0 Answer Sheet
Tutorial: Using Quartus Prime Lite

Name: Vishwas Mani Instructor/Time: Matar / Tues-Thurs, 3:00 - 4:15

Date: September 9, 2019

Task 0-1: Build a 2-input XOR gate using AND/OR/NOT gates in Intel Quartus

Include a picture of your Quartus circuit here:

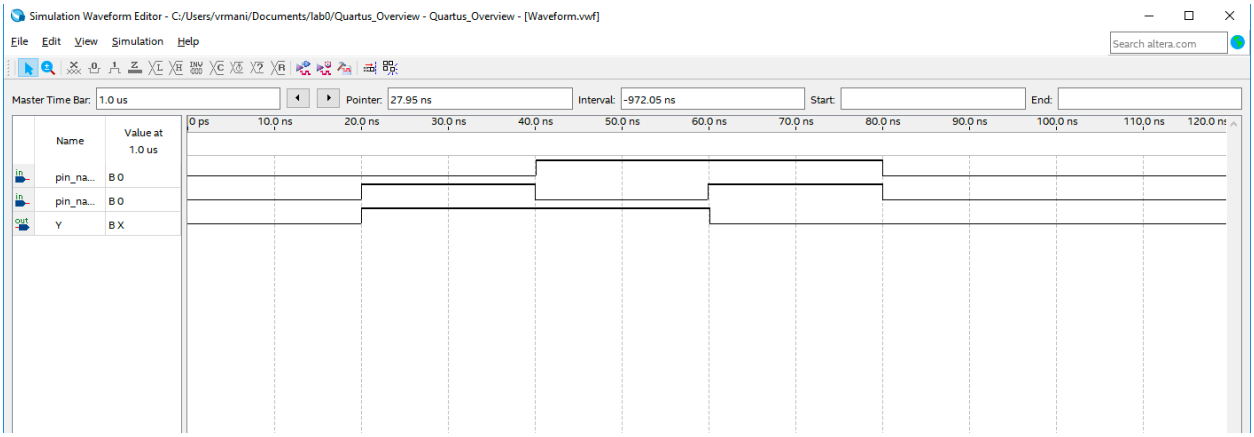


Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I faced when designing the circuit was getting a hang of using the various tools that we used during this portion of the lab. After I became comfortable with the location of all the tools, it was a lot easier to put the pieces together and make the circuit.

Task 0-2: Simulate the 2-input XOR gate using the University Waveform VWF and QSIM

Include a picture of your Quartus simulation (timing diagram) here:

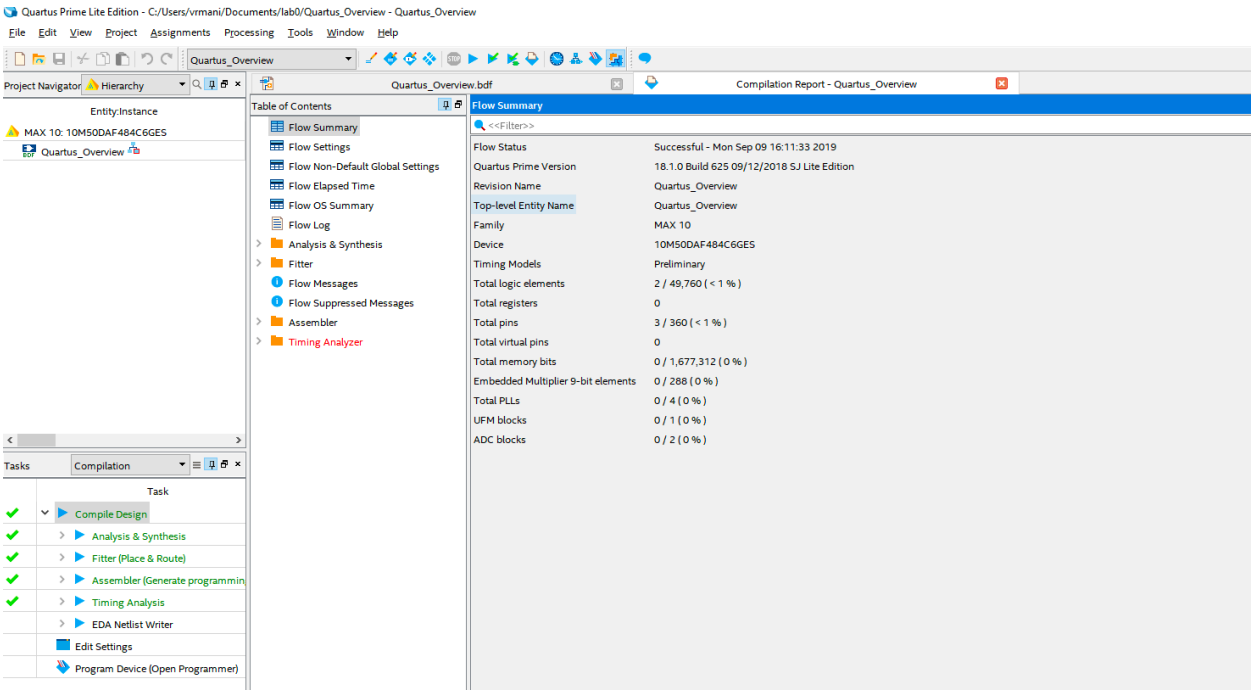


Please answer the following questions:

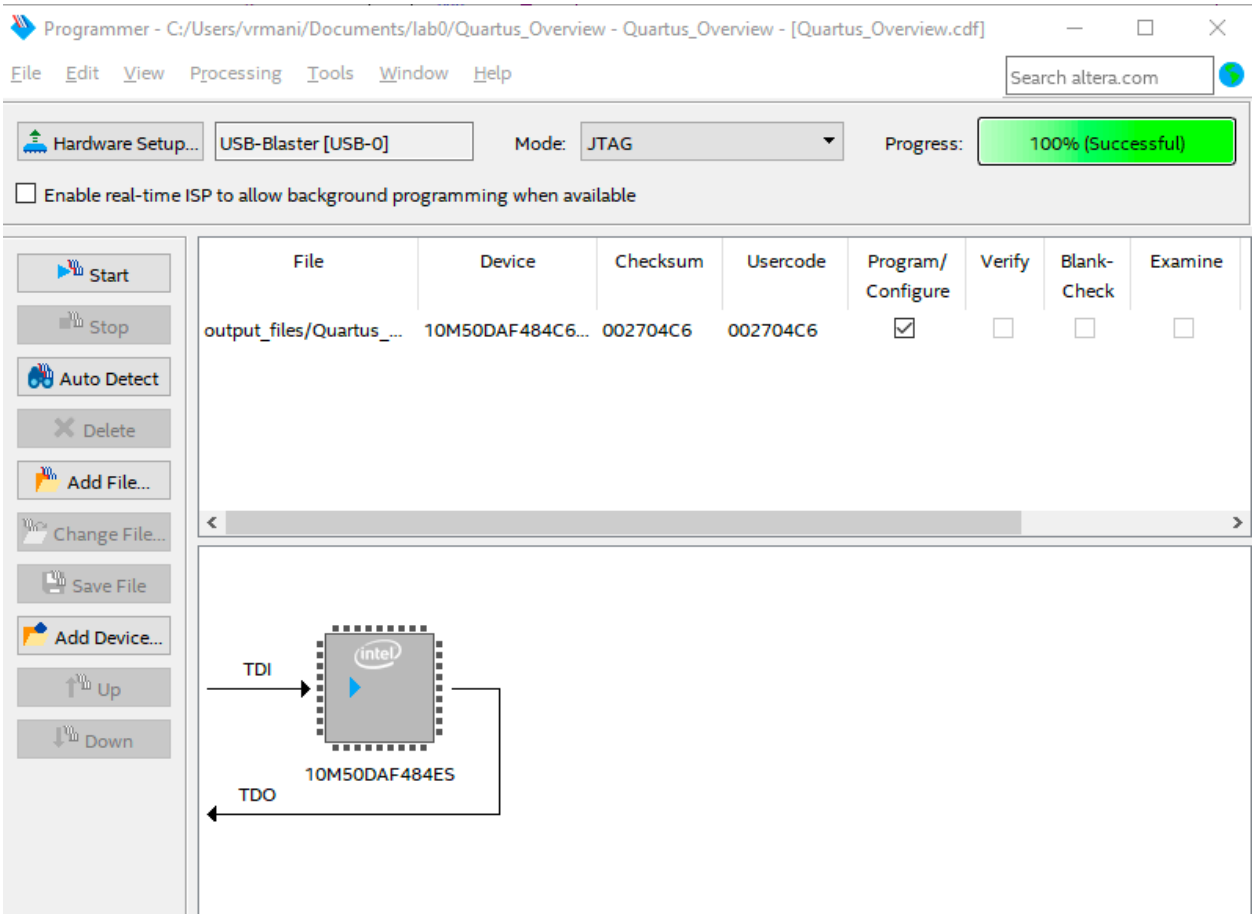
1. How do you expect the output of a 2-input XOR gate to behave?
    a. I expected the output of a 2 input XOR gate to act as I expected based on the truth table, and I had no surprises in the outcome during this Lab.
2. What tests did you perform to verify your logic circuit?
    a. I performed 4 tests of each possible combinations of inputs(0 and 1). All the combinations ended up working
3. Did the circuit behave as expected? If no, what was wrong?
    a. The circuit behaved as I expected to and passed all test cases

Task 0-3: Test the 2-input XOR gate Using LEDs on Hardware

Include a picture of your Quartus System Message Window here:



Include a picture of your Programmer Window here:



Was the test on the FPGA board successful?

The test on the FPGA board was successful and passed all the cases

What was the biggest issue you were facing when you prepared the design for hardware upload?

The Pin Assignments always kept changing when I compiled the program because I didn't them correctly, but after I changed the input to their respective names it ran properly.

Don’t forget to ask the TA to record your score for upload onto Canvas!

Lab 0: Lab Report Grade Sheet

Nam Vishwas Mani

Instructor Assessment

Grading Criteria	Max Points	Points Lost
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task 0-1: Build a 2-input XOR gate using AND/OR/ NOT gates in Intel Quartus	10	
Task 0-2: Simulate the 2-input XOR gate using the University Waveform VWF and QSIM	10	
Task 0-3: Test the 2-input XOR gate Using LEDs on Hardware	10	
Lab Score (30 points total)	**Points Lost**	
	Late Lab	
	Lab Score	