CSE/EEE 120

Lab 3 Answer Sheet

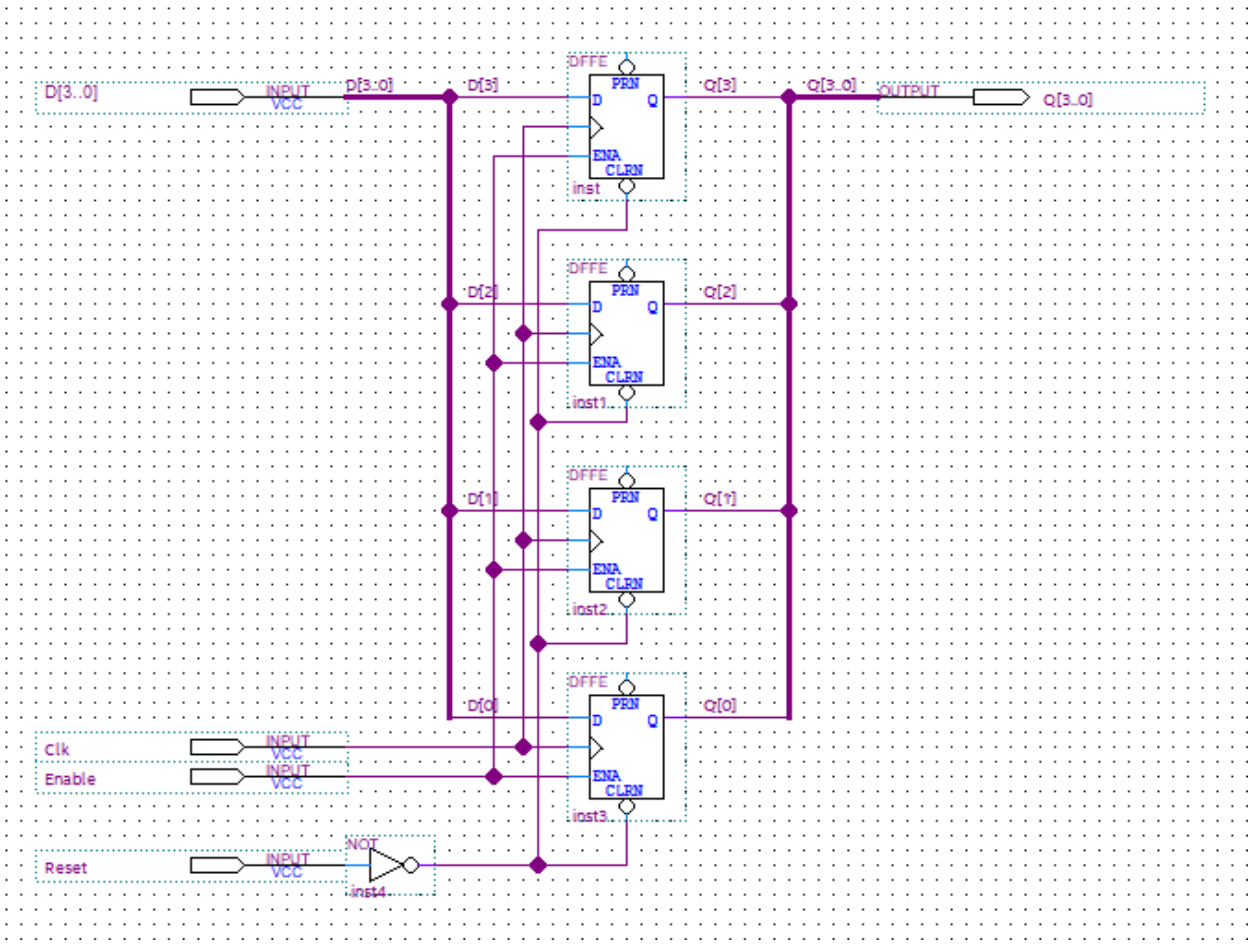
Registers, Counters and the “Brainless CPU”

Name: Vishwas Mani Instructor/Time: Matar, Tuesday, Thursday, 3:00 to 4:15

Date: November 4, 2019

Task 3-1: Build and Test a 4-Bit D Register with Enable

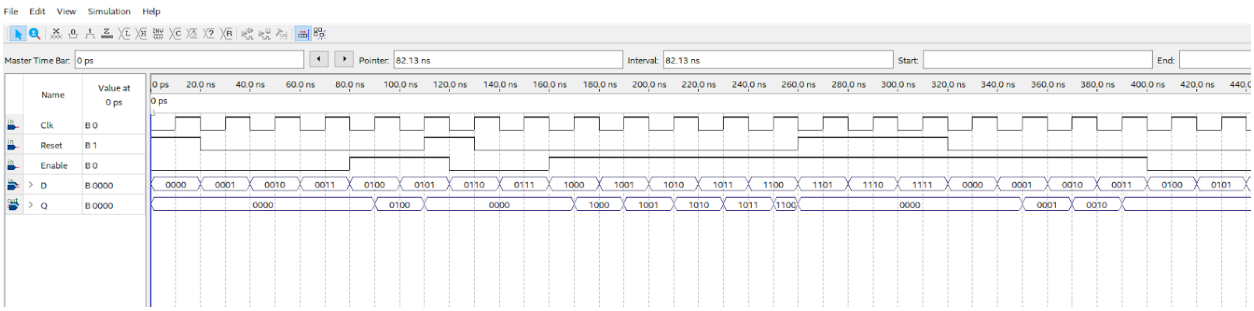
Include a picture of your Quartus circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

Naming all the individual components

Include a picture of your Quartus simulation (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

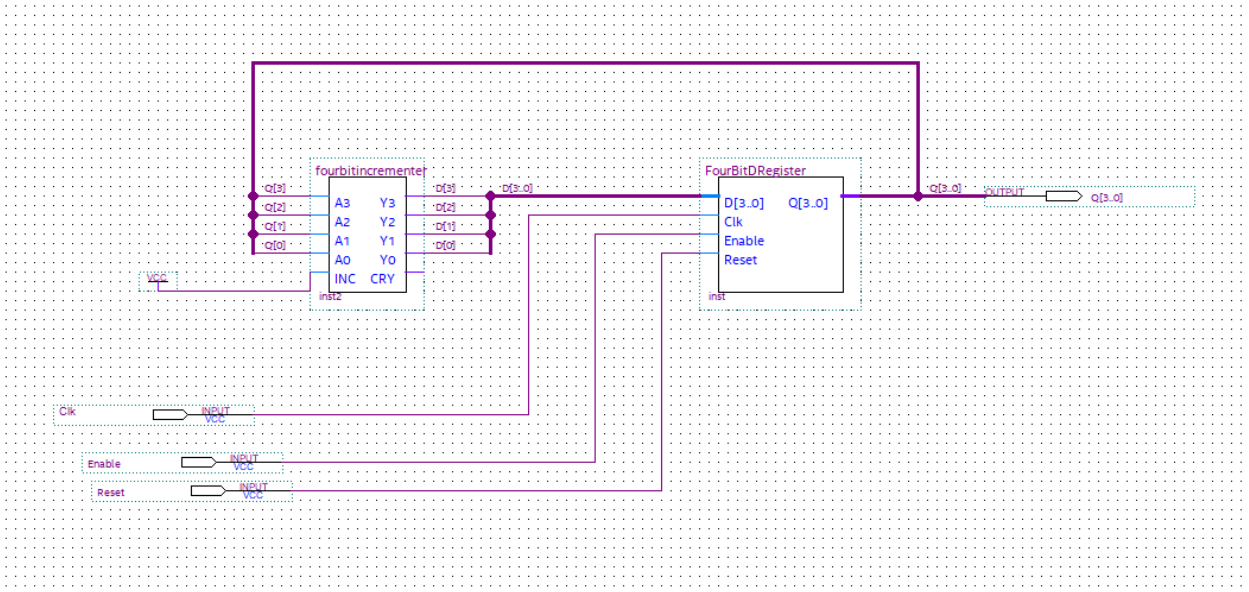
Yes it behaved as expected

Please comment on the single biggest issue you were facing when simulating the circuit.

Setting the value D to increment evenly

Task 3-2: Build and Test a 4-Bit UP Counter

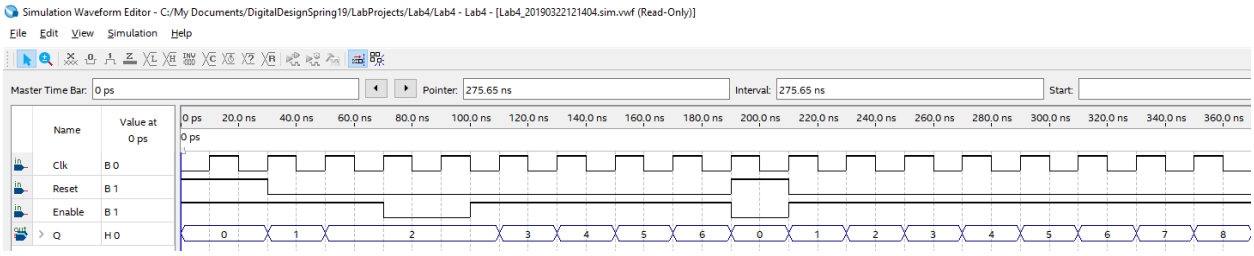
Include a picture of your Quartus circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

We did not understand the term vc to our fullest ability so we had to learn that at first

Include a picture of your Quartus simulation (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

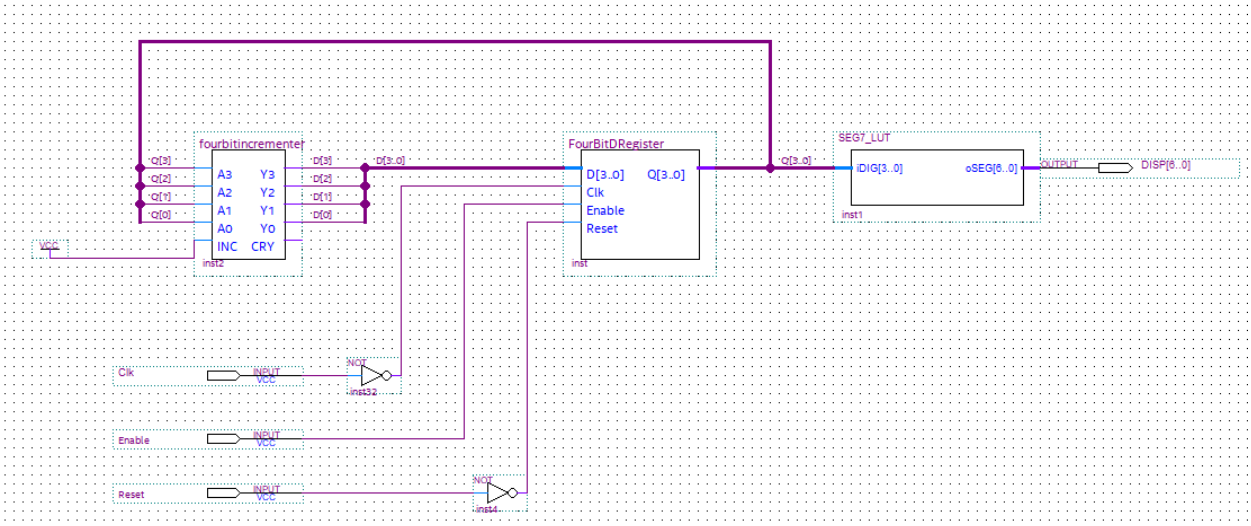
The circuit behaved as expected, no issues

Please comment on the single biggest issue you were facing when simulating the circuit.

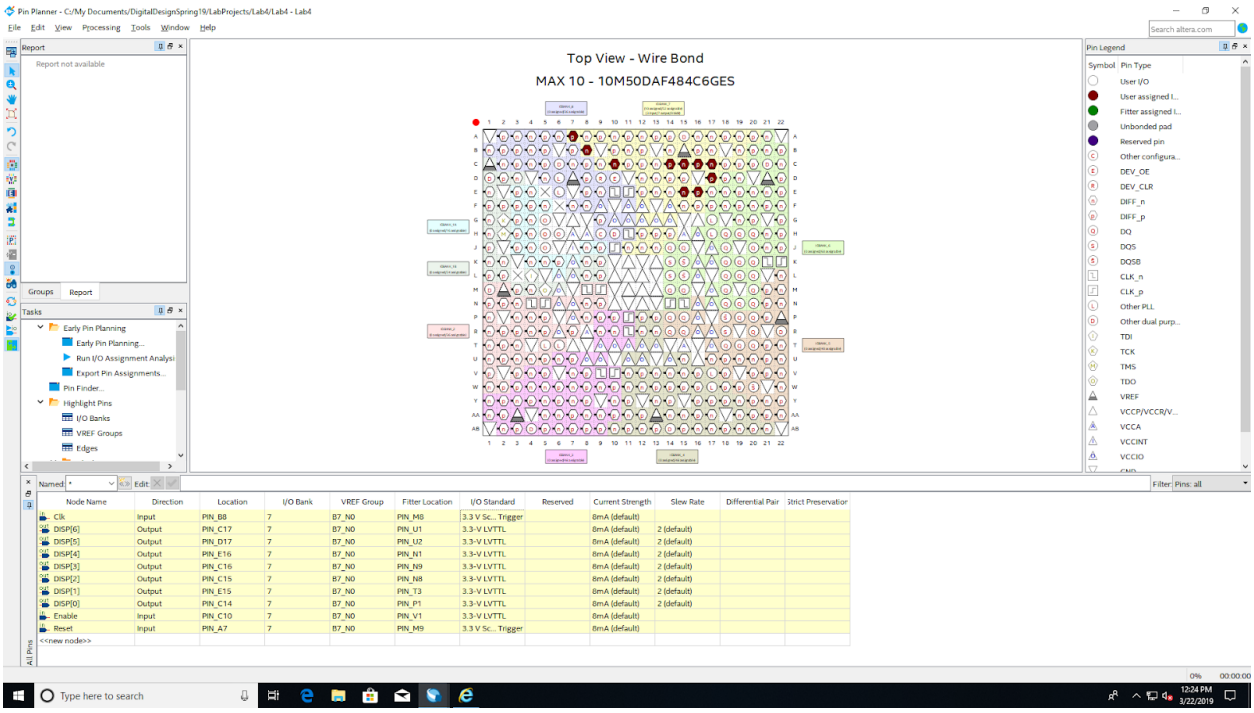
The waveform was incorrect and it took some time to figure out how to fix it

Task 3-3: Test the 4-Bit UP Counter on Hardware

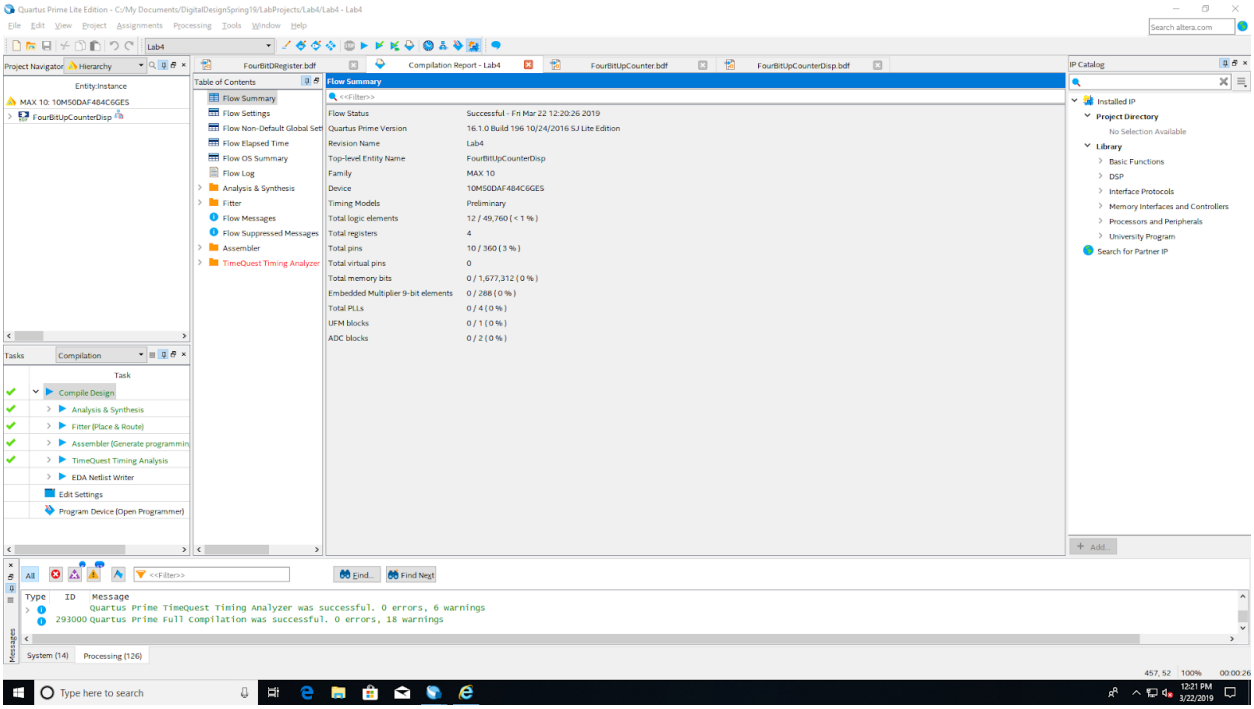
Include a picture of your Quartus circuit here:



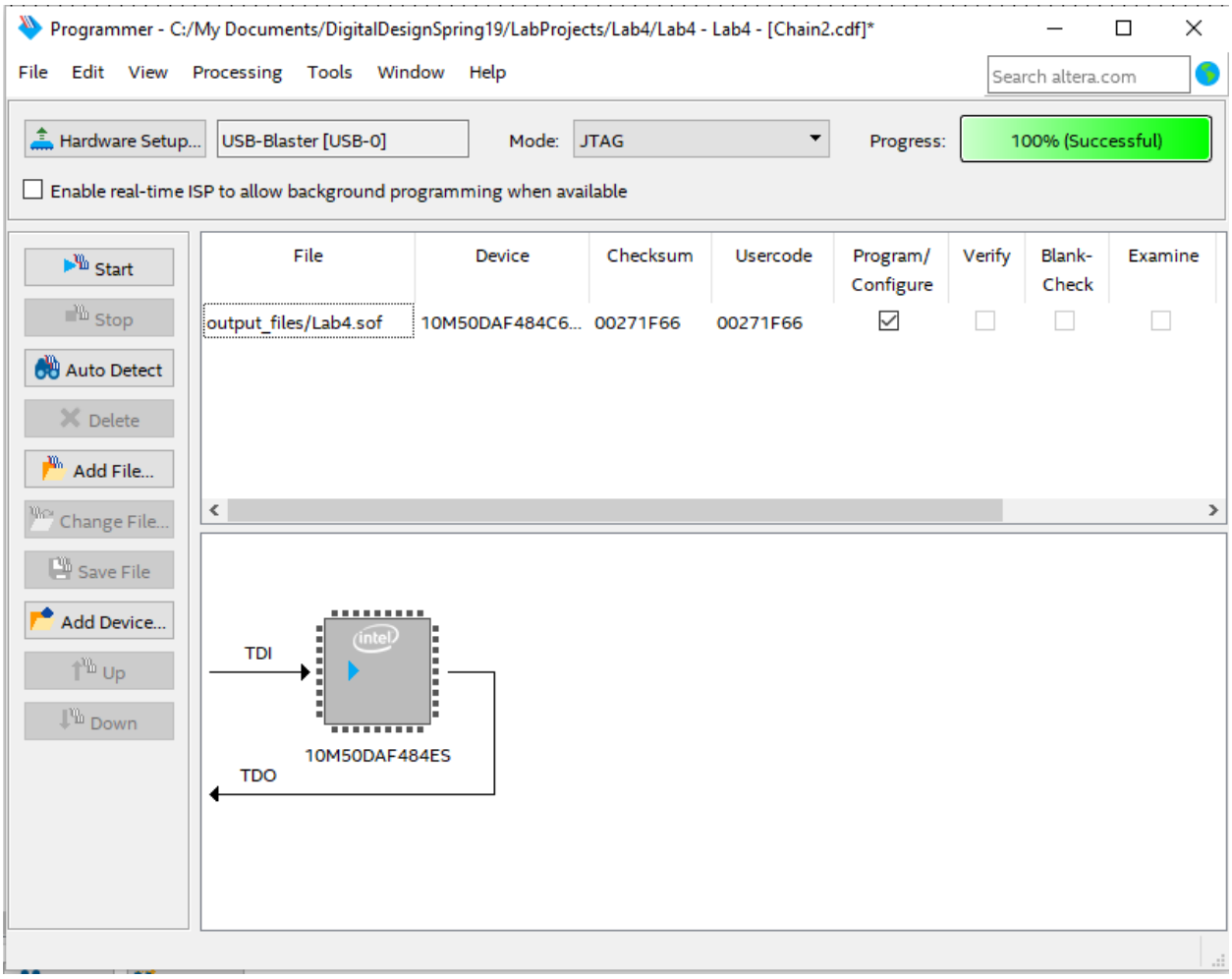
Include a picture of your Pin Planner assignment window here:



Include a picture of your Quartus System Message Window (Flow Summary) here:



Include a picture of your Programmer Window here:



Was the test on the FPGA board successful?

Yes it was

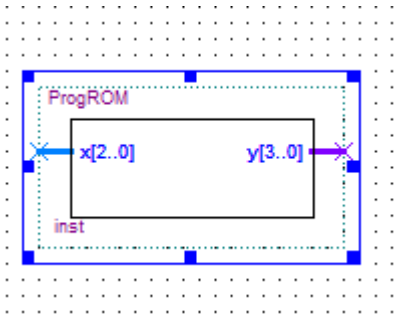
What was the biggest issue you were facing when you prepared the design for hardware upload?

The board was not programmed properly and it took some time to resolve this issue

Make sure that the TA verifies that you did complete the hardware tests and uploads your hardware demo score onto Canvas!

Task 3-4: Build a Verilog 4-Bit RAM Memory with sixteen cells

Include a picture of your RTL Netlist Schematic here:

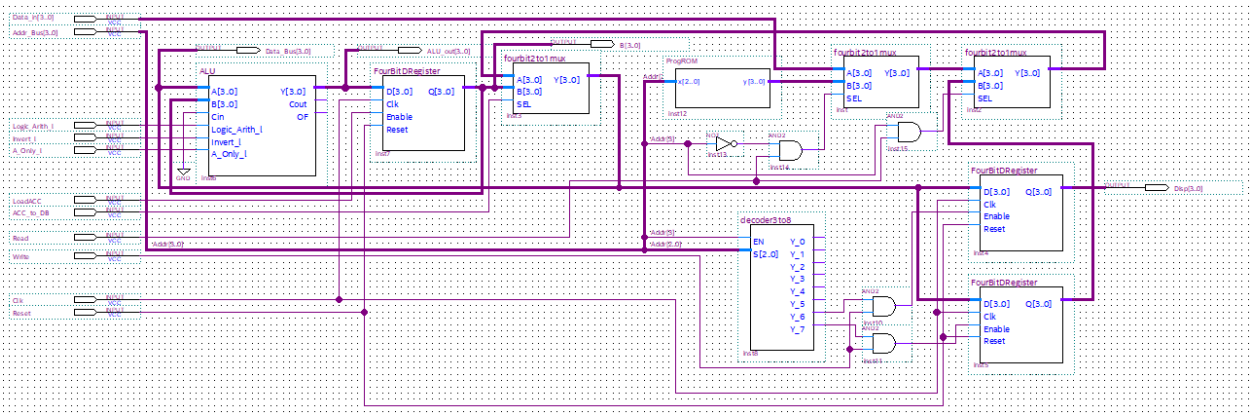


Please comment on the single biggest issue you were facing when creating the RAM memory.

Writing it all out took the biggest chunk of time

Task 3-5: Build and Test the Brainless Central Processing Unit

Include a picture of your Quartus circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

It was a very tedious process to figure out the steps for this part of the lab

Follow steps 1 through 3 outlined in the laboratory manual to test your brainless microprocessor circuit. It might be helpful to review the ALU Function Table from Lab 2. Table 1 is an example, for the ADD command, of how to fill out tables to record the values of the control lines during every clock cycle.

Table 1	
Instruction [Add operand to Accumulator (ACC)]	
Control Line	Value
4-bit Address_Bus	Address of operand
Write	0
Read	1
ACC_to_DB	0
LoadACC	1
A_Only_l	1
Invert_l	1
Logic_Arith_l	0

For all of the instructions you performed (i.e. Subtract, Load ACC, etc.) record the values of the control lines during every clock cycle in Table 2.

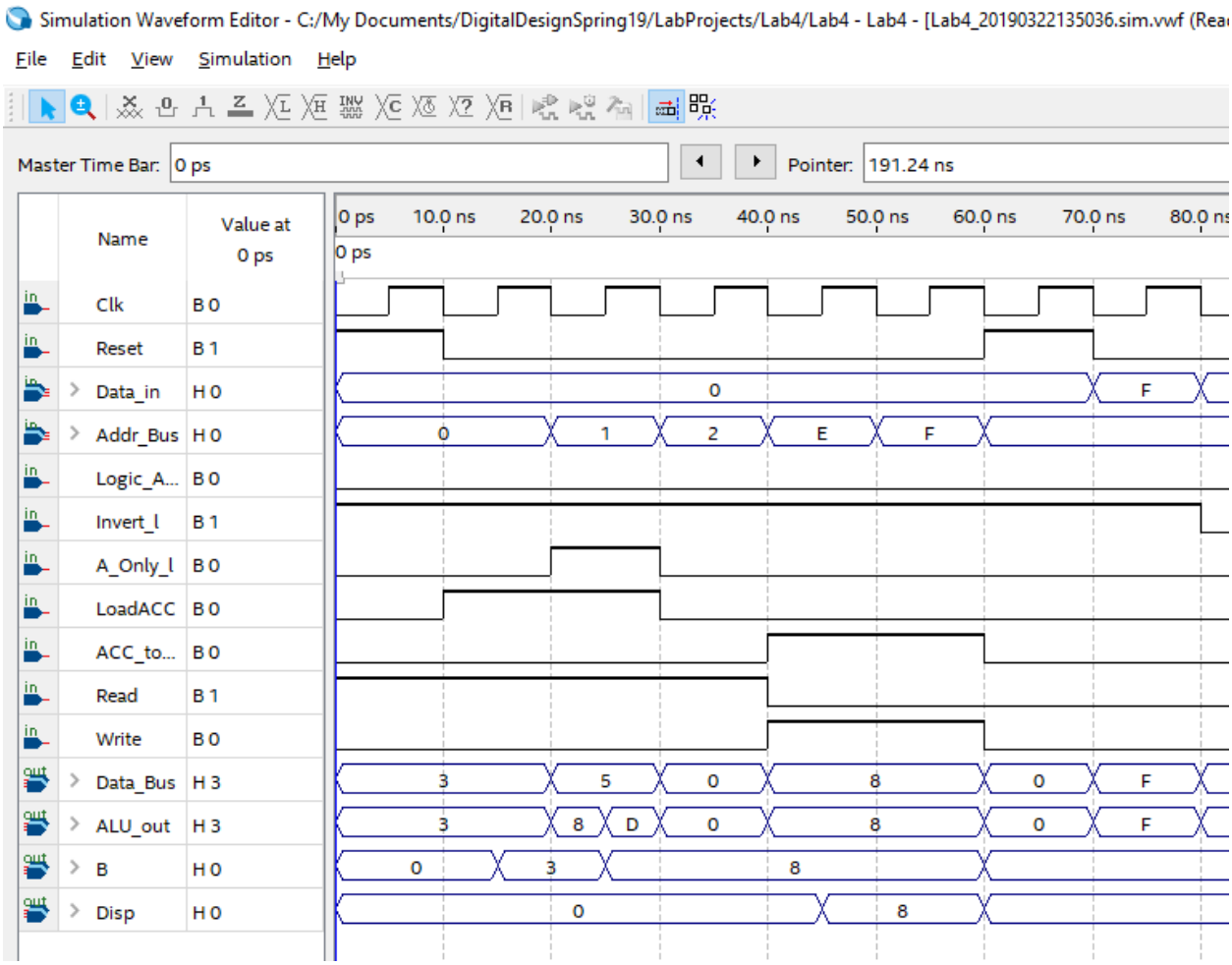
Table 2	
Instruction [Load ACC with operand]	
Control Line	Value
4-bit Address_Bus	Operand one address
Write	0
Read	1
ACC_to_DB	0
LoadACC	1
A_Only_l	0
Invert_l	1
Logic_Arith_l	1
Instruction [AND operand with ACC]	
Control Line	Value
4-bit Address_Bus	Operand one address
Write	0
Read	1
ACC_to_DB	0
LoadACC	1
A_Only_L	1
Invert_l	1
Logic_Arith_l	1
Instruction [Store ACC to RAM]	
Control Line	Value
4-bit Address_Bus	Address of output ram
Write	1

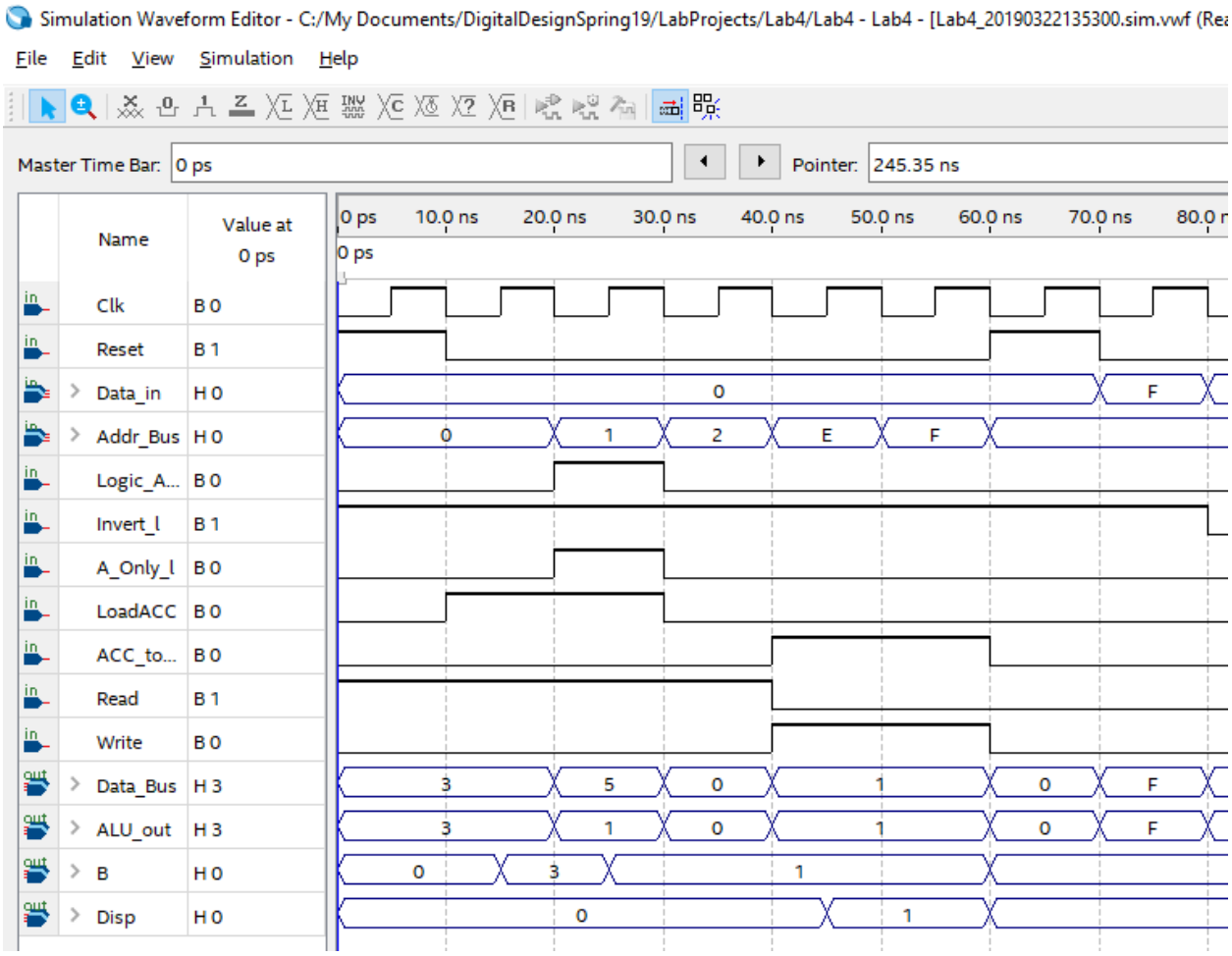
Read	0
ACC_to_DB	1
LoadACC	0
A_Only_L	0
Invert_l	1
Logic_Arith_l	0
Instruction [Subtract operand from ACC]	
Control Line	Value
4-bit Address_Bus	Operand one address
Write	0
Read	1
ACC_to_DB	0
LoadACC	1
A_Only_L	1
Invert_l	0
Logic_Arith_l	0

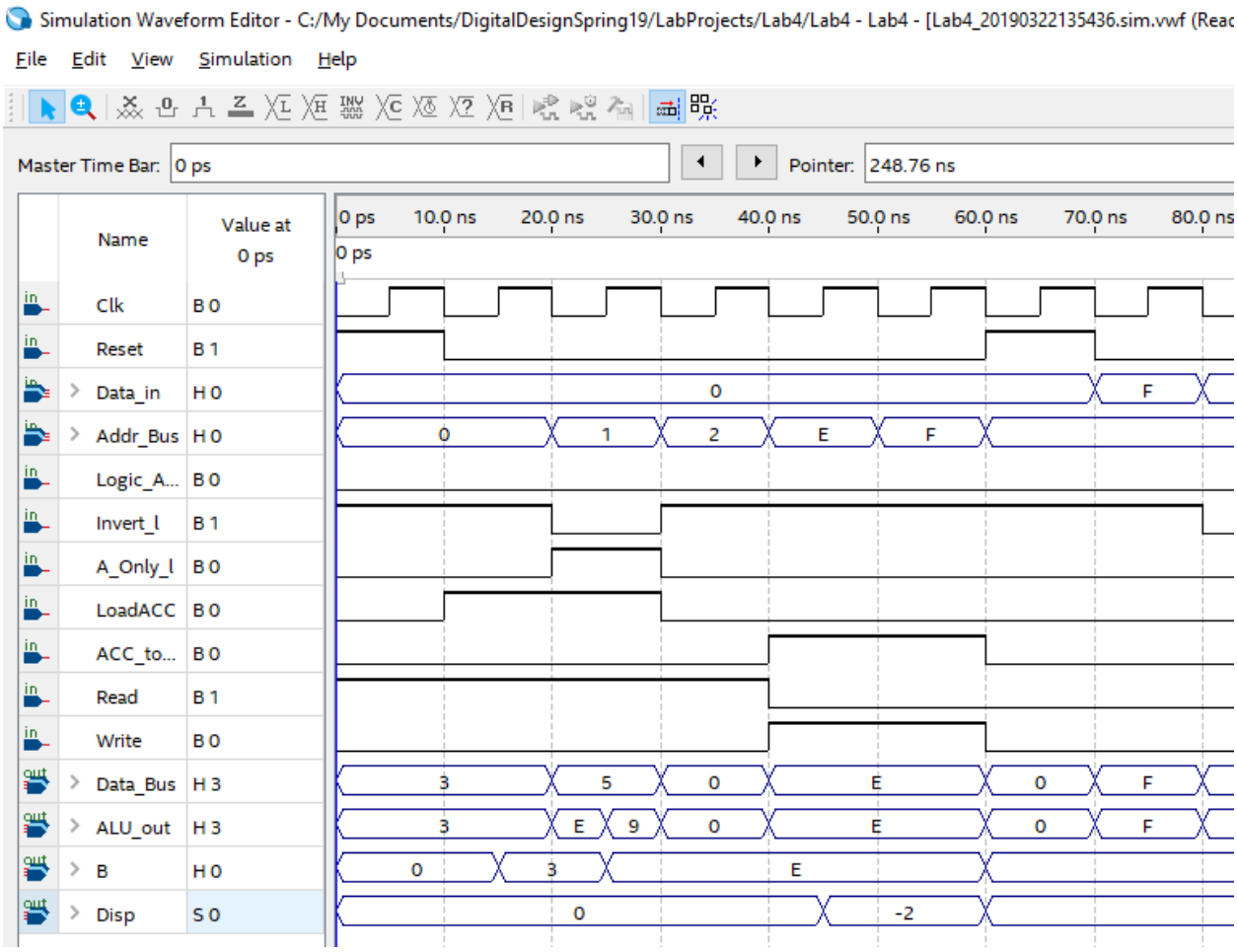
Describe any other tests that you performed.

Unfortunately, we did not perform any other test

Include pictures of your Quartus simulations (timing diagrams) here:


Simulation Waveform Editor - C:/My Documents/DigitalDesignSpring19/LabProjects/Lab4/Lab4 - Lab4 - [Lab4_20190322135036.sim.vwf (Rea
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 191.24 ns
Name
Value at 0 ps
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
Clk B 0
Reset B 1
Data_in H 0
Addr_Bus H 0
Logic_A... B 0
Invert_I B 1
A_Only_I B 0
LoadACC B 0
ACC_to... B 0
Read B 1
Write B 0
Data_Bus H 3
ALU_out H 3
B H 0
Disp H 0


Simulation Waveform Editor - C:/My Documents/DigitalDesignSpring19/LabProjects/Lab4/Lab4 - Lab4 - [Lab4_20190322135300.sim.vwf (Rea
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 245.35 ns
Name
Value at 0 ps
Clk B 0
Reset B 1
Data_in H 0
Addr_Bus H 0
Logic_A... B 0
Invert_I B 1
A_Only_I B 0
LoadACC B 0
ACC_to... B 0
Read B 1
Write B 0
Data_Bus H 3
ALU_out H 3
B H 0
Disp H 0
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 n



Did the circuit behave as expected? If no, what was wrong?

Yes, the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

The directory chosen was wrong, and it took some time to fix that

LAB 3: LAB REPORT GRADE SHEET

Nam _____

Instructor Assessment

Grading Criteria	Max Points	Points Lost
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task 3-1: Build and Test a 4-Bit D Register with	10	
Task 3-2: Build and Test a 4-Bit UP Counter	10	
Task 3-3: Test the 4-Bit UP Counter on Hardware	10	
Task 3-4: Build a Verilog 4-Bit RAM Memory with sixteen cells	10	
Task 3-5: Build and Test the Brainless Central Processing Unit	20	
Lab Score (60 points total)	**Points Lost**	
	Late Lab	
	Lab Score	