Comp E 475

Digital Systems

HW7 : ALU

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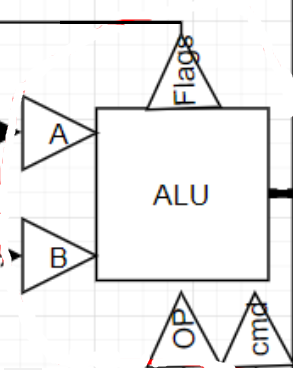
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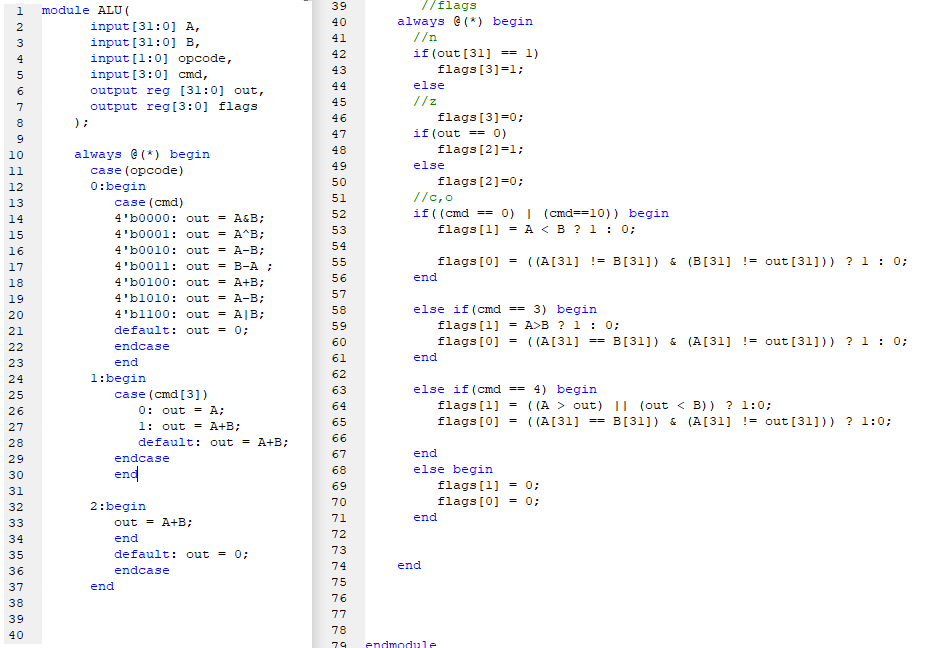
# Task Description

In this assignment we should design ALU, that implements the hardware necessary to execute the AND, XOR, ORR, SUB, RSB, ADD and CMP instructions in data processing; STR, LDR(standard addressing mode) in memory access and B in branching.

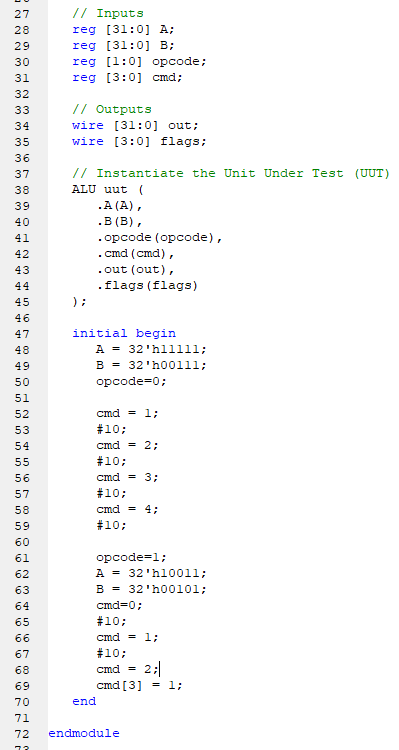


# Solution

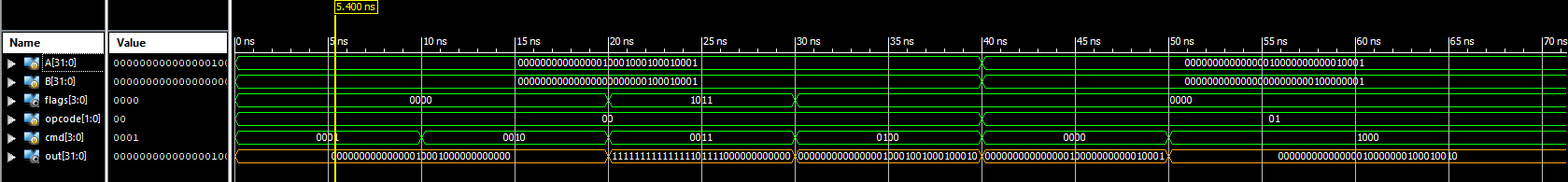
The solution is based on the scheme of the simple CPU, which we created during one of our lectures. According to it, ALU has two operands, opcode and cmd, or an operation as an input, and has flags and output as the output. The flags have also traditional outputs N, Z, C and O. the solution was straight forward, using mainly case statements when it was possible, otherwise, if-else statements.

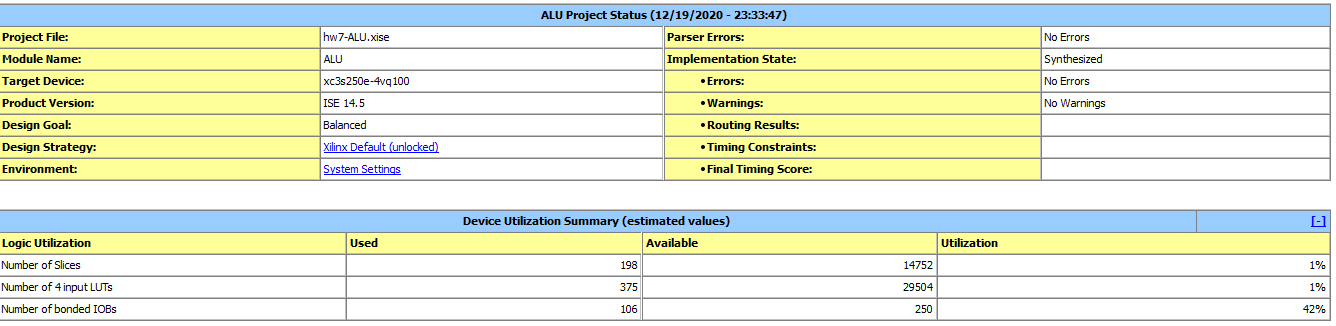


# Simulation & Verification



Here are the testbench code as well as the simulation data.



The code synthesized without any errors or warnings

# Conclusion

In this assignment we implemented the logic for the simple CPU ALU. Using the drawn scheme and appropriate data tables presented during the lectures, I wrote the code of the ALU with its i/o. The source code is uploaded on Github/vmazashvili on in a corresponding repository.