

5G PHY Layer Processing – receiver design (1)

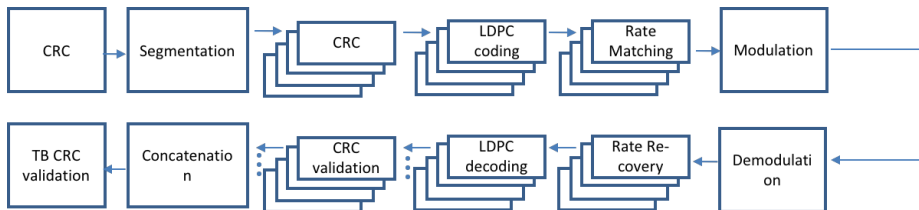
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Simulation-Based Design of 5G Wireless Standard (EE698H)

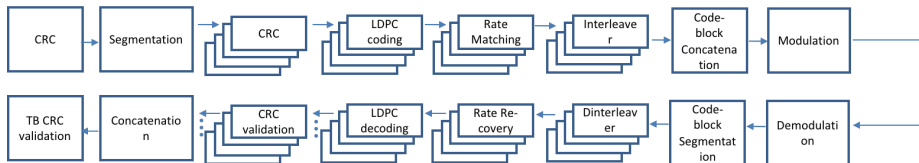
Agenda for today

- Discuss code block concatenation
 - References mentioned later in the slides
- Discuss receiver processing for the transmit chain discussed

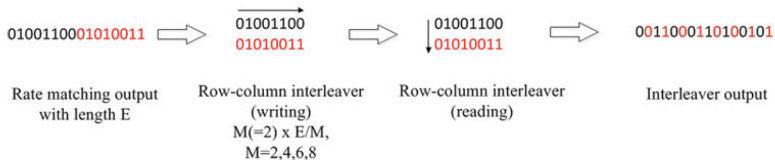
5G transceiver chain till rate matching/rate recovery



5G transceiver chain till code block concatenation



- Each **rate matched codeblocks** is interleaved using row-column interleaver



Pseudocode of interleaving¹

- Row size depends on modulation order - avoid burst errors
- Bits output of rate matcher are denoted as $e_0, e_1, f_2, e_3, \dots, e_{(E-1)}$
- Bits output of interleaver are denoted as $f_0, f_1, f_2, f_3, \dots, f_{(E-1)}$

for $j = 0$ to $E/Q_m - 1$

for $i = 0$ to $Q_m - 1$

$$f_{i+j \cdot Q_m} = e_{i \cdot E/Q_m + j};$$

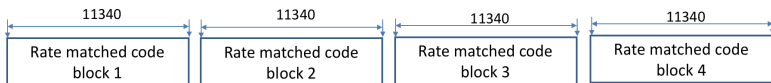
end for

end for

¹Sec 5.4.2.2 of 38.212

Concatenation of code blocks

- **Rate matched codeblocks** are sequentially concatenated when $C > 1$



- Rate matcher output is four code blocks of length 11340 bits
- Total rate matched output bits $11340 \times 4 = 45360$
- Recall total output bits allowed to transmit $G = \text{NPRB} \times \text{RE} \times Q_m = 70 \times 162 \times 4 = 45360$
- Input and output bit sequence for the code block concatenation are

$$\begin{aligned} f_{rj} & \text{ for } r = 0, \dots, (C - 1) \text{ and } j = 0, \dots, (E_r - 1) \\ g_k & \text{ for } k = 0, \dots, (G - 1) \end{aligned}$$

Pseudocode of code block concatenation²

Set $k = 0$ and $r = 0$

while $r < C$

Set $j = 0$

while $j < E_r$

$$g_k = f_{rj}$$

$$k = k + 1$$

$$j = j + 1$$

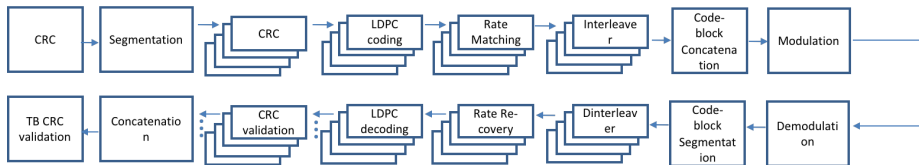
end while

$$r = r + 1$$

end while

²Sec 5.5 of 38.212

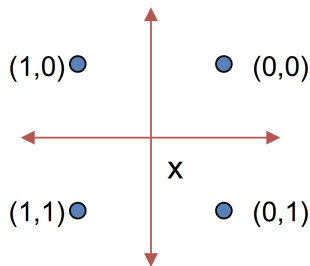
5G transceiver chain till modulation/demodulation³



- 5G NR allows 4/16/64/256-QAM modulation
- Demodulator detects bits from 4/16/64/256-QAM modulated symbols
- LDPC decoder works on the demodulated bits **and not symbols**
 - not practical to design decoder for different modulation schemes

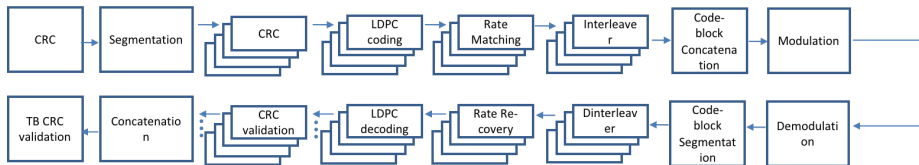
³(Sec 5.1 of 38.211)

Receiver processing - QPSK demodulation

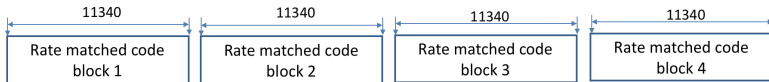


- Apply the nearest distance detection rule
- Threshold the equalized symbols to the nearest symbol
- Demap the symbols into bits

Receiver Processing – code block segmentation

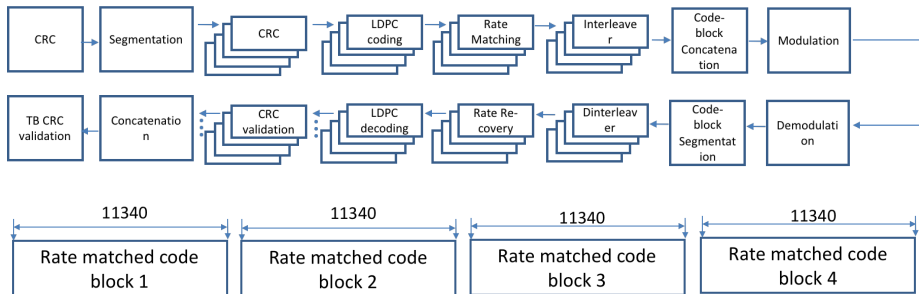


- Code block concatenation (recap)
- Rate matched codeblocks are sequentially concatenated when number of codeblocks $C > 1$



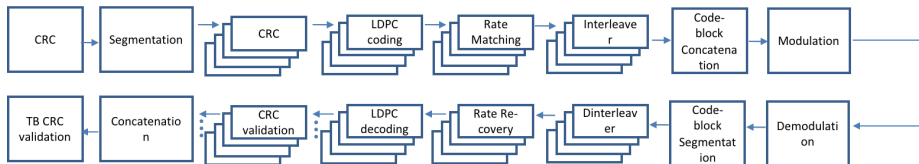
- Length of concatenated output $11340 \times 4 = 45360$

Receiver Processing – code block segmentation

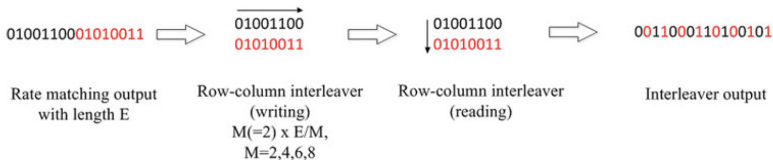


- Code block segmentation output is four code blocks of length 11340 bits
- Total output bits = $11340 \times 4 = 45360$

De-interleaving of code blocks



- Each **rate matched codeblock** is interleaved using row-column interleaver



- De-interleave them by reading them appropriately