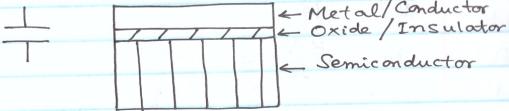


## Field Effect Transistor (FET)

Metal Oxide Semiconductors: MOS

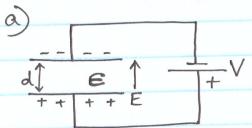


Metal: Gold, aluminum

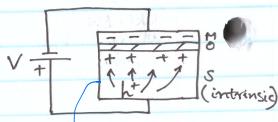
Oxide/Insulator: Silicon dioxide/Silicon nitride

Semiconductor: Silicon/germanium (doped preferably)

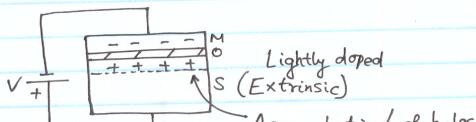
MOS is a special capacitor.



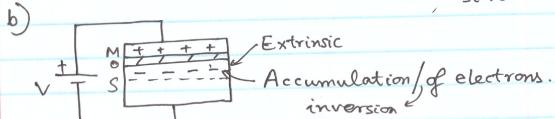
Standard capacitor biasing:



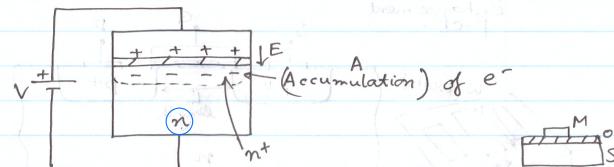
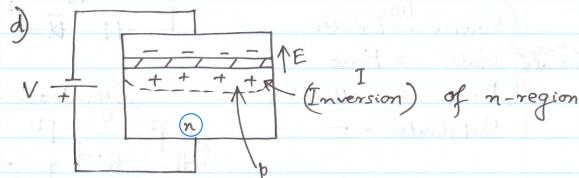
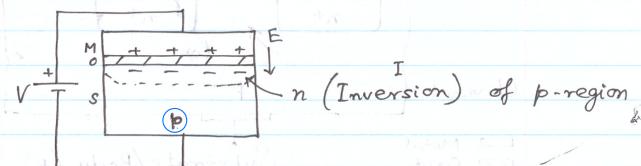
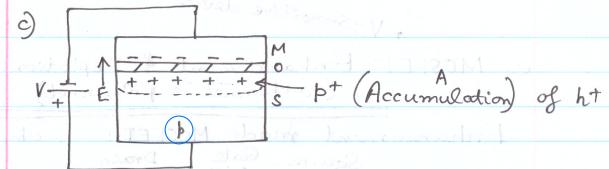
MOS biasing  
p-type semi



Lightly doped (Extrinsic)  
Accumulation of holes  
Inversion



Extrinsic  
Accumulation of electrons  
inversion



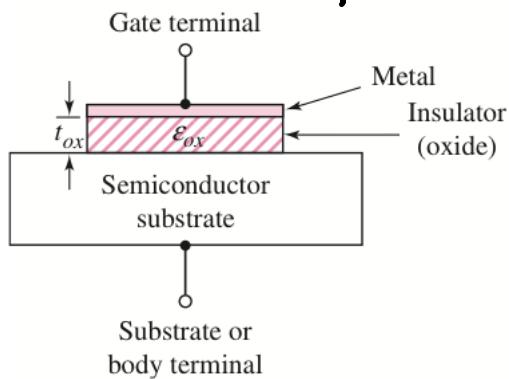
$V \rightarrow E \rightarrow A/I \rightarrow \text{Conductivity}$

E-field

Conductor  
Semiconductor  
Insulator

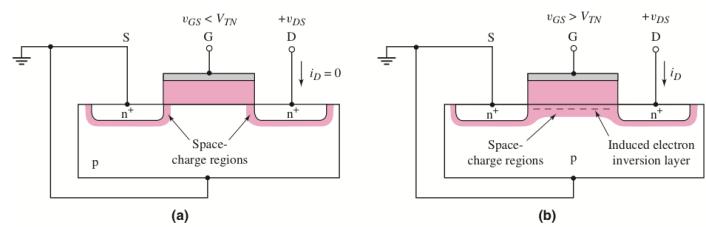
In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current. The phenomenon used to modulate the conductance of a semiconductor, or control the current in a semiconductor, by applying an electric field perpendicular to the surface is called the **field effect**. The basic transistor principle is that the voltage between two terminals controls the current through the third terminal.

## MOS Capacitor



**Figure 3.1** The basic MOS capacitor structure

The term **enhancement mode** means that a voltage must be applied to the gate to create an inversion layer. For the MOS capacitor with a p-type substrate, a positive gate voltage must be applied to create the electron inversion layer; for the MOS capacitor with an n-type substrate, a negative gate voltage must be applied to create the hole inversion layer.



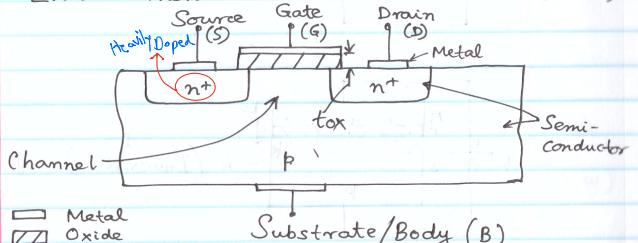
**Figure 3.7** The n-channel enhancement-mode MOSFET (a) with an applied gate voltage  $v_{GS} < V_{TN}$ , and (b) with an applied gate voltage  $v_{GS} > V_{TN}$



V-sensitive device

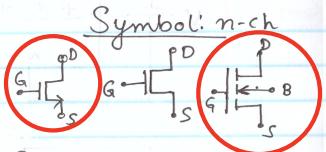
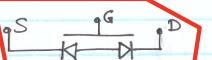
### e. MOSFET: Enhancement & Depletion. (n-channel & p-channel)

Enhancement mode MOSFETs: n-ch. (section)

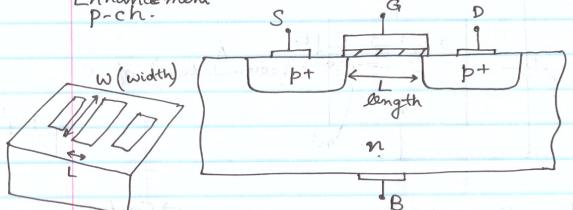


**Basic Terminals**

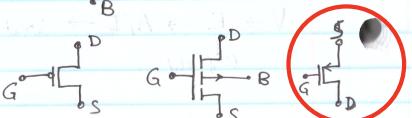
- { Source → Emitter
- Gate → Base
- Drain → Collector
- Substrate → -



Enhancement  
p-ch.

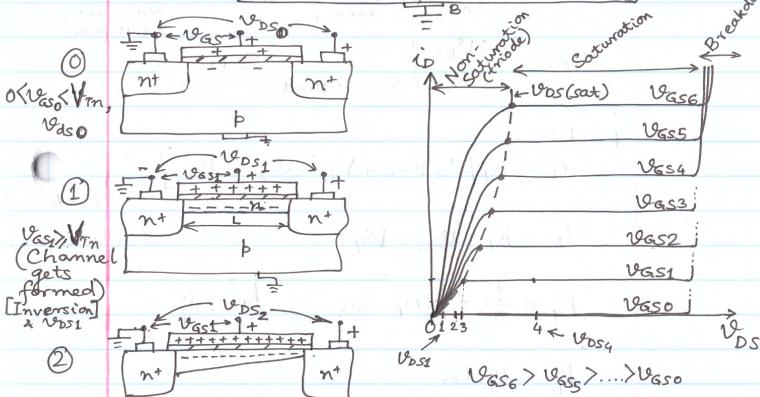
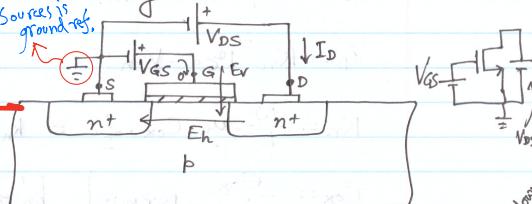


Symbol: p-ch.



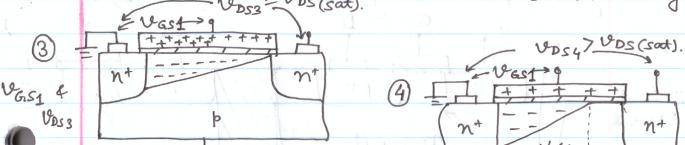
Threshold V (min.  $V_{GS}$  to form a channel)  
 $\mu = \text{constant}$   
 $V_T = \text{constant}$

### f. MOSFET biasing & V-I characteristics



$V_{GS6} > V_{GS5} > \dots > V_{GS0}$   
 $V_{GS1} > V_{GS2} > V_{GS3} > V_{GS4} > V_{GS5} > V_{GS6}$

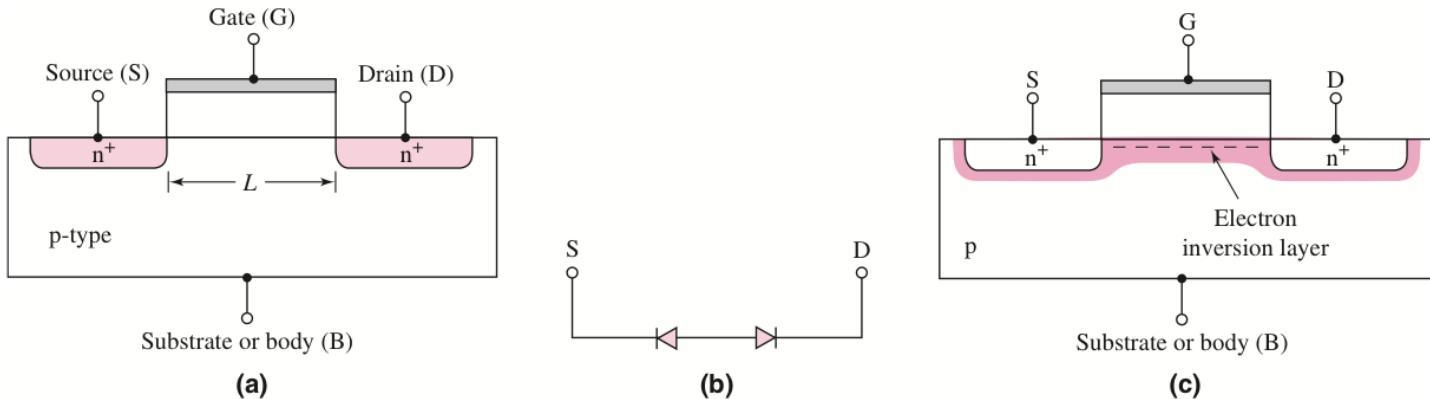
Threshold Voltage



$V_{GS1} & V_{GS4}$   
 $V_{GS1} > V_{GS4}$

## Basic Transistor Operation

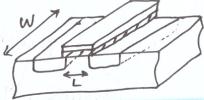
With zero bias applied to the gate, the source and drain terminals are separated by the p-region, as shown in Figure 3.6(a). This is equivalent to two back-to-back diodes, as shown in Figure 3.6(b). The current in this case is essentially zero. If a large enough positive gate voltage is applied, an electron inversion layer is created at the oxide–semiconductor interface and this layer “connects” the n-source to the n-drain,



**Figure 3.6** (a) Cross section of the n-channel MOSFET prior to the formation of an electron inversion layer, (b) equivalent back-to-back diodes between source and drain when the transistor is in cutoff, and (c) cross section after the formation of an electron inversion layer

The source terminal supplies carriers that flow through the channel, and the drain terminal allows the carriers to drain from the channel. For the n-channel MOSFET, electrons flow from the source to the drain with an applied drain-to-source voltage, which means the conventional current enters the drain and leaves the source. The magnitude of the current is a function of the amount of charge in the inversion layer, which in turn is a function of the applied gate voltage. Since the gate terminal is separated from the channel by an oxide or insulator, there is no gate current. Similarly, since the channel and substrate are separated by a space-charge region, there is essentially no current through the substrate.

n-ch:



3D Structure of a MOSFET

$$i_D = K_n \left[ 2(V_{GS} - V_{Tn}) V_{DS} - V_{DS}^2 \right] \quad (\text{Triode/Non-sat. region})$$

$$i_D = K_n (V_{GS} - V_{Tn})^2 \quad (\text{Sat. region})$$

$$K_n = \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot \frac{1}{2} = k_n' \cdot \frac{1}{2} \cdot \frac{W}{L}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \text{ per unit area}$$

$k_n'$  → Transconductance parameter  
 $\mu_n$  → Process conduction parameter

$$r_o = \left. \frac{\Delta V_{DS}}{\Delta i_D} \right|_{V_{GS}=\text{constant}} \cong \infty$$

p-ch:

$$i_D = K_p \left[ 2(V_{SG} + V_{Tp}) V_{SD} - V_{SD}^2 \right] \quad (\text{Triode})$$

$$i_D = K_p (V_{SG} + V_{Tp})^2 \quad (\text{Saturation})$$

$$K_p = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu_p \cdot C_{ox} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

$$k_p' = \mu_p \cdot C_{ox}$$

g. Complementary MOSFET (CMOS):

