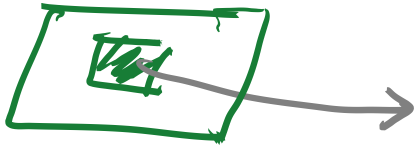
Patterning

What exactly is a Topographically Patterned Surface?

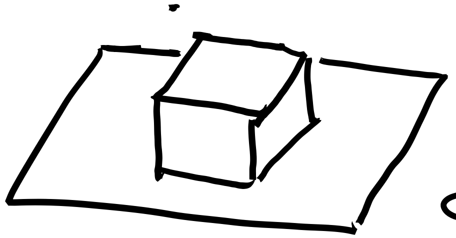
Photolithography

Chemical Patterns

Topographic Patterns



Different Chemical Properties.



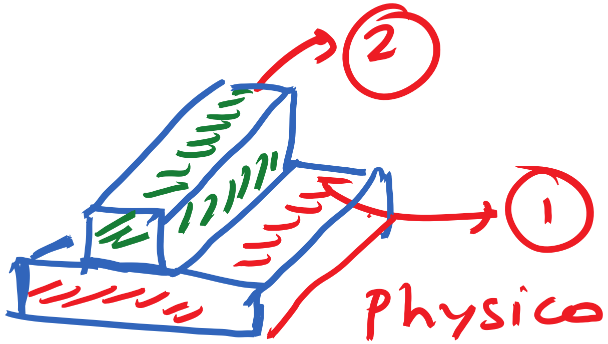
or

(No topographic contrast)

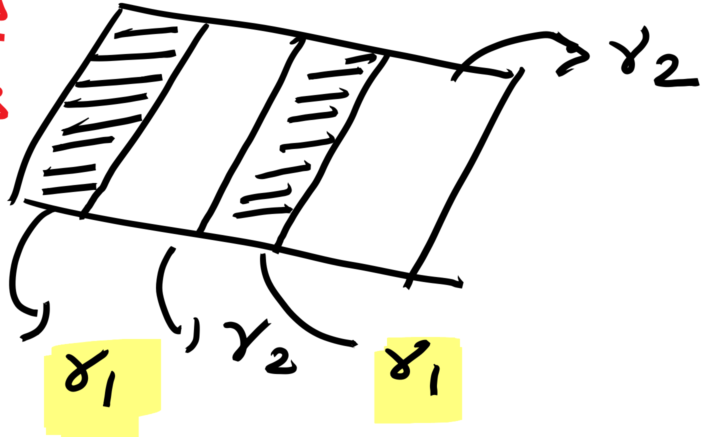
→ Flat

Dewetted Droplets

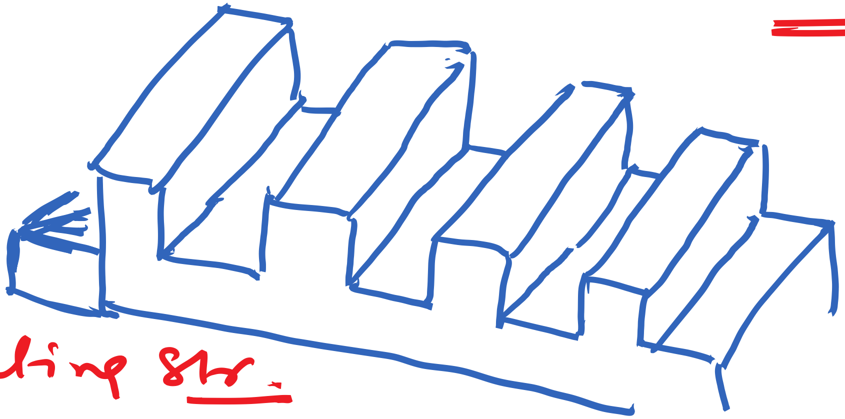
Disordered Patterns



Physico-Chemical patterns



Chemically Homogeneous



Line Grating Str.

Top Down Approaches:: Lithography

- Photolithography
- Soft Lithography
    - Micro contact printing
    - Nano Imprint Lithography group of methods
    - Capillary Force Lithography
    - Micro Molding in Capillaries

(1) How do you make Such Topographic Patterns.

(2) What are the potential applications of Such patterns.

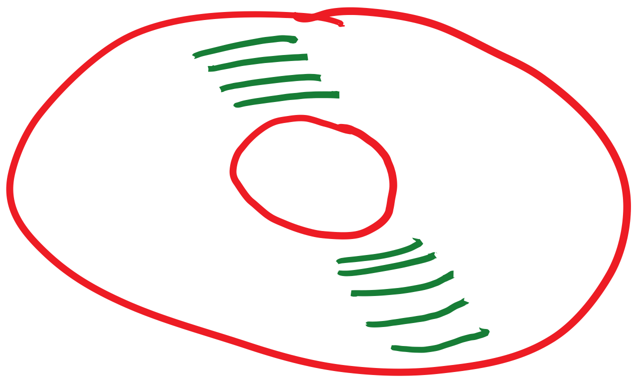
→ Structural Superhydrophobicity

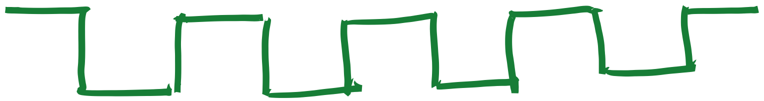
→ Self cleaning Surfaces

→ Diffraction of Light → Rainbow Color on the back side of a CD.

→ Insect Vision / Changing of color like

Back Side of a Compact Disc.

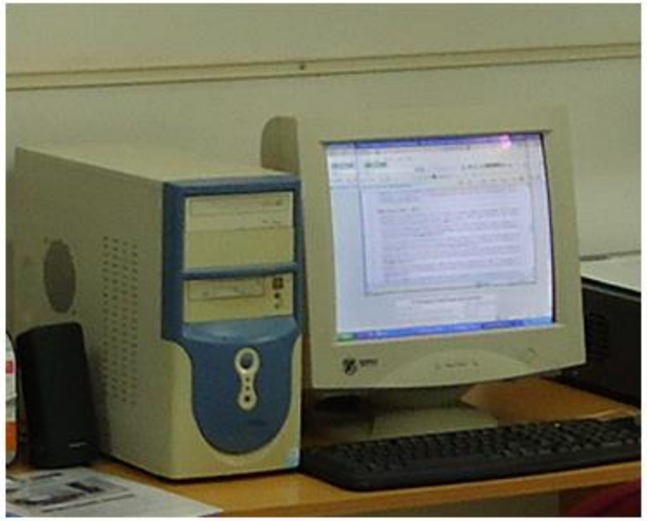




Some Topographic Patterns →
Which have feature size
Comparable to the WL of Visible
Light →

Structural Color

The BIGGEST application area of Patterning



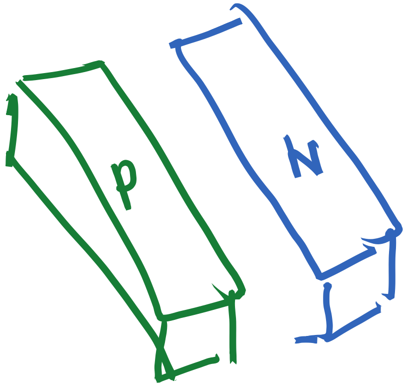
Pentium II processor	Intel Core i9-9980XE
200 M Hz Clock Speed	4.5 GHz speed
500 MBHDD	5 TB HDD
1999	*2019*

To what is this change attributed to?

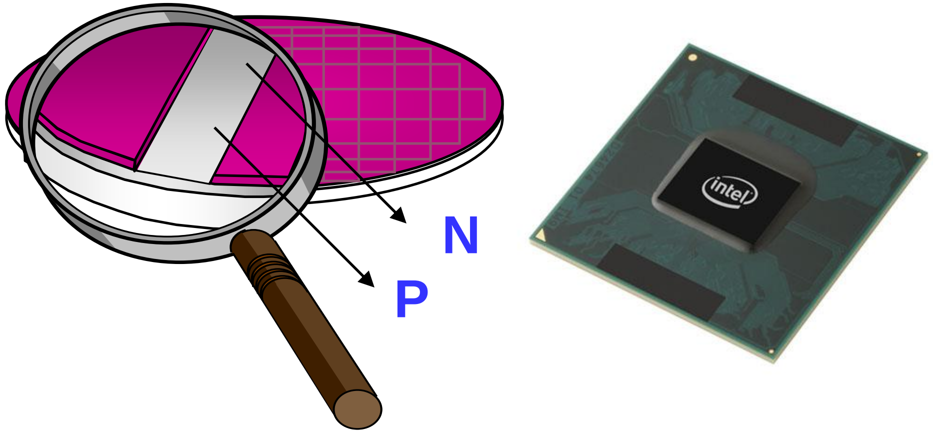
Patterning in Micro Electronics

The micro electronic industry
PC, Laptop, Cell Phone, i-pod ….

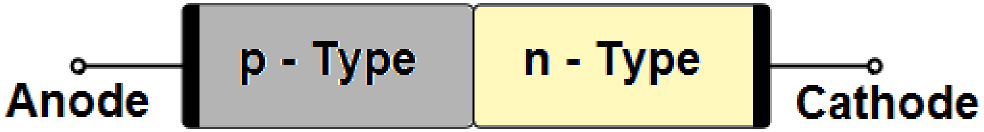
Have you ever thought how every year the speed of the computer processor becomes faster or how the memory sizes increases?



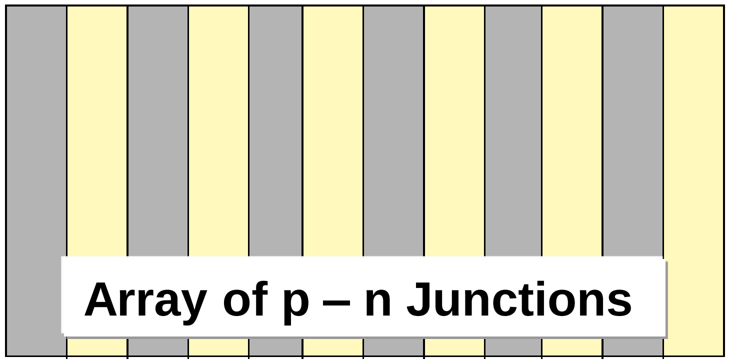
Reality is the tremendous progress in the field of micro electronics industry is attributed to the progress of a specific patterning technique, which is known as photolithography.



The p – n Junction

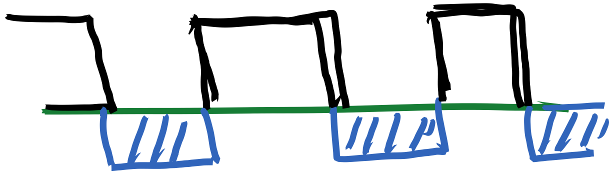


Chemical Pattern



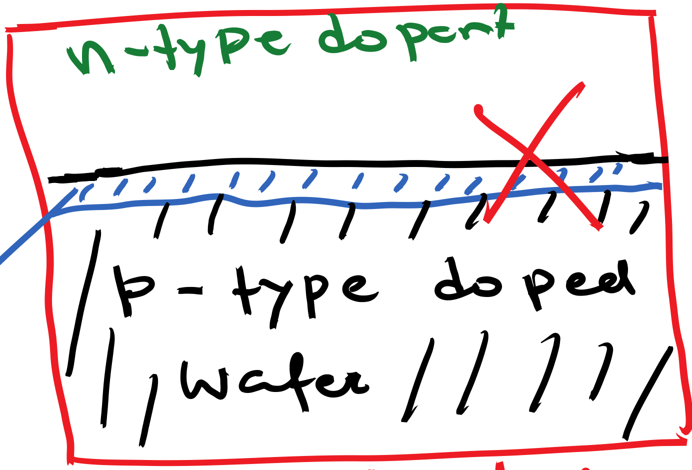
Flat Silicon wafer

Some Pa



Silicon
p – type doped.

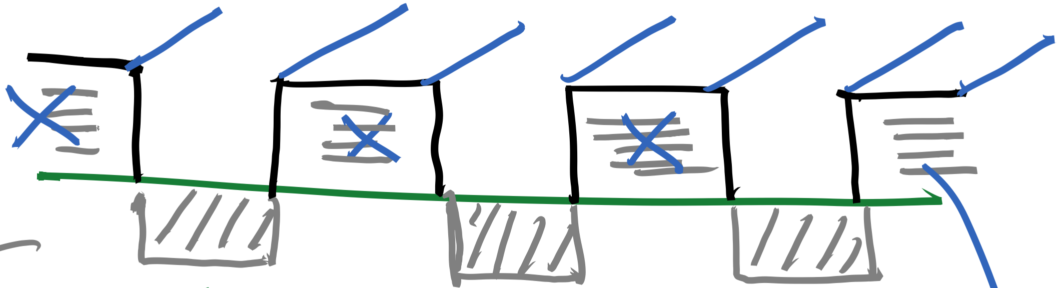
- A p–n junction is formed at the boundary between a p-type and n-type semiconductor.
- If two separate pieces of material were used, this would introduce a grain boundary between the semiconductors which severely inhibits its utility by scattering the electrons and holes.
- so p–n junctions are created in a single crystal of semiconductor by doping
- P–N junctions are elementary "building blocks" of many semiconductor electronic devices such as diodes, transistors, solar cells, and integrated circuits



Rxn Chamber

n - type doping over the entire surface.

n-type doping Chamber



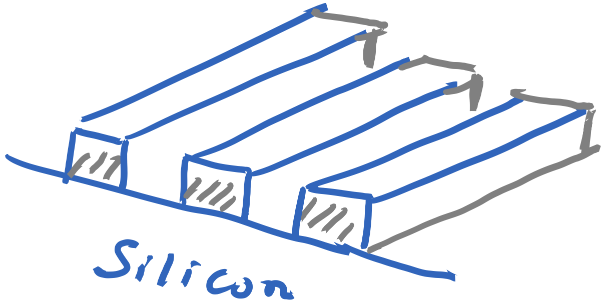
p-type doped

Doping of the exposed areas only.

(1) Some Topographic features on the wafer (of a material that does not react/degrade and prevents diffusion of the dopant)

(2) Place in n-type doping chamber.

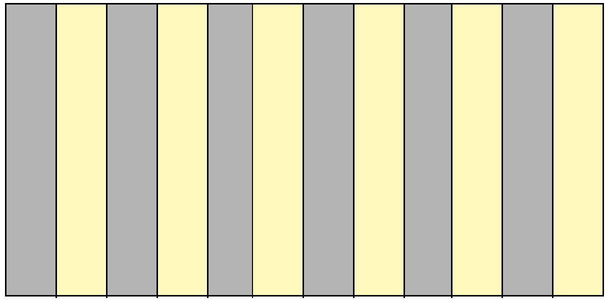
Diffusion Barrier

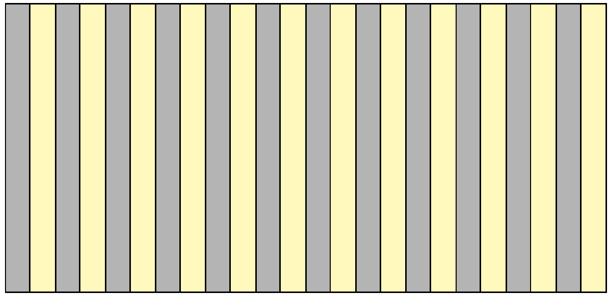


Physico-Chemical Pattern.

30.03.2022

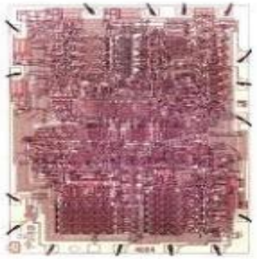
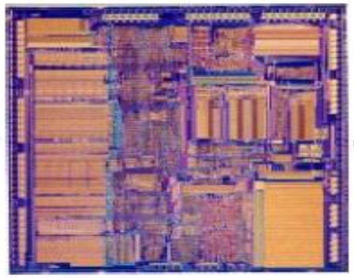
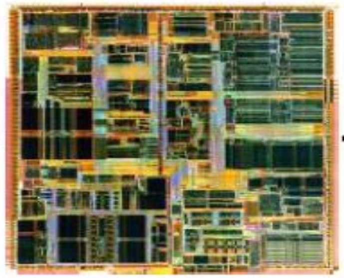
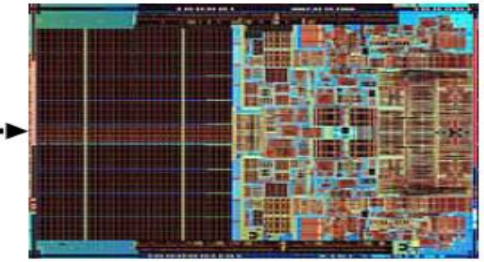
The p – n Junction





- So simply put if your lines become narrower, you can have more number of p – n junctions on a chip whose physical dimensions are the same.
- These lines are created by the method of Photolithography.
- For example while a Pentium II processor had lines which are 300 nm wide, the lines are about 32 nm wide in a i-core 5 processor.
- Similarly progress in patterning is also responsible for higher capacity memories.

Intel Microprocessors – Brief History

1971	1985	1997	2006
Intel 4004 μP	Intel 386 μP	Intel PII μP	Intel Core 2 Duo
2,300 transistors	275K transistors	7.5 M-transistor	291 M-transistor
108 KHz	33 MHz	300 MHz	2.4 GHz
10 μm linewidth	**1.5 μm**	**0.25 μm**	**0.065 μm**

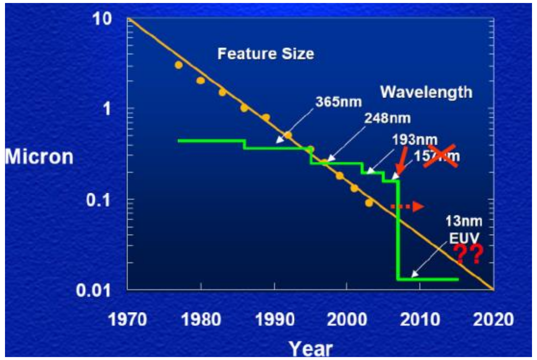
Historically, advances in microelectronics have been due to ability to making smaller and denser patterns.

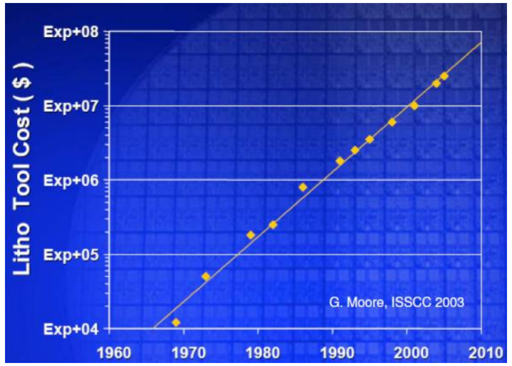
→Photolithography has been the workhorse of the semiconductor industry.

→ Lithography is key technology pacing Moore's Law

4

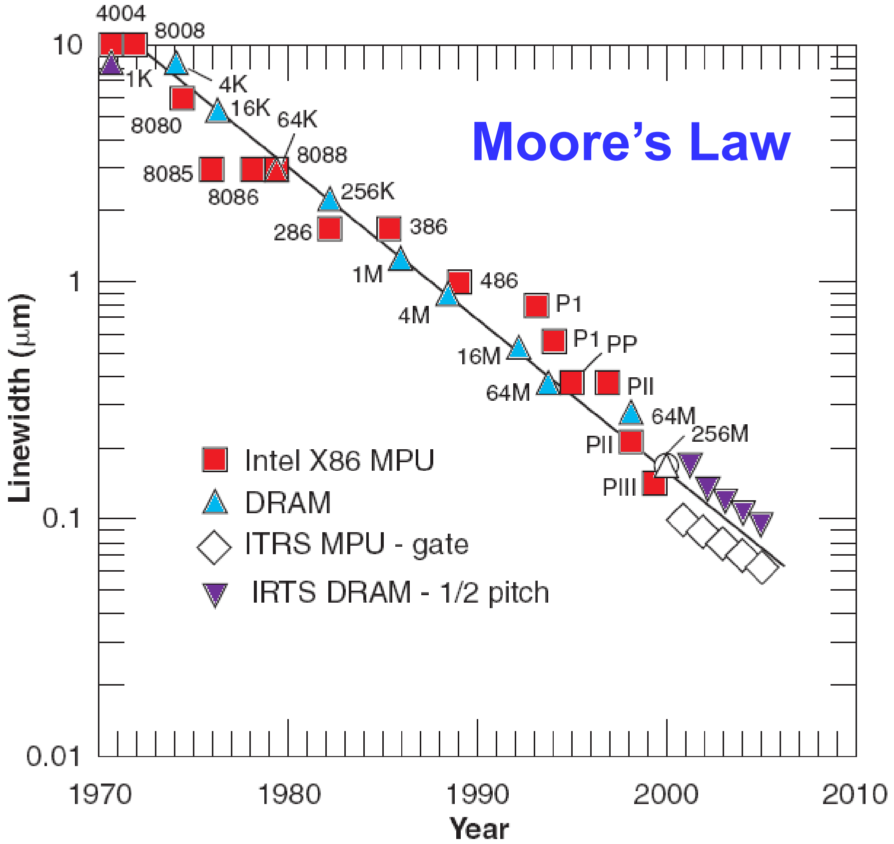


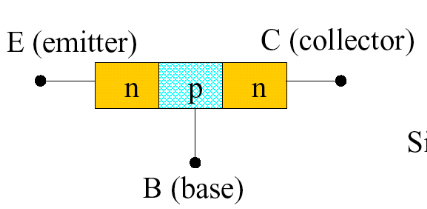


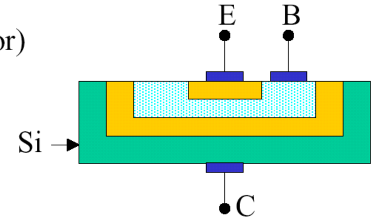


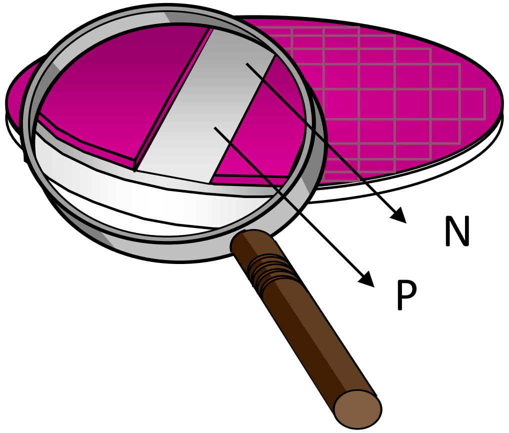
Photolithography

- Innovations in the integrated circuit industry is the main motive force for the tremendous advance in the field of surface patterning.
    - *Transistor invented in 1947.*
    - *The first Integrated Circuit built in 1960. The line width in integrated circuits was 5 μm.*
    - *First IBM PC (1981), 16 K Byte memory, 4.77 MHz clock speed.*
    - *Line widths of 350 nm was achieved, when 40 GB D-RAM was discovered in 1997.*
    - *Present state ~ 40 nm.*
- Narrower is the line size, closer is the packing, better is the performance of the circuit!









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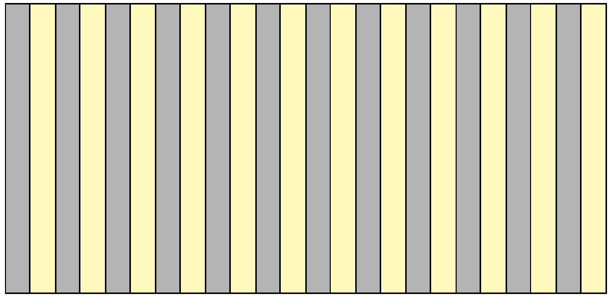
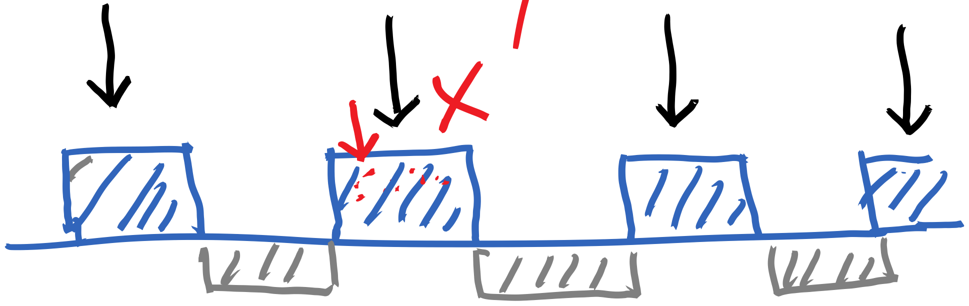
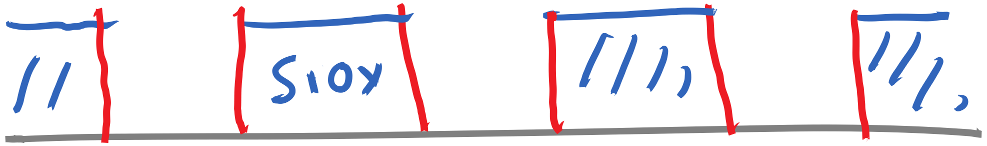


Dopants won't diffuse →

Doping Reactants to reach the surface (Silicon Oxide)



n or p doped wafer with which you start

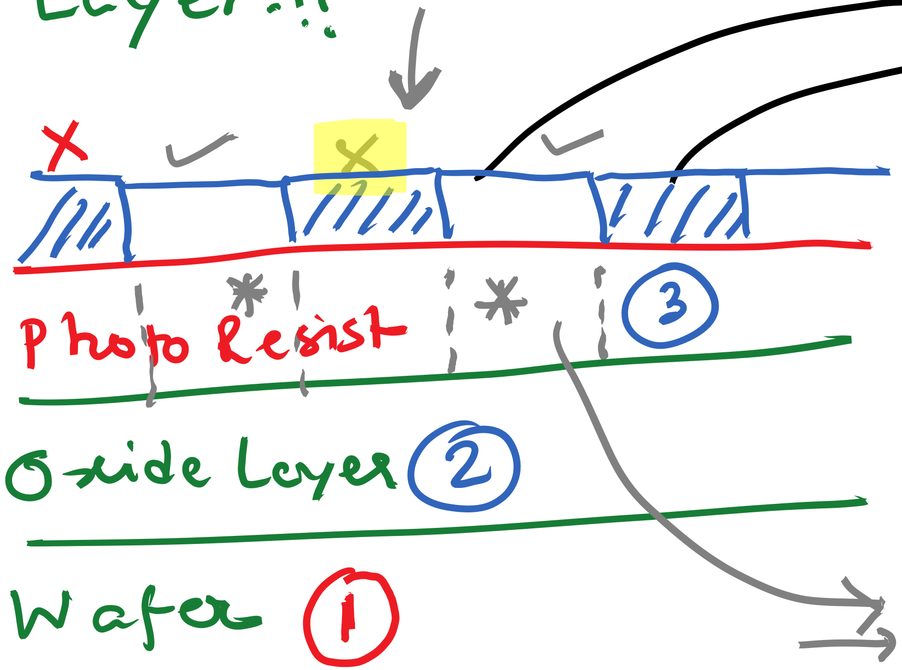


SiOx

(1) First take oxide layer

(2) Then scrape out some parts

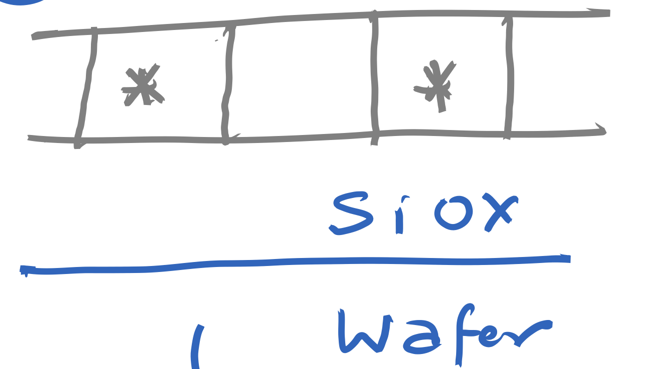
The patterns cannot be directly made in the oxide Layer.!!



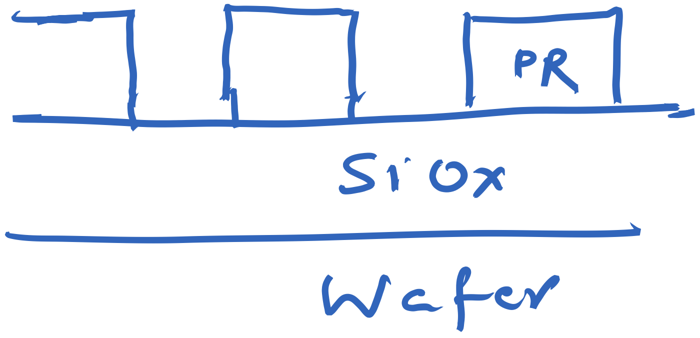
Transparent.
opaque

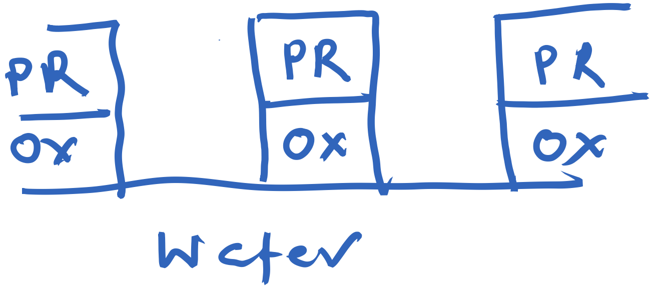
Spl. Polymer
(Photo Resist)

1. Wafer
2. Grow oxide Layer
3. Spin coat PR.
4. Place-Mask + Expose

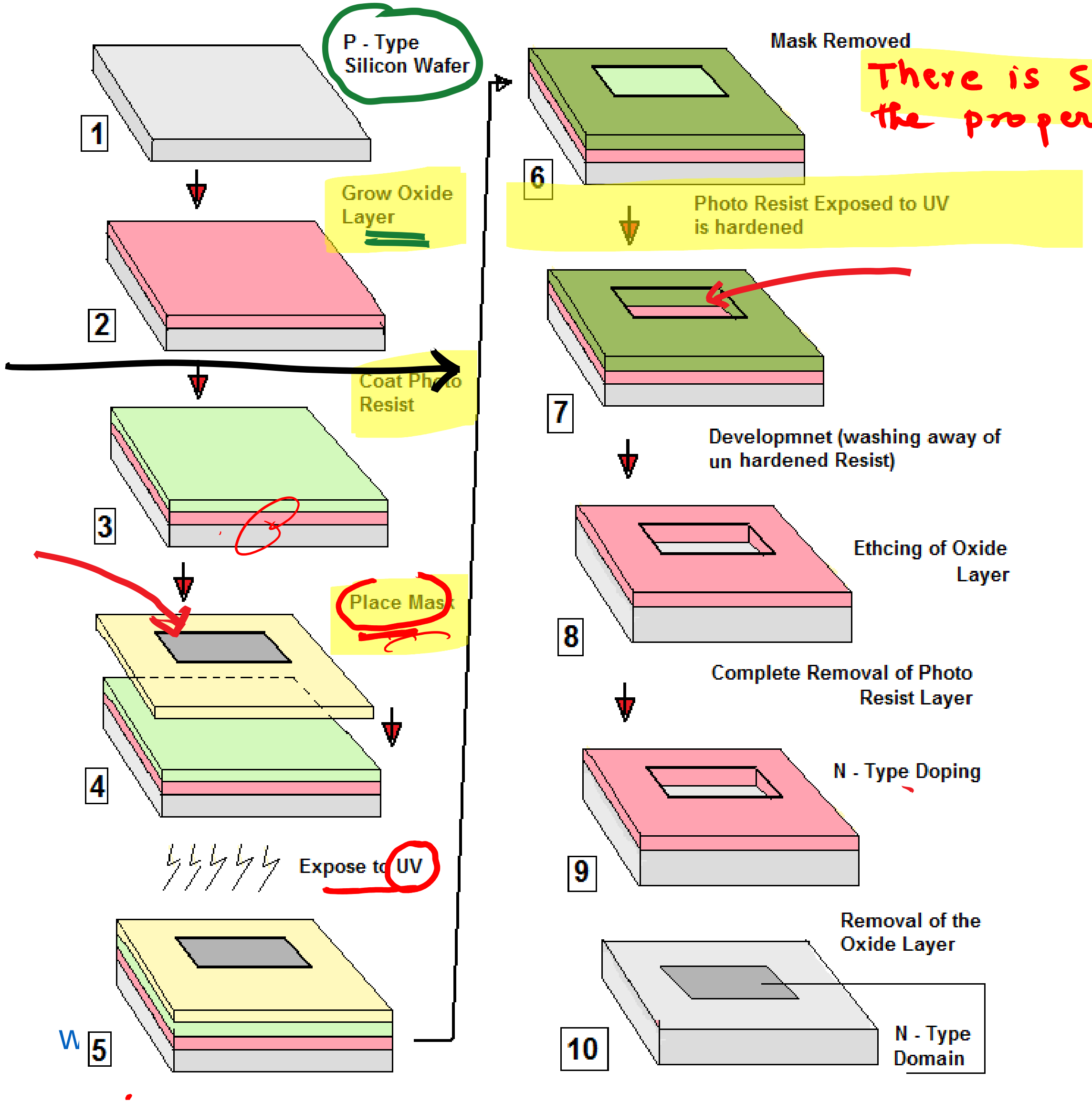


Upon Exposure these Zones will undergo some change in property.





Photolithography Process: Basic Steps



There is some change in the property of the PR Layer between areas that are Exposed or Not!

- Silicon Wafer
- Photo resist
- Spin Coating
- Mask
- Optical Source
- Mask Aligner
- Developer
- Etching

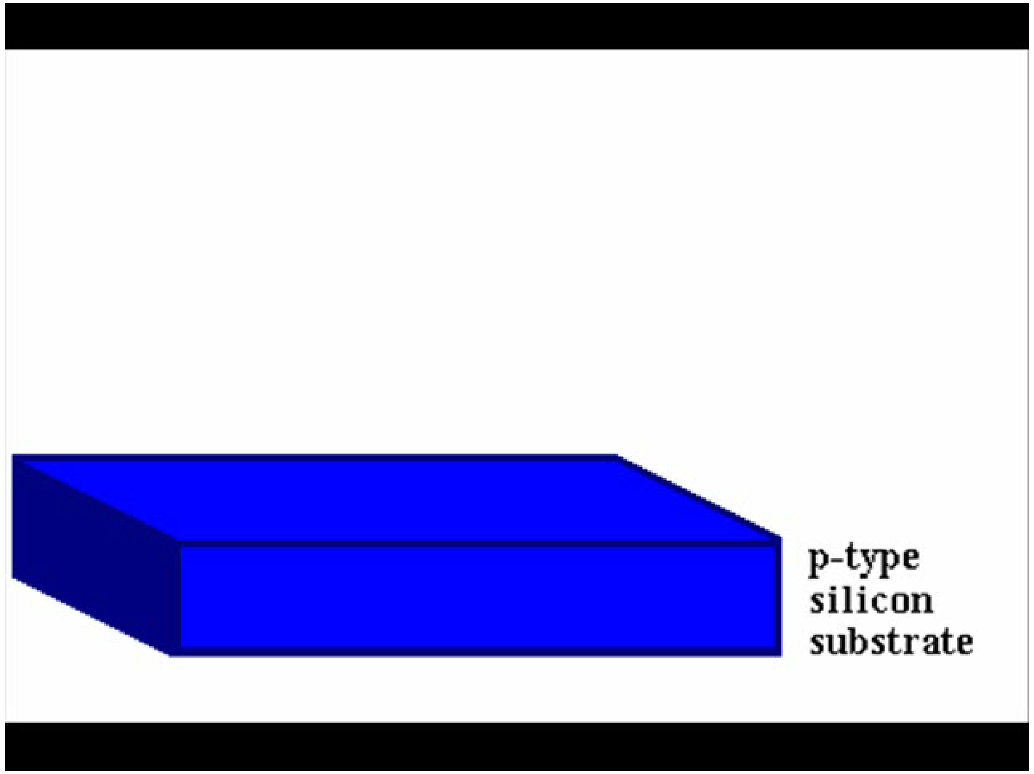
After step 2

Ox

Silicon wafer

Photolithography Process: Basic Steps

1. Surface Preparation
2. Deposition of the Barrier Layer (SiO_2)
3. Photoresist Application
4. Soft Bake
5. Mask Align
6. Expose to UV
7. Develop
8. Hard Bake
9. Etch
10. Resist Strip



www.ece.gatech.edu/research/ labs/vc/theory/photolith.html

Wafer Cleaning

In the first step, the wafers are chemically cleaned to remove particulate matter on the surface as well as any types of organic, inorganic and metallic impurities.

Barrier Formation

A Silicon Surface has very high surface energy and oxidizes immediately in contact with air. This oxide layer is very thin. This silica layer itself cannot be used as a barrier. So, SiO_2 layer is grown on the wafer at this stage.

Photo Resist Processing

Photo resist is coated on to the substrate by the method of spin coating, in most cases. It is possible to obtain films which are very thin (down to few nm) and are extremely smooth by the method of spin coating.

Spontaneous: Surface Rxn with oxygen

SiO_x

Silicon

very High γ

$\simeq 430 \frac{mJ}{m^2}$

Native Oxide Layer.

Thk ~ 1.8 nm

Still Grow the Thk of Oxide.

Silicon Wafer

Photo Resist Processing

Consists of Six steps:

1) Dehydration and Priming
2) Resist coating → Spin Coating.
3) Soft baking → Dry PR Layer
4) Exposure
5) Development and
6) Post-development inspection.

* → Despite the presence of Native Oxide Layer — we further need to grow the Ox Layer → To make the Layer thk enough to prevent diffusion.

3 PR Coated

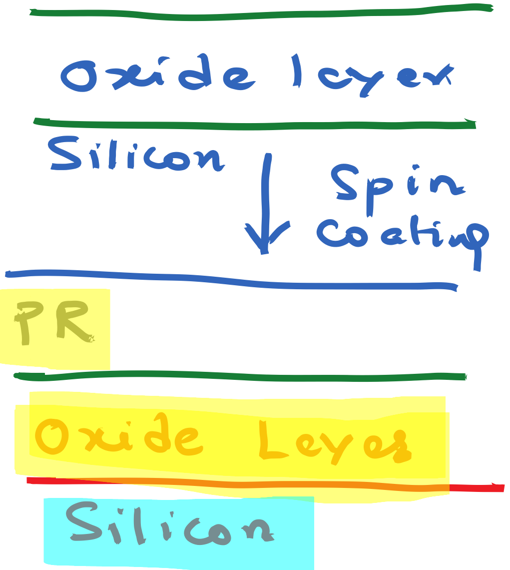


Photo Resist

It's a special class of Photo Sensitive Polymer.

Photoresist layers have two basic functions:

1) precise pattern formation; and

2) protection of the substrate from chemical attack during the etch process.

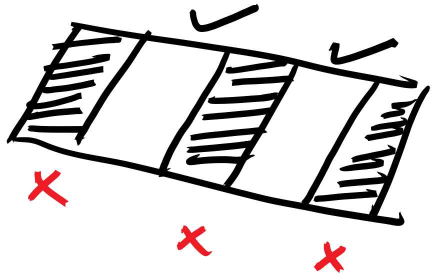
Typical resists consist of three components:

1) The resin, which serves as the binder of the film;

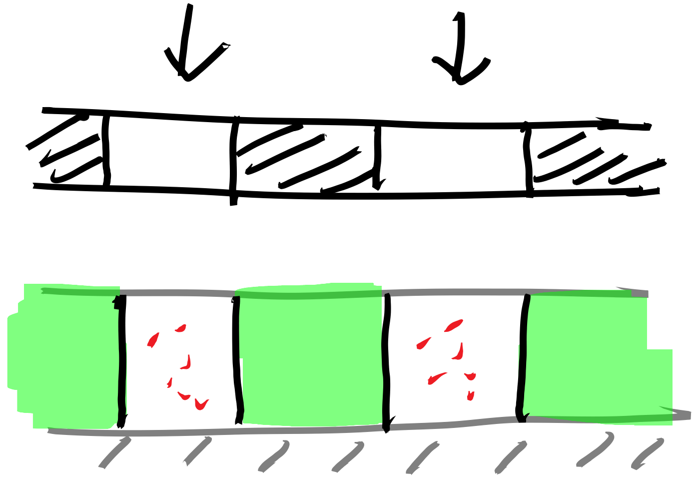
2) The inhibitor or sensitizer, which is the photoactive ingredient; and

3) The solvent, which keeps the resist in liquid state until it is processed.

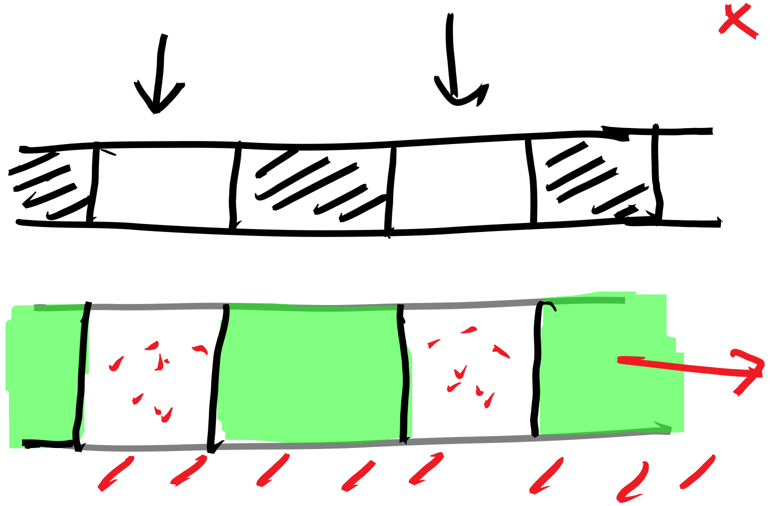
Photo Resist → Different PR Tones.



Mask



The Spotted Areas there is some Change



Green Areas no change ē PR property

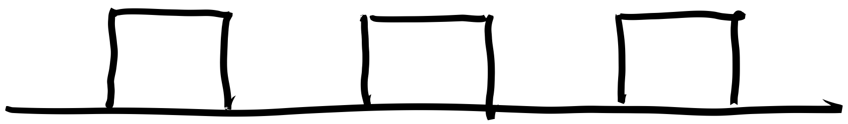
(1) The exposed Areas have got stronger

or

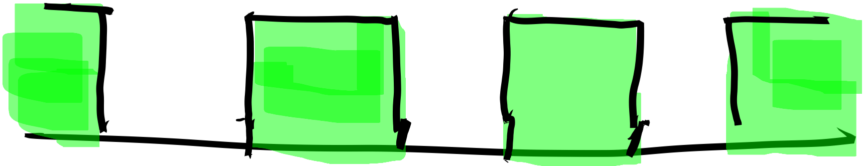
(2) The exposed Areas have got weaker.

Development

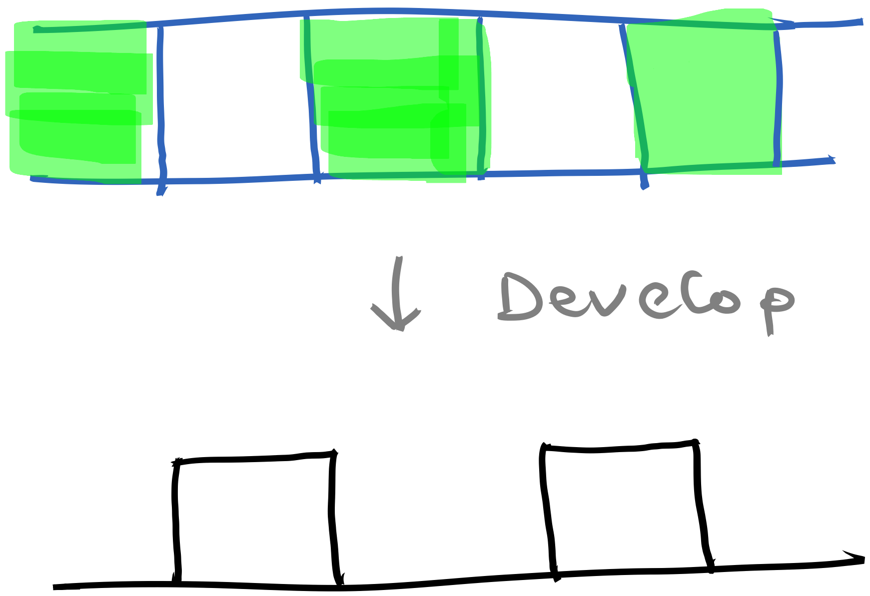
(Exposed PR Layer is now washed with a solvent for the PR)



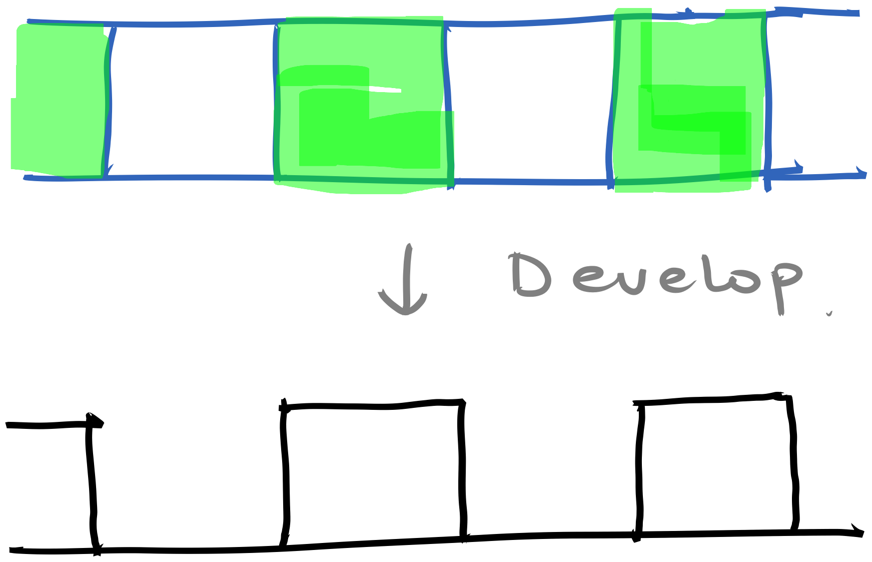
Exposed PR Layer upon Solvent washing →



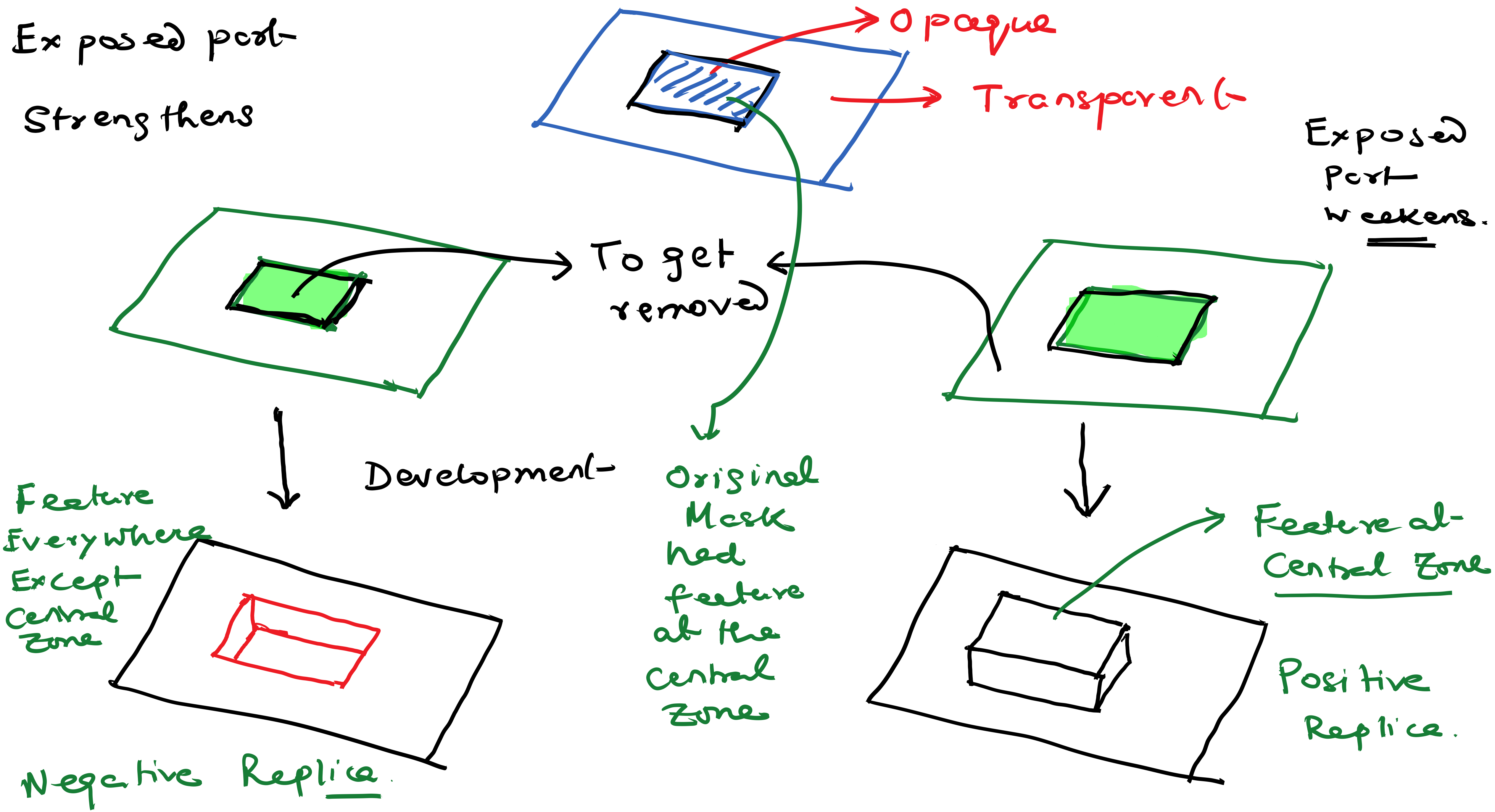
Chain Sescission



This got strengthened



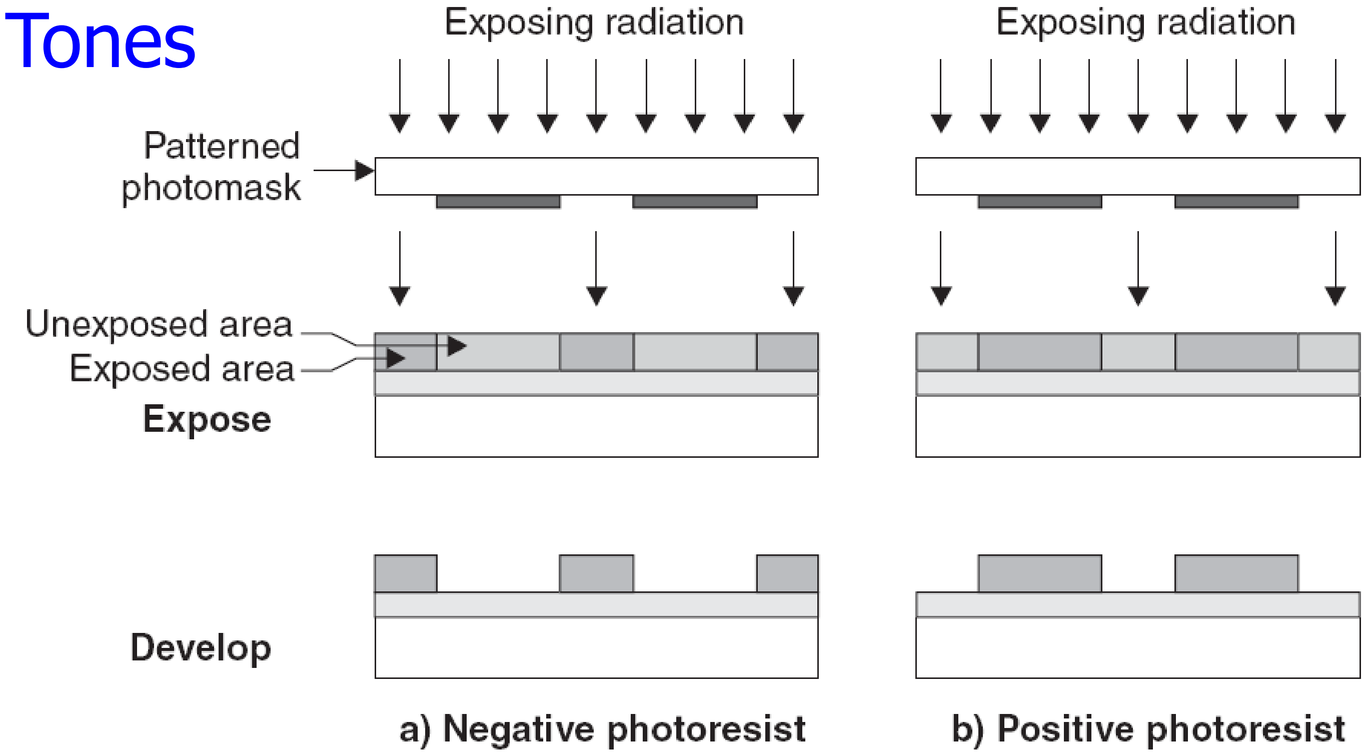
This got weakened


Exposed part
Strengthens
Opaque
Transparent
Exposed
Part
weakens.
To get
removed
Development
Feature
Everywhere
Except
Central
Zone
Original
Mask
had
feature
at the
central
Zone
Feature at
Central Zone
Positive
Replica.
Negative Replica

1. A photo resist that upon Exposure, creates a positive Replica is a Positive PR
(Exposed Parts to weaken)

2. A PR that upon Exposure creates a Negative Replica is a Negative Photo Resist
(Exposed Part to strengthen)

Photo Resist Tones



Characteristic	Positive	Negative
Adhesion to Si	fair	excellent
Relative cost	more	less
Developer Base	aqueous	organic
Minimum	0.5 µm	2 µm
Step Coverage	better	lower
Wet Chemical Resistance	fair	excellent

Present Day most ICs are fabricated based on Positive Photo resists

SU 8 is a very popular Negative Resist

AZ 111 XFS example of a Positive Resist

Modern Resist that work with DUV light (248 nm) have much higher sensitivity

Photo Resist

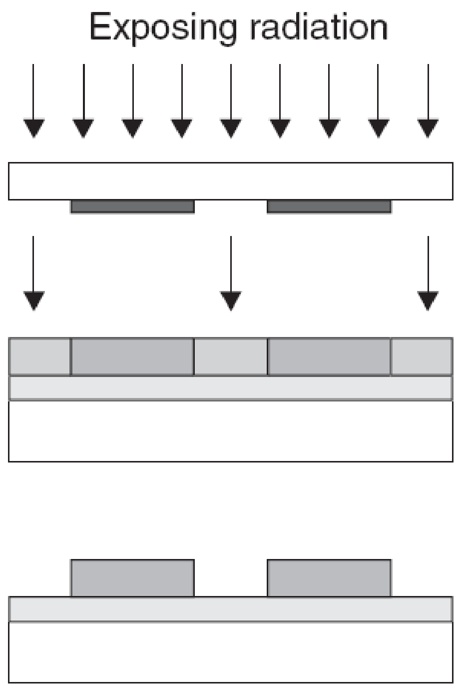
There are two different types of photo resists:

Positive and Negative. (Tones)

A Positive Photo resist when exposed to UV light undergoes structural changes (degradation) and becomes more soluble in the developer.

The exposed resist is then washed away by a developer solution.

An exact copy of the mask pattern is created on the resist layer (positive replica)



b) Positive photoresist

The First Commercial Photoresist was a Negative Photo Resist: Kodak Thin Film Resist

Photo Resist Processing

Consists of Six steps:

1) Dehydration and Priming

2) Resist coating

3) Soft baking

4) Exposure

5) Development and

6) Post-development inspection.

Dehydration and Priming

Before the resist is coated, the wafer must be free of moisture and contaminants, both of which cause a severe problem in resist processing.

Dehydration baking is performed to eliminate any moisture adsorbed on the wafer surfaces, as hydrated substrates lead to adhesion failures.

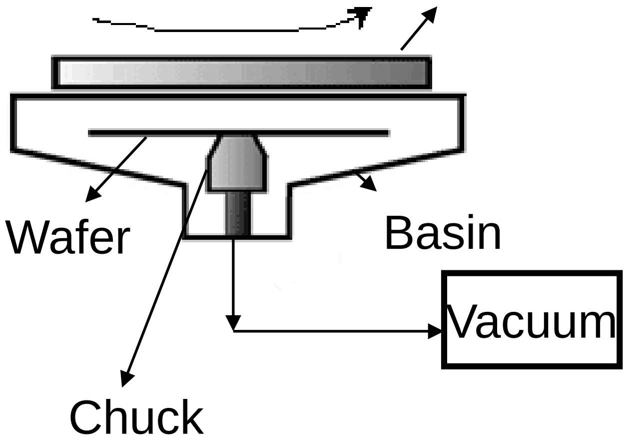
This is usually performed by heating to temperatures between 400 ^{O}C to 800 ^{O}C.

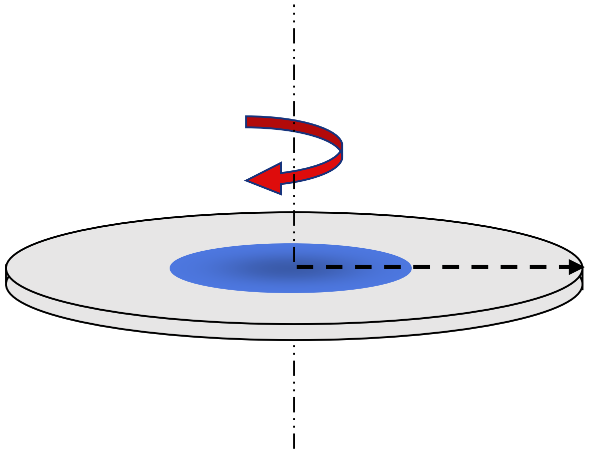
After dehydration baking, the wafer is coated with a pre-resist priming layer which enhances the adhesion properties of the wafer.

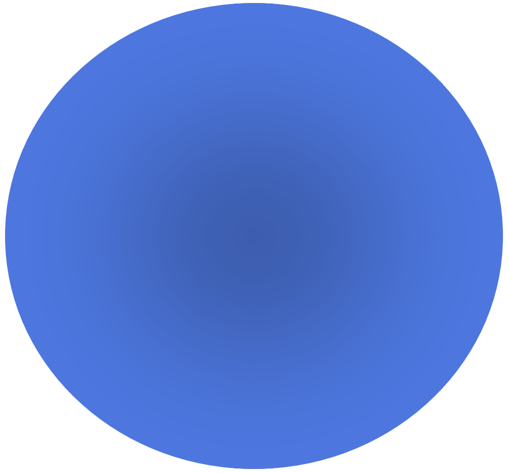
One of the most common primers used for this purpose is hexamethyldisilazane (HMDS). Resist coating must follow as soon as possible after priming

Spin Coating

- A process in which solution is spread evenly over a surface using centripetal force.
- Spin coating will result in a relatively uniform thin film of a specific thickness.
- Spin coating is an important way of creating thin films in the microelectronics industry.







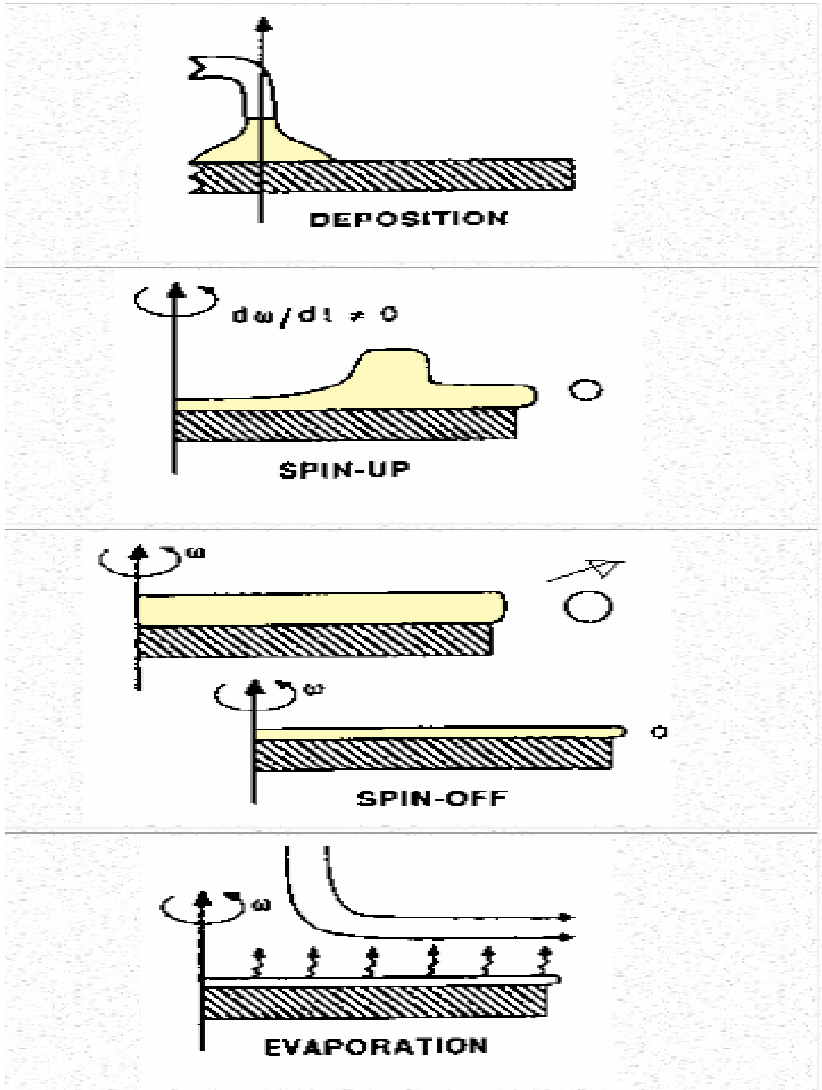
Different Steps of Spin Coating

Dispense the
Polymer Solution

Stage 1:
Meniscus traveling From
Centre to Edge

Stage 2:
Splash Drainage From
the Edges

Stage 3:
Evaporation dominated
Drying



Parameters Affecting Film Thickness in Spin Coating

Spin Speed (RPM)

Dispensed drop volume

Choice of Solvent

Duration of Spinning

Ambient Condition

(which in turn affects the solvent evaporation rate)

Spin Coating is followed by Edge Bead Removal

Soft Baking → To remove the Entrapped Solvent.

After spin coating, the solvent content in the as cast film drops to around 10 – 20%.

The remnant solvent has to be removed before exposure, which is achieved during the stage of Soft Baking.

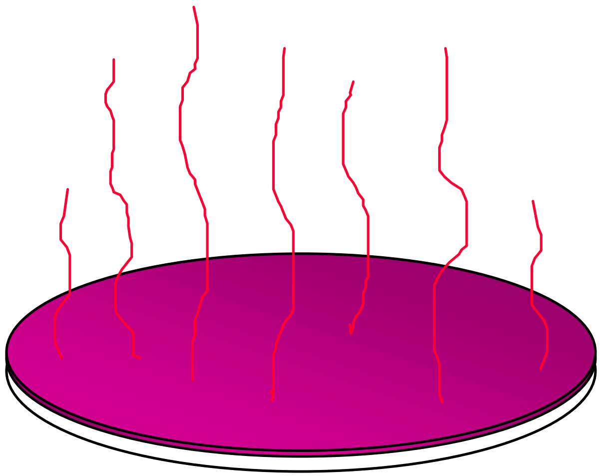
The photoresist coatings become photosensitive, or image-able, only after soft-baking.

When to stop rotation in spin coating?

Spin coating a polymer, within the film matrix, there is ENTANGLEMENT

About 10 – 20% Solvent Remains stuck within the matrix.

- Improves adhesion
- Improves uniformity
- Improves etch resistance
- Improves linewidth control
- Optimizes light absorbance characteristics of photoresist



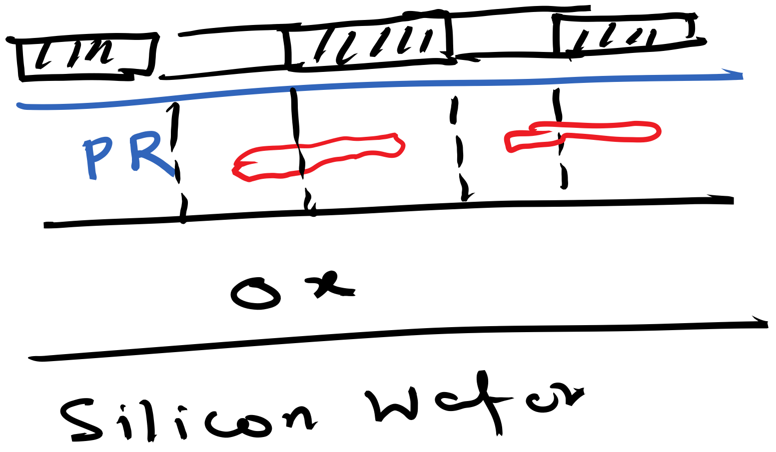
Temperature: 90 – 110 °C

Soft Baking

Over soft-baking will degrade the photosensitivity of resists by either reducing the developer solubility or actually destroying a portion of the sensitizer.

Under soft-baking will prevent light from reaching the sensitizer. Positive resists are incompletely exposed if considerable solvent remains in the coating.

A under soft-baked positive resists is readily attacked by the developer in both exposed and unexposed areas, causing less etching resistance



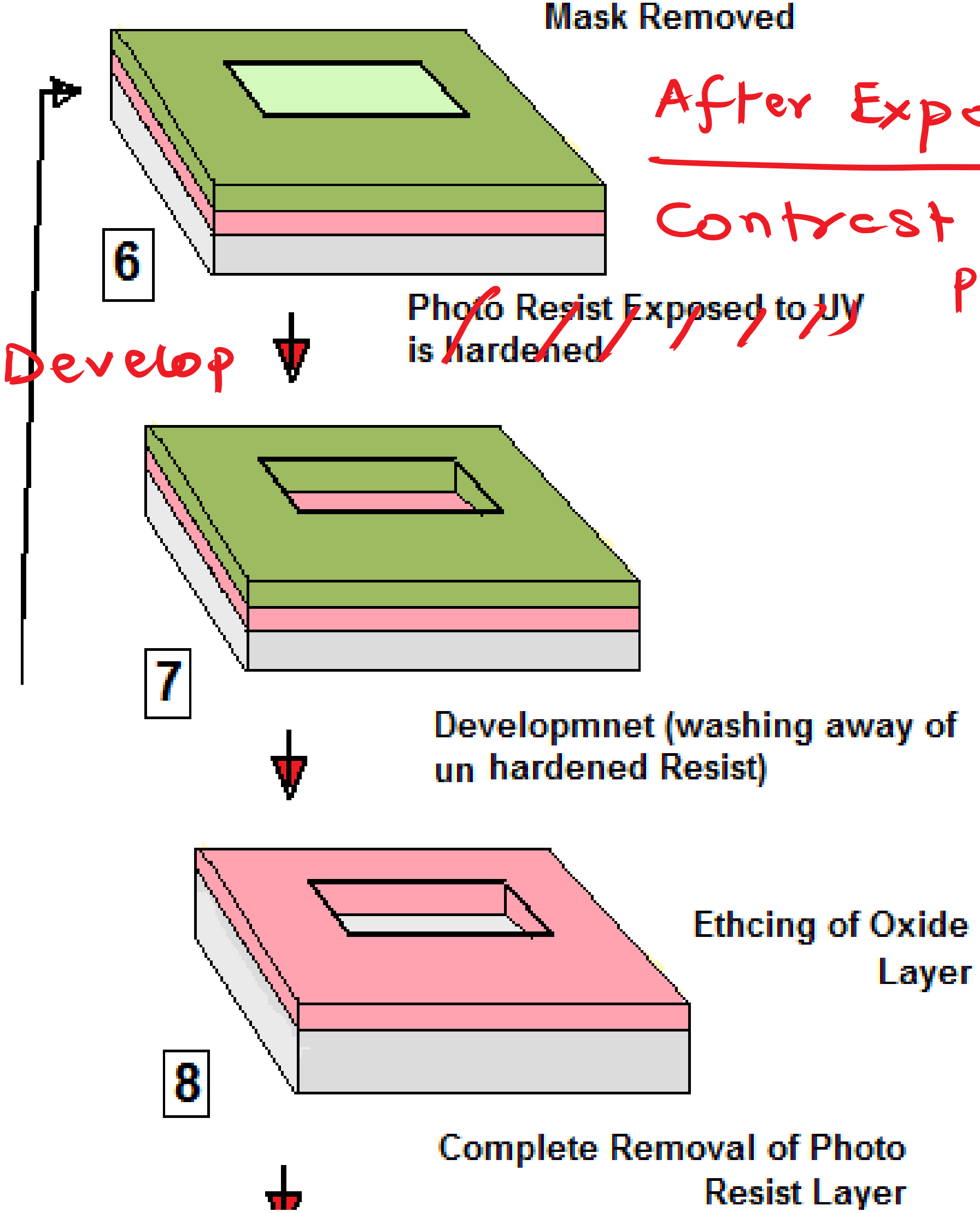
If there are some solvents present in the PR layer → the solvent upon exposure will

(1) Not change its property

(2) Solvent will try to evaporate, Distort the PR layer.

Mandatory to remove the solvent

↳ Soft Baking.

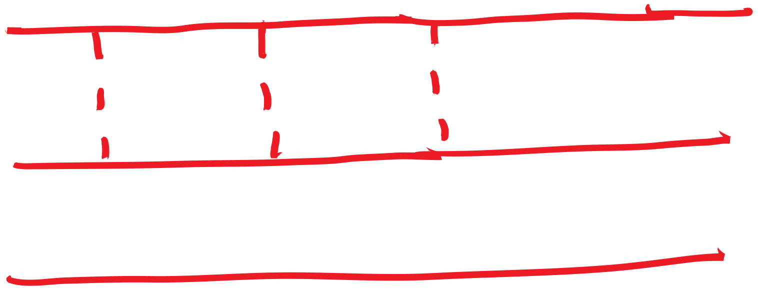


After Exposure

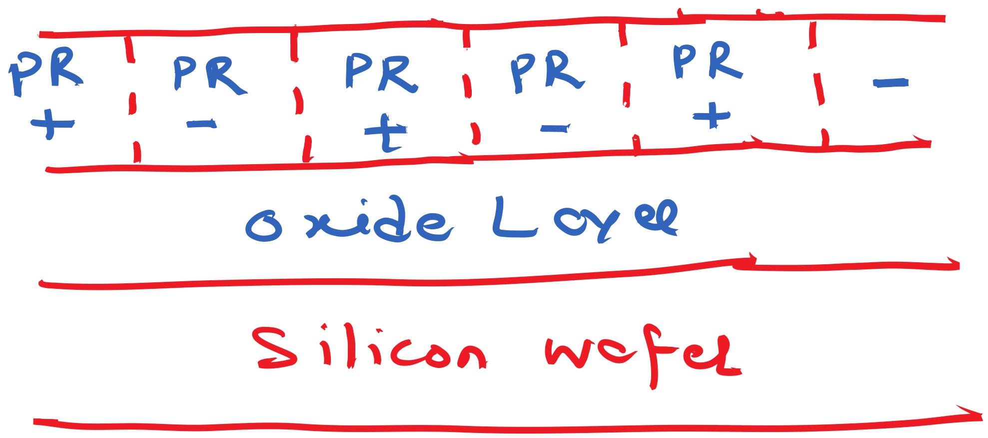
Contrast in the PR property.

Development

↳ Washing the exposed sample to a solvent that would remove the weakened PR part.



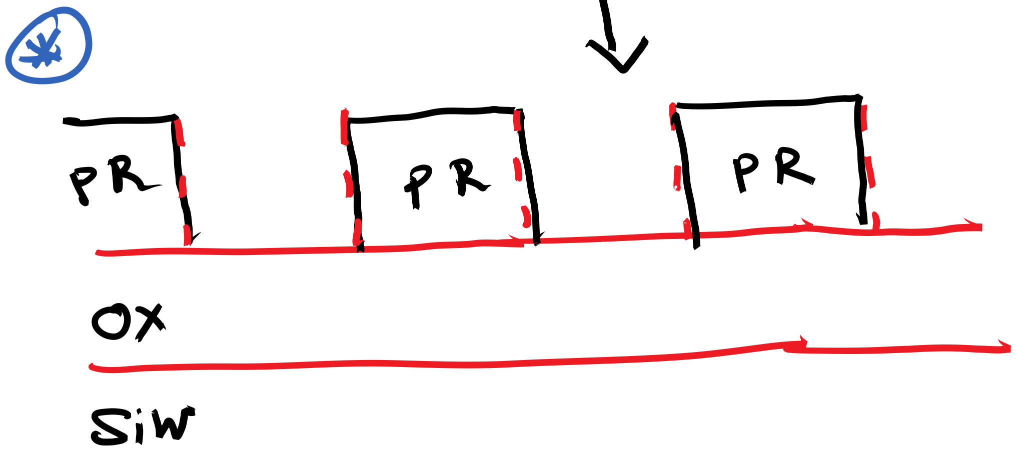
Development: Removal of the weakened PR domains.

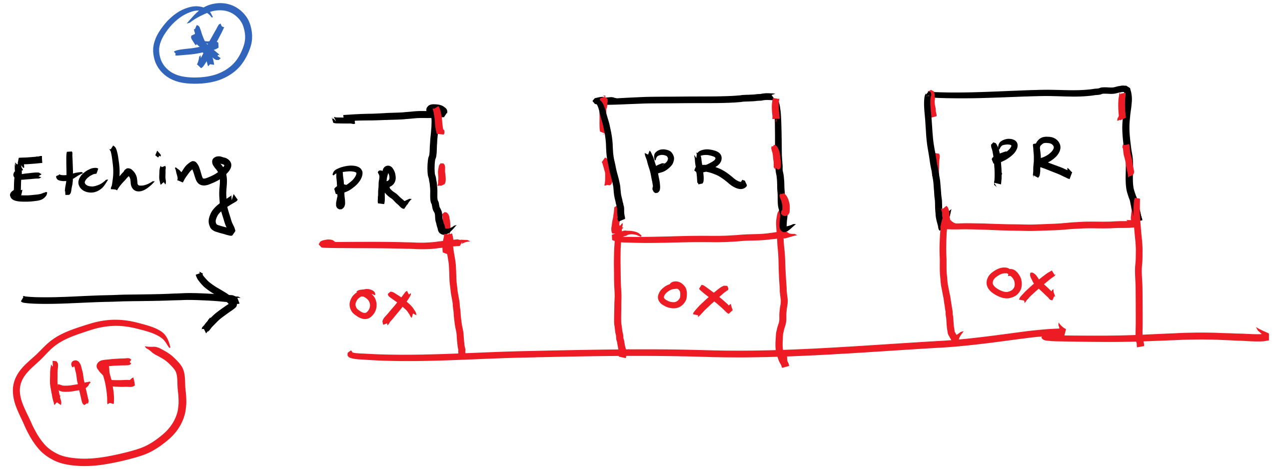


Etching is transfer of the patterns on the PR layer to the oxide layer.

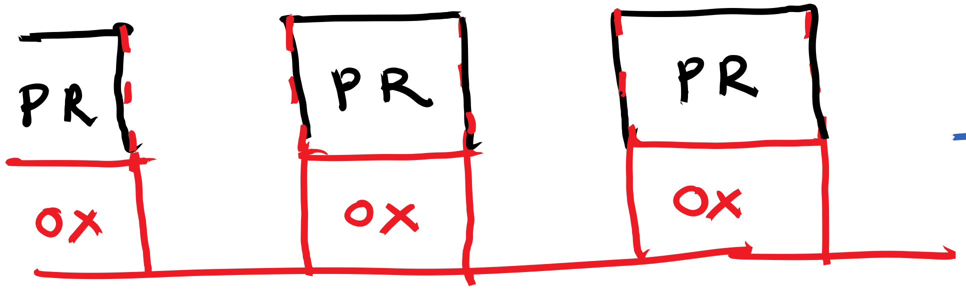
After Exposure

Development





Both after development and etching → we get physico-chemical patterns.



→ Is this sample sent for doping reaction?

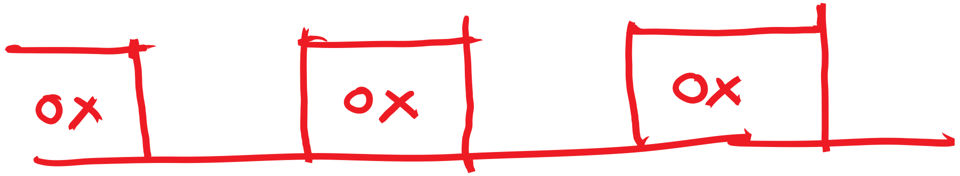
↓

NOT sent for doping as the strengthened PR domains will not be able to withstand the harsh conditions of doping

After etching → There is direct periodic exposure of the silicon wafer

↓

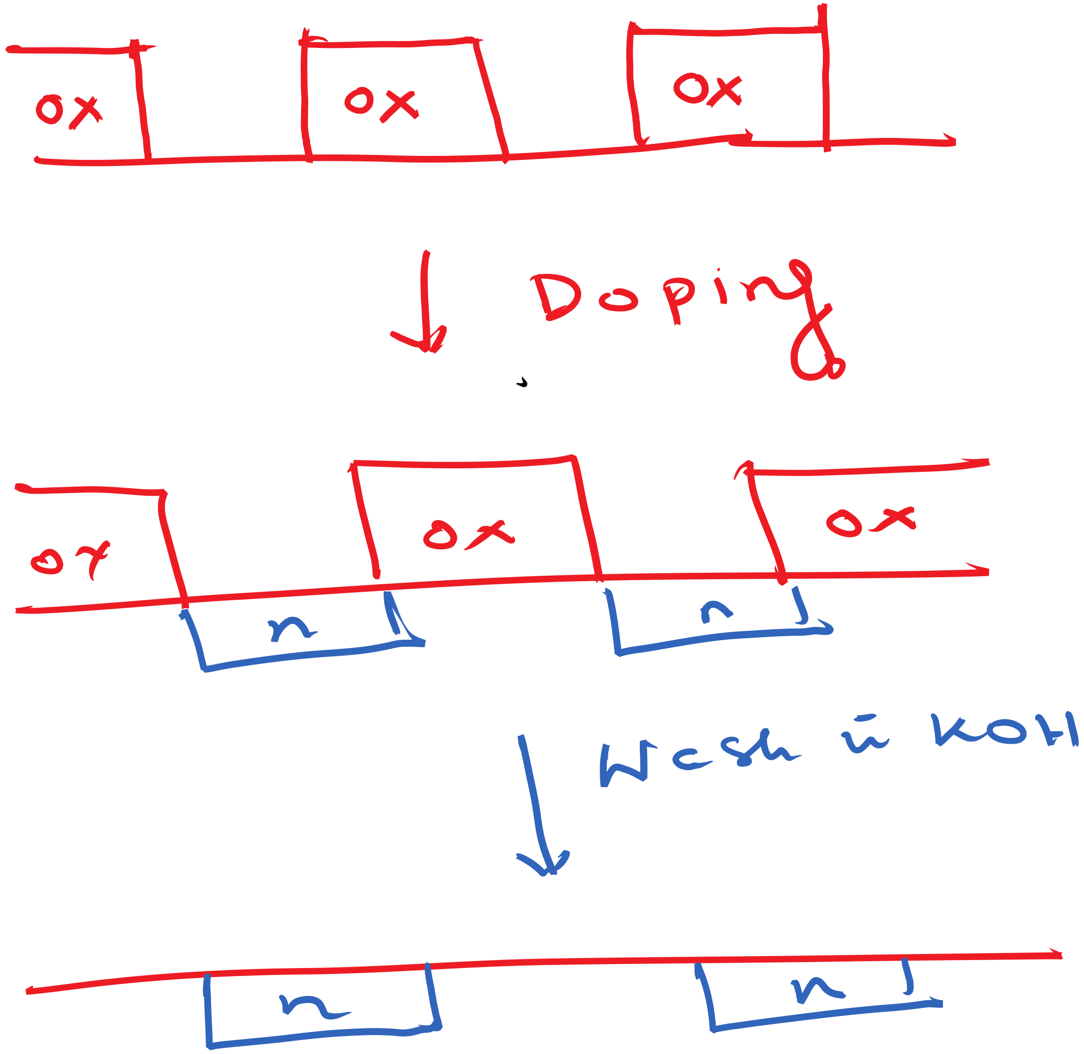
Remove the PR domains



(Patterns are there only in the oxide layer).

How the PR domains are removed? → with washing in Developer.

Stronger Part of PR takes longer to dissolve in developer



To remove any adhering liquid to the sample after each step when the sample comes in contact with a liquid, some heating/annealing/baking is done:-

(1) Dehydration

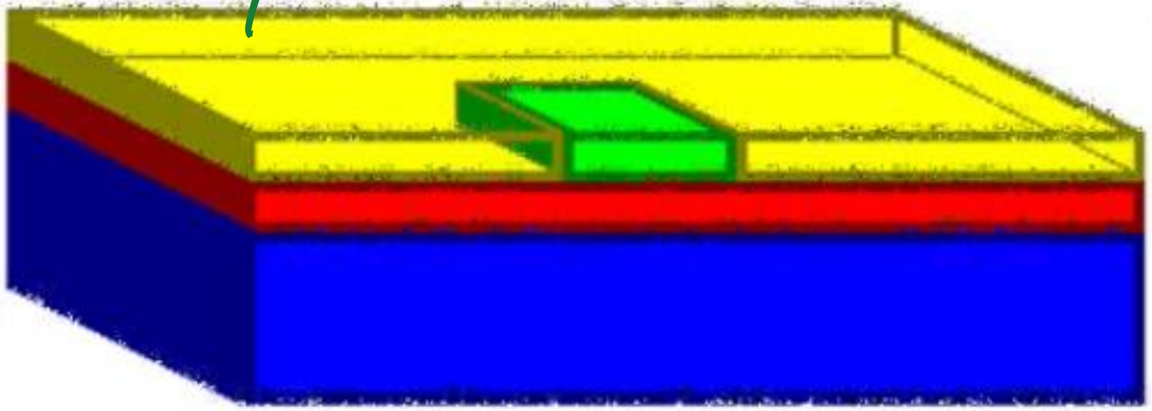
(2) Soft Baking → After spin coating

(3) Post Baking → after development

(4) Hard Baking → After etching + removal of strengthened PR.

upon exposure property has changed.

Not possible to comment if it is a negative resist or a positive resist.



mask lifted

feature to be etched is "imaged" by unhardened photoresist

Photo Mask

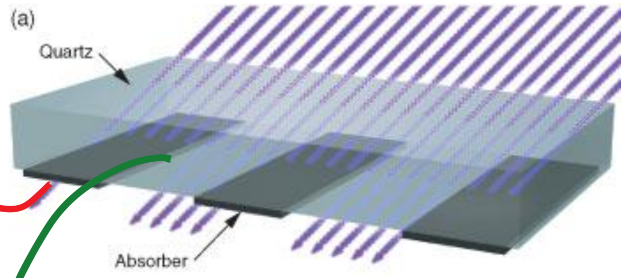
A photomask is an opaque plate with holes or transparencies that allow light to shine through in a defined pattern

• Lithographic photomasks are typically transparent fused silica blanks covered with a pattern defined with a chrome metal absorbing film.

• Use e-beam or laser or x-ray to strip off chromium

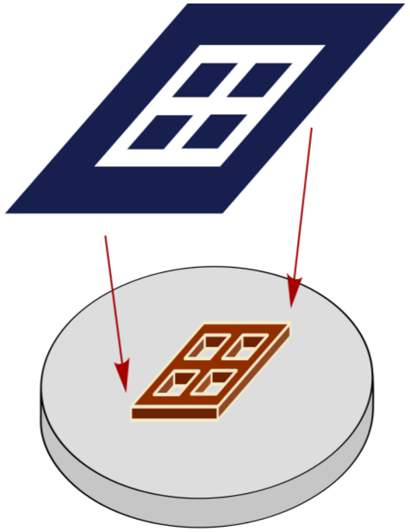
• For Integrated Circuits, multiple masks with multiple pattern are necessary.

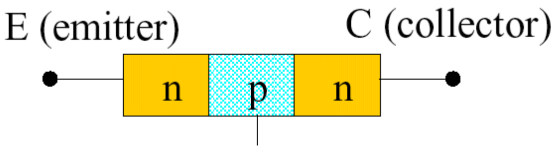
Cr strips

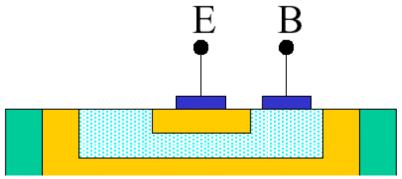


Pure Silica glass (Quartz Glass)

Mask is the primary source of the pattern that gets transferred to the PR Layer during Exposure.







Mask Aligners:

• Almost any microscale device or structure requires more than one photomask step.

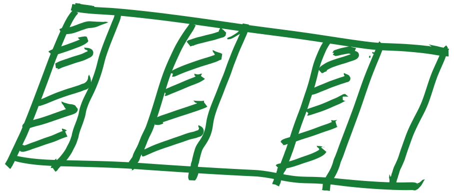
• The job of the aligner is to allow its user to align features on a substrate (wafer) to features on a photomask.

• The production of sophisticated electronic devices may involve ten or more of these alignment steps.

Where does the primary patterning take place?

↓

Mask making.



↓

Lateral dimension and feature geometry is controlled by the mask

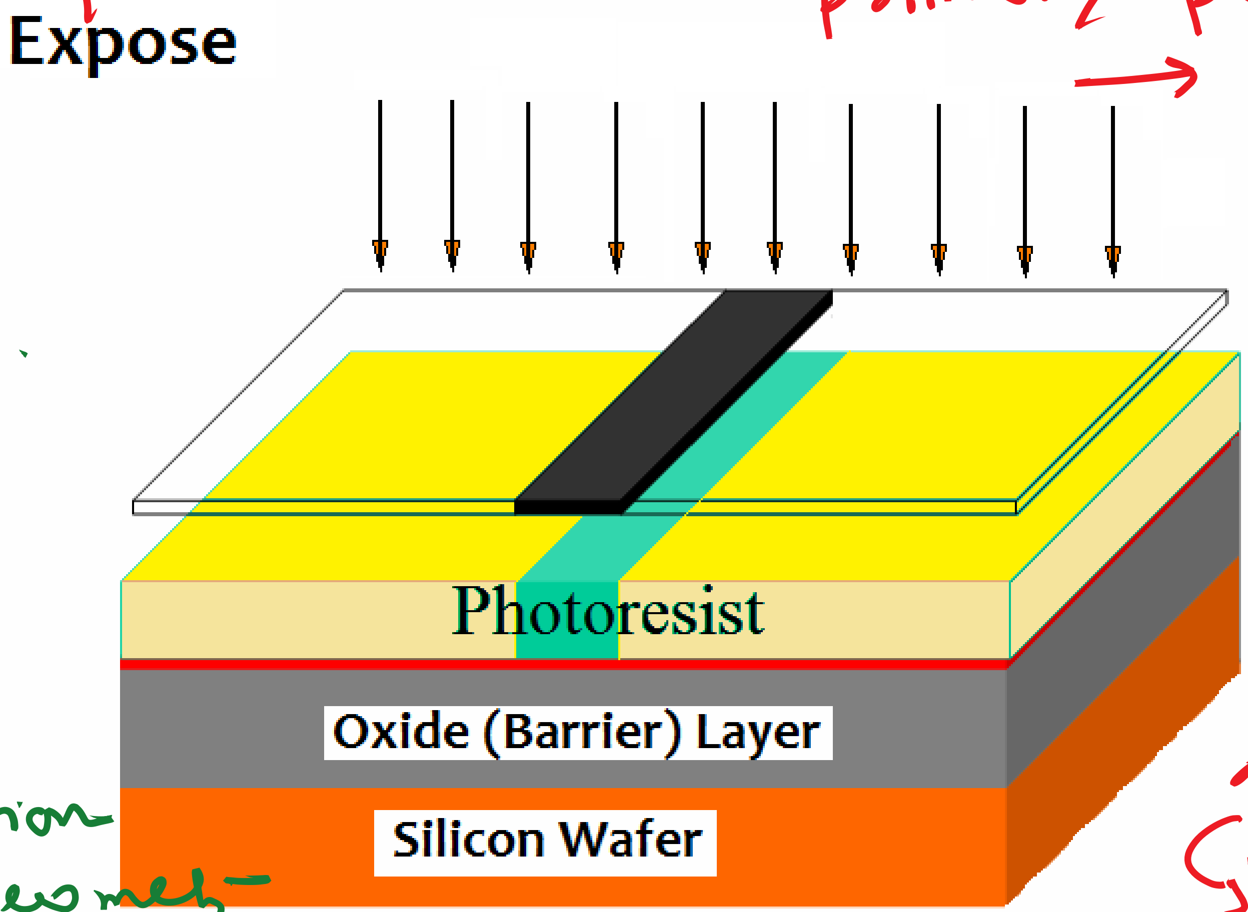
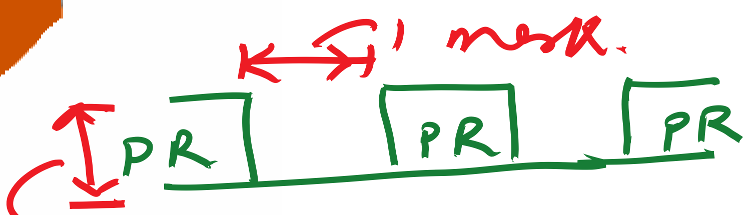


Photo Lithography is NOT a primary patterning technique → Transfers the patterns which are drawn on the mask on to the photo resist layer.

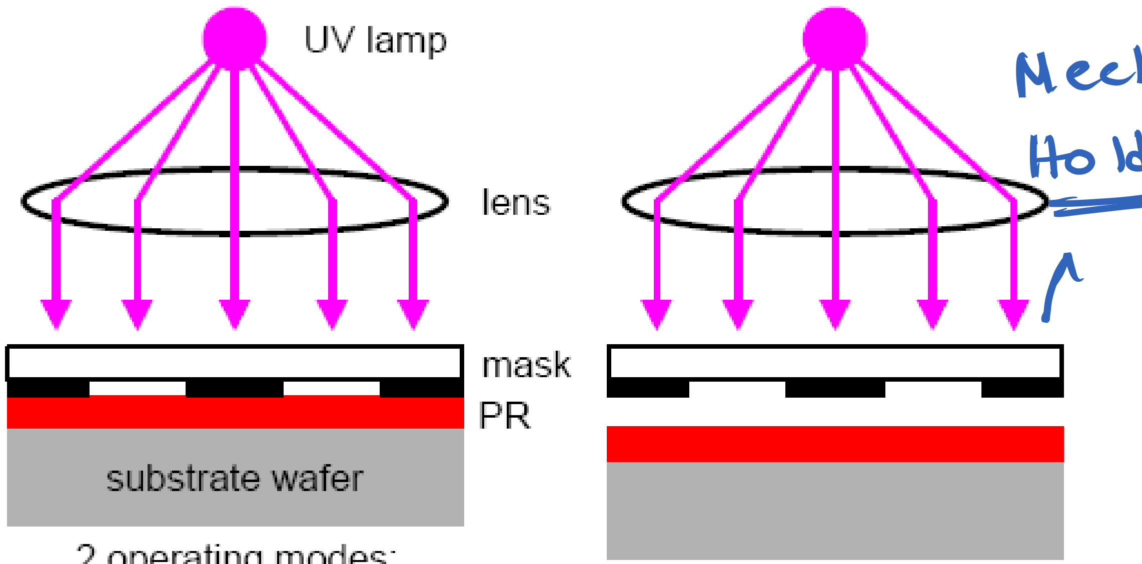


comes fm spin coating

Height of the patterns is controlled by ? → Thickness of the PR layer.

Optical Exposure: Printing Modes

CONTACT ~~ALIGNER~~ Printing | PROXIMITY ~~ALIGNER~~ Printing



Contact: 2 operating modes: contact for expose; separate for align.
<u>Examples:</u>
Kaspar 17A
Oriel
Karl Suss MJB3

Proximity: less wear on mask, but poorer image than from a contact aligner.
<u>Examples:</u>
Kaspar-Cobilt

Projection systems use imaging optics in between the mask and the wafer

Printing modes

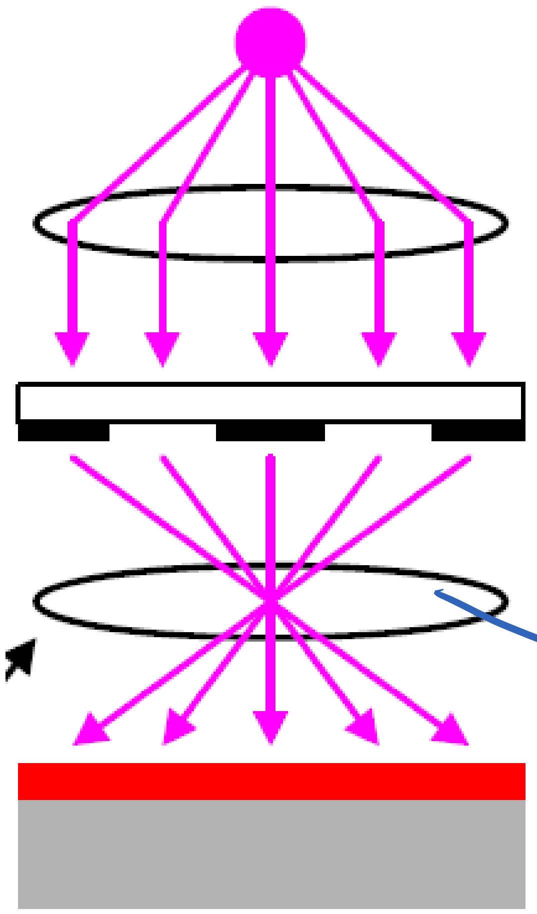
(1) Contact printing → Bring the mask and place over PR layer.

⇒ Contact printing is prone to mask damage.

(2) Proximity Printing → Resolution ≈ True feature size on the mask. No contact damage.

Optical Exposure: Printing Modes

PROJECTION ALIGNER



Examples:
Perkin-Elmer Micralign

R. B. Darling / EE-527

Projection Printing

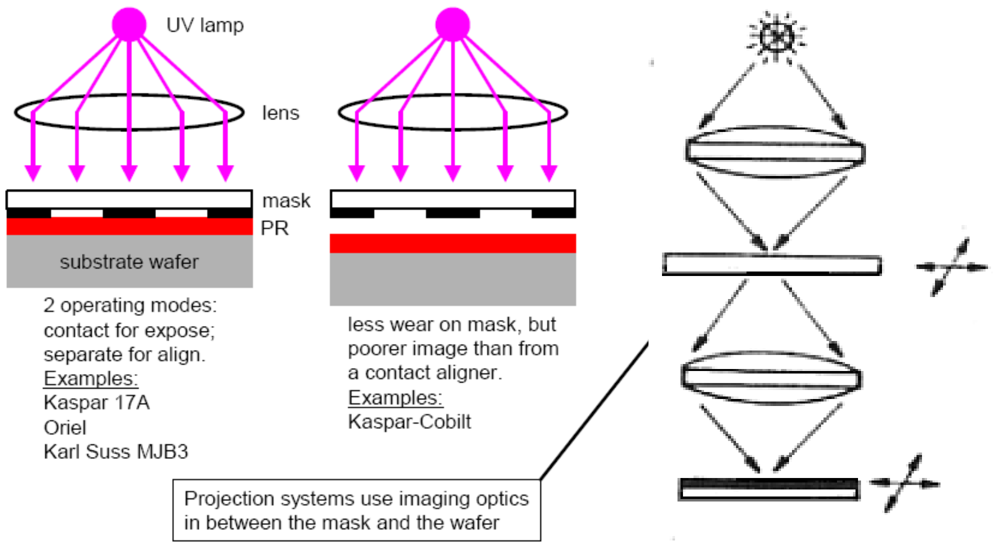
an additional lens is used between the mask and the PR coated sample to achieve enhanced miniaturization.

⇒ Still Evolving.

→ Optics → allow making features that are much smaller than the diffraction limitation

Optical Exposure: Printing Modes

Contact Printing | Proximity Printing | Projection Printing



Proximity printer resolution versus gap.

Gap (μm)	Resolution (μm)
10	1.47
15	1.77
20	2.03
30	2.46

Contact Printing

- The resist-coated silicon wafer is kept at physical contact with the photomask during exposure.
- Because of the contact between the resist and mask, very high resolution is possible in contact printing (e.g. 1-micron features)
- The problem with contact printing is that debris, trapped between the resist and the mask, can damage the mask and cause defects

Proximity Printing

- The proximity exposure method is similar to contact printing except that a small gap ~ 10 to 25 microns, is maintained between the wafer and the mask during exposure.
- This gap minimizes (but may not eliminate) mask damage. Approximately 2- to 4-micron resolution is possible with proximity printing

Post Bake

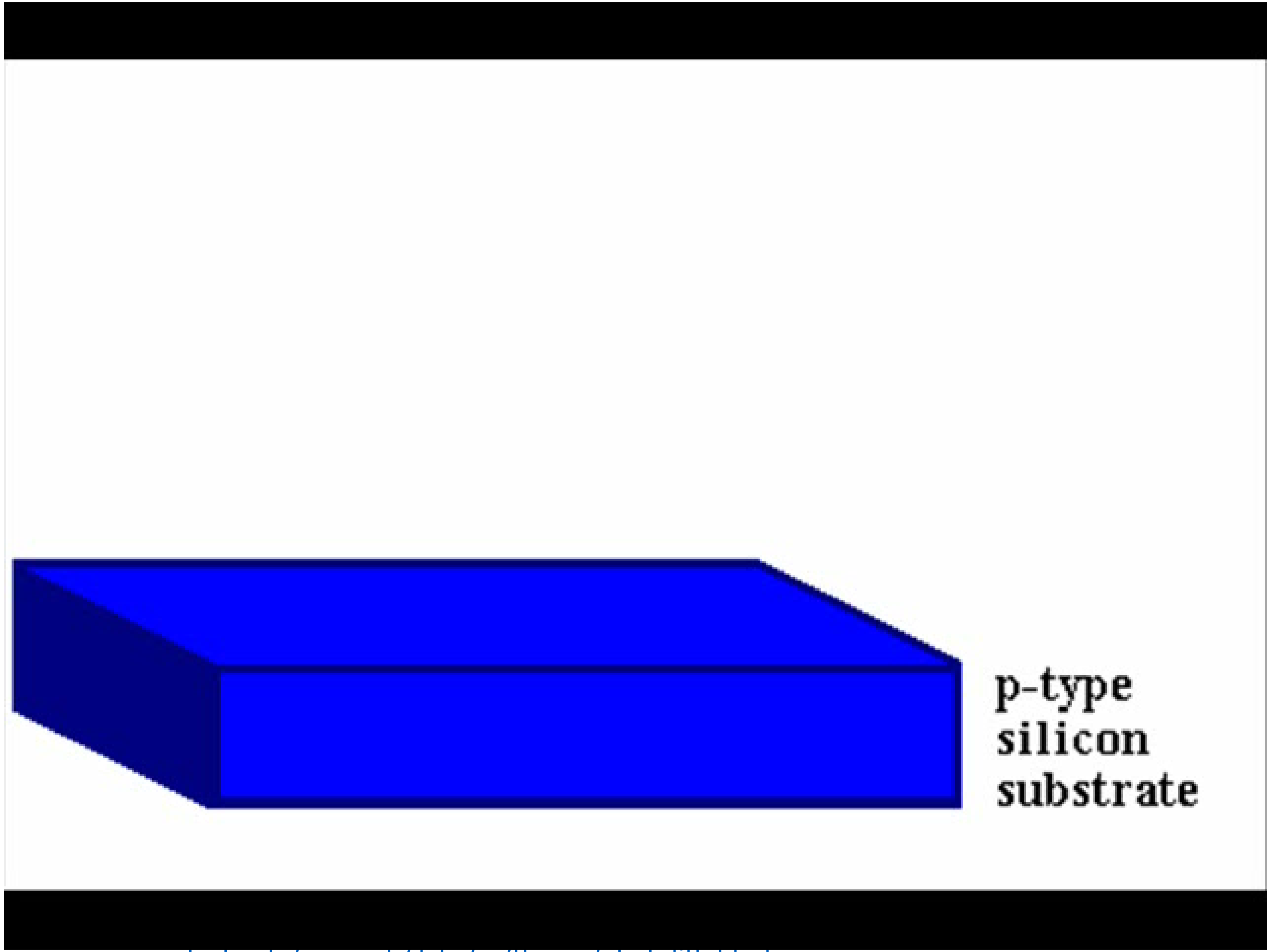
Post bake is performed after exposure, at temperatures slighly higher than soft bake.

Developing

This step a special solvent is used to wash the exposed/ un-exposed photo resist layer, resulting in the patterns on the PR layer.

Hard Bake

Final baking step to increase stiffness of the patterned photo resist layer and increase adhesion as well



www.ece.gatech.edu/research/ labs/vc/theory/photolith.html

Photolithography: Limitations → Still the main stay for micro electronic Industry.

(1) It requires expensive instruments and facilities with high capital investment

(2) The pattern resolution is limited by optical diffraction

(3) The method is not suitable for patterning all types of polymers, and only photosensitive resist materials (photoresists) can be directly patterned

(4) The technique requires harsh processing conditions such as exposure to UV radiation, chemical etching, and so on, and therefore has limited application for sensitive materials such as biological samples with living cells

(5) the method cannot be easily applied for patterning of nonplanar or curved surfaces

Planer geometry