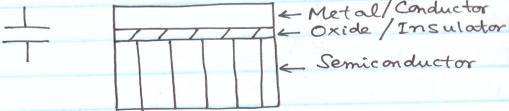


## Field Effect Transistor (FET)

Metal Oxide Semiconductors: MOS

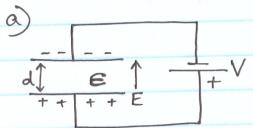


Metal: Gold, aluminum

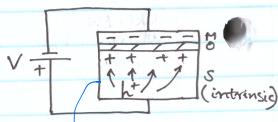
Oxide/Insulator: Silicon dioxide/Silicon nitride

Semiconductor: Silicon/germanium (doped preferably)

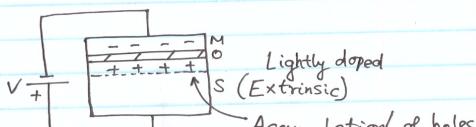
MOS is a special capacitor.



Standard capacitor biasing:

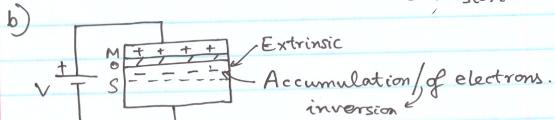


MOS biasing  
p-type semi



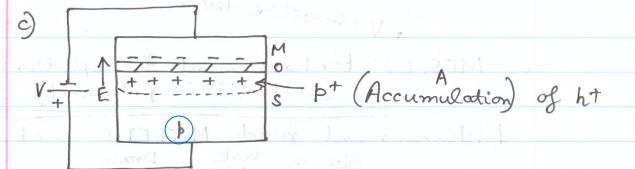
Lightly doped  
(Extrinsic)

Accumulation of holes  
Inversion

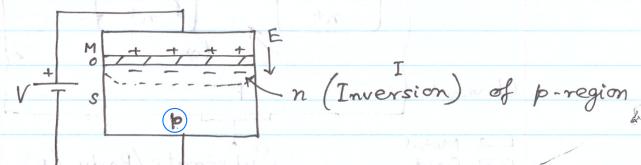


Extrinsic

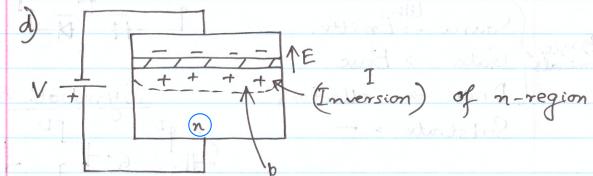
Accumulation of electrons.  
inversion



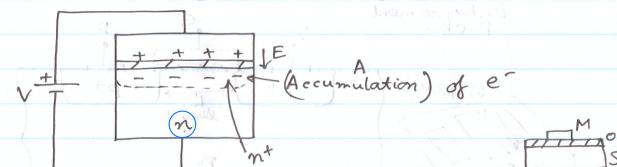
$V \rightarrow E \rightarrow A/I \rightarrow$  Conductivity  
 $E$ -field



$V \rightarrow E \rightarrow A/I \rightarrow$  Conductivity  
 $E$ -field



$V \rightarrow E \rightarrow A/I \rightarrow$  Conductivity  
 $E$ -field



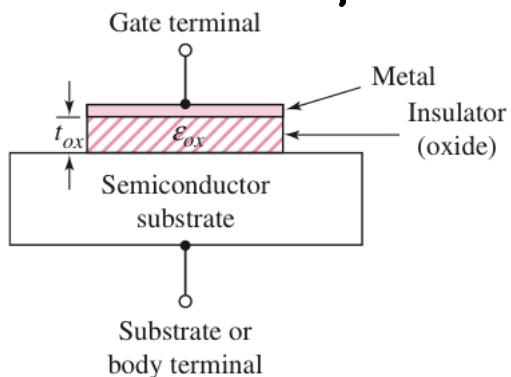
$V \rightarrow E \rightarrow A/I \rightarrow$  Conductivity  
 $E$ -field

$V \rightarrow E \rightarrow A/I \rightarrow$  Conductivity  
 $E$ -field

Conductor  
Semiconductor  
Insulator

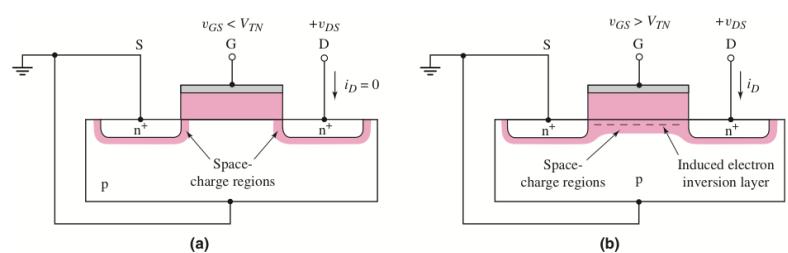
In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current. The phenomenon used to modulate the conductance of a semiconductor, or control the current in a semiconductor, by applying an electric field perpendicular to the surface is called the **field effect**. The basic transistor principle is that the voltage between two terminals controls the current through the third terminal.

## MOS Capacitor



**Figure 3.1** The basic MOS capacitor structure

The term **enhancement mode** means that a voltage must be applied to the gate to create an inversion layer. For the MOS capacitor with a p-type substrate, a positive gate voltage must be applied to create the electron inversion layer; for the MOS capacitor with an n-type substrate, a negative gate voltage must be applied to create the hole inversion layer.



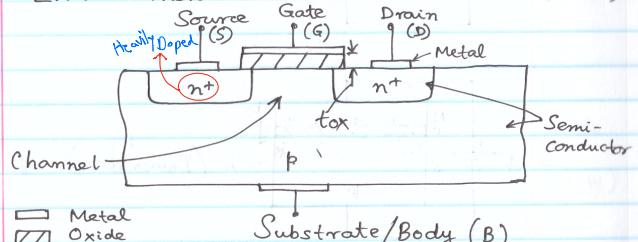
**Figure 3.7** The n-channel enhancement-mode MOSFET (a) with an applied gate voltage  $v_{GS} < V_{TN}$ , and (b) with an applied gate voltage  $v_{GS} > V_{TN}$



V-sensitive device

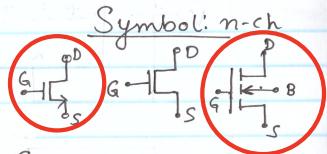
### e. MOSFET: Enhancement & Depletion. (n-channel & p-channel)

Enhancement mode MOSFETs: n-ch. (section)

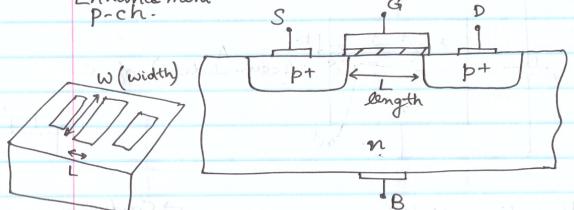


**Basic Terminals**

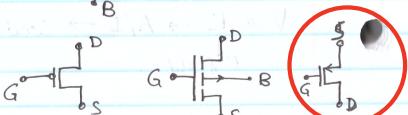
- { Source → Emitter
- Gate → Base
- Drain → Collector
- Substrate → -



Enhancement  
p-ch.

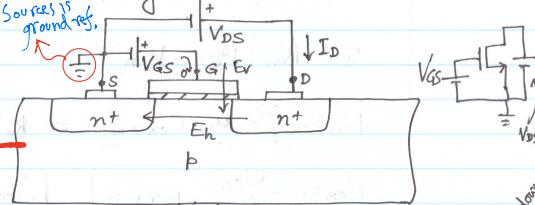


Symbol: p-ch.



Threshold V (min.  $V_{GS}$  to form a channel)  
 $\mu = \text{constant}$   
(assume:  $V_T = \text{constant}$ )

### f. MOSFET biasing & V-I characteristics



$$0 < V_{GS} < V_{Tn}, \\ V_{DS} > 0$$

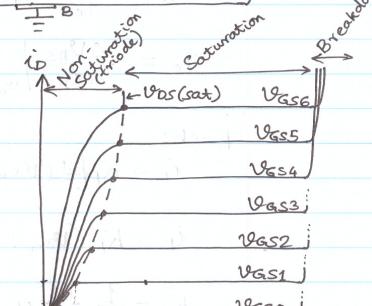
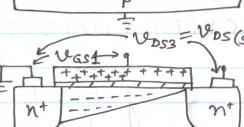
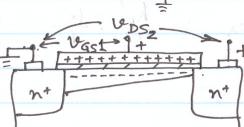
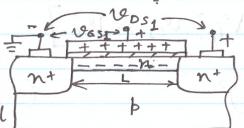
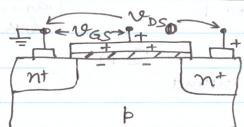
$$V_{GS} > V_{Tn} \\ (\text{Channel gets formed})$$

$$V_{GS1} & V_{DS1}$$

$$V_{GS1} & V_{DS3}$$

$$V_{GS2} & V_{DS2}$$

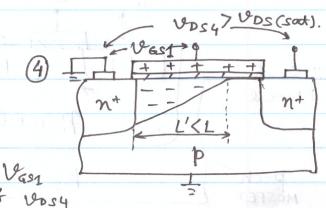
$$V_{GS4} & V_{DS4}$$



$$V_{GS6} > V_{GS5} > \dots > V_{GS0}$$

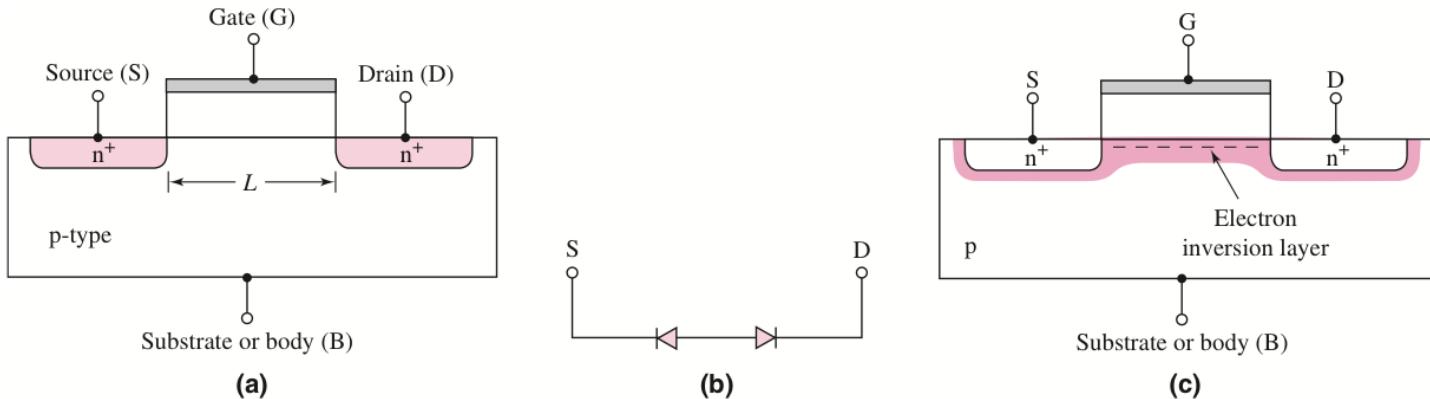
$$V_{GS1} > V_{Tn} > V_{GS0}$$

Threshold Voltage



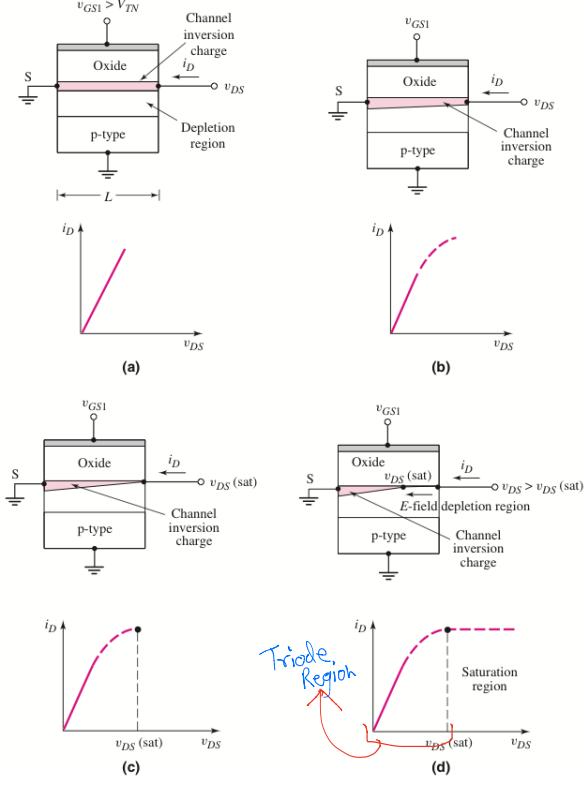
## e) Basic Transistor Operation

With zero bias applied to the gate, the source and drain terminals are separated by the p-region, as shown in Figure 3.6(a). This is equivalent to two back-to-back diodes, as shown in Figure 3.6(b). The current in this case is essentially zero. If a large enough positive gate voltage is applied, an electron inversion layer is created at the oxide–semiconductor interface and this layer “connects” the n-source to the n-drain,



**Figure 3.6** (a) Cross section of the n-channel MOSFET prior to the formation of an electron inversion layer, (b) equivalent back-to-back diodes between source and drain when the transistor is in cutoff, and (c) cross section after the formation of an electron inversion layer

The source terminal supplies carriers that flow through the channel, and the drain terminal allows the carriers to drain from the channel. For the n-channel MOSFET, electrons flow from the source to the drain with an applied drain-to-source voltage, which means the conventional current enters the drain and leaves the source. The magnitude of the current is a function of the amount of charge in the inversion layer, which in turn is a function of the applied gate voltage. Since the gate terminal is separated from the channel by an oxide or insulator, there is no gate current. Similarly, since the channel and substrate are separated by a space-charge region, there is essentially no current through the substrate.



**Figure 3.9** Cross section and  $i_D$  versus  $v_{DS}$  curve for an n-channel enhancement-mode MOSFET when  $v_{GS} > V_{TN}$  for (a) a small  $v_{DS}$  value, (b) a larger  $v_{DS}$  value but for  $v_{DS} < v_{DS(\text{sat})}$ , (c)  $v_{DS} = v_{DS(\text{sat})}$ , and (d)  $v_{DS} > v_{DS(\text{sat})}$

Figure 3.9(b) shows the situation when  $v_{DS}$  increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases. The incremental conductance of the channel at the drain then decreases, which causes the slope of the  $i_D$  versus  $v_{DS}$  curve to decrease. This effect is shown in the  $i_D$  versus  $v_{DS}$  curve in the figure.

As  $v_{DS}$  increases to the point where the potential difference,  $v_{GS} - v_{DS}$ , across the oxide at the drain terminal is equal to  $V_{TN}$ , the induced inversion charge density at the drain terminal is zero. This effect is shown schematically in Figure 3.9(c). For this condition, the incremental channel conductance at the drain is zero, which means that the slope of the  $i_D$  versus  $v_{DS}$  curve is zero. We can write

$$v_{GS} - v_{DS}(\text{sat}) = V_{TN} \quad (3.1(a))$$

or

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN} \quad (3.1(b))$$

where  $v_{DS}(\text{sat})$  is the drain-to-source voltage that produces zero inversion charge density at the drain terminal.

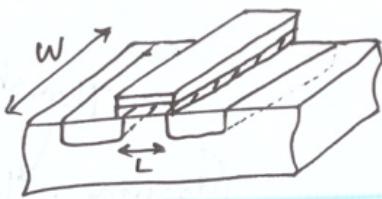
When  $v_{DS}$  becomes larger than  $v_{DS}(\text{sat})$ , the point in the channel at which the inversion charge is just zero moves toward the source terminal. In this case, electrons enter the channel at the source, travel through the channel toward the drain, and then, at the point where the charge goes to zero, are injected into the space-charge region, where they are swept by the  $E$ -field to the drain contact. In the ideal MOSFET, the drain current is constant for  $v_{DS} > v_{DS}(\text{sat})$ . This region of the  $i_D$  versus  $v_{DS}$  characteristic is referred to as the **saturation region**, which is shown in Figure 3.9(d).

As the applied gate-to-source voltage changes, the  $i_D$  versus  $v_{DS}$  curve changes. In Figure 3.8, we saw that the initial slope of  $i_D$  versus  $v_{DS}$  increases as  $v_{GS}$  increases. Also, Equation (3.1(b)) shows that  $v_{DS}(\text{sat})$  is a function of  $v_{GS}$ . Therefore, we can

generate the family of curves for this n-channel enhancement mode MOSFET as shown in Figure 3.10.

Although the derivation of the current–voltage characteristics of the MOSFET is beyond the scope of this text, we can define the relationships. The region for which  $v_{DS} < v_{DS}(\text{sat})$  is known as the **nonsaturation or triode region**. The ideal current–voltage characteristics in this region are described by the equation

$$i_D = K_n [2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2] \quad (3.2(a))$$



3D Structure  
of a MOSFET

n-ch:

$$i_D = K_n [2(V_{GS} - V_{Tn}) V_{DS} - V_{DS}^2] \quad (\text{Triode/Non-sat. region})$$

$$= K_n V_{DS} [2V_{DS(\text{sat})} - V_{DS}]$$

$$i_D = K_n (V_{GS} - V_{Tn})^2 \quad (\text{Sat. region})$$

Unit  
 $A/r^2$

$$K_n = \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot \frac{1}{2} = k_n' \cdot \frac{1}{2} \cdot \frac{W}{L}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \left| \begin{array}{l} \text{oxide permittivity} \\ \text{oxide thickness} \\ \text{per unit area} \end{array} \right|$$

$k_n'$  → Transconductance parameter  
 $k_n$  → Process conduction parameter  
( $\propto \mu_n \cdot C_{ox}$ )

$$r_o = \left. \frac{\Delta V_{DS}}{\Delta i_D} \right|_{V_{GS}=\text{constant}} \approx \infty$$

p-ch:

$$i_D = K_p [2(V_{SG} + V_{Tp}) V_{SD} - V_{SD}^2] \quad (\text{Triode})$$

$$i_D = K_p (V_{SG} + V_{Tp})^2 \quad (\text{Saturation})$$

$$K_p = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu_p \cdot C_{ox} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

$$k_p' = \mu_p \cdot C_{ox}$$

g. Complementary MOSFET (CMOS):

