Muralidaran Vijayaraghavan

Contact Information

Computer Science and Artificial Intelligence Laboratory
Massachuesetts Institute of Technology, Cambridge MA

Mobile: +1 408 839 3356
Email: vmurali@csail.mit.edu

Research Interests

Automated theorem proving, formal verification and high-level languages for hardware design, correct-by-construction approach to hardware design

Education

Massachusetts Institute of Technology, Cambridge, MA
Ph.D., Electrical Engineering and Computer Science, ***Expected: Summer 2014***

- Thesis topic: *Language for designing and refining latency-tolerant hardware modules*
- Advisor: Prof. Arvind

S.M., Electrical Engineering and Computer Science, ***February 2009***

- Thesis topic: *Theory of composable latency-insensitive refinements*
- Advisor: Prof. Arvind

Indian Institute of Technology, Madras, Chennai, India
B.Tech., Computer Science and Engineering, ***June 2006***

Work Experience

Research Intern, IBM T.J. Watson Research Center, Yorktown Heights, NY
Supervisor: Dr. Kattamuri Ekanadham, Ph.D.
Developed a high-level language for writing synchronous hardware modules, and a tool to convert them automatically to latency-tolerant modules. This was used in the design of next generation PowerPC systems. ***May 2010 – Aug 2010***

Research Intern, VSSAD group, Intel Corporation, Hudson, MA
Supervisor: Prof. Joel Emer.

- Developed an infrastructure, called HASim, for building FGPA-based performance models for faster simulations and performance studies ***May 2007 – Aug 2007***
- Developed an FPGA-based performance model of an out-of-order superscalar processor using HASim ***May 2008 – Aug 2008***

Refereed Publications

1. **Vijayaraghavan, M.**, Dave, N., Arvind. "Distributed Modular Hardware Compilation of Guarded Atomic Actions" *MEMOCODE 2013*
2. Khan, A., **Vijayaraghavan, M.**, Boyd-Wickizer, S., Arvind."Fast and cycle-accurate modeling of a multicore processor" *ISPASS 2012*
3. Khan, A., **Vijayaraghavan, M.**, Arvind. "A general technique for deterministic model-cycle-level debugging" *MEMOCODE 2012*
4. Pellauer, M., Agarwal, A., Khan, A., Ng, M. C., **Vijayaraghavan, M.**, Brewer, F., Emer, J. S. "Design contest overview: Combined architecture for network stream categorization and intrusion detection (CANSCID)" *MEMOCODE 2010*
5. Pellauer, M., **Vijayaraghavan, M.**, Adler, M., Arvind, Emer, J. S. "A-Port Networks: Preserving the Timed Behavior of Synchronous Systems for Modeling on FPGAs" *TRETS 2(3) (2009)*
6. Agarwal, A., Dave, N., Fleming, K., Khan, A., King, M., Ng, M. C., **Vijayaraghavan M.** " Implementing a fast cartesian-polar matrix interpolator" *MEMOCODE 2009*
7. **Vijayaraghavan, M.**, Arvind. "Bounded Dataflow Networks and Latency-Insensitive circuits" *MEMOCODE 2009*
8. Pellauer, M., **Vijayaraghavan, M.**, Adler, M., Arvind, Emer, J. S. "A-Ports: an efficient abstraction for cycle-accurate performance models on FPGAs" *FPGA 2008*
9. Pellauer, M., **Vijayaraghavan, M.**, Adler, M., Arvind, Emer, J. S. "Quick Performance Models Quickly: Closely-Coupled Partitioned Simulation on FPGAs" *ISPASS 2008*
10. Fleming, K., King, M., Ng, M. C., Khan, A., **Vijayaraghavan, M.** "High-throughput Pipelined Mergesort" *MEMOCODE 2008*
11. Ng, M. C., **Vijayaraghavan, M.**, Dave, N., Arvind, Raghavan, G., Hicks, J. "From WiFi to WiMAX: Techniques for High-Level IP Reuse across Different OFDM Protocols" *MEMOCODE 2007*
12. Dave, N., Fleming, K., King, M., Pellauer, M., **Vijayaraghavan, M.** "Hardware Acceleration of Matrix Multiplication on a Xilinx FPGA" *MEMOCODE 2007*