EE5314 Class Notes

Hardware Guide

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Basic Components

- 100mil (0.1”) square grid PCB with solder donuts
- 28p machine pin 300mil DIP socket
- Reset resistors and capacitor
- Voltage core capacitor
- Ceramic resonator (alt: crystal or TTL clock)
- User interface (push button, LED, …)
- Power supply (batteries, ext supply, ICD3)
- Power supply filtering and bypass

Suggested Tools

- Soldering iron (30W or less) with small tip (chisel or needle point) properly tinned
- Solder (can contain lead, so be cautious)
- Cleaning device for solder tip
- Solder wick (for unsoldering)
- Diagonal cutter (watch for flying wires)
- Wire strippers
- Needle-nose pliers (for forming wires)
- Safety goggles! (for flying solder and wires)

Why Solder a Board?

- White breadboards
  - Connections are often intermittent
  - Ceramic resonators and crystal are problematic due to stray capacitance
  - Large pins will spring contacts
  - Larger current devices will have to be off-boarded
- Wire wrapping
  - Ceramic resonators and crystal are problematic due to extra lead inductance
  - Many devices under control exceed the current rating of 30ga wire (off-board issue above)

Basic Layout

- Start by arranging the parts with respect to the controller pins to minimize wiring runs
- Ceramic resonator should be very close to pins 8, 9, and 10
- Reset circuit should be by pin 1
- ICD3 connector should be by pin 1 and a PGECx/PGEDx pair
- Power supply bypassing by power pins

Power Distribution

- Our boards do not have a ground plane, so particular attention needs to be paid to power routing
- Point to point wiring can be very problematic, especially if transient high current devices are in the chain
- Try to star-wire (bring back ground and rail separately back to supply) to minimize source impedance
- Use storage caps for high current devices
- Use bypass caps on power pins of all devices
- Handle over-current, over-voltage correctly with TVS (transient voltage protection), fuse, PTC

Bypass Capacitance

- It is suggested that a 0.1 μF surface mount or 0.01uF radial leaded ceramic cap should be placed close to the power pins of every device in the circuit
(note: SMD has a lower ESL than a leaded capacitor)
- A 0.01 μF radial leaded cap is approximated by a series RLC circuit with an ESL of 6 nH (not including DIP pin) and an ESR of 0.2ohms, which is resonant at ~20 MHz
- A bypass cap allows high-frequency currents to be supplied quickly to the local device and effectively lowers the series inductance of the supply to the device
- In other words, the short-term transient needs of the device are supplied by the capacitor and when the event is over, the capacitor is re-charged by the power supply
- The value of the capacitor is large function of the ground planes, capacitor packaging (SMD v. leaded), total number of decoupling caps and many other factors

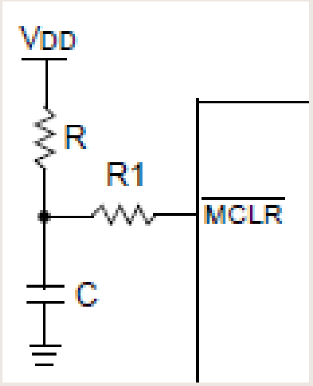
Storage Capacitance

- Many devices, like memories, have large inrush currents at power up or when enabled
- This can create power “brown-outs” or transients on the board due to source or wiring impedances
  - This can lead to incomplete processor resets, raised noise floor in analog circuits like the A/D
- Larger caps (25-500 μF) act as a energy storage device, which effectively lowers the source impedance of the power supply at lower frequencies
- A 10 uF, low ESR capacitor is needed from Vcore toVss for the processor core regulator

Π Filters

- A parallel C, series L, parallel C circuit is useful in creating a high-current low pass filter for noisy loads
- Some examples of noisy loads are switching capacitor and switched inductor power supplies, motors, and solenoids

Reset Circuit



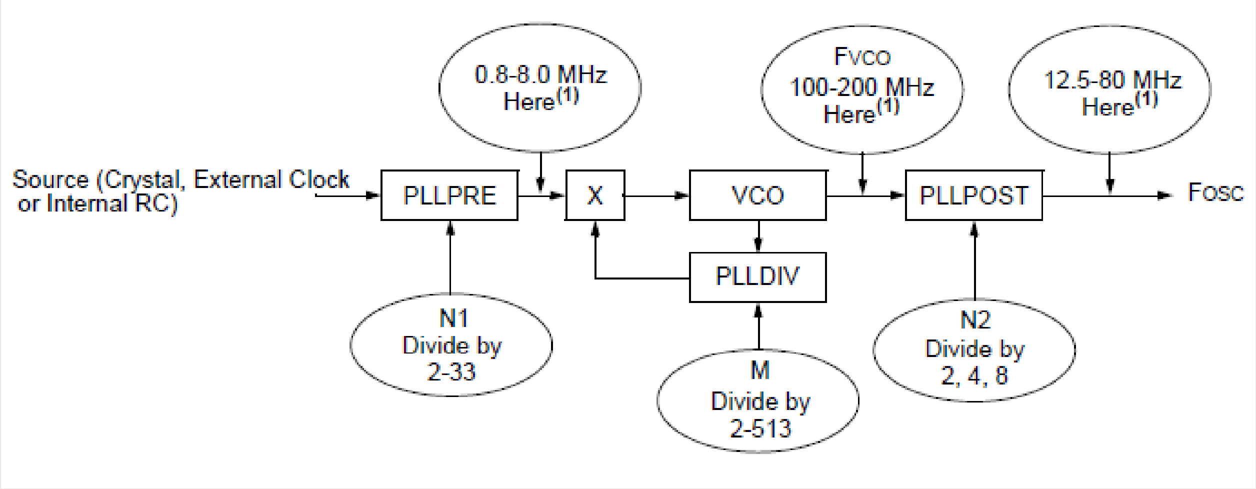
- Integrator consisting of a current source, R, and the storage device C
- When the circuit is de-energized, Vdd will be at 0V and the cap will discharge through R
- On power-up, R will charge C pulling ~MCLR high after some time
- R1 limits current from C into the pin
- R = 10kohms, C = 0.1uF, R1 = 10ohms

Clock Sources

- Internal RC clock circuit (not accurate)
- External crystal or ceramic resonator used in a parallel resonant oscillator (on silicon)
  - XT mode (3-10 MHz)
  - HS mode (10-40 MHz)
- External clock source (EC mode)
- External crystal used by the secondary oscillator
  - Normally uses a 32.768 kHz oscillator used for the real-time clock

Phase-locked Loop

- Used in XT, HS, and EC modes to allow a lower frequency resonator or clock source to be used
- Clock is prescaled (÷2 to ÷33) to 0.8 to 8 MHz
- Voltage-controlled oscillator (VCO) output between 100-200 MHz is maintained at 2× to 513× by the PLL



Phase-locked Loop

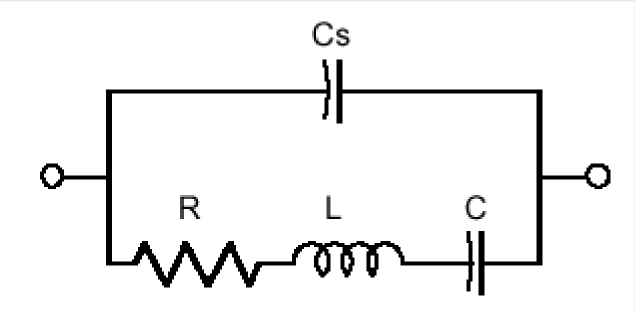
- Output of VCO is post-scaled (÷2, ÷4, or ÷8)
- Our designs use a final clock of 80 MHz and an 8 MHz ceramic resonator (XT mode)
- Important VCO Limitations
  - The VCO design only allows for a 100-200 MHz output
  - With power-on defaults of ÷2 pre-scale, x50 VCO/PLL, ÷4, the frequency input from the external clock or primary oscillator is bounded by 4 MHz and 8 MHz due
  - If outside this range, start the chip using the internal RC oscillator, reconfig the PLL, and switch to pri osc

Crystals

- Constructed from thin slabs of quartz (or similar material) sandwiched between two metal plates (electrodes)
- Simplest model (ignoring mechanical overtones) is a series RLC circuit (the motivational arm of the crystalline material) in parallel with a shunt capacitance C_S (due to the electrodes and the contained dielectric)
  - Looks like a 3-10 pF capacitor when not resonant (negative reactance)
  - Reactance is positive (inductive) when crystal is anti-resonant and real when crystal is series-resonant

Crystals

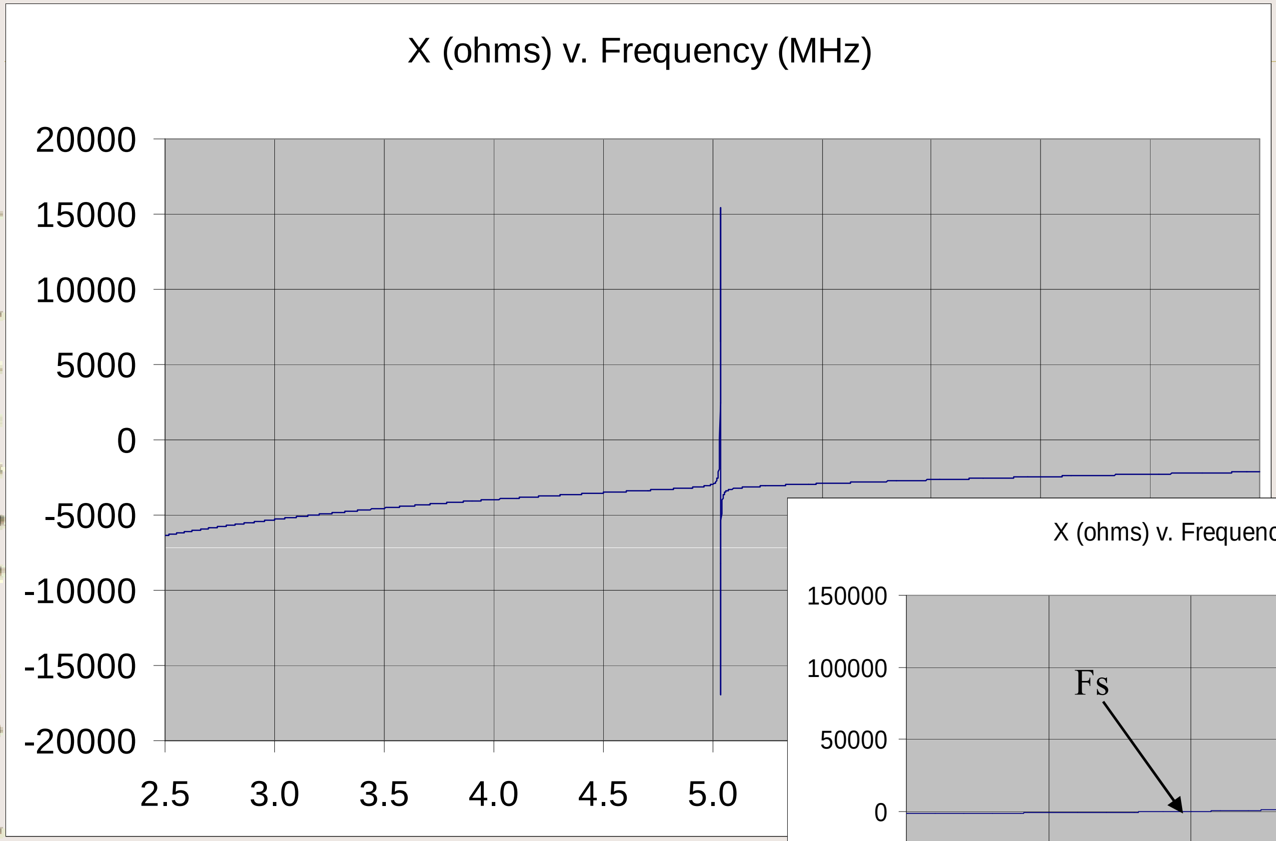
- For a typical crystals (1-20 MHz)
  - $L = 1\text{-}500$ mH, $C = .01\text{-}.03$ pF, $R = 10\text{-}100\ \Omega$, $C_s = 3\text{-}7$ pF
- Impedance:
  - $Z = (j\omega L + R + 1/j\omega C)\ //\ (1/j\omega(C_S + C_L)]$ where C_L is the load of the stray capacitance, oscillator circuit loading, and discrete capacitors across the crystal

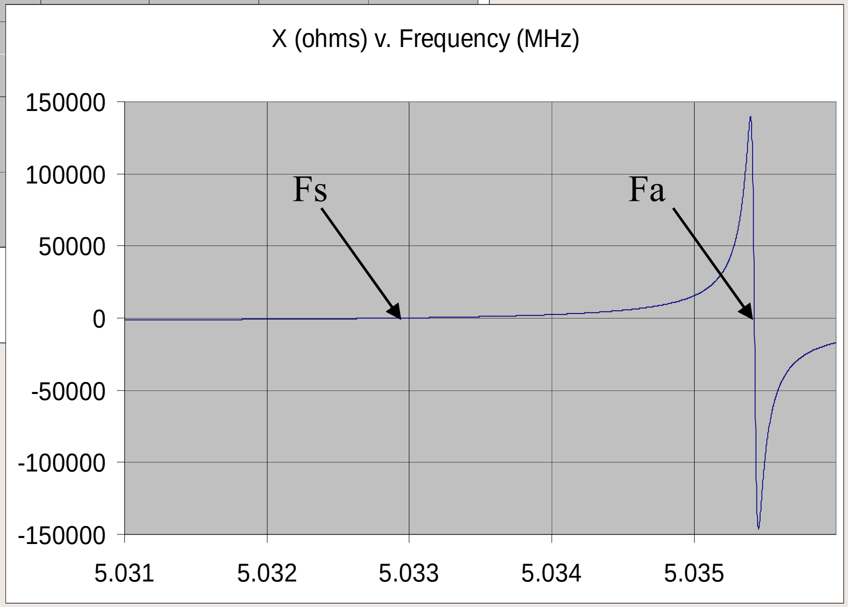


Crystal Resonance

- Series resonance (where L and C are in resonance):
  - $f_S = [2 \times \pi \times (LC)^{1/2}]^{-1}$
  - Z = R || XCs -> R (X -> 0) at f_S
- Anti-resonance (resonance of RLC in parallel with C_S and C_L (load):
  - $f_A = [2\pi (LC (C_L + C_S)/(C + C_L + C_S)^{1/2}]^{-1}$
  - X is positive from f_S to f_A

Crystal Reactance





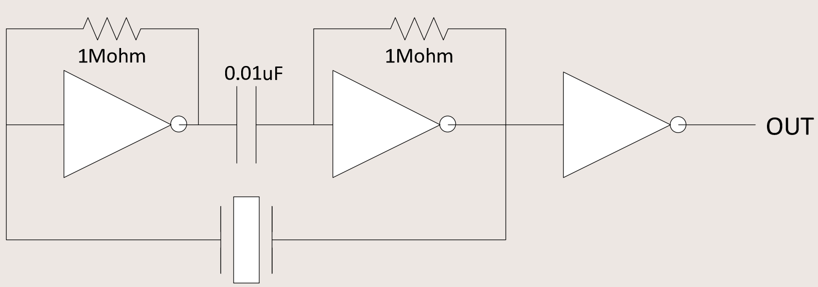
- R = 35 Ω
- L = 100 mH
- C = 0.01 pF
- $C_L + C_0$= 10 pF
- F_S = 5.033 MHz

Oscillation

- Barkhausen Stability Criteria
  - Total phase shift around loop must be N * 360º, where N is an integer
  - Closed loop gain must be greater than or equal to 1
- CMOS inverters are often used as the active device in oscillator circuits
  - Series resonating oscillators have two inverters and a crystal in the feedback term
  - Parallel resonating oscillators have one inverter and a crystal in the feedback term (the primary oscillator in the PIC OSC1/2 pins)

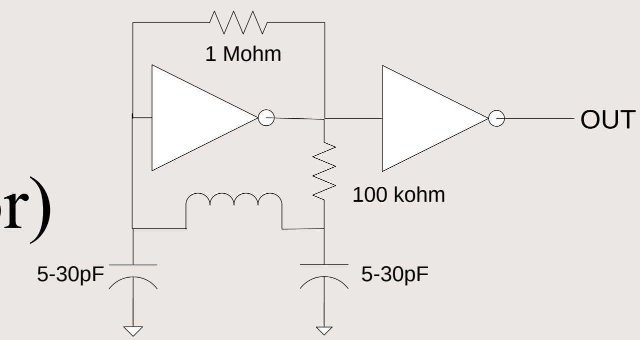
Series Resonant Oscillator

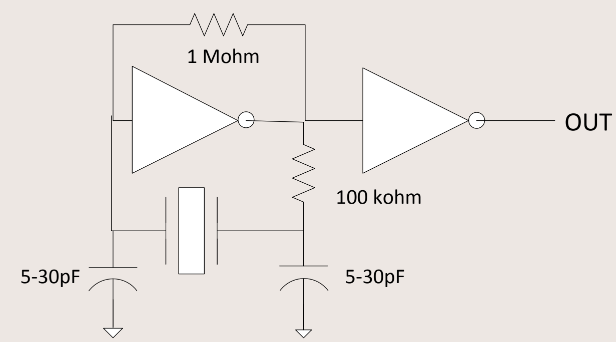
- Phase delay of the two inverters is $2 \times \tau_p \times f_{osc} \times 360°$
- Crystal operating in the series resonant point give 0º of phase shift, so oscillator should work
- Problem: There is no way to accurately set the oscillation frequency and the circuit can oscillate at a non-resonant frequencies



Parallel Resonant Oscillator

- One inverter gives a $\tau p \times fosc \times 360°$ phase shift
- A phase shift network consisting of two parallel capacitors and a series inductor is used in the feedback path
- Between f_S and f_A the crystal reactance is positive (inductor)
- The exact frequency can be tweaked by varying the shunt C values
- This is the commonly used implementation





Ceramic Resonators

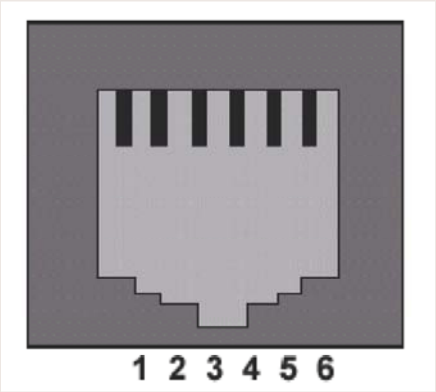
- Made of piezoelectric materials, like lead zirconate titanate (PZT)
- Lower cost alternative to crystals
- Less frequency accuracy than crystals
- Lower Q than crystals
- Can generally be used in the crystal circuits, with small modifications to the shunt capacitance to accommodate different resonator parameters

Clock Oscillator

- Crystal, parallel resonant oscillator, and logic-compatible driver
- Common clock oscillators are in metal hermetically-sealed package with 4 pins (power, ground, and output present)
- Lower part count, but higher cost
- The output is connected to OSC1 and the OSC2 pin can be used for general I/O

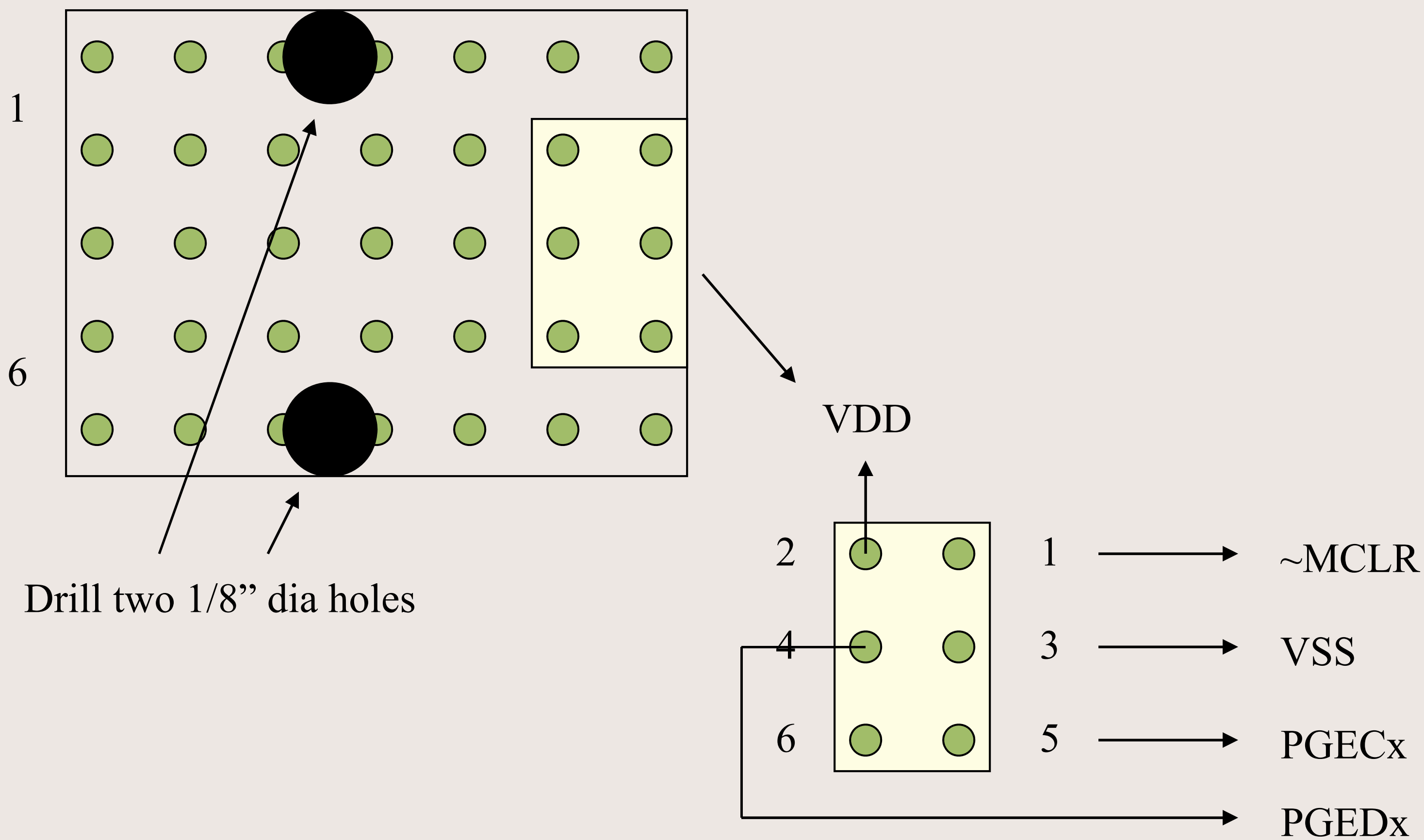
ICD3 Pinout

- Pin 1 ~MCLR
- Pin 2 Vdd
- Pin 3 Vss
- Pin 4 PGEDx
- Pin 5 PGECx
- Pin 6 N.C.



ICD3 Mechanics

RJ-12 Jack Top View



MPLAB Project Setup

- Project>New
  Name the project and select a path, click OK
- Project>Select Language Toolsuite
  Ensure MPLAB ASM30 Toolsuite is selected
  (use MPLAB C30 Toolsuite for C code)
- View>Project
- Create ASM or C file (or use one from class) and save file at the path above
- In project toolbar, right click on Source Files to add the file above
- In project toolbar, right click on Linker Script to add the file "p33fj128mc802.gld" from the following location:
  C:\Program Files\Microchip\MPLAB ASM30 Suite\Support\dsPIC33F\gld

MPLAB Settings for H/W Target

- Configure>Select Device: select 33FJ128MC802 device
- Configure>Configuration Bits
  set as appropriate for your hardware
- Typical deviations from the default configuration bit settings for 8 MHz ceramic resonator:
  - IESO is Start-up device with user-selected oscillator
  - FNOSC is Primary oscillator with PLL
  - POSCMS is XT Crystal Oscillator mode
  - FWDTEN is Watchdog timer enabled/disables by user
  - ICS as appropriate

Programming

- Programmer>Select Programmer>ICD3
- If your circuit needs only +3.3V and < 100 mA, then you can power the target hardware from the ICD3 checking the box Programmer>Settings…>Power>Power target circuit from ICD3
- Programmer>Program
- Your hardware should be running