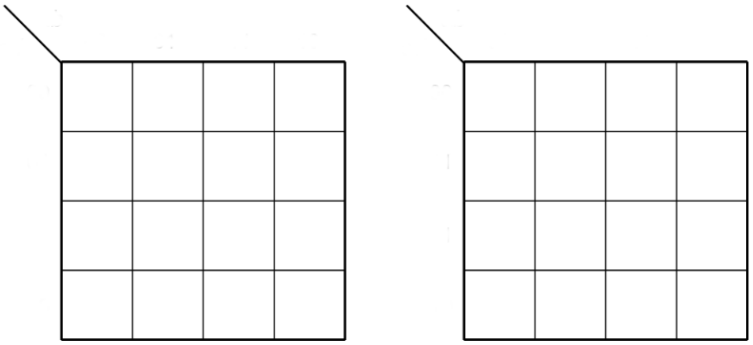
EXAM 2 CHAPTERS 3, 5, & 6.1 NOVEMBER 4TH 2021

The exam will be in this classroom and scheduled for 75 minutes.
Notes will not be allowed and you should work in pencil. The legibility rule applies here.

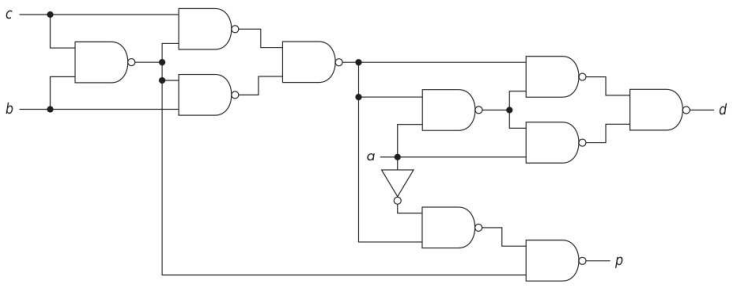
All problems are inspired by lecture material, solved problems from our book, and homework.

As per our syllabus, without documentation from an appropriate provider, make-up exams will not be given. In the event of an appropriate excuse, the final exam grade will take the place of this midterm.

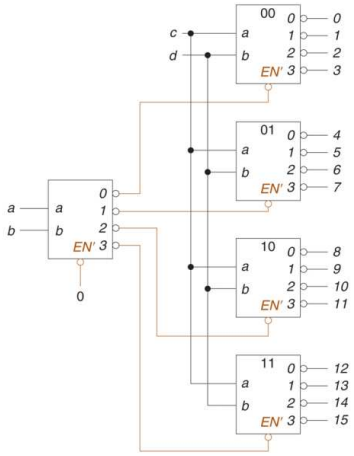
- Chapter 3: The Karnaugh Map
  - Minimum SoP Expressions from K-Maps: 3.1, 3.2
  - Minimum SoP Expressions with Don't Cares: 3.3
  - Minimum PoS Expressions from K-Maps: 3.4
  - Minimum SoP Expressions for Multiple Output: 3.6 (for use in 5.6 gate arrays)



- Chapter 5
  - Iterative Systems: 5.1

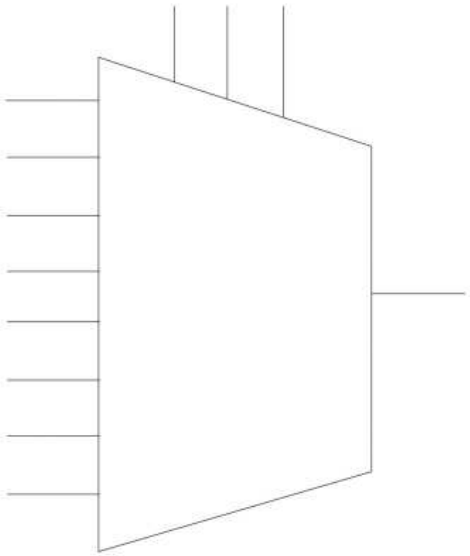


– Binary Decoders: 5.2



Consider problems similar to 5–8 from pages 309–314. You should be able to draw a Decoder from description, e.g., a 2-to-4 Decoder with an active low enable.

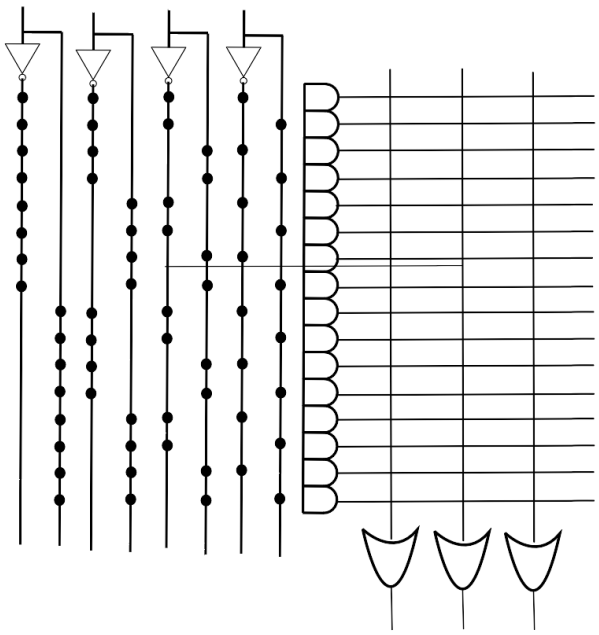
– Multiplexers and Demultiplexers: 5.4



Consider problems similar to 11 and 12 from pages 316–318. You should be able to draw a MUX from description, e.g., a 4-way MUX.

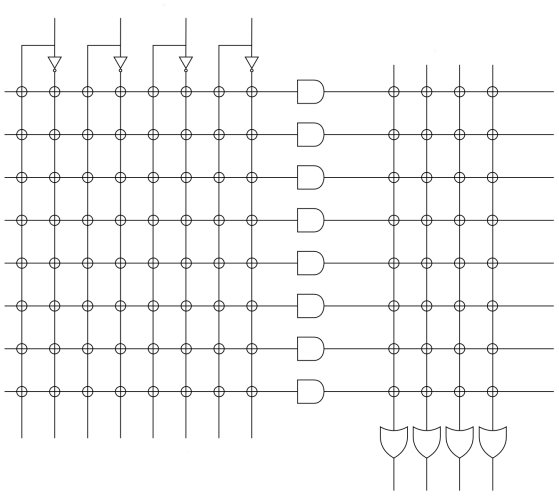
Cont.

- Gate Arrays: 5.6
  - Designing with ROMs



Consider problems like 13.a from pages 318–319 and 14.a from pages 322–323. Practice programming ROMs with partially minimized functions. Graphics will be provided for ROM programming.

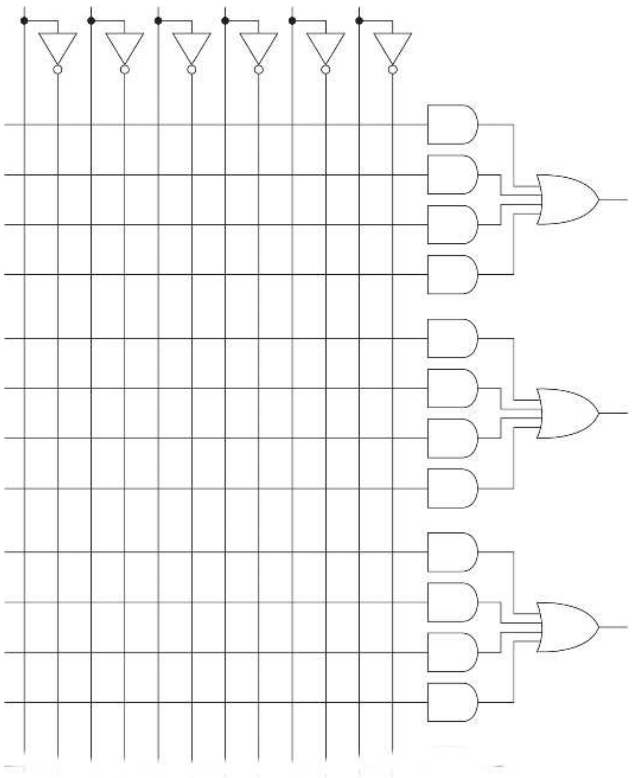
  - Designing with PLAs



Consider problems like 13.d from pages 318–322 and 14.b from pages 322–324. Practice minimizing multiple functions together. Graphics will be provided for PLA programming.

Cont.

* Designing with PALs



Consider problems like 13.c from pages 318–321 and Example 5.12 from pages 287–288. You will need to be able to minimize multiple functions together to indicated total terms and literals. Graphics will be provided for PAL programming.

- Chapter 6
  - State Tables and Diagrams: 6.1

Consider problems like 1.a and 1.b (pages 390–392). You should be able to convert between State Tables and State Diagrams and execute a timing trace.

The End.