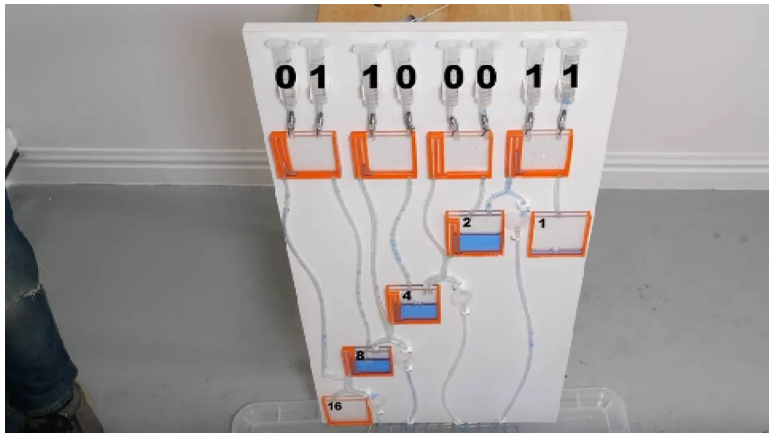
Gates From Transistors

Instructor: Dr. Vinicius Prado da Fonseca (vpradodafons@online.mun.ca)

Beneath the Digital Abstraction

- Measurements of continuous physical quantities
  - Real-world
  - voltage on a wire
  - the position of a gear
  - level of fluid in a cylinder
- Designer must choose a way to relate the continuous value to the discrete value
- Voltage levels to represent bits
  - Water adder computer by Steve Mould



Vinicius Prado da Fonseca, PhD (vpradodafons@mun.ca)

Beneath the Digital Abstraction

- Noise Margins (NM)/ tolerance
- The Static Discipline
  - given logically valid inputs, every circuit element will produce logically valid outputs.
- Freedom
  - arbitrary analog circuit elements
- vs simplicity and robustness
  - digital circuits

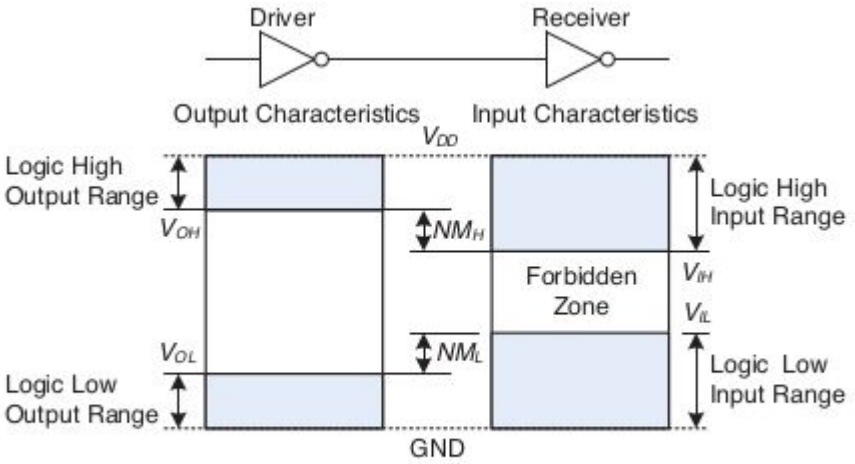


Figure 1.23 Logic levels and noise margins

Beneath the Digital Abstraction

- The highest voltage in the system comes from the power supply and is usually called V_{DD}
- Choice of V_{DD} and logic levels is arbitrary
- Grouped into logic families

Table 1.4 Logic levels of 5 V and 3.3 V logic families

Logic Family	V_{DD}	V_{IL}	V_{IH}	V_{OL}	V_{OH}
TTL	5 (4.75–5.25)	0.8	2.0	0.4	2.4
CMOS	5 (4.5–6)	1.35	3.15	0.33	3.84
LVTTL	3.3 (3–3.6)	0.8	2.0	0.4	2.4
LVCMOS	3.3 (3–3.6)	0.9	1.8	0.36	2.7

Beneath the Digital Abstraction

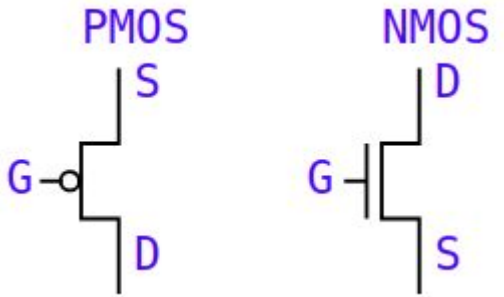
- Babbage's Analytical Engine was built from gears
  - The computer Ada Lovelace programmed
- Early electrical computers used relays or vacuum tubes
- Modern computers use transistors
  - cheap, small, and reliable.
- Transistors
  - electrically controlled switches
  - turn ON or OFF when a voltage or current is applied to the control terminal

MOSFETS

- The two main types of transistors
  - Bipolar junction transistors
  - Metal-oxide-semiconductor field effect transistors
    - MOSFETs or MOS transistors
    - pronounced “moss-fets” or “M-O-S”, respectively

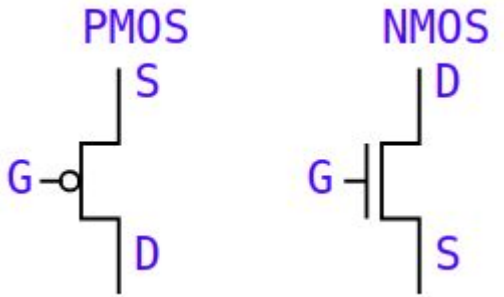
NMOS and PMOS Transistors

- NMOS and PMOS FET (field effect transistors)
- N-channel/P-channel Metal Oxide Semiconductor
- The terminals are called:
  - G for gate
  - D for drain, and
  - S for source
- The gate control the connection between S and D.
- voltage ranges: 0V to 5V, 0V to 3.3V and 0V to 1.8V

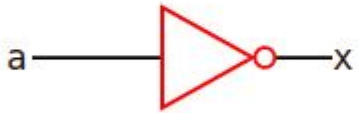


NMOS and PMOS Transistors

- PMOS
  - G high voltage -> “opens”
    - S not connected to D
  - G low voltage -> “closes”
    - S connected to D
- NMOS
  - G high voltage -> “closes”
    - S connected to D
  - G low voltage -> “opens”
    - S not connected to D
- S and D direction is important
  - Flow of electrons due to the construction
  - Source of PMOS connected to VDD
  - Source of NMOS connected to GND
- CMOS - Complementary Metal-Oxide Semiconductor

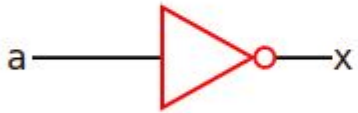


CMOS Inverter

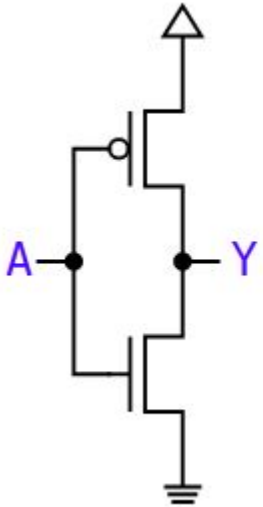


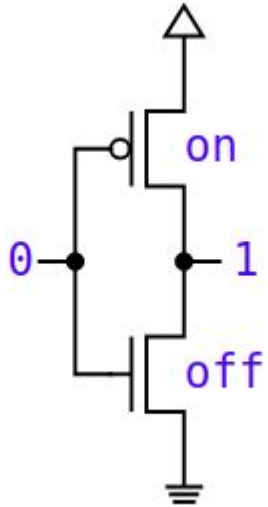
A PMOS and a NMOS transistor

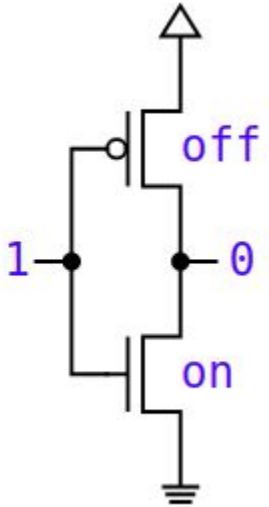
CMOS Inverter



A PMOS and a NMOS transistor

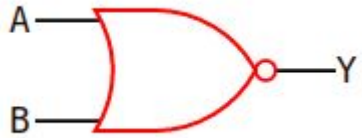






CMOS NOR

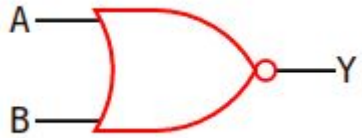
A two input NOR gate can be constructed with four transistor, two NMOS and two PMOS



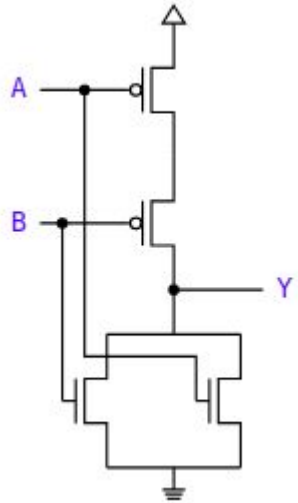
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

CMOS NOR

A two input NOR gate can be constructed with four transistor, two NMOS and two PMOS

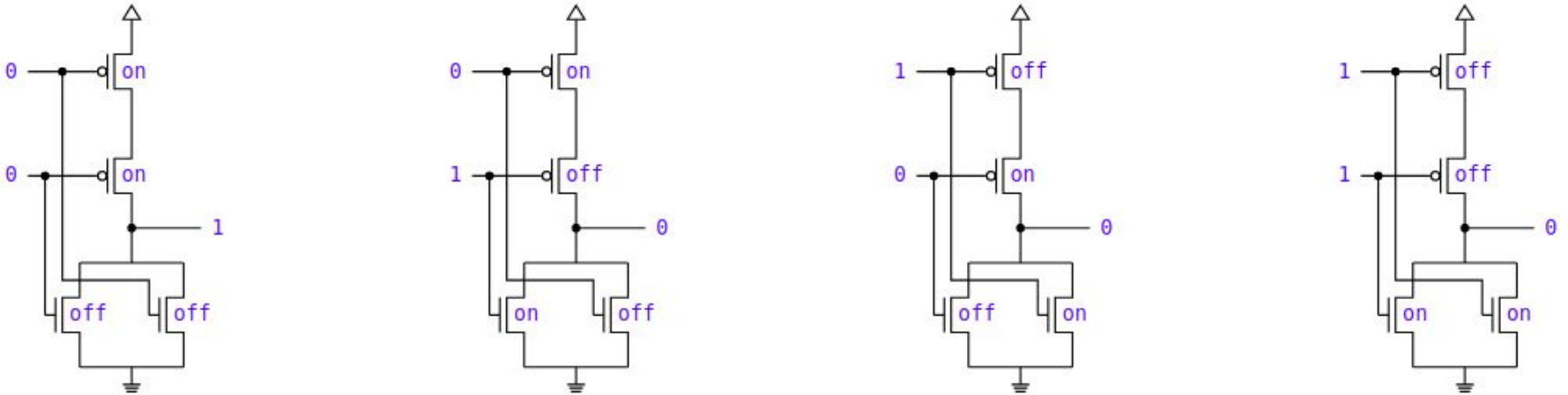


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



CMOS NOR

A two input NOR gate can be constructed with four transistor, two NMOS and two PMOS



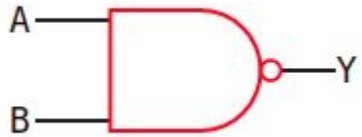
CMOS NAND

A two input NAND gate can be constructed with four transistor, two NMOS and two PMOS.

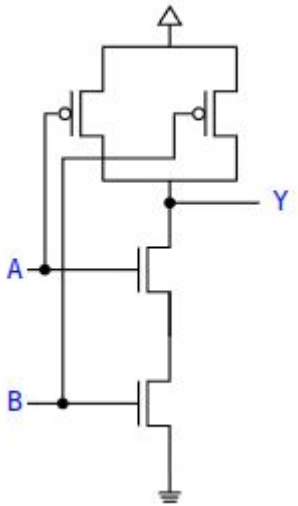
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NAND

A two input NAND gate can be constructed with four transistor, two NMOS and two PMOS.

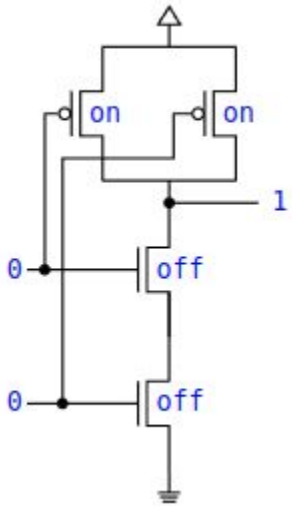


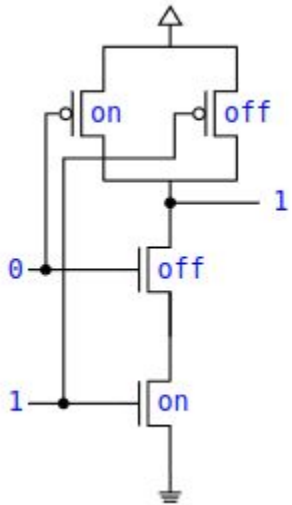
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

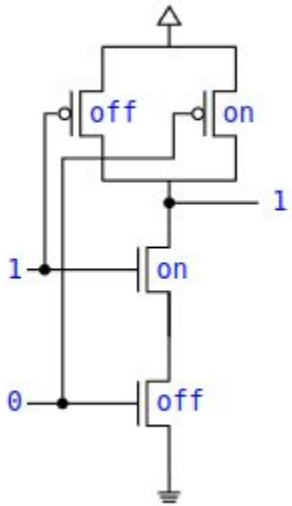


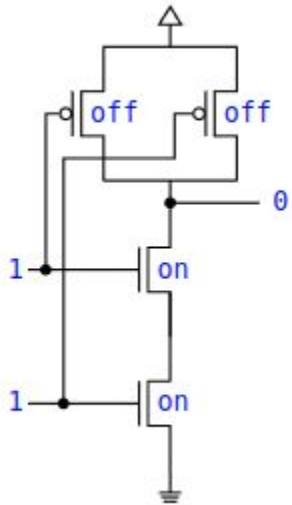
CMOS NAND

A two input NAND gate can be constructed with four transistor, two NMOS and two PMOS.



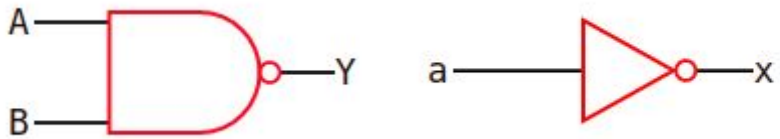






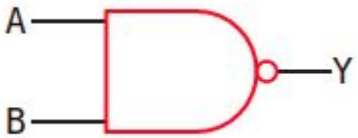
Building Other Gates

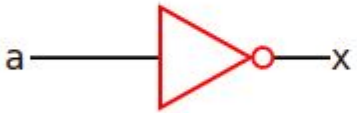
- In CMOS all other two input logic gates are constructed using
  - NOT, NOR, and NAND gates
- Thus an AND gate requires six transistors
  - 4 transistors for the NAND
  - 2 transistors for the following NOT gate

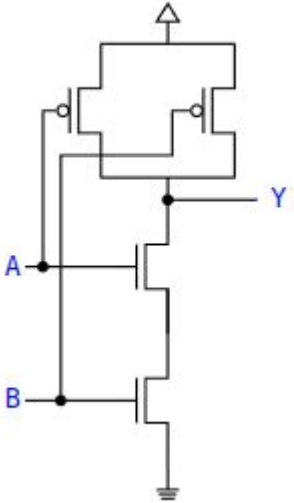


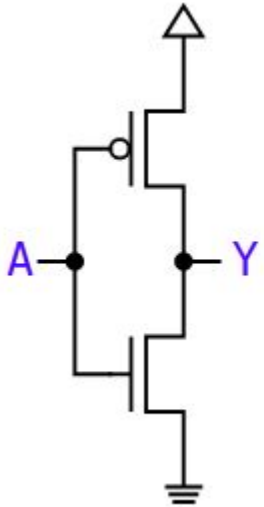
Higher levels of abstraction

Transistor allow us to implement complex equations on higher levels of abstraction.





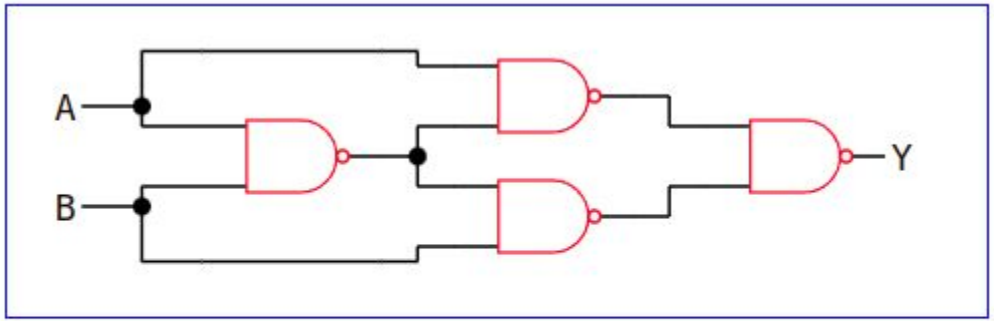




Building Other Gates

An XOR gate can be constructed using four NAND gates.

How many transistors this design has?



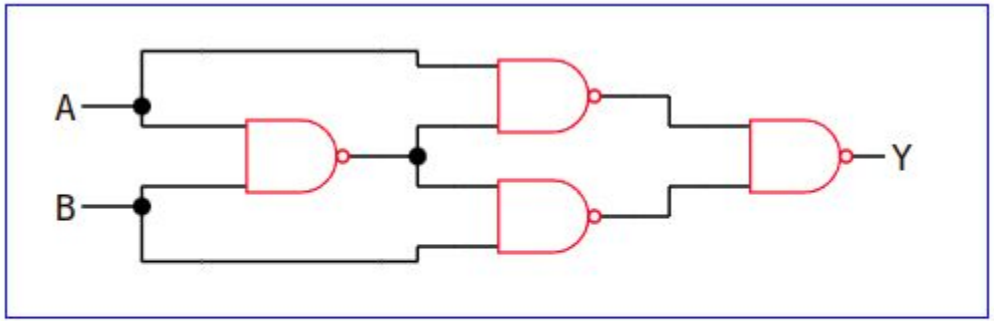
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

An XOR can be constructed with six transistors, all thought this design is not as common.

Building Other Gates

An XOR gate can be constructed using four NAND gates.

How many transistors this design has? 16



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

An XOR can be constructed with six transistors, all thought this design is not as common.

Questions?

Next: Unit 2