ELECTENG 734 - Power Electronics

Laboratory Assignment – Buck Converter

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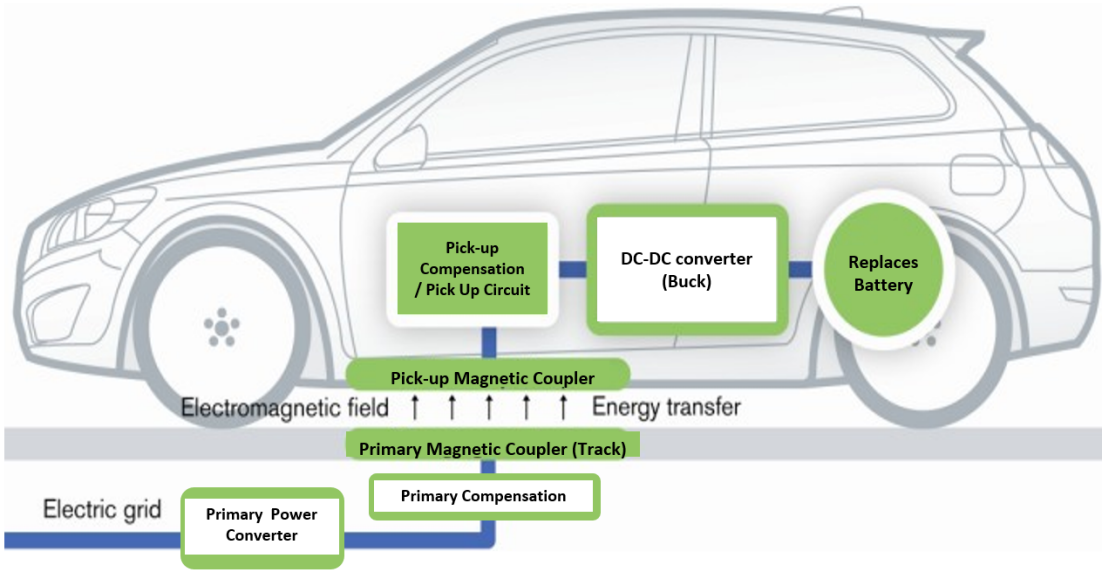
Introduction

In this laboratory you will be performing theoretical calculations as well as simulations using PLECS of a buck converter circuit similar to what you will design and construct later in this course.



Simulation with PLECs

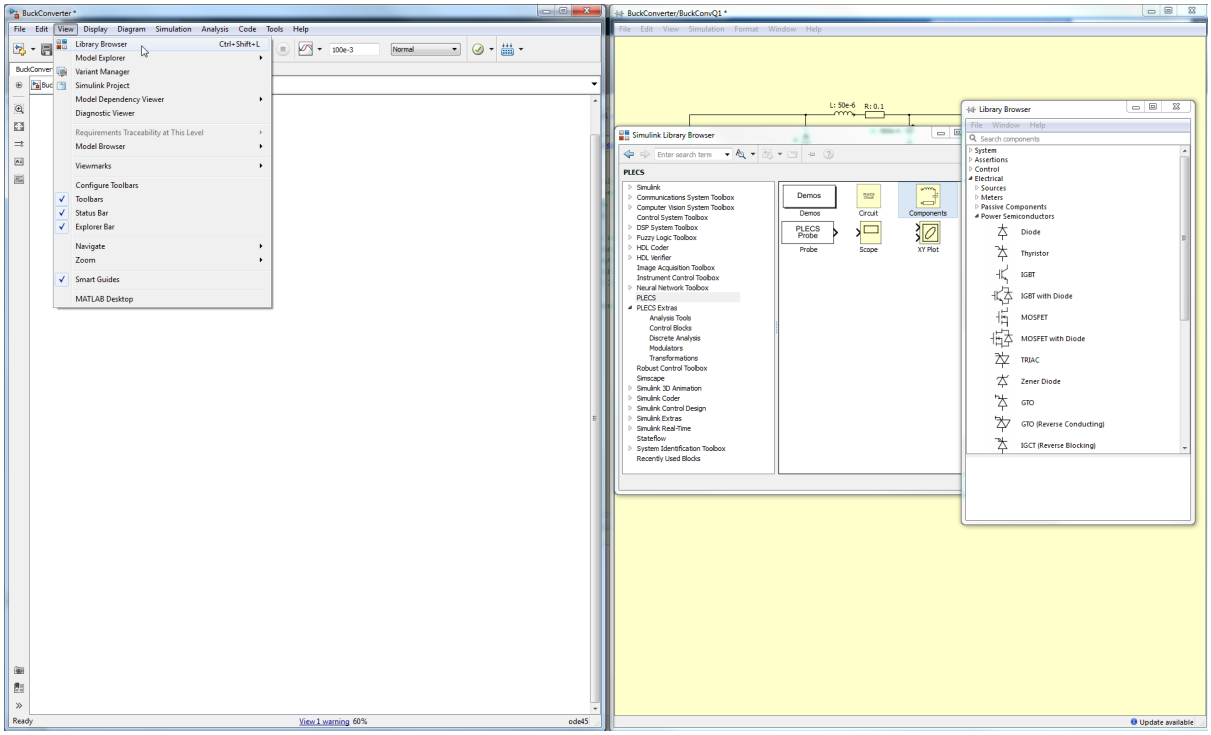
These simulations are run using PLECS Blockset package for Matlab Simulink. To open the simulation software and load a file:

- Open MATLAB
- Open Simulink file Lab_DCDC_Student.slx (*may take a little while to load*)
- Double click on the BuckConvQ1 PLECS circuit to view it (*right click menu will allow you to comment out PLECS circuits)*
- Ctrl-T to run simulation

Note that in PLECS, plots are produced by using a probe block connected to a scope block. Components may be added to the probe block by dragging and dropping them to the open probe block. You may redefine the number of scope channels in the scope if you want to.

You may add components by going (from the Simulink window) View -> Library Browser, then selecting PLECS and double clicking the Components block.

For further information on how to use PLECS refer to the PLECS user manual (www.plexim.com/files/plecsmanual.pdf).



Buck Converter Specifications

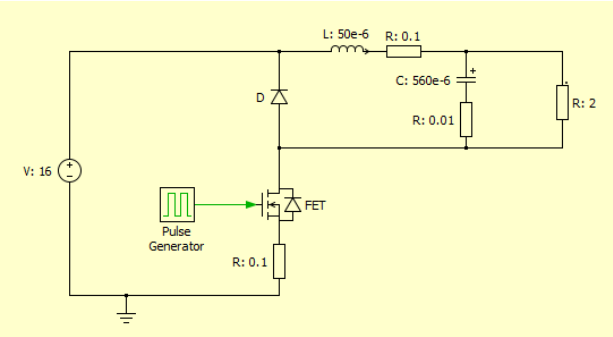
In this lab we will look at the operating principles of the buck converter used in your toy car by simulating an buck converter with following parameters in PLECS.

Parameter	**Symbol**	**Value**	**Unit**
Input Voltage	V_{in}	16	V
Switching Frequency	f_s	100	kHz
Buck Inductor	L	50	μH
Output Capacitor	C	560	μF
Output Capacitor ESR	R_{esr}	10	mΩ
Output Voltage	V_{out}	10	V

Task I – Ideal Voltage Source as Input Source

A partially completed simulation model is provided to you in Lab_DCDC_ Student.slx. Ensure BuckConvQ1 is the only circuit uncommented and double click to open it.

Setup the Buck converter circuit model, which is powered by an ideal voltage source as shown. The pulse generator generates a driver signal to control the switch at a duty-cycle of 62.5% to generate approximately 10 V at the output.



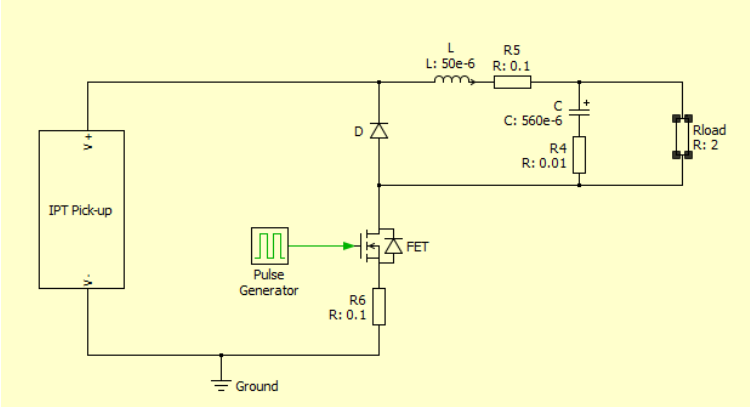
Question

a) Plot the theoretical (assuming ideal conditions) and simulated output voltage and output power for load resistance values of 2, 4, 6, 8 and 10 Ω. You are expected to do individual simulations for each load resistance value.

Task II – IPT Pick-up as Input Source

To investigate the impact of deriving the input to the Buck converter from the IPT pick-up, replace the ideal voltage source with the IPT block as shown and repeat the above exercise. Keep the duty-cycle of the switch constant at 62.5%.

A partially completed simulation model is provided to you, simply comment out BuckConvQ1 and ensure BuckConvQ2 is the only circuit uncommented and double click to open it.



Questions

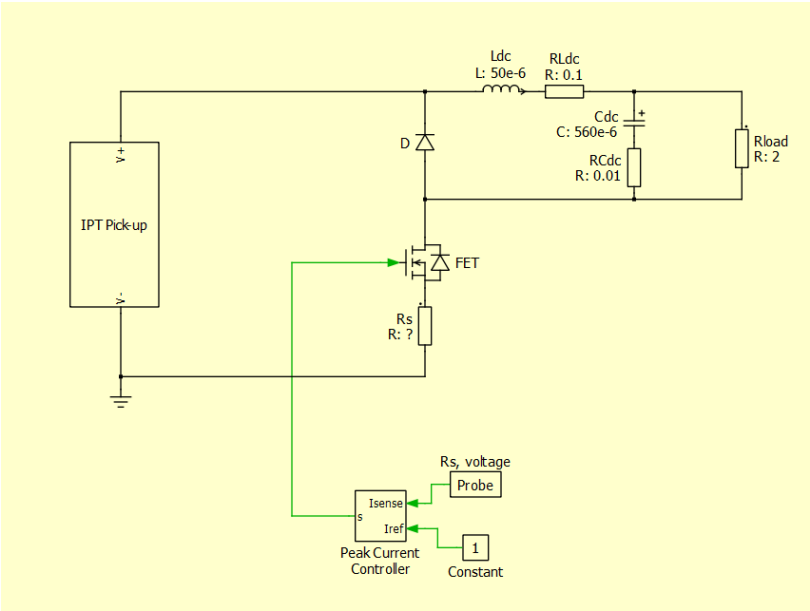
a) Plot the theoretical (assuming ideal conditions) and simulated output voltage and output power for load resistance values of 2, 4, 6, 8 and 10 Ω. You are expected to do individual simulations for each load resistance value.

b) Why is the power delivered to the load different in comparison to what you observed in Task I? At which load resistance do you observe maximum output power? Why?

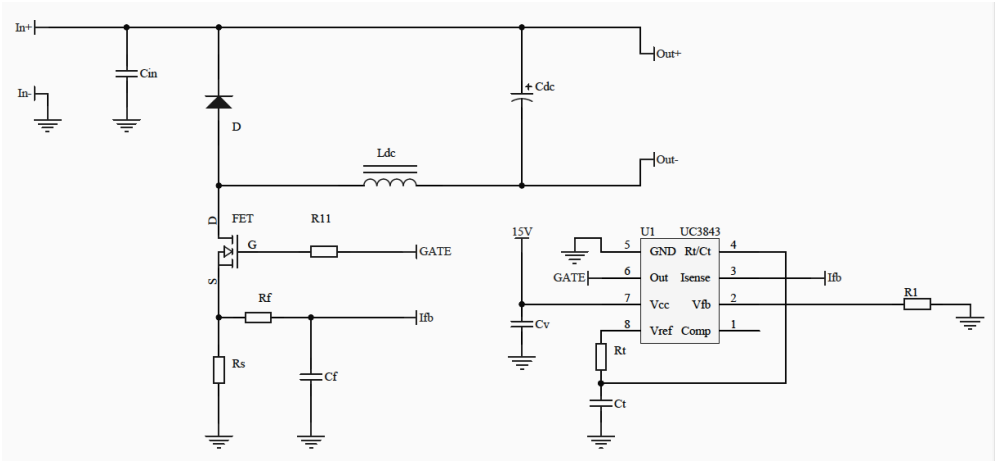
Task III – Current Loop

A current mode controller block is available in PLECS, which is a simplification of what an electronic implementation of a current mode controller similar to UC3843 would be. You can learn more about the Peak Current Controller block by double clicking on the block.

A partially completed simulation model is provided to you, simply comment out BuckConvQ2 and ensure BuckConvQ3 is the only circuit uncommented and double click to open it.



Note that a real implementation of a peak current mode controller using UC3843 in shown below. Read the UC3843 datasheet and application notes to learn more about the implementation.



Add a peak current mode controller to limit the peak current through the switch to $I_{L(avg)} + \frac{\Delta I_L}{2}$ at a 2 Ω load (A peak current controller is usually designed for the maximum current, and in this example peak current is observed at the 2 Ω load). As discussed in the lectures (non-ideal buck converter design example) $I_{L(avg)}$ at 2 Ω load is the value of average inductor current that will deliver maximum available input power from the pick-up circuit to the output load of the buck-converter. To set the peak inductor current, change the value of R_S since with I_{ref} set as 1 V the peak current will be $I_{L(peak)} = \frac{1}{R_s}$ (refer to the UC3843 data sheet and application notes regarding how Rs sets the peak current). Assume a conversion efficiency of 90% for your calculations ($\eta = \frac{P_{out}}{P_{in}} = 0.9$).

Question

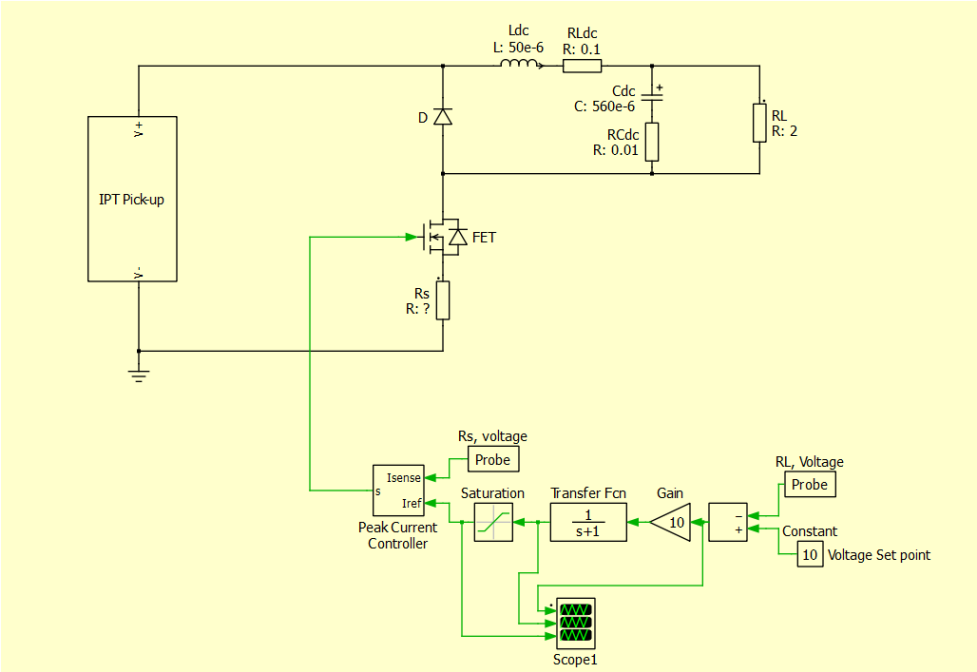
a) Observe simulation results for output voltage, output power and inductor current for 2, 4, 6, 8 and 10 Ω load. Note down the results and discuss the difference in comparison to what you observed in the previous tasks. Plot the theoretical (assuming ideal conditions) and simulated output voltage and output power for these load resistance values.

Task IV – Voltage Loop

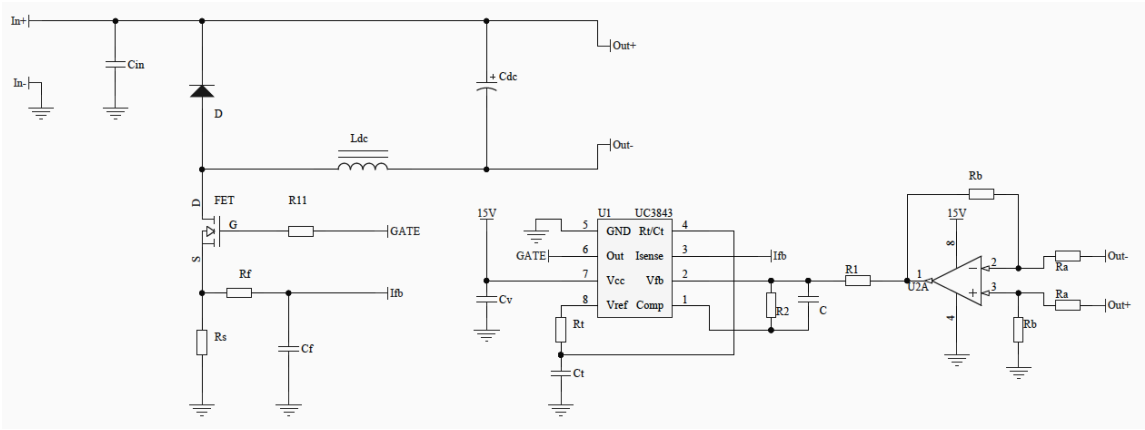
Now add a voltage feedback loop to the current mode controller design to regulate the output voltage to 10 V.

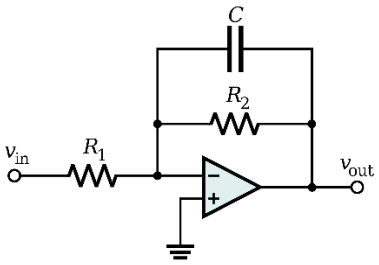
A partially completed simulation model is provided to you, simply comment out BuckConvQ3 and ensure BuckConvQ4 is the only circuit uncommented and double click to open it.

As discussed in the lectures a compensator is required to improve the response of the controller by negating the effect of the LHP zero caused by the output capacitor and its ESR. This is implemented in PLECS as a Transfer Function block. A gain block is used to set the low-frequency gain of the controller.



Note that a real implementation of a controller using UC3843 is shown below. The gain of the error amplifier circuit is given below, where the values of the resistors required for implementation can be derived by relating to the gain and transfer function block. Read the UC3843 datasheet and application notes to learn more about the implementation.





$$Gain = \frac{R_2}{R_1} \times \frac{\frac{1}{CR_2}}{s + \frac{1}{CR_2}}$$

Design the voltage feedback circuit to limit the output voltage to 10V.

Question

a) Observe simulation results for output voltage, output power and inductor current for 2, 4, 6, 8 and 10 Ω load. Note down the results and discuss the difference in comparison to what you observed in the previous tasks. Plot the theoretical (assuming ideal conditions) and simulated output voltage and output power for these load resistance values.

Optional Tasks

a) Analyse loop response of the buck converter. (Use the impulse response analysis tool.)

b) Investigate losses of the buck converter. (*Thermal simulation is done separately and thus is not included in standard simulation. Resistance losses can be measured from Pin – Pout, but switch losses and diode losses need to be accounted for in thermal simulation.*)