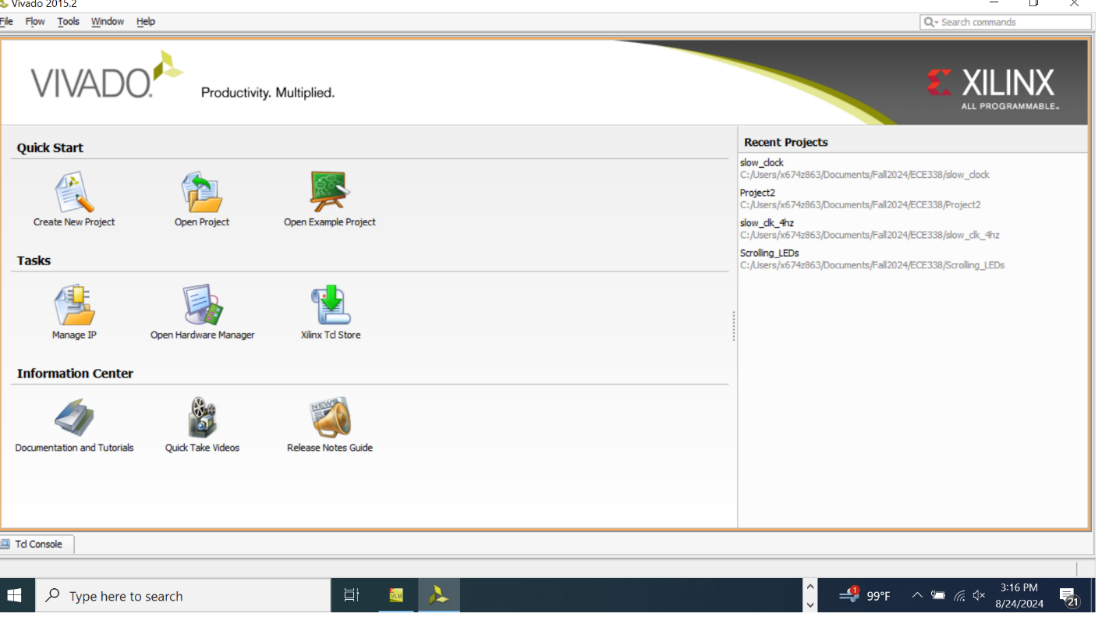
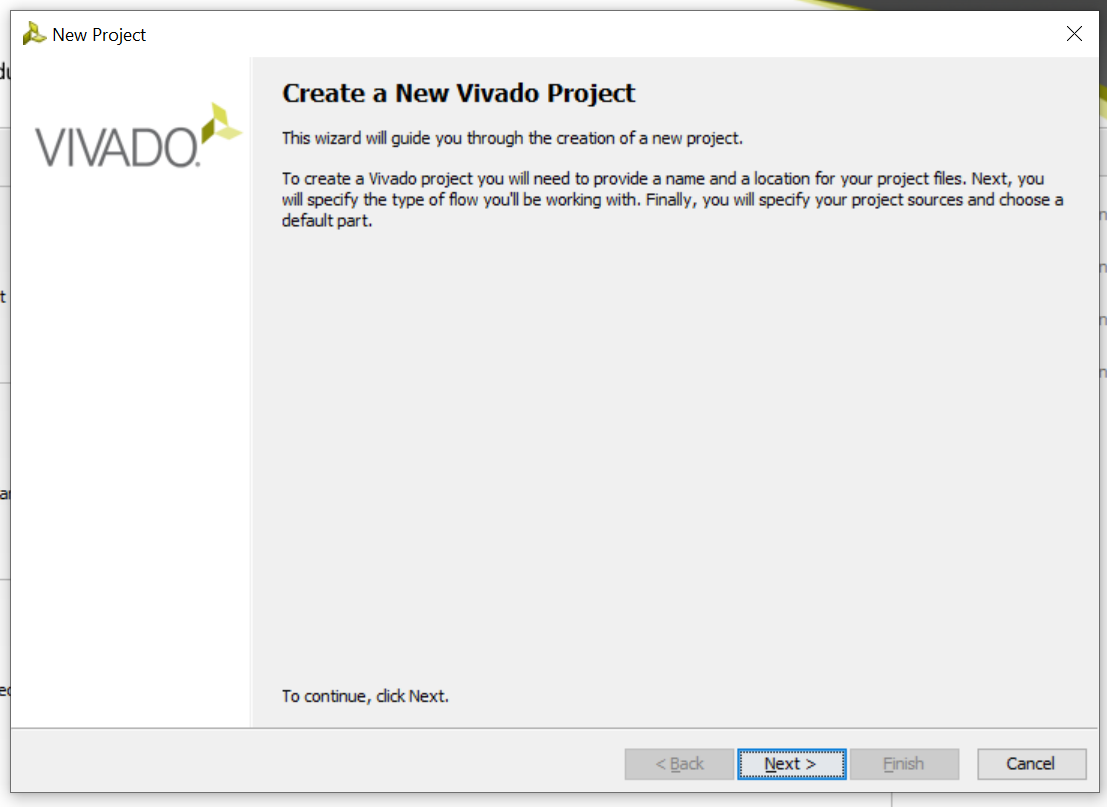
**Introduction to Xilinx Vivado environment with blinking led project:**

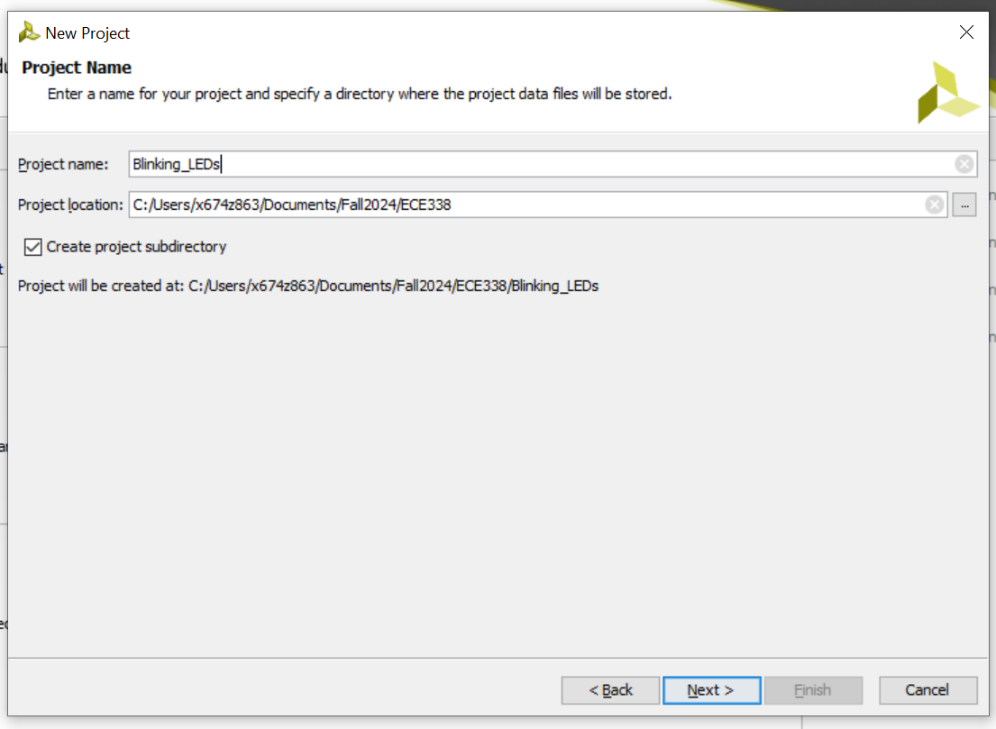
Start Vivado Design Suite by clicking on Vivado icon



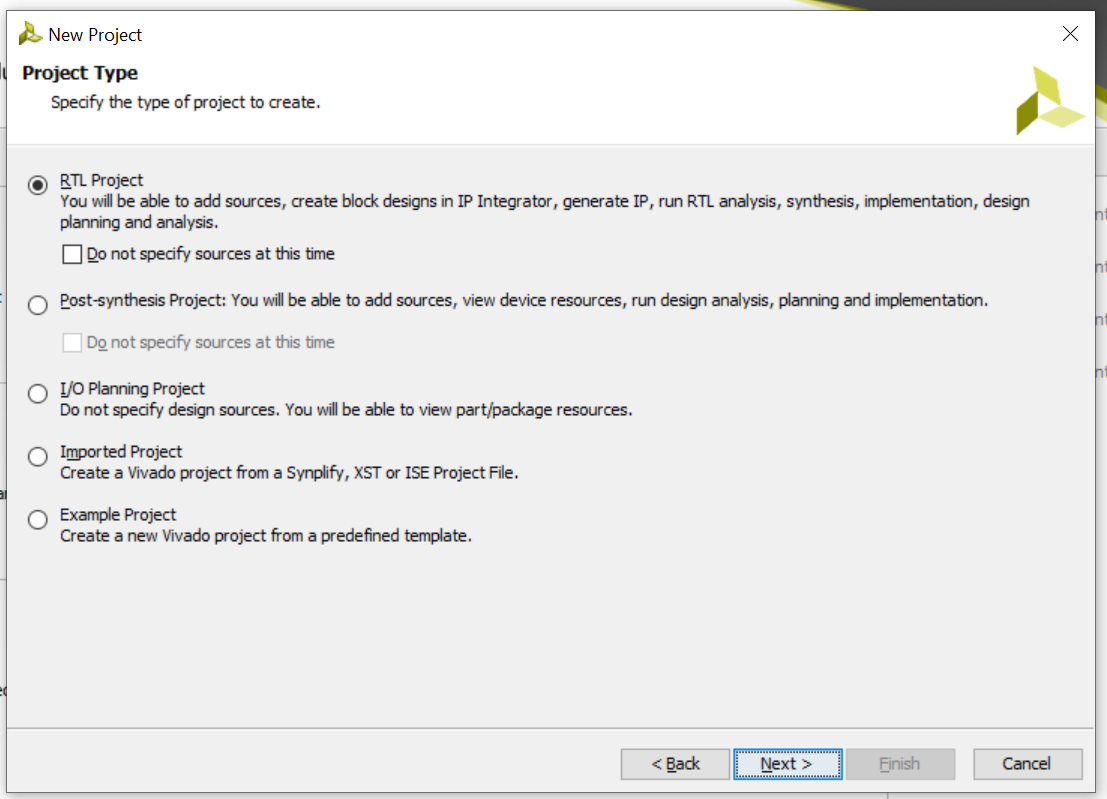
Select Create New Project.

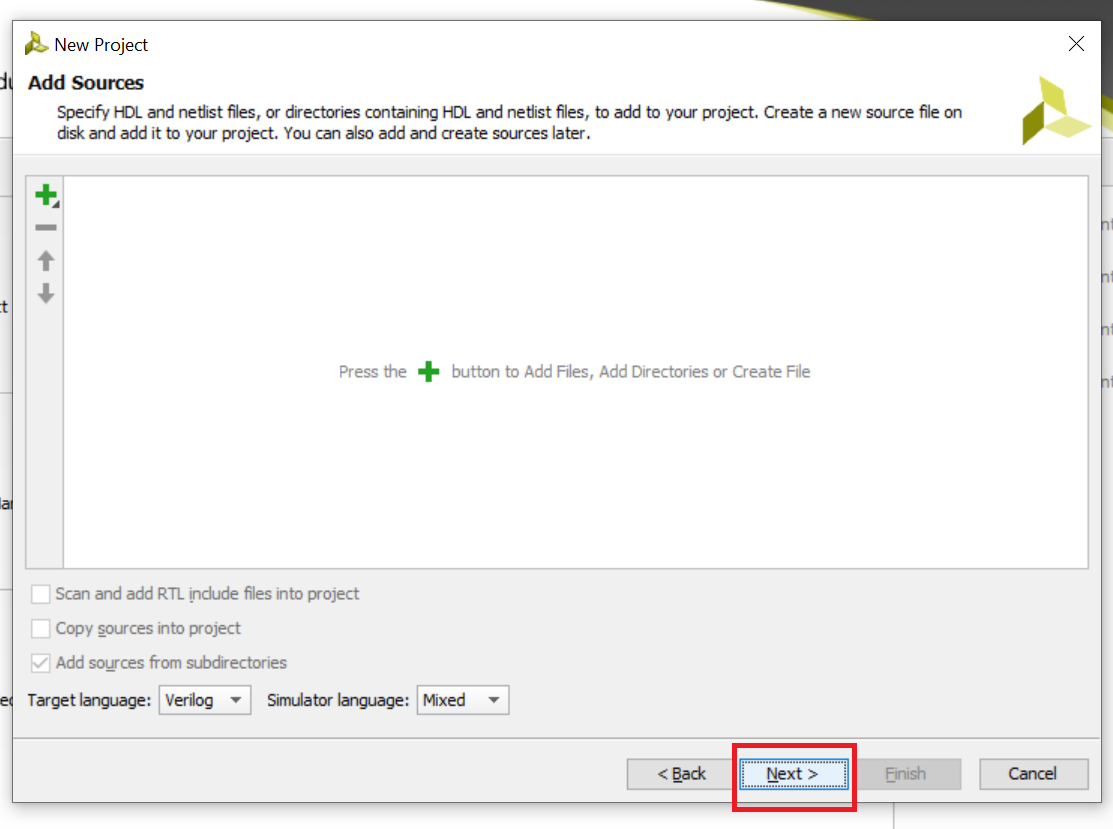


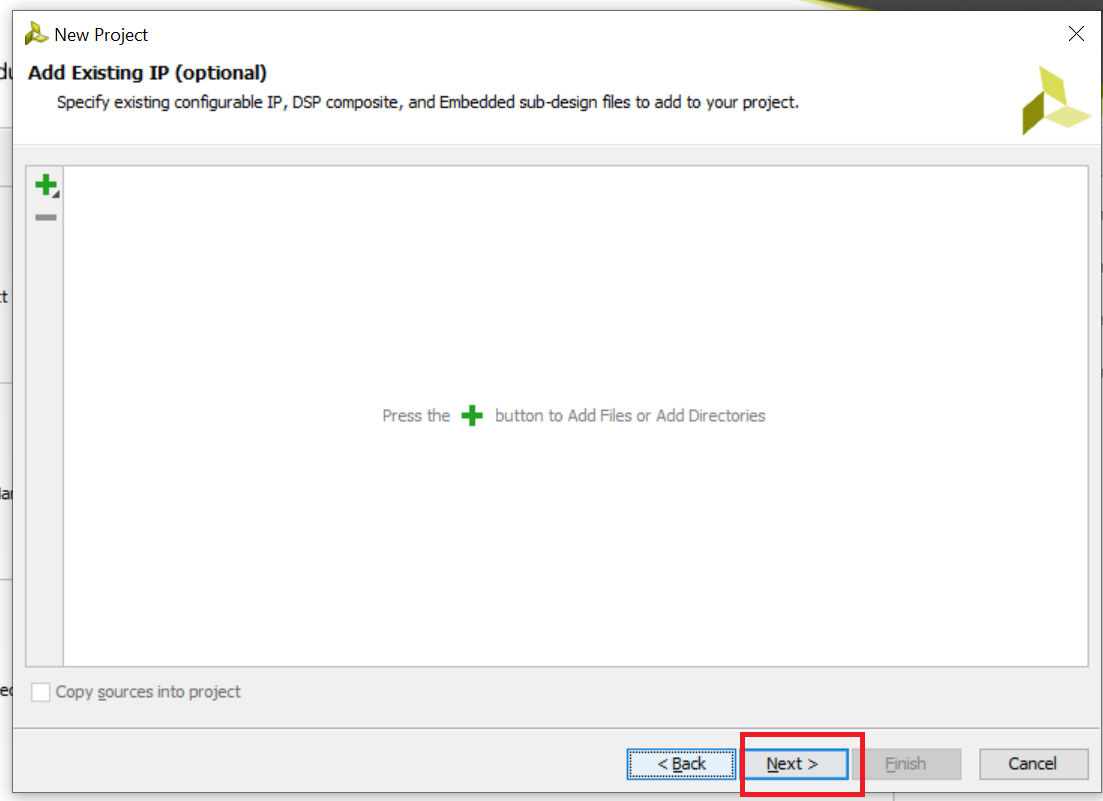
Click Next and then enter a Project name and location for your project

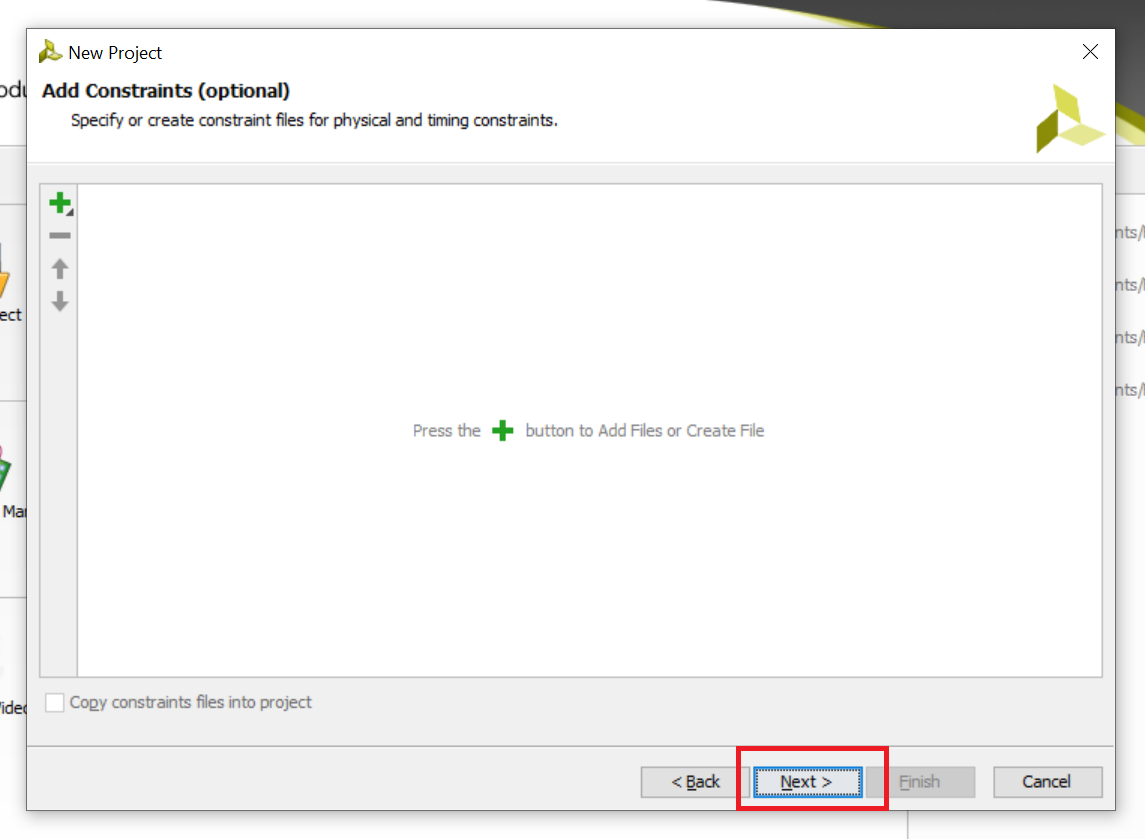


Click Next and select the RTL project type





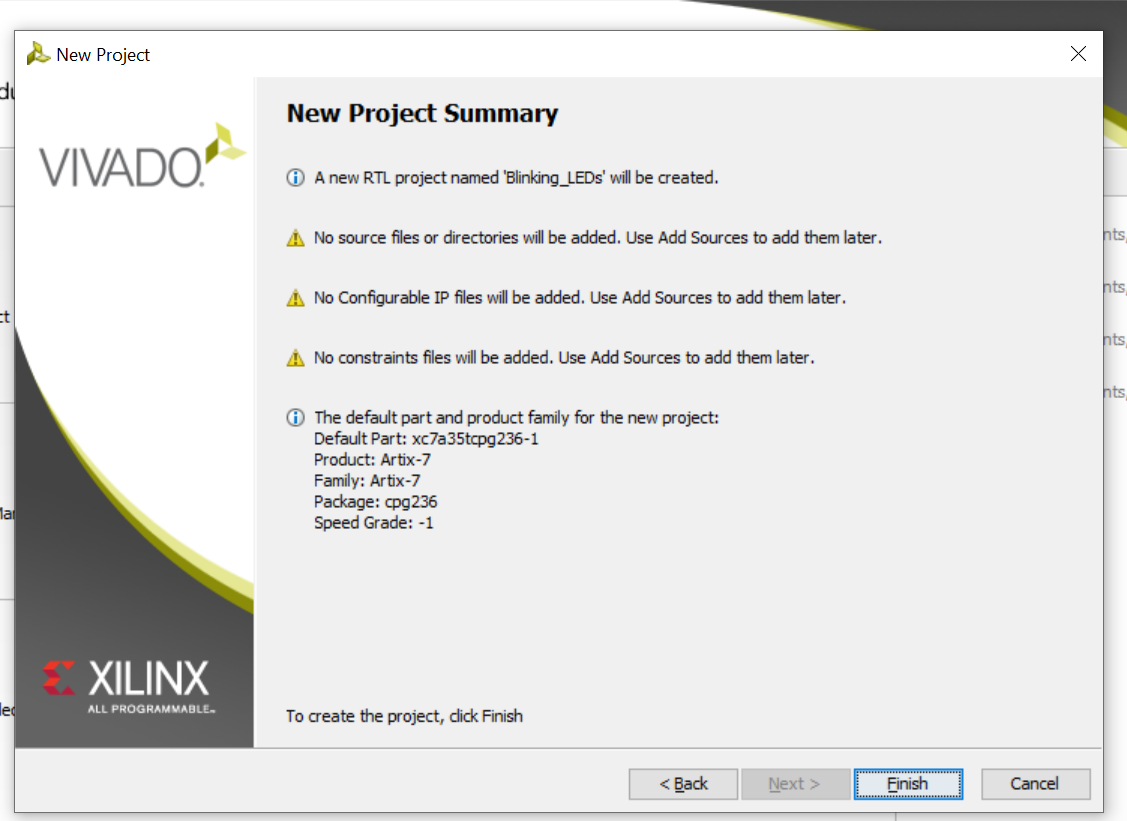




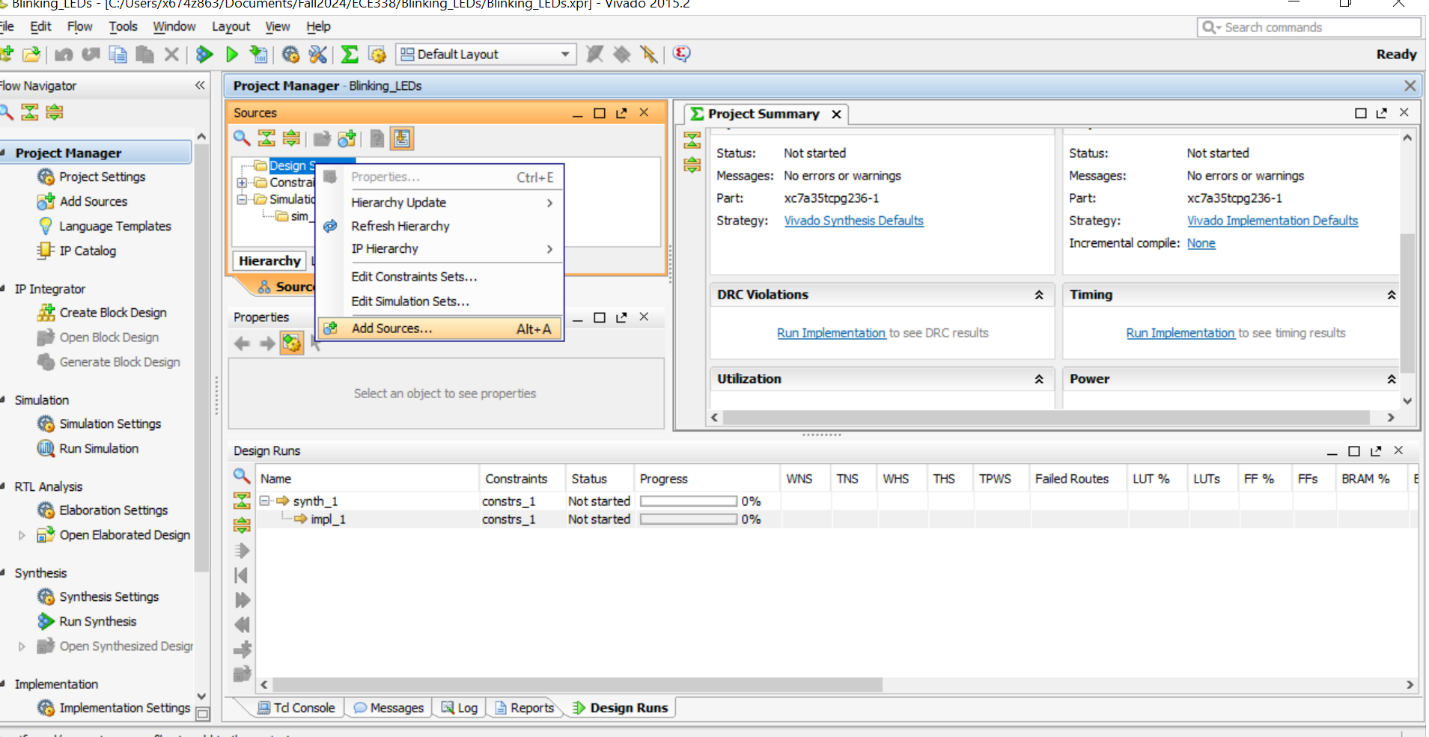
Select the correct Xilinx FPGA that is on the Basys3 board (XC7A35T-1CPG236C)

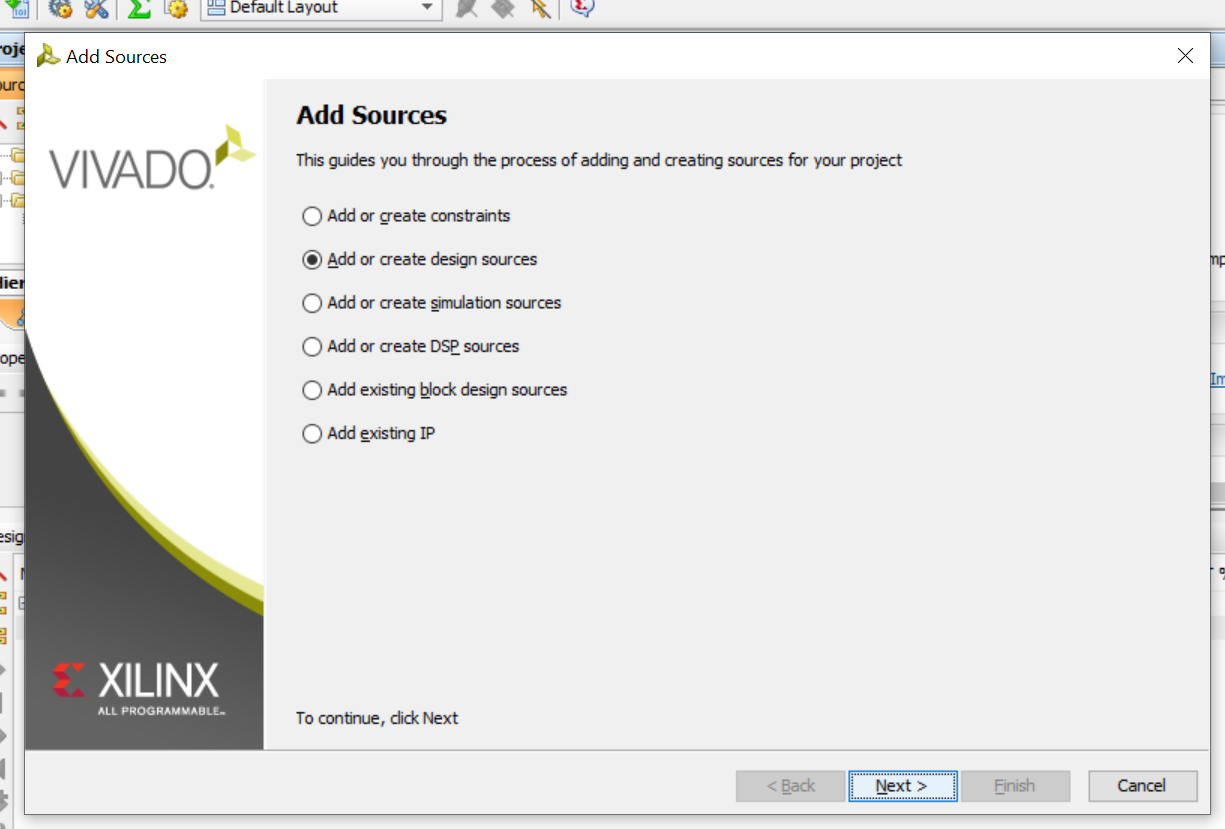


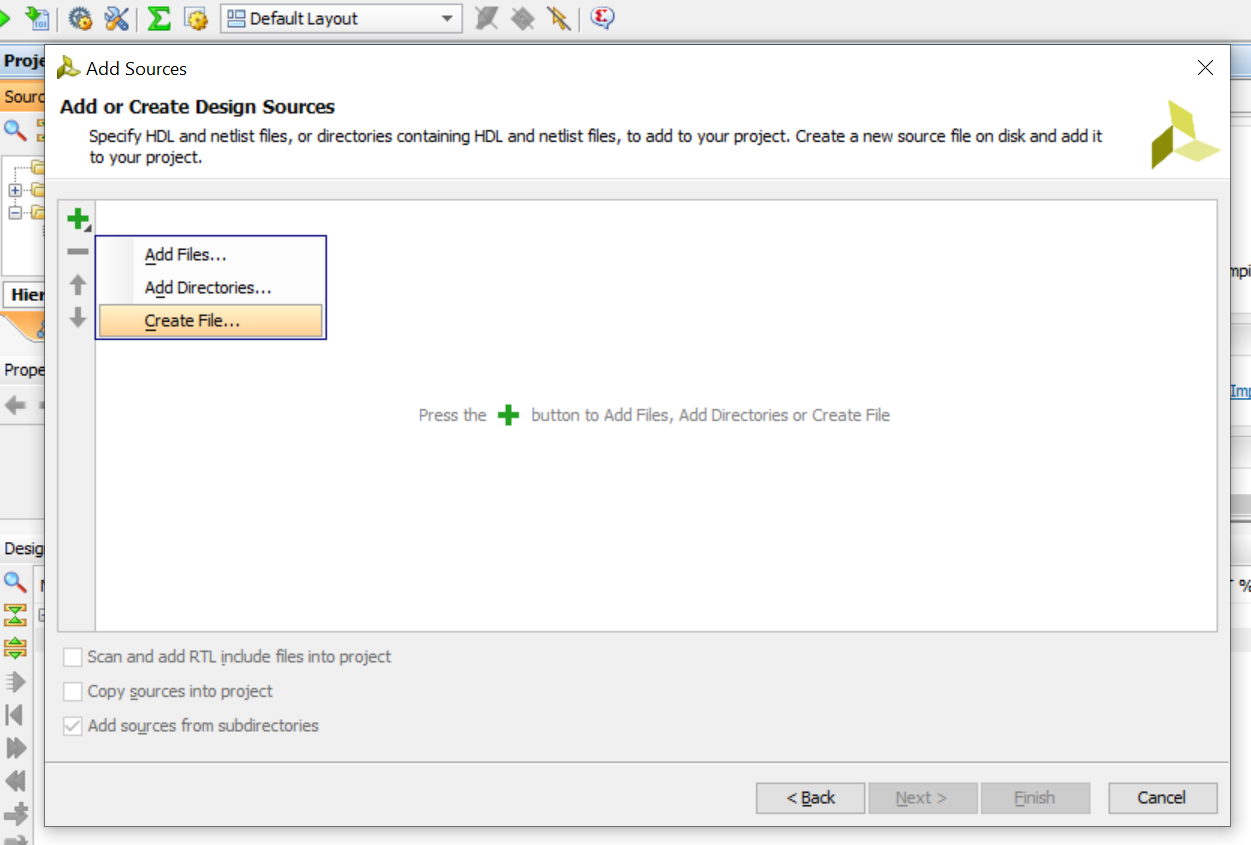
Click Next, and then Finish

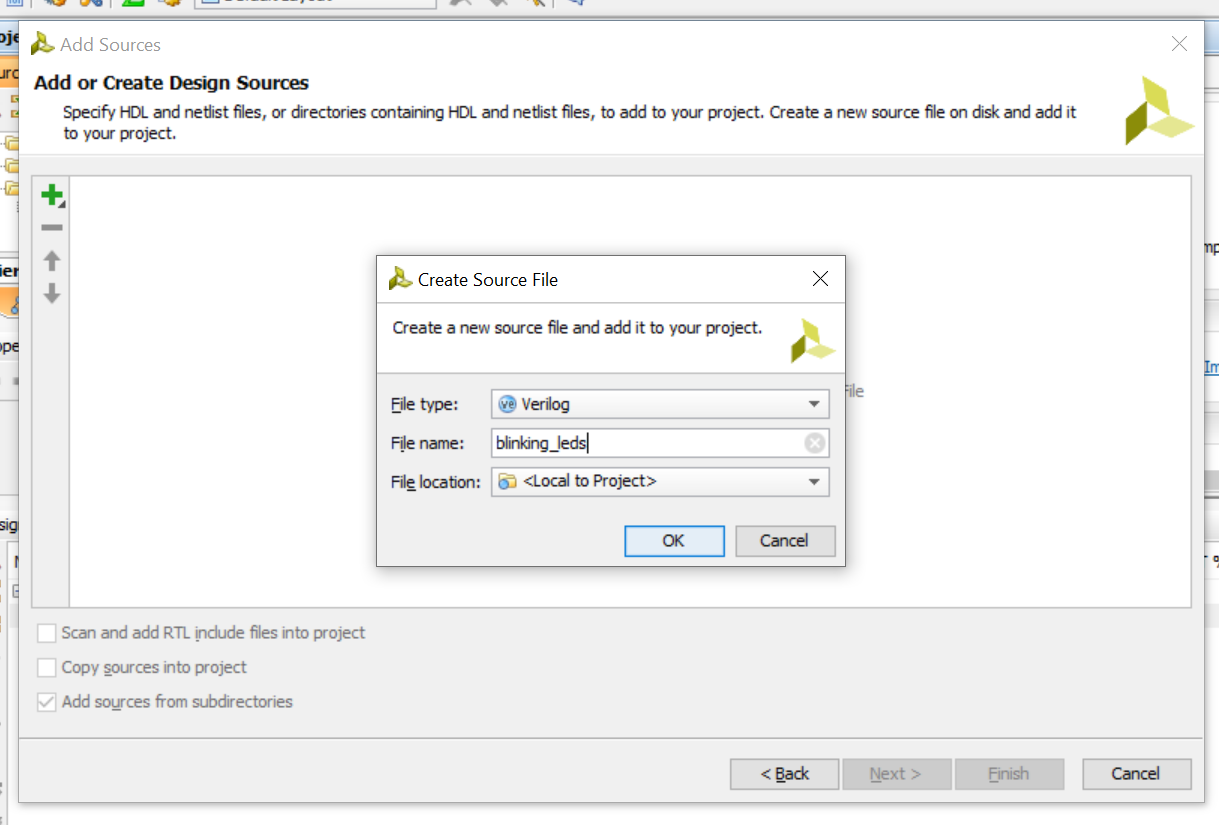


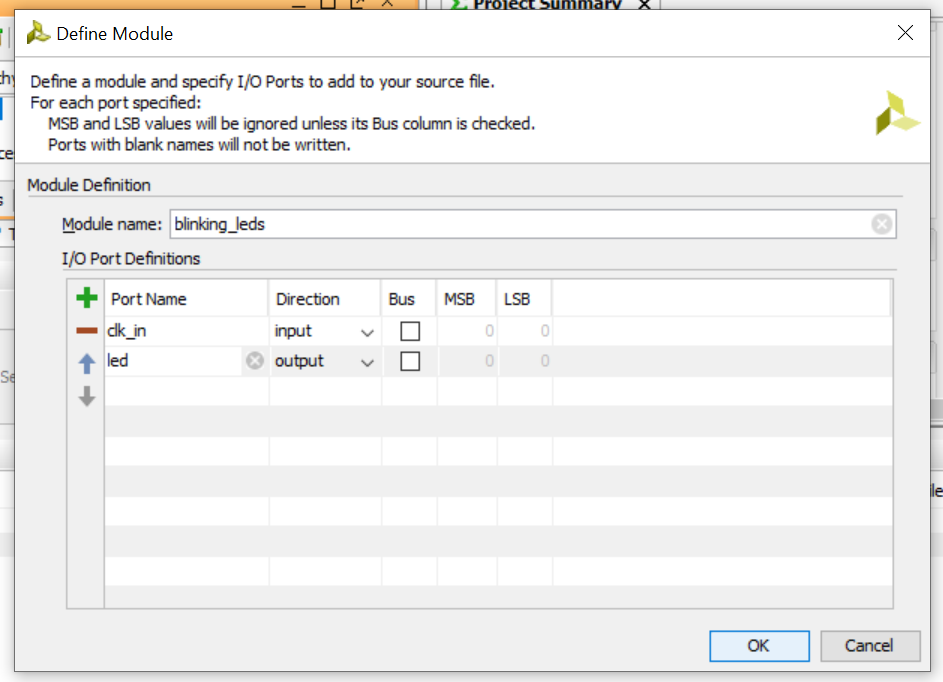
The Project window opens. We now need to add a Verilog design source to describe our blinking led project

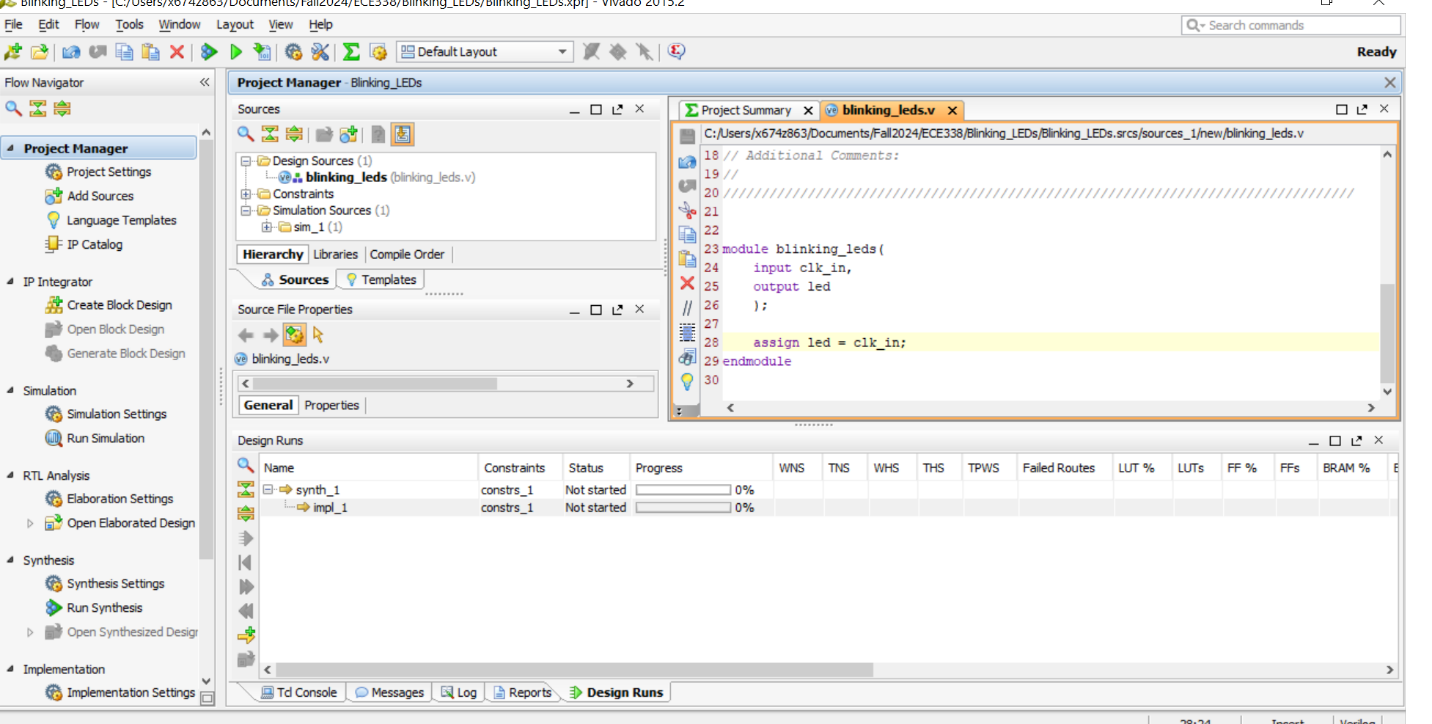


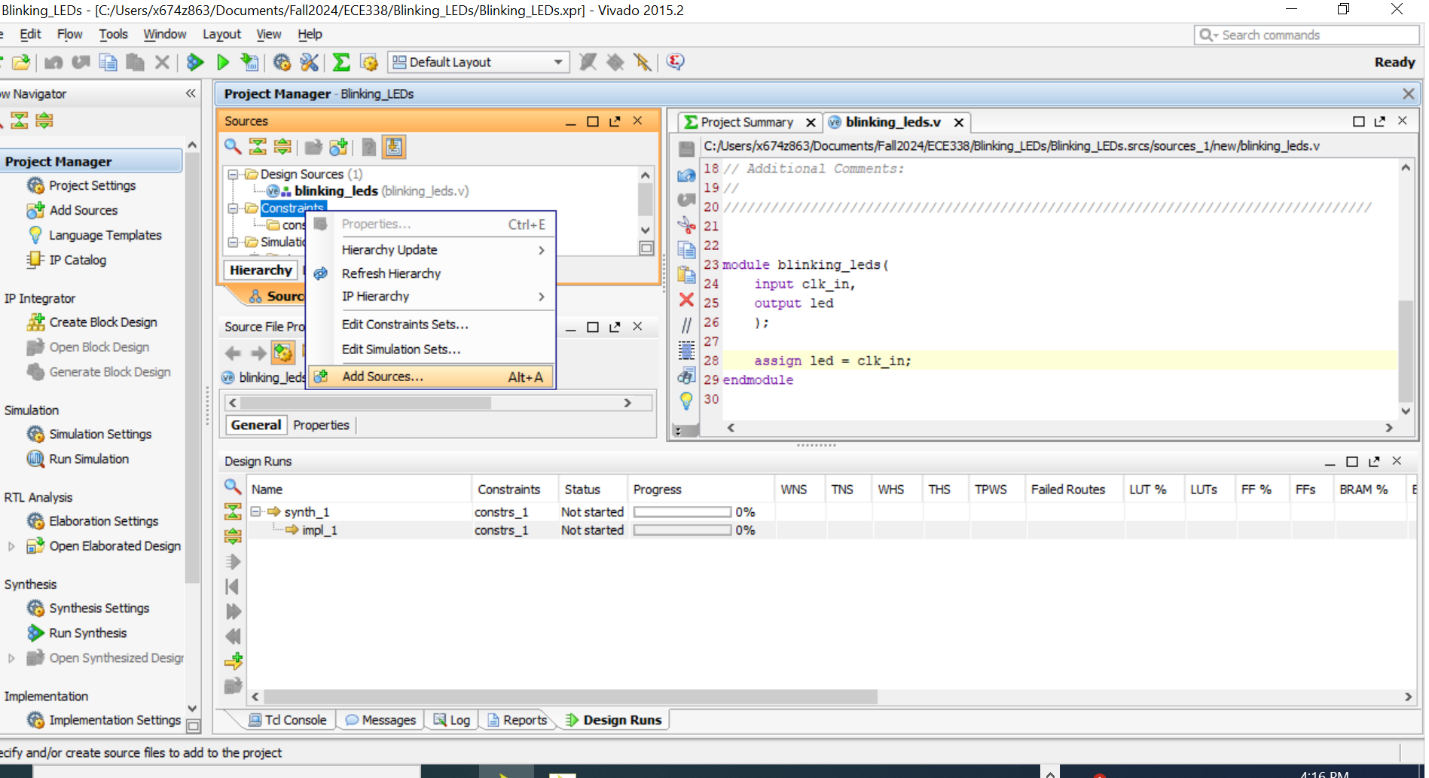


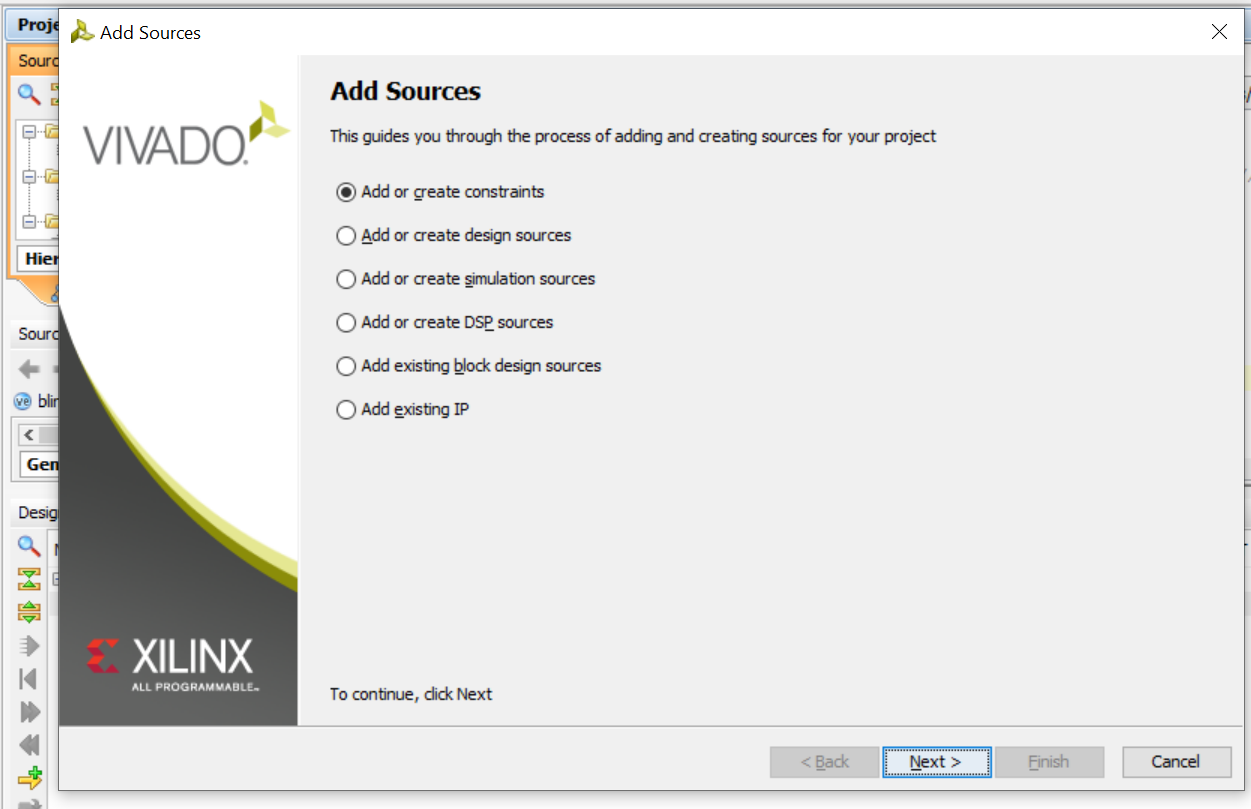


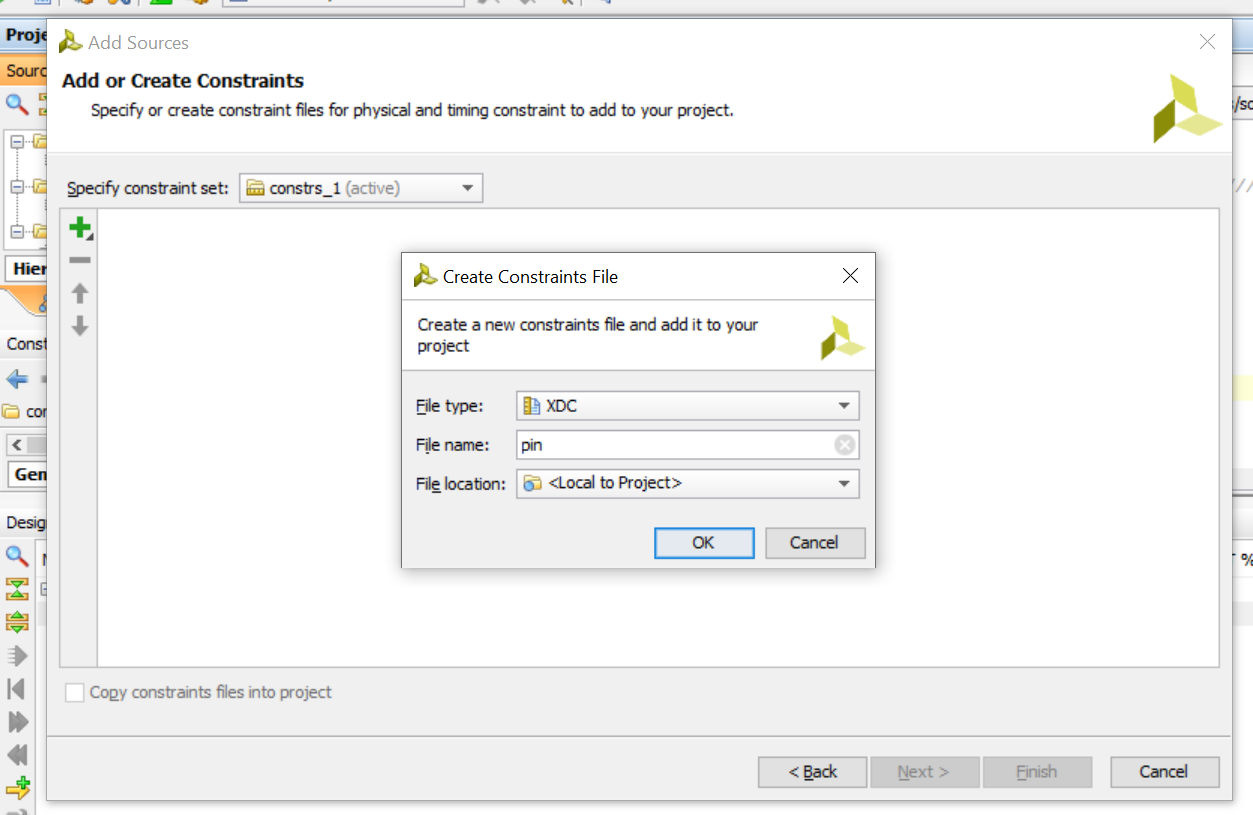


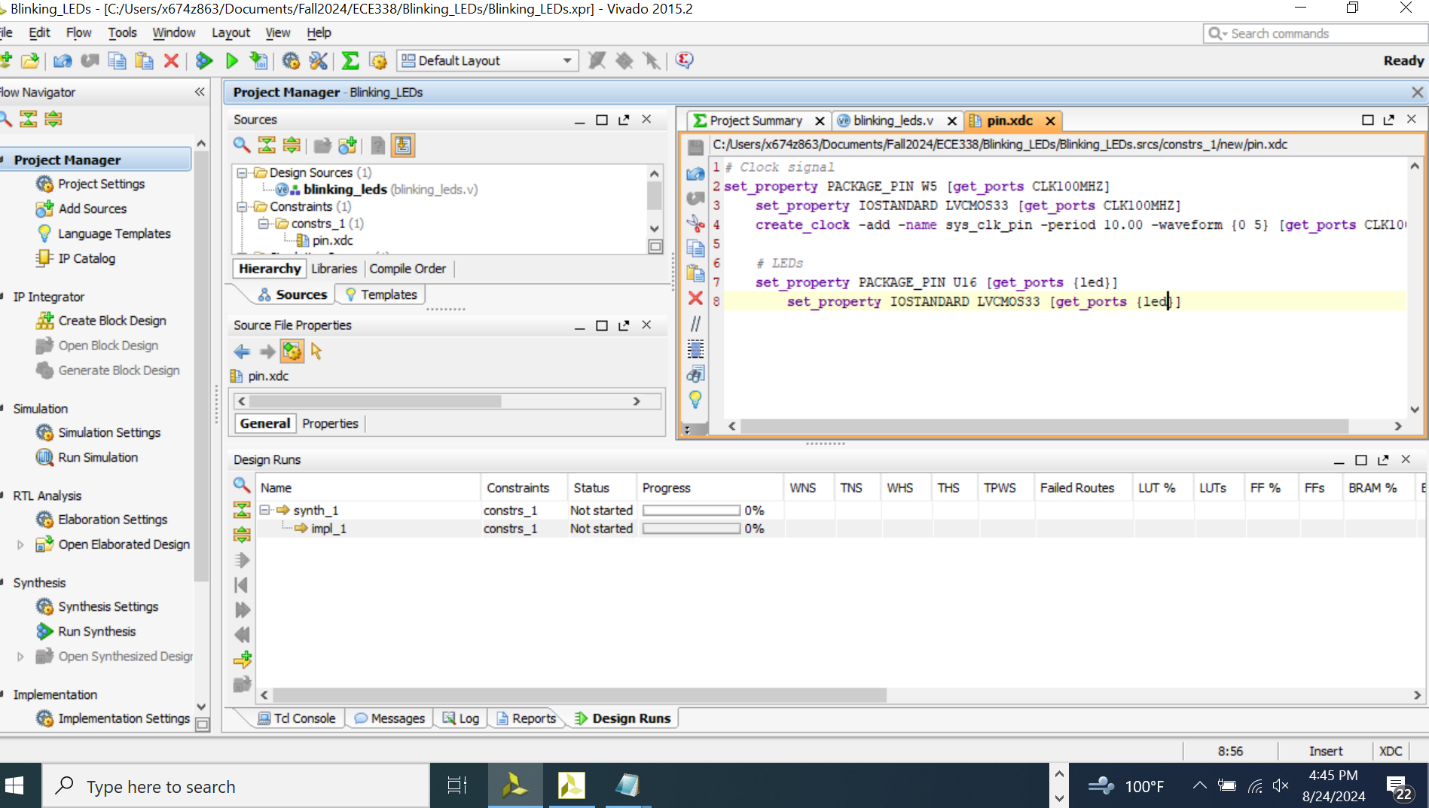


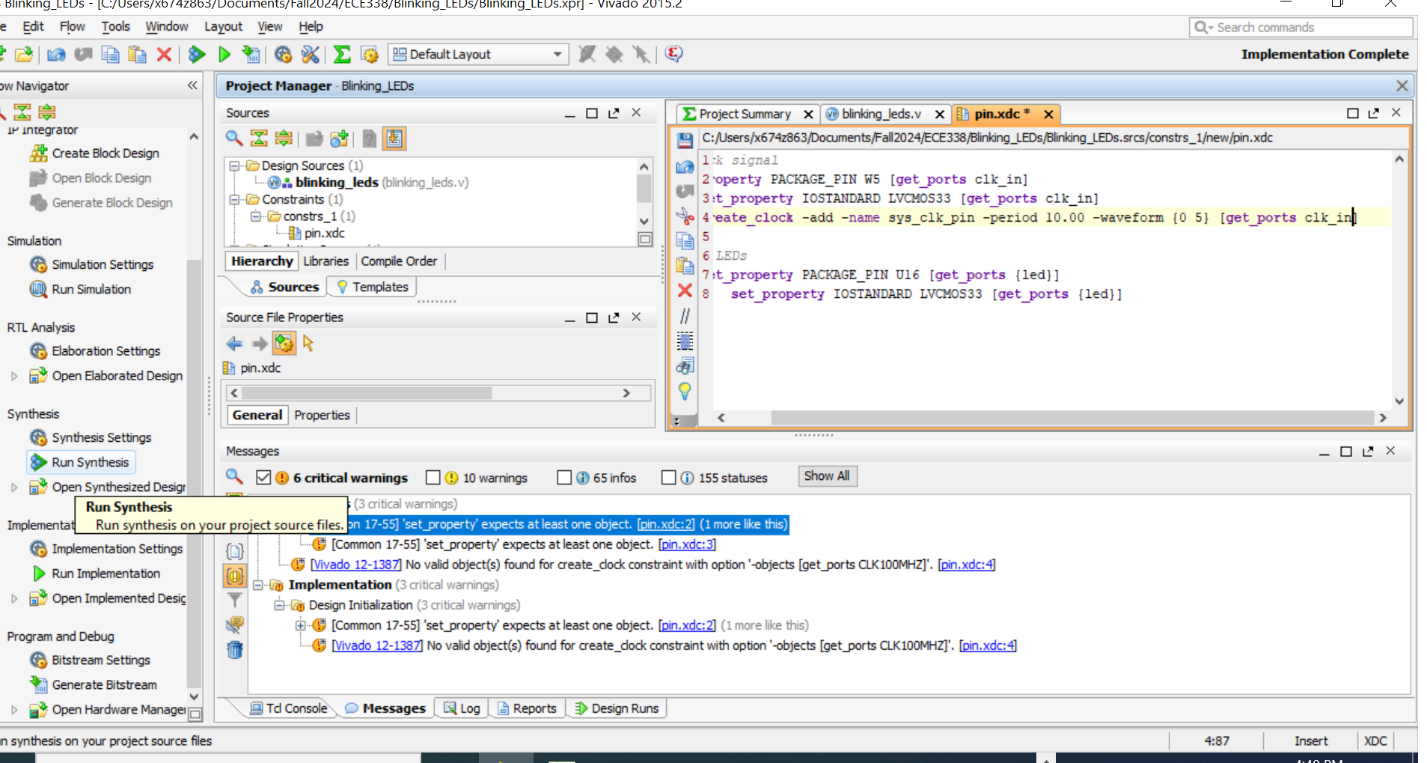


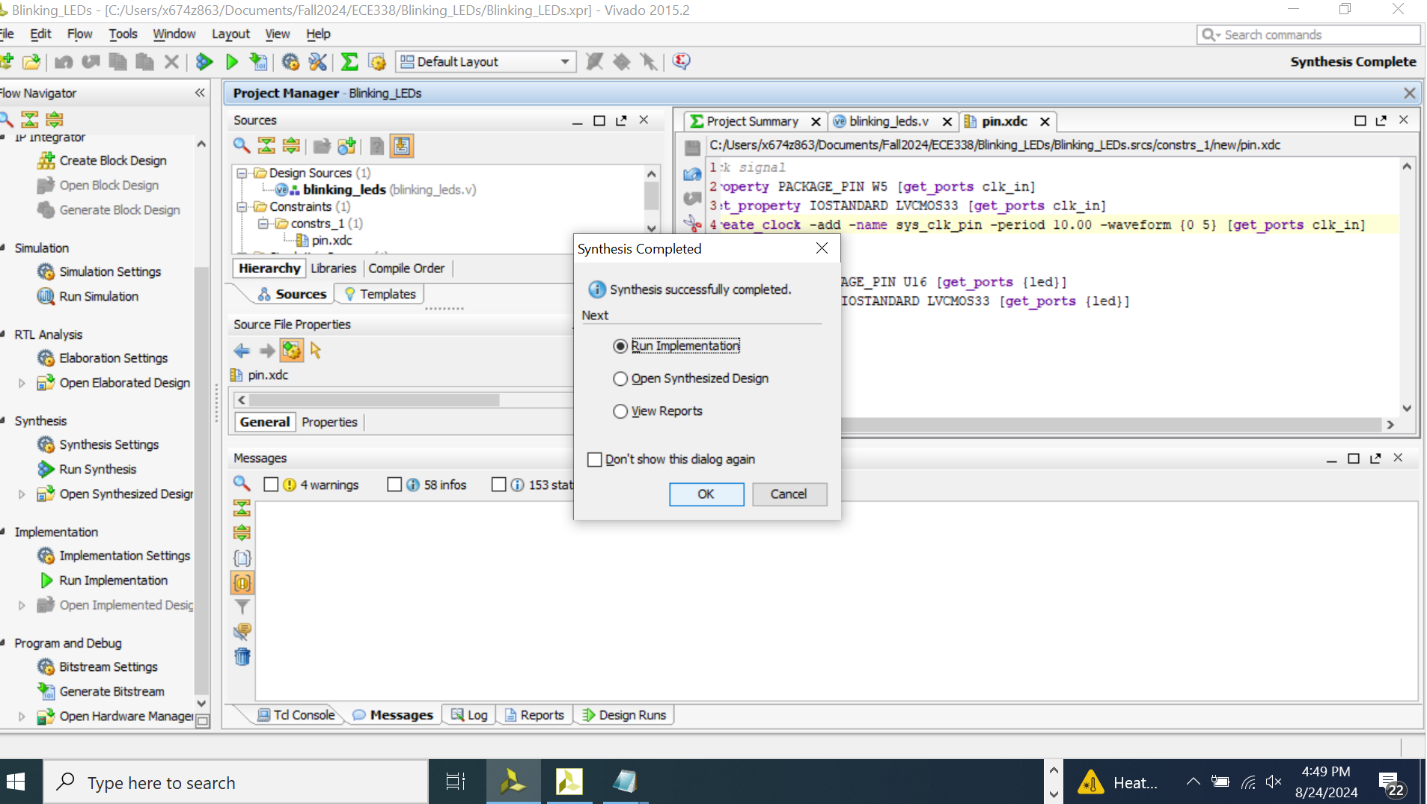






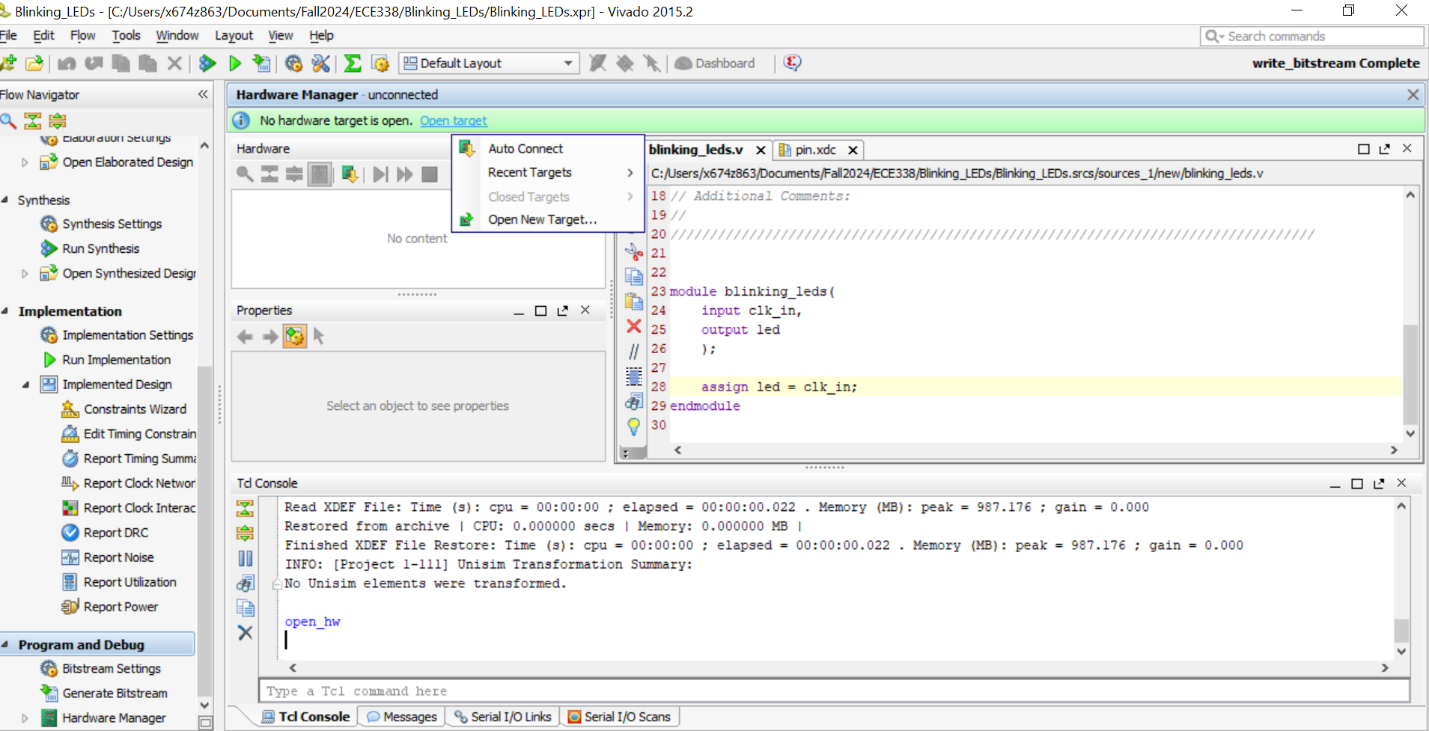




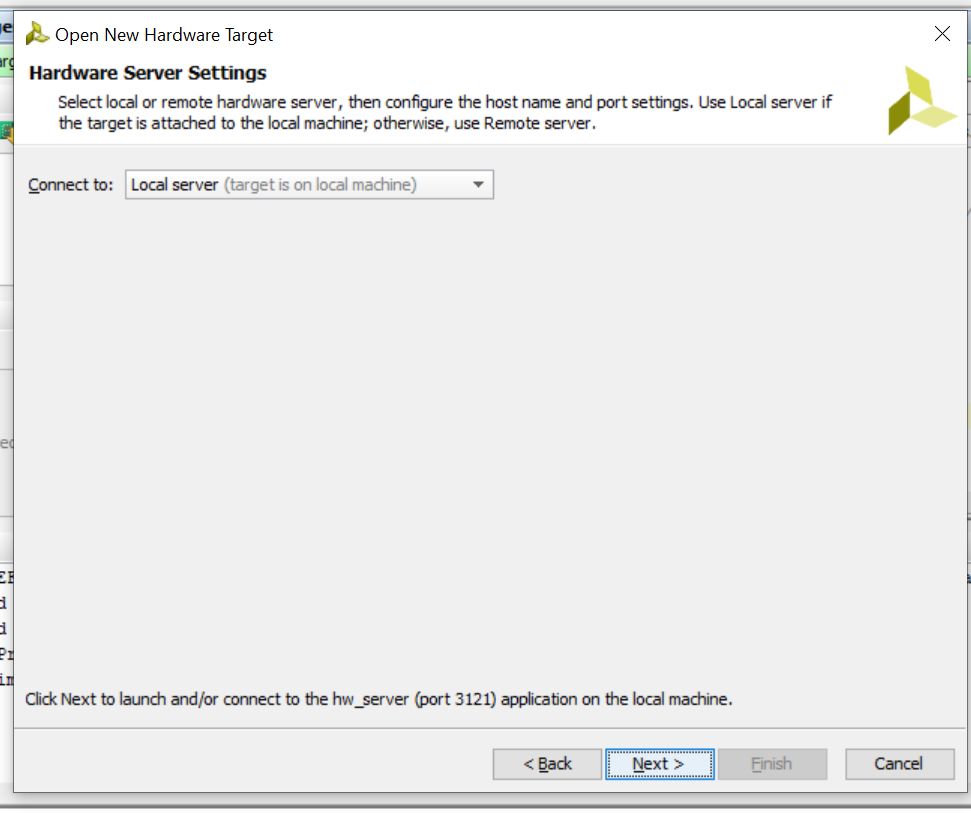


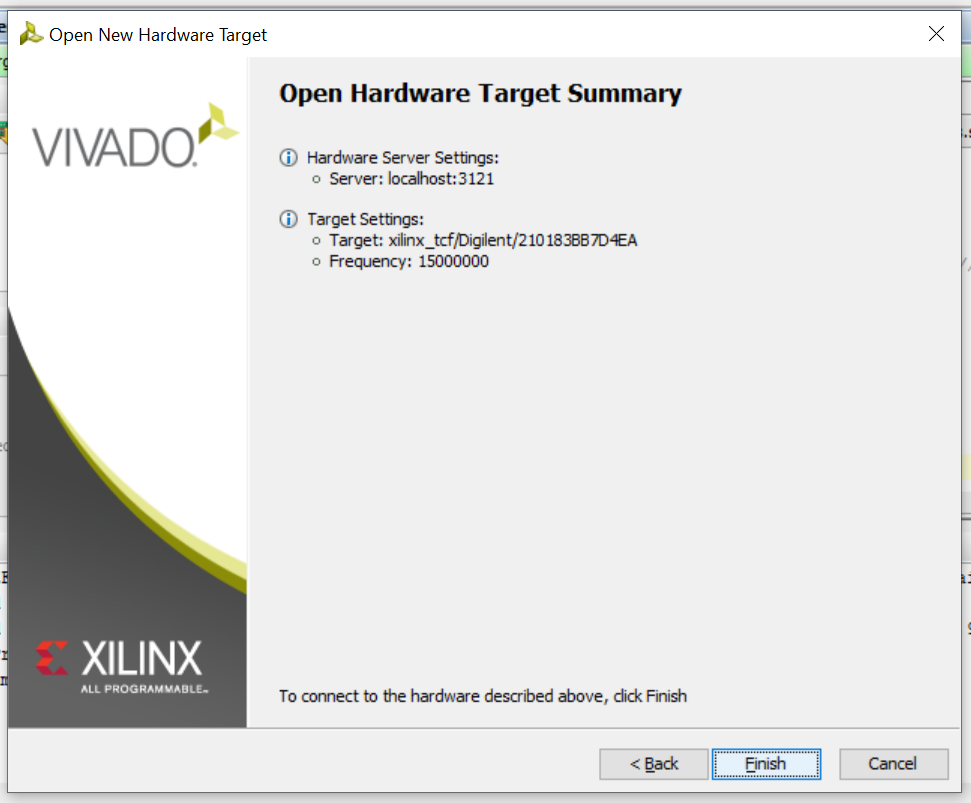
We can now generate the bitstream. Click on Generate Bitstream in the Project Manager window.

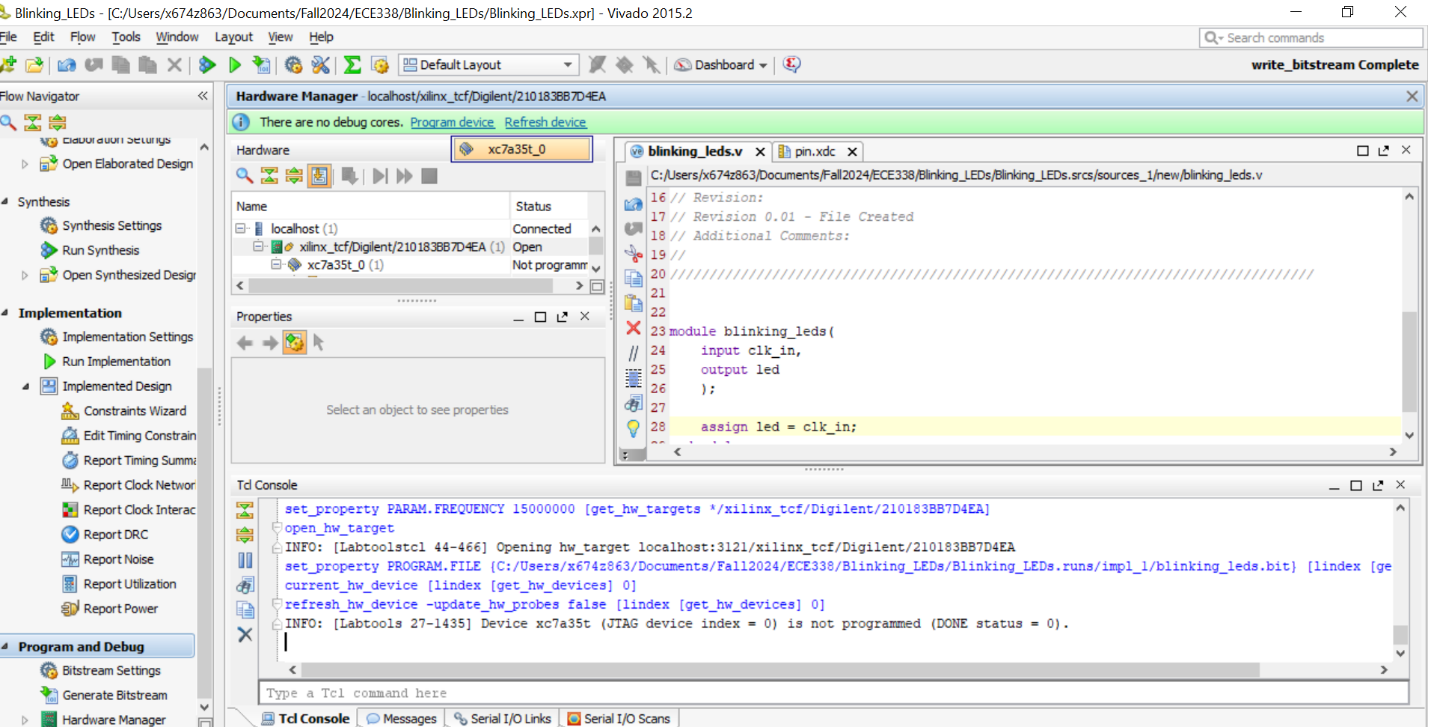
Next step is to program the FPGA with the bitsream.

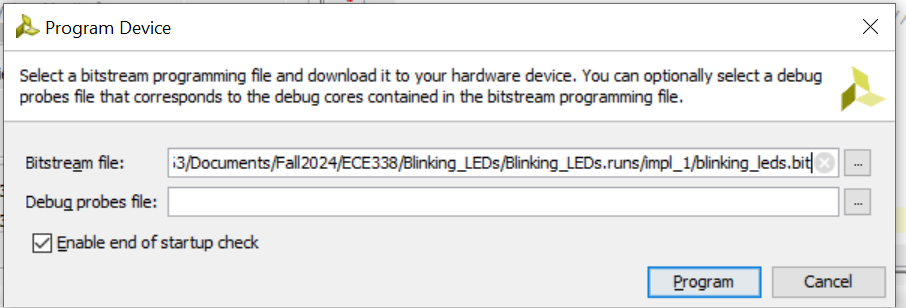












Congratulations!

You have entered a design and then Synthesized, Implemented, and programmed the FPGA with

the generated bit file. This was a simple design example but the same steps are just repeated for

any design.