Seat No -

Total number of questions : 60

11342_High Performance Computing

Time : 1hr

Max Marks : 50

N.B

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A : Mandatory Instructions/sec

B : Millions of Instructions/sec

C : Most of Instructions/sec

D : Many Instructions / sec

Q.no 2. Depth First Search is equivalent to which of the traversal in the Binary Trees?

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Q.no 3. Regarding implementation of Breadth First Search using queues, what is the maximum distance between two nodes present in the queue? (considering each edge length 1)

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C : 6

D : 8

Q.no 10. Which of the following is not an in-place sorting algorithm?

A : Selection sort

B : Heap sort

C : Quick Sort

D : Merge sort

Q.no 11. The time complexity of heap sort in worst case is

A : O(log n)

B : O(n)

C : O(nlogn)

D : O(n^2)

Q.no 12. Most message-passing programs are written using

A : the single program multiple data (SPMD) model.

B : the multiple program and single data(MPSD) model

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B : Dividing no of processors

C : Dividing number of tasks

D : Dividing number of operation

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A : symetric Paradigm

B : asymetric Paradigm

C : asynchronous paradigm

D : synchronous paradigm

Q.no 15. Following is not mapping technique

A : Static Mapping

B : Dynamic Mapping

C : Hybrid Mapping

D : All of Above

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B : When the graph is a Linked List

C : When the graph is a n-ary Tree

D : When the graph is a Ternary Tree

Q.no 21. Which of the following is not an application of Depth First Search?

A : For generating topological sort of a graph

B : For generating Strongly Connected Components of a directed graph

C : Detecting cycles in the graph

D : Peer to Peer Networks

Q.no 22. The logical view of a machine supporting the message-passing paradigm consists of p processes, each with its own _____

A : Partitioned Address space

B : Exclusive address space

C : Logical Adress Space

D : Non shared Adress Space

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B : stack

C : both program counter and stack

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C : Deadlock

D : Starvation

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A : Centralized computing

B : Decentralized computing

C : Parallel computing

D : All of Above

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C : Parallel development

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B : CPU

C : I/O

D : Memory

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C : both single threaded and multithreaded

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B : network clusters

C : both a and b

D : Beowulf clusters

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B : Shared memory

C : Message passing

D : Both A and B

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A : Counting sort

B : Bucket sort

C : Radix sort

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B : Parallelism

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A : greater than the time required to create a new process

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D : none of the mentioned

Q.no 43. RMI stands for?

A : Remote Mail InvocationRemote Message Invocation

B : Remaining Method Invention

C : Remaining Method Invocation

D : Remote Method Invocation

Q.no 44. Dynamic networks of networks, is a dynamic connection that grows is called

A : Multithreading

B : Cyber cycle

C : Internet of things

D : None of these

Q.no 45. If one thread opens a file with read privileges then _____

A : other threads in the another process can also read from that file

B : other threads in the same process can also read from that file

C : any other thread can not read from that file

D : all of the mentioned

Q.no 46. the basic operations in the message-passing programming paradigm are ___

A : initiate and listen

B : wait and acknoweldge

C : request and reply

D : send and receive

Q.no 47. What is Inter process communication?

A : allows processes to communicate and synchronize their actions when using the same address space

B : allows processes to communicate and synchronize their actions without using the same address space

C : allows the processes to only synchronize their actions without communication

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Q.no 48. Which of the ceramic components are easier through nano structuring?

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B : Coating

C : Fabrication

D : Wear

Q.no 49. Execution of several activities at the same time.

A : multi processing

B : parallel processing

C : serial processing

D : multitasking

Q.no 50. It is _____ speed and _____ latency.

A : High, high

B : Low, low

C : High, low

D : Low, high

Q.no 51. Process synchronization of programs is done by

A : input

B : output

C : operating system

D : memory

Q.no 52. The management of data flow between computers or devices or between nodes in a network is called

A : Flow control

B : Data Control

C : Data Management

D : Flow Management

Q.no 53. Which of the following are TRUE for direct communication?

A : A communication link can be associated with N number of process(N = max. number of processes supported by system)

B : A communication link can be associated with exactly two processes

C : Exactly N/2 links exist between each pair of processes(N = max. number of processes supported by system)

D : Exactly two link exists between each pair of processes

Q.no 54. Thread synchronization is required because _____

A : all threads of a process share the same address space

B : all threads of a process share the same global variables

C : all threads of a process can share the same files

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Q.no 55. Which of the following two operations are provided by the IPC facility?

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Q.no 56. Which of the following is not the possible ways of data exchange?

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Q.no 58. A thread shares its resources(like data section, code section, open files, signals) with _____

A : other process similar to the one that the thread belongs to

B : other threads that belong to similar processes

C : other threads that belong to the same process

D : all of the mentioned

Q.no 59. The parallelism achieved on the basis of conditions is called as

A : Instruction level

B : Thread level

C : Transaction level

D : None of Above

Q.no 60. The register context and stacks of a thread are deallocated when the thread?

A : terminates

B : blocks

C : unblocks

D : spawns

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B : Finding bipartiteness of a graph

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B : Newtonian mechanics

C : Macro-dynamic

D : Geophysics

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B : Mesh

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B : Cyber cycle

C : Internet of things

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A : Scope

B : Capacity

C : Bandwidth

D : Limitation

Q.no 54. Octa-core processor are the processors of the computer system that contains

A : 2 processors

B : 4 processors

C : 6 processors

D : 8 processors

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B : Bucket sort

C : Radix sort

D : Quick sort

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A : first thread of the process

B : first two threads of the process

C : all threads within the process

D : no thread within the process

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C : Most of Instructions/sec

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D : Both A and B

Q.no 32. RMI stands for?

A : Remote Mail InvocationRemote Message Invocation

B : Remaining Method Invention

C : Remaining Method Invocation

D : Remote Method Invocation

Q.no 33. Which of the following is not a noncomparison sort?

A : Counting sort

B : Bucket sort

C : Radix sort

D : Shell sort

Q.no 34. What is Inter process communication?

A : allows processes to communicate and synchronize their actions when using the same address space

B : allows processes to communicate and synchronize their actions without using the same address space

C : allows the processes to only synchronize their actions without communication

D : none of the mentioned

Q.no 35. _____ are major issues with non-buffered blocking sends

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B : Selection sort

C : Bubble sort

D : Merge sort

Q.no 41. It is _____ speed and _____ latency.

A : High, high

B : Low, low

C : High, low

D : Low, high

Q.no 42. Consider the situation in which assignment operation is very costly. Which of the following sorting algorithm should be performed so that the number of assignment operations is minimized in general?

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Q.no 50. Writing parallel programs is referred to as

A : Parallel computation

B : Parallel processes

C : Parallel development

D : Parallel programming

Q.no 51. Which of the following is not the possible ways of data exchange?

A : Simplex

B : Multiplex

C : Half-duplex

D : Full-duplex

Q.no 52. A thread shares its resources(like data section, code section, open files, signals) with _____

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B : other threads that belong to similar processes

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B : Concurrency transparency

C : Performance transparency

D : Replication transparency

Q.no 57. Multi-processor systems of the computer system has advantage of

A : cost

B : reliability

C : uncertainty

D : scalability

Q.no 58. Process synchronization of programs is done by

A : input

B : output

C : operating system

D : memory

Q.no 59. The management of data flow between computers or devices or between nodes in a network is called

A : Flow control

B : Data Control

C : Data Management

D : Flow Management

Q.no 60. A thread is also called _____

A : Light Weight Process(LWP)

B : Heavy Weight Process(HWP)

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11342_High Performance Computing

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B : CPU

C : I/O

D : Memory

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B : A communication link can be associated with exactly two processes

C : Exactly N/2 links exist between each pair of processes(N = max. number of processes supported by system)

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A : a) there is another process R to handle and pass on the messages between P and Q

B : there is another machine between the two processes to help communication

C : there is a mailbox to help communication between P and Q

D : none of the mentioned

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C : Quick Sort

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A : Data Decomposition

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Q.no 14. Calling a kernel is typically referred to as _____.

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A : Mandatory Instructions/sec

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Q.no 17. The time complexity of heap sort in worst case is

A : O(log n)

B : O(n)

C : O(nlogn)

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Q.no 18. Which of the following is not a stable sorting algorithm?

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B : Selection sort

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Q.no 19. When the Breadth First Search of a graph is unique?

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B : Dynamic Mapping

C : Hybrid Mapping

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Q.no 28. Execution of several activities at the same time.

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B : parallel processing

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D : multitasking

Q.no 29. the basic operations in the message-passing programming paradigm are ___

A : initiate and listen

B : wait and acknoweldge

C : request and reply

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Q.no 30. Nanoscience can be studied with the help of _____

A : Quantum mechanics

B : Newtonian mechanics

C : Macro-dynamic

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B : Shared memory

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Q.no 32. _____ leads to concurrency.

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B : Parallelism

C : Serial processing

D : Distribution

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B : Selection sort

C : Bubble sort

D : Merge sort

Q.no 34. Dynamic networks of networks, is a dynamic connection that grows is called

A : Multithreading

B : Cyber cycle

C : Internet of things

D : None of these

Q.no 35. A process can be _____

A : single threaded

B : multithreaded

C : both single threaded and multithreaded

D : none of the mentioned

Q.no 36. The network topology used for interconnection network.

A : Bus based

B : Mesh

C : Linear Array

D : All of above

Q.no 37. Parallel computing uses _____ execution

A : sequential

B : unique

C : simultaneous

D : none of the answers is correct

Q.no 38. It is _____ speed and _____ latency.

A : High, high

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Q.no 46. Consider the situation in which assignment operation is very costly. Which of the following sorting algorithm should be performed so that the number of assignment operations is minimized in general?

A : Insertion sort

B : Selection sort

C : Bubble sort

D : Merge sort

Q.no 47. _____ are major issues with non-buffered blocking sends

A : concurrent and mutual exclsion

B : Idling and deadlocks

C : synchronization

D : scheduling

Q.no 48. Running merge sort on an array of size n which is already sorted is

A : O(n)

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Q.no 53. Resources and clients transparency that allows movement within a system is called

A : Mobility transparency

B : Concurrency transparency

C : Performance transparency

D : Replication transparency

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B : there is another machine between the two processes to help communication

C : there is a mailbox to help communication between P and Q

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Q.no 55. The architecture which can compute several tasks simultaneously at processor level itself is called as:

A : Multi core architecture

B : Multi processor architecture

C : Multi threaded architecture

D : All of above

Q.no 56. The amount of data that can be carried from one point to another in a given time period is called

A : Scope

B : Capacity

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D : Limitation

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B : output

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Q.no 59. The transparency that enables accessing local and remote resources using identical operations is called _____

A : Access transparency

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D : Scaling transparency

Q.no 60. Termination of the process terminates _____

A : first thread of the process

B : first two threads of the process

C : all threads within the process

D : no thread within the process

Answer for Question No 1. is a

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11342_High Performance Computing

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Q.no 10. Which one of the following is not shared by threads?

A : program counter

B : stack

C : both program counter and stack

D : none of the mentioned

Q.no 11. Decomposition stands for

A : Dividing Problem statement

B : Dividing no of processors

C : Dividing number of tasks

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B : Media mass

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B : Coating

C : Fabrication

D : Wear

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A : sequential

B : unique

C : simultaneous

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B : other threads that belong to similar processes

C : other threads that belong to the same process

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B : blade server

C : clustered system

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A : Instruction level

B : Thread level

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A : input

B : output

C : operating system

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B : Data Control

C : Data Management

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Q.no 59. A thread is also called _____

A : Light Weight Process(LWP)

B : Heavy Weight Process(HWP)

C : Process

D : None of the mentioned

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A : Instruction level

B : Thread level

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Answer for Question No 1. is c

Answer for Question No 2. is c

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11342_High Performance Computing

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D : void

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B : communicate with one another by resorting to shared data

C : share data

D : name the recipient or sender of the message

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A : High, high

B : Low, low

C : High, low

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B : allows processes to communicate and synchronize their actions without using the same address space

C : allows the processes to only synchronize their actions without communication

D : none of the mentioned

Q.no 32. Network interfaces allow the transfer of messages from buffer memory to desired location without ____ intervention

A : DMA

B : CPU

C : I/O

D : Memory

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A : multi processing

B : parallel processing

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B : Shared memory

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B : Parallelism

C : Serial processing

D : Distribution

Q.no 37. High performance computing of the computer system tasks are done by

A : node clusters

B : network clusters

C : both a and b

D : Beowulf clusters

Q.no 38. The network topology used for interconnection network.

A : Bus based

B : Mesh

C : Linear Array

D : All of above

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Q.no 41. A process can be _____

A : single threaded

B : multithreaded

C : both single threaded and multithreaded

D : none of the mentioned

Q.no 42. Broader concept offers Cloud computing .to select which of the following.

A : Parallel computing

B : Centralized computing

C : Utility computing

D : Decentralized computing

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A : Remote Mail InvocationRemote Message Invocation

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B : wait and acknoweldge

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A : input

B : output

C : operating system

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Q.no 53. One that is not a type of multiprocessor of the computer system is

A : dual core

B : blade server

C : clustered system

D : single core

Q.no 54. A thread shares its resources(like data section, code section, open files, signals) with _____

A : other process similar to the one that the thread belongs to

B : other threads that belong to similar processes

C : other threads that belong to the same process

D : all of the mentioned

Q.no 55. NVIDIA thought that 'unifying theme' of every forms of parallelism is the

A : CDA thread

B : PTA thread

C : CUDA thread

D : CUD thread

Q.no 56. Termination of the process terminates _____

A : first thread of the process

B : first two threads of the process

C : all threads within the process

D : no thread within the process

Q.no 57. Given a number of elements in the range [0….n^3]. which of the following sorting algorithms can sort them in O(n) time?

A : Counting sort

B : Bucket sort

C : Radix sort

D : Quick sort

Q.no 58. Which of the following two operations are provided by the IPC facility?

A : write & delete message

B : delete & receive message

C : send & delete message

D : receive & send message

Q.no 59. In indirect communication between processes P and Q _____

A : a) there is another process R to handle and pass on the messages between P and Q

B : there is another machine between the two processes to help communication

C : there is a mailbox to help communication between P and Q

D : none of the mentioned

Q.no 60. Octa-core processor are the processors of the computer system that contains

A : 2 processors

B : 4 processors

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D : 8 processors

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11342_High Performance Computing

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B : Media mass

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Q.no 51. Multi-processor systems of the computer system has advantage of

A : cost

B : reliability

C : uncertainty

D : scalability

Q.no 52. The parallelism achieved on the basis of operations is called as

A : Instruction level

B : Thread level

C : Transaction level

D : None of Above

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B : output

C : operating system

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B : all threads of a process share the same global variables

C : all threads of a process can share the same files

D : all of the mentioned

Q.no 56. Data access and storage are elements of Job throughput, of _____.

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B : Adaptation

C : Efficiency

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B : have to be a variable size

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A : terminates

B : blocks

C : unblocks

D : spawns

Answer for Question No 1. is c

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Answer for Question No 3. is c

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C : kernel termination

D : kernel invocation

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B : Exclusive address space

C : Logical Adress Space

D : Non shared Adress Space

Q.no 25. Type of HPC applications of

A : Management

B : Media mass

C : Business

D : Science

Q.no 26. Which of the following is NOT a characteristic of parallel computing?

A : Breaks a task into pieces

B : Uses a single processor or computer

C : Simultaneous execution

D : May use networking

Q.no 27. It is _____ speed and _____ latency.

A : High, high

B : Low, low

C : High, low

D : Low, high

Q.no 28. Broader concept offers Cloud computing .to select which of the following.

A : Parallel computing

B : Centralized computing

C : Utility computing

D : Decentralized computing

Q.no 29. _____ leads to concurrency.

A : Serialization

B : Parallelism

C : Serial processing

D : Distribution

Q.no 30. the basic operations in the message-passing programming paradigm are ___

A : initiate and listen

B : wait and acknoweldge

C : request and reply

D : send and receive

Q.no 31. Dynamic networks of networks, is a dynamic connection that grows is called

A : Multithreading

B : Cyber cycle

C : Internet of things

D : None of these

Q.no 32. Running merge sort on an array of size n which is already sorted is

A : O(n)

B : O(nlogn)

C : O(n^2)

D : O(log n)

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A : Bus based

B : Mesh

C : Linear Array

D : All of above

Q.no 34. Message passing system allows processes to _____

A : communicate with one another without resorting to shared data

B : communicate with one another by resorting to shared data

C : share data

D : name the recipient or sender of the message

Q.no 35. We have an internet cloud of resources In cloud computing to form

A : Centralized computing

B : Decentralized computing

C : Parallel computing

D : All of Above

Q.no 36. If one thread opens a file with read privileges then _____

A : other threads in the another process can also read from that file

B : other threads in the same process can also read from that file

C : any other thread can not read from that file

D : all of the mentioned

Q.no 37. Consider the situation in which assignment operation is very costly. Which of the following sorting algorithm should be performed so that the number of assignment operations is minimized in general?

A : Insertion sort

B : Selection sort

C : Bubble sort

D : Merge sort

Q.no 38. Parallel computing uses _____ execution

A : sequential

B : unique

C : simultaneous

D : none of the answers is correct

Q.no 39. RMI stands for?

A : Remote Mail InvocationRemote Message Invocation

B : Remaining Method Invention

C : Remaining Method Invocation

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B : CPU

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Q.no 44. High performance computing of the computer system tasks are done by

A : node clusters

B : network clusters

C : both a and b

D : Beowulf clusters

Q.no 45. Time complexity of bubble sort in best case is

A : θ (n)

B : θ (nlogn)

C : θ (n^2)

D : θ (n(logn)^2)

Q.no 46. Writing parallel programs is referred to as

A : Parallel computation

B : Parallel processes

C : Parallel development

D : Parallel programming

Q.no 47. Execution of several activities at the same time.

A : multi processing

B : parallel processing

C : serial processing

D : multitasking

Q.no 48. Which of the ceramic components are easier through nano structuring?

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B : Coating

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D : Wear

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Q.no 50. _____ are major issues with non-buffered blocking sends

A : concurrent and mutual exclsion

B : Idling and deadlocks

C : synchronization

D : scheduling

Q.no 51. A thread is also called _____

A : Light Weight Process(LWP)

B : Heavy Weight Process(HWP)

C : Process

D : None of the mentioned

Q.no 52. NVIDIA thought that 'unifying theme' of every forms of parallelism is the

A : CDA thread

B : PTA thread

C : CUDA thread

D : CUD thread

Q.no 53. In indirect communication between processes P and Q _____

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D : 8 processors

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C : Radix sort

D : Quick sort

Q.no 57. Which of the following is not the possible ways of data exchange?

A : Simplex

B : Multiplex

C : Half-duplex

D : Full-duplex

Q.no 58. The register context and stacks of a thread are deallocated when the thread?

A : terminates

B : blocks

C : unblocks

D : spawns

Q.no 59. Dynamic networks is a dynamic connection that grows is called

A : Multithreading

B : Cyber cycle

C : Internet of things

D : Cyber-physical system

Q.no 60. Multi-processor systems of the computer system has advantage of

A : cost

B : reliability

C : uncertainty

D : scalability

Answer for Question No 1. is c

Answer for Question No 2. is c

Answer for Question No 3. is c

Answer for Question No 4. is b

Answer for Question No 5. is b

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Answer for Question No 7. is c

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Answer for Question No 14. is b

Answer for Question No 15. is a

Answer for Question No 16. is a

Answer for Question No 17. is a

Answer for Question No 18. is d

Answer for Question No 19. is b

Answer for Question No 20. is b

Answer for Question No 21. is d

Answer for Question No 22. is d

Answer for Question No 23. is d

Answer for Question No 24. is b

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Answer for Question No 26. is a

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Answer for Question No 31. is c

Answer for Question No 32. is b

Answer for Question No 33. is d

Answer for Question No 34. is a

Answer for Question No 35. is d

Answer for Question No 36. is b

Answer for Question No 37. is b

Answer for Question No 38. is c

Answer for Question No 39. is d

Answer for Question No 40. is b

Answer for Question No 41. is a

Answer for Question No 42. is a

Answer for Question No 43. is b

Answer for Question No 44. is d

Answer for Question No 45. is a

Answer for Question No 46. is d

Answer for Question No 47. is b

Answer for Question No 48. is c

Answer for Question No 49. is b

Answer for Question No 50. is b

Answer for Question No 51. is a

Answer for Question No 52. is c

Answer for Question No 53. is c

Answer for Question No 54. is a

Answer for Question No 55. is d

Answer for Question No 56. is c

Answer for Question No 57. is b

Answer for Question No 58. is a

Answer for Question No 59. is c

Answer for Question No 60. is b

Seat No -

Total number of questions : 60

11342_High Performance Computing

Time : 1hr

Max Marks : 50

N.B

1) All questions are Multiple Choice Questions having single correct option.

2) Attempt any 50 questions out of 60.

3) Use of calculator is allowed.

4) Each question carries 1 Mark.

5) Specially abled students are allowed 20 minutes extra for examination.

6) Do not use pencils to darken answer.

7) Use only black/blue ball point pen to darken the appropriate circle.

8) No change will be allowed once the answer is marked on OMR Sheet.

9) Rough work shall not be done on OMR sheet or on question paper.

10) Darken ONLY ONE CIRCLE for each answer.

Q.no 1. MIPS stands for?

A : Mandatory Instructions/sec

B : Millions of Instructions/sec

C : Most of Instructions/sec

D : Many Instructions / sec

Q.no 2. In ..... only one process at a time is allowed into its critical section, among all processes that have critical sections for the same resource.

A : Mutual Exclusion

B : Synchronization

C : Deadlock

D : Starvation

Q.no 3. Which of the following is not an application of Breadth First Search?

A : Finding shortest path between two nodes

B : Finding bipartiteness of a graph

C : GPS navigation system

D : Path Finding

Q.no 4. Regarding implementation of Breadth First Search using queues, what is the maximum distance between two nodes present in the queue? (considering each edge length 1)

A : Can be anything

B : 0

C : At most 1

D : Insufficient Information

Q.no 5. The decomposition technique in which the input is divided is called as_____

A : Data Decomposition

B : Recursive Decomposition

C : Speculative Decomposition

D : Exploratory Decomposition

Q.no 6. Which of the following is a stable sorting algorithm?

A : Merge sort

B : Typical in-place quick sort

C : Heap sort

D : Selection sort

Q.no 7. Which one of the following is not shared by threads?

A : program counter

B : stack

C : both program counter and stack

D : none of the mentioned

Q.no 8. Several instructions execution simultaneously in _____

A : processing

B : parallel processing

C : serial processing

D : multitasking

Q.no 9. When the Breadth First Search of a graph is unique?

A : When the graph is a Binary Tree

B : When the graph is a Linked List

C : When the graph is a n-ary Tree

D : When the graph is a Ternary Tree

Q.no 10. Message-passing programs are often written using

A : symetric Paradigm

B : asymetric Paradigm

C : asynchronous paradigm

D : synchronous paradigm

Q.no 11. How many Attibutes required to characterize messsage passing paragdigm

A : 2

B : 4

C : 6

D : 8

Q.no 12. Following is not mapping technique

A : Static Mapping

B : Dynamic Mapping

C : Hybrid Mapping

D : All of Above

Q.no 13. The time complexity of a quick sort algorithm which makes use of median, found by an O(n) algorithm, as pivot element is

A : O(n^2)

B : O(nlogn)

C : O(nlog(log(n))

D : O(n)

Q.no 14. Following is not decomposition technique

A : Data Decomposition

B : Recursive Decomposition

C : Serial Decomposition

D : Exploratory Decomposition

Q.no 15. Most message-passing programs are written using

A : the single program multiple data (SPMD) model.

B : the multiple program and single data(MPSD) model

C : the single program single data (SPSD) model

D : the Multiple program multiple data (SPMD) model

Q.no 16. The logical view of a machine supporting the message-passing paradigm consists of p processes, each with its own _____

A : Partitioned Address space

B : Exclusive address space

C : Logical Adress Space

D : Non shared Adress Space

Q.no 17. The time complexity of heap sort in worst case is

A : O(log n)

B : O(n)

C : O(nlogn)

D : O(n^2)

Q.no 18. Decomposition stands for

A : Dividing Problem statement

B : Dividing no of processors

C : Dividing number of tasks

D : Dividing number of operation

Q.no 19. Type of HPC applications of

A : Management

B : Media mass

C : Business

D : Science

Q.no 20. The kernel code is dentified by the _____qualifier with void return type

A : _host_

B : __global__

C : _device_

D : void

Q.no 21. Which of the following is not a stable sorting algorithm?

A : Insertion sort

B : Selection sort

C : Bubble sort

D : Merge sort

Q.no 22. Which of the following is not an application of Depth First Search?

A : For generating topological sort of a graph

B : For generating Strongly Connected Components of a directed graph

C : Detecting cycles in the graph

D : Peer to Peer Networks

Q.no 23. Calling a kernel is typically referred to as _____.

A : kernel thread

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C : kernel termination

D : kernel invocation

Q.no 24. Which of the following is not an in-place sorting algorithm?

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B : Heap sort

C : Quick Sort

D : Merge sort

Q.no 25. Depth First Search is equivalent to which of the traversal in the Binary Trees?

A : Pre-order Traversal

B : Post-order Traversal

C : Level-order Traversal

D : In-order Traversal

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C : both single threaded and multithreaded

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B : Coating

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D : Wear

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A : Bus based

B : Mesh

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A : allows processes to communicate and synchronize their actions when using the same address space

B : allows processes to communicate and synchronize their actions without using the same address space

C : allows the processes to only synchronize their actions without communication

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B : Newtonian mechanics

C : Macro-dynamic

D : Geophysics

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C : Radix sort

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Q.no 52. Thread synchronization is required because _____

A : all threads of a process share the same address space

B : all threads of a process share the same global variables

C : all threads of a process can share the same files

D : all of the mentioned

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A : communication link

B : message-passing link

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Answer for Question No 24. is d

Answer for Question No 25. is a

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Answer for Question No 27. is d

Answer for Question No 28. is c

Answer for Question No 29. is d

Answer for Question No 30. is a

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Answer for Question No 32. is c

Answer for Question No 33. is b

Answer for Question No 34. is d

Answer for Question No 35. is a

Answer for Question No 36. is b

Answer for Question No 37. is c

Answer for Question No 38. is c

Answer for Question No 39. is b

Answer for Question No 40. is a

Answer for Question No 41. is a

Answer for Question No 42. is b

Answer for Question No 43. is b

Answer for Question No 44. is d

Answer for Question No 45. is b

Answer for Question No 46. is b

Answer for Question No 47. is d

Answer for Question No 48. is b

Answer for Question No 49. is d

Answer for Question No 50. is a

Answer for Question No 51. is c

Answer for Question No 52. is d

Answer for Question No 53. is c

Answer for Question No 54. is b

Answer for Question No 55. is a

Answer for Question No 56. is d

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Answer for Question No 58. is c

Answer for Question No 59. is a

Answer for Question No 60. is c

Our telegram channel - **https://t.me/sppumcq**
click here to join

Which of the following statements are true with regard to compute capability in CUDA

A. Code compiled for hardware of one compute capability will not need to be re-compiled to run on hardware of another

B. Different compute capabilities may imply a different amount of local memory per thread

C. Compute capability is measured by the number of FLOPS a GPU accelerator can compute.

Answer : B

True or False: The threads in a thread block are distributed across SM units so that each thread is executed by one SM unit.

A. True

B. False

Answer : B

The style of parallelism supported on GPUs is best described as

A. SISD - Single Instruction Single Data

B. MISD - Multiple Instruction Single Data

C. SIMT - Single Instruction Multiple Thread

Answer : C

True or false: Functions annotated with the __global__ qualifier may be executed on the host or the device

A. True

B. Flase

Answer : A

Which of the following correctly describes a GPU kernel

A. A kernel may contain a mix of host and GPU code

B. All thread blocks involved in the same computation use the same kernel

C. A kernel is part of the GPU's internal micro-operating system, allowing it to act as in independent host

Answer : B

Which of the following is *not* a form of parallelism supported by CUDA

A. Vector parallelism - Floating point computations are executed in parallel on wide vector units

B. Thread level task parallelism - Different threads execute a different tasks

C. Block and grid level parallelism - Different blocks or grids execute different tasks

D. Data parallelism - Different threads and blocks process different parts of data in memory

Answer :A

What strategy does the GPU employ if the threads within a warp diverge in their execution?

A. Threads are moved to different warps so that divergence does not occur within a single warp

B. Threads are allowed to diverge

C. All possible execution paths are run by all threads in a warp serially so that thread instructions do not diverge

Answer : C

Which of the following does *not* result in uncoalesced (i.e. serialized) memory access on the K20 GPUs installed on Stampede

A. Aligned, but non-sequential access

B. Misaligned data access

C. Sparse memory access

Answer : A

Which of the following correctly describes the relationship between Warps, thread blocks, and CUDA cores?

A. A warp is divided into a number of thread blocks, and each thread block executes on a single CUDA core

B. A thread block may be divided into a number of warps, and each warp may execute on a single CUDA core

C. A thread block is assigned to a warp, and each thread in the warp is executed on a separate CUDA core

Answer : B

Shared memory in CUDA is accessible to:

A. All threads in a single block

B. Both the host and GPU

C. All threads associated with a single kernel

Answer : A

CUDA Architecture CPU consist of

A. CUDA Libraries

B. CUDA Runtime

C. CUDA Driver

D. All Above

Answer : D

CUDA platform works on

A. C

B. C++

C. Forton

D. All Above

Answer : D

Threads support Shared memory and Synchronization

A. True

B. False

Answer : A

Application of CUDA are

A. Fast Video Transcoding

B. Medical Imaging

C. Computational Science

D. Oil and Natural Resources exploration

E. All Above

Answer : E

GPU execute device code

A. True

B. False

Answer : A

What are the issues in sorting?

A. Where the Input and Output Sequences are Stored

B. How Comparisons are Performed

C. All above

Answer : C

The parallel run time of the formulation for Bubble sort is

A. Tp = O(n/plogn/p) + O(n) + O(n)

B. Tp = O(n/plogn/p) + O (n/plogp) + O(ln/p)

C. Non of the above

Answer : A

What are the variants of Bubble sort?

A. Shell sort

B. Quick sort

C. Odd-Even transposition

D. Option A & C

Answer : D

What is the overall complexity of parallel algorithm for quick sort?

A. Tp = O(n/p logn/p) + O(n/p logp) + O($\log^2$p)

B. Tp = O(n/p logn/p) + O(n/p logp)

C. Tp = O(n/p logn/p) + O($\log^2$p)

Answer : A

Formally, given a weighted graph $G(V, E, w)$, the ***all-pairs shortest paths*** problem is to find the shortest paths between all pairs of vertices. True or False?

A. True
B. False

Answer : A

What is true for parallel formulation of Dijkstra's Algorithm?

A. One approach partitions the vertices among different processes and has each process compute the single-source shortest paths for all vertices assigned to it. We refer to this approach as the ***source-partitioned formulation.***
B. Another approach assigns each vertex to a set of processes and uses the parallel formulation of the single-source algorithm to solve the problem on each set of processes. We refer to this approach as the ***source-parallel formulation***.
C. Both are true
D. Non of these is true

Answer : C

Search algorithms can be used to solve discrete optimization problems. True or False ?

A. True
B. False

Answer : A

Examples of Discrete optimization problems are ;

A. planning and scheduling,
B. The optimal layout of VLSI chips,
C. Robot motion planning,
D. Test-pattern generation for digital circuits, and logistics and control.
E. All of above

Answer : E

List the important parameters of Parallel DFS

A. Work- Splitting Strategies

B. Load balancing Schemes

C. All of above

Answer : C

List the communication strategies for parallel BFS.

A. Random communication strategy

B. Ring communication strategy

C. Blackboard communication strategy

D. All of above

Answer : D

The lower bound on any comparison-based sort of *n* numbers is $\Theta(n \log n)$

A. True
B. False

Answer : A

In a compare-split operation

A. Each process sends its block of size n/p to the other process
B. Each process merges the received block with its own block and retains only the appropriate half of the merged block
C. Both A & B

Answer : C

In a typical sorting network

A. Every sorting network is made up of a series of columns
B. Each column contains a number of comparators connected in parallel
C. Both A & B

Answer : C

Bubble sort is difficult to parallelize since the algorithm has no concurrency

A. True
B. False

Answer : A

What are the sources of overhead?

A. Essential /Excess Computation
B. Inter-process Communication
C. Idling
D. All above

Answer : D

Which are the performance metrics for parallel systems?

A. Execution Time
B. Total Parallel Overhead
C. Speedup
D. Efficiency
E. Cost
F. All above

Answer : F

The efficiency of a parallel program can be written as: ***E = Ts / pTp.*** True or False?

A. True
B. False

Answer : A

Overhead function or ***total overhead*** of a parallel system as the total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element. True or False?

A. True
B. False

Answer : A

What is Speedup?

A. A measure that captures the relative benefit of solving a problem in parallel. It is defined as the ratio of the time taken to solve a problem on a single processing element to the time required to solve the same problem on a parallel computer with *p* identical processing elements.
B. A measure of the fraction of time for which a processing element is usefully employed.
C. None of the above

Answer : A

In an ideal parallel system, speedup is equal to *p* and efficiency is equal to one. True or False?

A. True
B. False

Answer : A

A parallel system is said to be _____ if the cost of solving a problem on a parallel computer has the same asymptotic growth (in Θ terms) as a function of the input size as the fastest-known sequential algorithm on a single processing element.

A. Cost optimal
B. Non Cost optimal

Answer : A

Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called _____ a parallel system in terms of the number of processing elements.

A. Scaling down
B. Scaling up

Answer : B

The _____ function determines the ease with which a parallel system can maintain a constant efficiency and hence achieve speedups increasing in proportion to the number of processing elements.

A. Isoefficiency
B. Efficiency
C. Scalability
D. Total overhead

Answer : A

Minimum execution time for adding n numbers is *Tp = n/p + 2 logp* True or False ?

A. True
B. False

Answer : A

The overhead function To = pTP – TS.

A. True
B. False

Answer : A

Performance Metrics for Parallel Systems: Speedup(S) =TS/TP

A. True
B. False

Answer : A

Matrix Vector multiplication 2D Partitions requires some basic communication operations

A. one-to-one communication to align the vector along the main diagonal
B. one-to-all broadcast of each vector element among the n processes of each column
C. all-to-one reduction in each row
D. All Above

Answer : D

HPC MCQ QB for Mock Insem Examination

Unit I

1. Conventional architectures coarsely comprise of a_

   A. A processor
   B. Memory system
   C Data path.
   D All of Above

2. Data intensive applications utilize_

   A **High aggregate throughput**
   B High aggregate network bandwidth
   C High processing and memory system performance.
   D None of above

3. A pipeline is like_

   A Overlaps various stages of instruction execution to achieve performance.
   B House pipeline
   C Both a and b
   D A gas line

4. Scheduling of instructions is determined_

   A True Data Dependency
   B Resource Dependency
   C Branch Dependency
   D All of above

5. VLIW processors rely on_

   A **Compile time analysis**
   B Initial time analysis
   C Final time analysis
   D Mid time analysis

6. Memory system performance is largely captured by_

   A Latency
   B Bandwidth
   C Both a and b
   D none of above

7. The fraction of data references satisfied by the cache is called_

A Cache *hit ratio*
B Cache *fit ratio*
B Cache *best ratio*
C none of above

8. A single control unit that dispatches the same Instruction to various processors is__

A SIMD
B SPMD
C MIMD
D None of above

9. The primary forms of data exchange between parallel tasks are_

A Accessing a shared data space
B Exchanging messages.
C Both A and B
D None of Above

10. Switches map a fixed number of inputs to outputs.
A True
B False

Unit 2

1. The First step in developing a parallel algorithm is_

   A. To Decompose the problem into tasks that can be executed concurrently
   B. Execute directly
   C. Execute indirectly
   D. None of Above

2. The number of tasks into which a problem is decomposed determines its_

   A. Granularity
   B. Priority
   C. Modernity
   D. None of above

3. The length of the longest path in a task dependency graph is called_
   A. the critical path length
   B. the critical data length
   C. the critical bit length
   D. None of above

4. The graph of tasks (nodes) and their interactions/data exchange (edges)_

A. Is referred to as a *task interaction graph*
B. Is referred to as a *task Communication graph*
C. Is referred to as a *task interface graph*
D. None of Above

5. Mappings are determined by_

A. task dependency
B. task interaction graphs
C. Both A and B
D. None of Above

6. Decomposition Techniques are_
A. recursive decomposition
B. data decomposition
C. exploratory decomposition
D. speculative decomposition
E. All of Above

7. The *Owner Computes Rule* generally states that the process assigned a particular data item is responsible for_

A. All computation associated with it
B. Only one computation
C. Only two computation
D. Only occasionally computation

8. A simple application of exploratory decomposition is_

A. The solution to a 15 puzzle
B. The solution to 20 puzzle
C. The solution to any puzzle
D. None of Above

9. Speculative Decomposition consist of _

A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B

10. task characteristics include:
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.
D. All of Above

Unit 3

1. Group communication operations are built using point-to-point messaging primitives
   A. True
   B. False

2. Communicating a message of size m over an uncongested network takes time ts + tmw

   A. True
   B. False

3. The dual of one-to-all broadcast is_

   A. *All-to-one reduction*
   B. *All-to-one receiver*
   C. *All-to-one Sum*
   D. *None of Above*

4. A hypercube has_

   A. 2^d nodes
   B. 2d nodes
   C. 2n Nodes
   D. N Nodes

5. A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes.

   A. True
   B. False

6. In All-to-All Broadcast each processor is the source as well as destination.

   A. True
   B. False

7. The Prefix Sum Operation can be implemented using the_

   A. All-to-all broadcast kernel.
   B. All-to-one broadcast kernel.
   C. One-to-all broadcast Kernel
   D. Scatter Kernel

8. In the *scatter* operation_

A. **Single node send a unique message of size m to every other node**
B. Single node send a same message of size m to every other node
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D. None of Above

9. The gather operation is exactly the inverse of the_

   A. **Scatter operation**
   B. Broadcast operation
   C. Prefix Sum
   D. Reduction operation

10. In All-to-All Personalized Communication Each node has a distinct message of size m for every other node

   A. **True**
   B. False

1. It is _____ strength and _____ permeability.
a) High, high
b) Low, low
c) High, low
d) Low, high
View Answer
Answer: c
Explanation: It is specifically chosen so as to have particularly appropriate properties for the expected use of the structure such as high strength and low permeability.

2. High Performance concrete works out to be economical.
a) True
b) False
View Answer
Answer: a
Explanation: High Performance concrete works out to be economical, even though its initial cost is high.

3. HPC is not used in high span bridges.
a) True
b) False
View Answer
Answer: b
Explanation: Major applications of high-performance concrete in the field of Civil Engineering constructions have been in the areas of long-span bridges, high-rise buildings or structures, highway pavements, etc.

4. Concrete having 28- days' compressive strength in the range of 60 to 100 MPa.
a) HPC
b) VHPC
c) OPC
d) HSC
View Answer
Answer: a
Explanation: High Performance Concrete having 28- days' compressive strength in the range of 60 to 100 MPa.

5. Concrete having 28-days compressive strength in the range of 100 to 150 MPa.
a) HPC
b) VHPC
c) OPC
d) HSC
View Answer
Answer: b
Explanation: Very high performing Concrete having 28-days compressive strength in the range of 100 to 150 MPa.

6. High-Performance Concrete is _____ as compared to Normal Strength Concrete.
a) Less brittle
b) Brittle
c) More brittle
d) Highly ductile
View Answer
Answer: c
Explanation: High-Performance Concrete is more brittle as compared to Normal Strength Concrete (NSC), especially when high strength is the main criteria.

7. The choice of cement for high-strength concrete should not be based only on mortar-cube tests but it should also include tests of compressive strengths of concrete at _____ days.
a) 28, 56, 91
b) 28, 60, 90
c) 30, 60, 90

d) 30, 45, 60
View Answer
Answer: a
Explanation: The choice of cement for high-strength concrete should not be based only on mortar-cube tests but it should also include tests of compressive strengths of concrete at 28, 56, and 91 days.

8. For high-strength concrete, a cement should produce a minimum 7-days mortar-cube strength of approximately ___ MPa.
a) 10
b) 20
c) 30
d) 40
View Answer
Answer: c
Explanation: For high-strength concrete, a cement should produce a minimum 7-days mortar-cube strength of approximately 30 MPa.

9. _____ mm nominal maximum size aggregates gives optimum strength.
a) 9.5 and 10.5
b) 10.5 and 12.5
c) 9.5 and 12.5
d) 11.5 and 12.5
View Answer
Answer: c
Explanation: Many studies have found that 9.5 mm to 12.5 mm nominal maximum size aggregates gives optimum strength.

10. Due to low w/c ratio _____
a) It doesn’t cause any problems
b) It causes problems
c) Workability is easy
d) Strength is more
View Answer
Answer: b
Explanation: Due to the low w/c ratio, it causes problems so superplasticizers are used.

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B. False

SN	Question	Option 1	Option 2
1	Any condition that causes a processor to stall is called as _____.	Hazard	Page fault
2	The time lost due to branch instruction is often referred to as _____.	Latency	Delay
3	_____ method is used in centralized systems to perform out of order executio	Scorecard	Score boar
4	The computer cluster architecture emerged as an alternative for ____.	ISA	Workstatio
5	NVIDIA CUDA Warp is made up of how many threads?	512	1024
6	Out-of-order instructions is not possible on GPUs.	WAHR	FALSCH
7	CUDA supports programming in	C or C++ or	Java, Pytho
8	FADD, FMAD, FMIN, FMAX are ----- supported by Scalar Processors of NVIDIA G	32-bit IEEE	32-bit integ
9	Each streaming multiprocessor (SM) of CUDA herdware has ------ scalar proces	1024	128
10	Each NVIDIA GPU has ------ Streaming Multiprocessors	8	1024
11	CUDA provides ------- warp and thread scheduling. Also, the overhead of thread	“programm	“zero-overl
12	Each warp of GPU receives a single instruction and “broadcasts” it to all of its t	SIMD (Sing	SIMT (Singl
13	Limitations of CUDA Kernel	recursion,	No recursic
14	What is Unified Virtual Machine	It is a techr	It is a techr
15	_____ became the first language specifically designed by a GPU Company to	Python, GP	C, CPUs.
16	The CUDA architecture consists of --------- for parallel computing kernels and fu	RISC instru	CISC instru
17	CUDA stands for --------, designed by NVIDIA.	Common U	Complex U
18	The host processor spawns multithread tasks (or kernels as they are known in	WAHR	FALSCH
19	The NVIDIA G80 is a ---- CUDA core device, the NVIDIA G200 is a ---- CUDA core	128, 256, 5	32, 64, 128
20	NVIDIA 8-series GPUs offer -------- .	50-200 GFL	200-400 GF
21	IADD, IMUL24, IMAD24, IMIN, IMAX are ---------- supported by Scalar Processo	32-bit IEEE	32-bit integ
22	CUDA Hardware programming model supports: a) fully generally data-parallel	a,c,d,f	b,c,d,e
23	In CUDA memory model there are following memory types available: a) Regist	a, b, d, f	a, c, d, e, f
24	What is the equivalent of general C program with CUDA C: int main(void) { prin	int main (v	__global__
25	Which function runs on Device (i.e. GPU): a) __global__ void kernel (void) { } b	a	b
26	A simple kernel for adding two integers: __global__ void add(int *a, int *b, int	add() will e	add() will e
27	If variable a is host variable and dev_a is a device (GPU) variable, to allocate m	cudaMalloc	malloc(&d
28	If variable a is host variable and dev_a is a device (GPU) variable, to copy input	memcpy(d	cudaMemc
29	Triple angle brackets mark in a statement inside main function, what does it in	a call from	a call from
30	What makes a CUDA code runs in parallel	__global__	main() func
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44			
45			
46			
47			

Option 3	Option 4	Correct Ans	Level	Marks
System err	None of the	1	1	1
Branch pen	None of the	3	1	1
Optimizing	Redundanc	2	1	1
Super com	Distributed	3	1	1
312	32	4	1	1
--	--	2	1	1
C, C++, thir	Pascal	3	1	1
both	none of the	1	1	1
512	8	4	1	1
512	16	4	1	1
64, 2 clock	32, 1 clock	2	2	2
SISD (Single	SIST (Single	2	1	1
recursion, r	No recursic	2	2	2
It is a techr	It is a techr	1	1	1
CUDA C, GF	Java, CPUs.	3	1	1
ZISC instruc	PTX instruc	4	1	1
Compute U	Complex U	3	1	1
---	---	1	1	1
64, 128, 25	256, 512, 1	1	3	3
400-800 GF	800-1000 G	1	1	1
both	none of the	2	1	1
a,d,e,f	a,b,c,d,e,f	4	2	2
a, b, c, d, e,	b, c, e, f	3	2	2
__global__	__global__	2	2	2
both a,b	---	1	1	1
add() will b	add() will b	1	1	1
cudaMalloc	malloc((vo	3	1	1
memcpy((v	cudaMemc	2	1	1
less than co	greater tha	1	1	1
Kernel nam	first param	4	1	1

	marks	question	A	B	C	D	ans
0	1	Interconnection Networks can be classified as?	Both	Dynamic	Static	Direct Network	Both Static and Dynamic.
1	1	Parallel Computers are used to solve which types of problems.	Both	Algorithmic Problems	Optimization Problems	None	This is an explaination.
2	1	How many clocks control all the stages in a pipeline?	One	Three	Four	Five	One clock Is used to control all the stages.
3	1	Main memory in parallel computing is____?	Shared	Parallel	Fixed	None	Main memory is shared in parallel computing.
4	1	Which of these is not a class of parallel computing architetcture?	Application Checkpointing	Distributed Computing	Symmetric Multiprocessing	Multicore Computing	Ans- (d)- Application checkpoiting. is not a class of parallel computer architecture.
5	1	Parallel Computing software solutions and Techniques includes:	All	Automatic Parallelization	Parallel Programming languages.	Application Checkpointing	Parallel computing software solutionincludes all of the following.. This is an explanation
6	2	The Processors are connected to the memory through a set of?	Switches	Cables	Buses	Registers	The Processors are connected thru. the switches.
7	2	Superscalar Architetcure has how many execution units?	Two	One	Three	Four	This is an explaination.
8	2	What is used to hold the intermediate output in a pipeline	Intermediate Register	Cache	RAM	ROM	The Intermediate Registers are used to hold the output.
9	2	Which oranization performs sequencing of Human Genome?	International Human Genome Sequencing and Consortium	International Sequencing and Consortium for Human Genome	Human Genome Sequencing and Constrium, Org.	Genome Sequencing for Humans and Consortium, Org.	This is an explaination.
10	2	There are how many stages in RISC Processor?	Five	Three	Two	Six	Ans(c)- Five stages are there in a RISC processor.
11	2	Over the last decade, The DRAM access time has improved at what rate per year?	0.1	0.2	0.15	None of the above	The DRAM acess time rate has improved at a rate of 10% over the last decade.

	marks	question	A	B	C	D	ans
12	2	Which memory acts as low-latency high bandwidth storage?	Cache	Register	DRAM	EPROM	Cache acts as low latency high bandwidth storage .This is an explanation.
13	2	Which processor architecture is this?	SIMD	MIMD	MISD	MIMD	This is an explaination.
14	2	Which core processor is this?	Quad-Core	Dual-Core	Octa-Core	Single-Core	This diagram shows Quad-Core.
15	2	Which of these is not a scalable design principle?	Data Caching	Decomposition	Simplification	Parsimony	Data Caching is not a prinicple of scable design.
16	2	The distance between any two nodes in Bus Based network is?	O(1)	O(n Logn)	O(N)	O(n^2)	O(1) is the ditance between any two nodes.
17	2	Early SIMD computers include:	All	MPP	CM-2	Illiac IV	All of these are early staged SIMD parallel computers.
18	2	This is which configuration in Omega networks.	Pass-through	Cross-Over	Shuffle	None	This is called Pass-through configuration.
19	2	Automatic Parallelization technique doesnâ€™t ncludes:	Share Memory	Analyse	Schedule	Parse	Parallelization includes parse, analyse schedule and code generation.
20	2	The Pentuim 4 or P4 processor has how many stage pipeline?	20	15	18	10	The P4 processor has 20 staged pipeline. This is an explanation.
21	3	Which protocol is not used to remove concurrent writes?	Identify	Priority	Common	Sum	Sum, Prioirity and common are used to remove concurrent writes.
22	3	EREW PRAM stands for?	Exclusive Read and Exclusive Write	Erasable Read and Erasable Write PRAM	Easily Read and Easily Write	None	EREW stands for Exclusive Read and Exclsuive Write PRAM.
23	3	During each clock cycle, multiple instructions are piped into the processor in_____?	Parallel	Series	Both a and b	None	Multiple Instuctiion are piped in parallel. This is an explanation.
24	3	Which Interconnection Network uses this equation.	Multistage Networks	Cross-Bar	Dynamic Networks	Bus-Staged	Multistaged Network uses this eqn.

	marks	question	A	B	C	D	ans
25	3	How many types of parallel computing are available from both proprietary and open source parallel computing vendors?	4	2	3	6	There are generally four types of parallel computing, available from both proprietary and open source parallel computing vendors.
26	3	If a piece of data is repeatedly used, the effective latency of this memory system can be reduced by the cache. The fraction of data references satisfied by the cache is called?	Hit Ratio	Memory ratio	Hit Fraction	Memory Fraction.	If a piece of data is repeatedly used, the effective latency of this memory system can be reduced by the cache. The fraction of data references satisfied by the cache is called the cache hit ratio.
27	3	Superscalar Architetcure can create problem in?	Scheduling	Phasing	Data Extraction	Data-Compiling	SuperScalar Architecture can cause problems in CPU scheduling.
28	3	In cut-through routing, a message is broken into fixed size units called?	Flits	Flow Digits	Control Digits	All	In cut-through routing, a message is broken into fixed size units called flits.
29	3	The total communication time for cut-through routing is?	A	B	C	D	This is an explaination.
30	1	The Disadvantage of GPU Pipeline is?	Load-balancing	Data balancing	Process balancing	All of the above	This is an explaination.
31	1	Examples of GPU Processors are:	Both	AMD Processors	NVIDIA	None	Both AMD and NVIDIA.
32	1	Simultaneous execution of different programs on a data stream is called?	Stream Parallelism	Data Execution	Data-paralleism	None	Simultaneous execution of different programs on a data stream is called Stream Parallelism.
33	1	Early GPU controllers were known as?	Video Shifters	GPU Shifters	GPU Controllers	Video-Movers	This is an Explaination.
34	1	_____development is a critical component of problem solving using computers?	Algorithm	Code	Pseudocode	Problem	Algorithm development is a critical component of problem solving using computers

	marks	question	A	B	C	D	ans
35	1	GPU stands for?	Graphics Processsing Unit	Graphical Processing Unit	Gaming Processing Unit	Graph Processing Unit	This is an Explaination.
36	1	What leads to concurrency?	Parallelism	Serial Processing	Decomposition	All	Parallelism leads naturally to Concurrency. For example, Several processes trying to print a file on a single printer.
37	2	The process of determining which screen-space pixel locations are covered by each\ntriangle is known as?	Rasterization	Pixelisation	Fragmentation	Space-Determining Process	Rasterization is the process of determining which screen-space pixel locations are covered by each\ntriangle.
38	2	The programmable units of the GPU follow which programming model?	SPMD	MISD	MIMD	SIMD	The programmable units of the GPU follow a single program multiple-data (SPMD) programming model.
39	2	Which space can ease the programming effort, especially if the distribution of data is different in different phases of the algorithm?	Shared Address	Parallel Address	Data- Address	Series-Address	Shared Address space can ease the programming effort, especially if the distribution of data is different in different phases of the algorithm.
40	2	Which are the hardware units that physically perform computations?	Processsor	ALU	CPU	CU	Processors are the hardware units that physically perform computations
41	2	Examples of Graphics API are?	All	DirectX	CUDA	Open-CL	All of the these are examples of Graphics API
42	2	The mechanism by which tasks are assigned to processes for execution is called___?	Mapping	Computation	Process	None	The mechanism by which tasks are assigned to processes for execution is called mapping.

	marks	question	A	B	C	D	ans
43	2	A decomposition into a large number of small tasks is called_____ granularity.	Fine- grained	Coarse-grained	Vector-granied	All	A decomposition into a large number of small tasks is called fine-grained granularity.
44	2	Identical operations being applied concurrently on different data items is called?	Data-Parallelism	Parallelism	Data Serialsm	Concurrency	Identical operations being applied concurrently on different data items is called Data Parallelism.
45	2	System which do not have parallel processsing capabiities?	SISD	SIMD	MISD	MIMD	This is the explainantion.
46	2	The time and the location in the program of a static one-way interaction is known as ?	Priori	Polling	Decomposition	Execution	The time and the location in the program of a static one-way interaction is known a priori.
47	2	Memory access in RISC architecture is limited to which instructions?	STA and LDA	CALL and RET	Push and POP	MOV and JMP	This is the explaination.
48	2	Which Algorithms can be implemented in both shared-address-space and message-passing paradigms?	Data-Parallel Algo.	Quick-Sort Algo.	Data Algorithm	Bubble Sort Algo.	Data Parallel algorithms can be implemented in both shared-address-space and message-passing paradigms
49	2	Which type of Distribution is this?	Randomized Block Distribution	Block-Cyclic Distribution	Cyclic Distribution	None	This figure shows Randomized Block Distribution.
50	2	An abstraction used to express such dependencies among tasks and their relative order of execution is known as_____?	Task-Dependency Graph.	Dependency Graph.	Time-Dependency Graph	None	An abstraction used to express such dependencies among tasks and their relative order of execution is known as a task-dependency graph.

	marks	question	A	B	C	D	ans
51	3	Which is the simplest way to distribute an array and assign uniform contiguous portions of the array to different processes?	Block Distrbution	Array Distrbution	Process Distribution	All	Block distributions are some of the simplest ways to distribute an array and assign uniform contiguous portions of the array to different processes
52	3	An example of a decomposition with a regular interaction pattern is?	Image-dethering problem.	Travelling Salesman Problem	Time-complexity Problens	8 Queen problem.	An example of a decomposition with a regular interaction pattern is the problem of image dithering.
53	3	A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is	Critical-path	Process-path	Granularity.	Concurrency	A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is critical path.
54	3	The shared-address-space programming paradigms can handle which interactions?	Both	Two way	One way	None	The shared-address-space programming paradigms can handle both one-way and two-way interactions.
55	3	Which distribution can result in an almost perfect load balance due to the extreme fine-grained underlying decomposition.	Cyclic Distribution.	Array Distribution	Block-Cyclic Distribution	Block Distribution.	Cyclic Distribution can result in an almost perfect load balance due to the extreme fine-grained underlying decomposition.
56	3	Data sharing interactions can be categorized as_____interactions?	Both	Read-Write	Read only	None	Data sharing interactions can be categorized as either read-only or read-write interactions

	marks	question	A	B	C	D	ans
57	3	What is the way of structuring a parallel algorithm by selecting a decomposition and mapping technique and applying the appropriate strategy to minimize interactions called?	Algorithm Model	Parallel Model	Data Model	Mapping Model	Algo. Model is a way of structuring a parallel algorithm by selecting a decomposition and mapping technique and applying the appropriate strategy to minimize interactions.
58	3	Which Algorithm is this?	Serial column based Algo.	Column-Algorithm	Bubble Sort Algo.	None.	This is Serial Column based algorithm.
59	3	Algorithms based on the task graph model include:	All	Matrix-Factorization	Parallel QuickSort	Quicksort	This is an Explaination.
60	1	Which model permits simultaneous communication on all the channels connected to a node?	All-port communication	One-port communication	Dual-port communication	Quad-port communication	All-port communication model permits simultaneous communication on all the channels connected to a node.
61	1	A process sends the same m-word message to every other process, but different processes may broadcast different messages. It is called?	All to All Broadcast	One to All Broadcast	All to All Reduction	None	This is an Explaination.
62	1	The Matrix is transposed using which operation?	All to All personalized communication	One-to-all personalized communication	All-to-one personalized communication	One to one personalized communication.	This is an Explaination.
63	1	Each node in a two-dimensional wraparound mesh has how many ports?	Four	Two	Three	One	Each node in a two-dimensional wraparound mesh has four ports
64	1	Circular shift is a member of a broader class of global communication operations known as?	Permutation	Combination.	Both a and b	None	This is ann explaination.
65	1	We define_____ as the operation in which node i sends a data packet to node (i + q) mod p in a p-node ensemble (0 < q < p).	Circular q-shift	Linear shift	Circular shift	Linear q-shift.	We define a circular q-shift as the operation in which node i sends a data packet to node (i + q) mod p in a p-node ensemble (0 < q < p).

	marks	question	A	B	C	D	ans
66	1	Parallel algorithms often require a single process to send identical data to all other processes or to a subset of them. This operation is known as?	One to All Broadcast	One to One Broadcast	All to One Broadcast	None	Parallel algorithms often require a single process to send identical data to all other processes or to a subset of them. This operation is known as One to All Broadcast.
67	1	In which Communication each node sends a distinct message of size m to every other node?	All to All personalized communication	One to One personalized communication	All-to-one personalized communication	One-to-all personalized communication.	This is an Explaination.
68	1	All to All personalized communication operation is not used in a which of these parallel algorithms?	Quick Sort	Matrix-Transpose	Fourier Transformation	Database Join operation	This is an Explaination.
69	1	The Dual of one-to-all broadcast is?	All to one Reduction	All to one Broadcast	One to Many Reduction	All to All Broadcast	The dual of one to all Broadcast is called all to one reduction.
70	1	Reduction on a linear array can be performed by_____ the direction and the sequence of communication?	Reversing	Forwarding	Escaping	Widening	Reduction on a linear array can be performed by simply reversing the direction and the sequence of communication
71	2	This equation is used to solve which topology operations in all to all communications?	Hypercube	Mesh	Ring	Linear-Array	This is an Explaination.
72	2	\nThe communication pattern of all-to-all broadcast can be used to perform_____?	Third Variation of Reduction	Second Variation of Reduction	First Variation of Reduction	Fifth Variation of Reduction	This is an Explaination.
73	2	A single node sends a unique message of size m to every other node. This operation is known as_____?	Scatter	Reduction	Gather	Concatenate	In the scatter operation, a single node sends a unique message of size m to every other node.
74	2	The Algorithm represents which broadcast?	All to All Broadcast	All to All Broadcast	All to All Reduction	One to One Reduction	This is an explaination.
75	2	The message can be broadcast in how many steps?	Log(p)	Log(p^2)	One	Sin(p)	The message can be broadcast in log p steps.
76	2	This equation is used to solve which operations?	All to All personalized communication	One-to-all personalized communication	One to one personalized communication	All-to-one personalized communication.	This is an Explaination.

	marks	question	A	B	C	D	ans
77	2	There are how many computations for n^2 words of data transferred among the nodes?	N^3	Tan n	E^n	Log n	There are n^3 computations for n^2 words of data transferred among the nodes.
78	2	Scatter Operation is also known as?	One-to-all personalized communication	One-to-one personalized communication	All-to-one personalized communication	All-to-all personalized communication.	Scatter opeartion is also known as One-to-all personalized communication.
79	2	A Hypercube with 2d nodes can be regarded as a d-dimensional mesh with____ nodes in each dimension.	Two	One	Three	Four	A hypercube with 2d nodes can be regarded as a d-dimensional mesh with two nodes in each dimension
80	2	One-to-all broadcast and all-to-one reduction are used in several important parallel algorithms including?	All	Gausiian Elimination	Shortest path Algo.	Matrix- Vector multiplication	This is an Explaination.
81	2	Each node of the distributed-memory parallel computer is a_____ shared-memory multiprocessor.	NUMA	UMA	CCMA	None	Each node of the distributed-memory parallel computer is a NUMA shared-memory multiprocessor.
82	2	To perform a q-shift, we expand q as a sum of distinct powers of_____?	2	3	e	Log p	To perform a q-shift, we expand q as a sum of distinct powers of 2 .
83	3	In which implementation of circular shift, the entire row to data set is shifted by	Mesh	Hypercube	Ring	Linear	This is an Explaination
84	3	On a p-node hypercube with all-port communication, the coefficients of tw in the expressions for the communication times of one-to-all and all-to-all broadcast and personalized communication are all smaller than their single-port counterparts by a factor of?	Log(p)	Cos(p)	Sin(p)	E^p	On a p-node hypercube with all-port communication, the coefficients of tw in the expressions for the communication times of one-to-all and all-to-all broadcast and personalized communication are all smaller than their single-port counterparts by a factor of log p.

	marks	question	A	B	C	D	ans
85	3	The Equation represents which analysis in All to All Broadcasts?	Cost Analysis	Time Analysis	Data Model Analysis	Space-Time Analysis	Ans-(c) Cost Analysis.
86	3	On a p-node hypercube, the size of each message exchanged in the i th of the log p steps is?	A	B	C	D	A
87	3	Which broadcast is applied on this 3D hypercube?	One to All Broadcast	One to One Broadcast	All to One Broadcast	All to one Reduction	This figure shows One to All Broadcast being applied on 3D hypercube.
88	3	The Equation represents which analysis in One to All Broadcasts?	Cost Analysis	Time Analysis	Data Analysis	Space Analysis	This is an explaination.
89	3	The time for circular shift on a hypercube can be improved by almost a factor of _____ for large messages.	Log p	Cos(p)	e^p	Sin p	The time for circular shift on a hypercube can be improved by almost a factor of log p for large messages.
90	1	The execution time of parallel algorithm doesnâ€™t depends upon?	Processor	Input Size	Relative computation	Communication speed	The execution time of a parallel algorithm depends not only on input size but also on the number of processing elements used, and their relative computation and interprocess communication speeds.
91	1	Processing elements in a parallel system may become idle due to many reasons such as:	Both	Synchronization	Load Imbalance	The processing element doesnâ€™t become idle.	Both synchronization and load imbalance
92	1	If the scaled-speedup curve is close to linear with respect to the number of processing elements, then the parallel system is considered as?	Scalable	Iso-scalable	Non-Scalable	Scale-Efficient	If the scaled-speedup curve is close to linear with respect to the number of processing elements, then the parallel system is considered scalable

	marks	question	A	B	C	D	ans
93	1	Which system is the combination of an algorithm and the parallel architecture on which it is implemented?	Parallel System	Data- Parallel System	Architecture System	Series System	A parallel system is the combination of an algorithm and the parallel architecture on which it is implemented
94	1	What is defined as the speedup obtained when the problem size is increased linearly with the number of processing elements?	Scalable Speedup	Unscalable Speedup	Superlinearity Speedup	Isoefficiency Speedup	Scalable Speedup defined as the speedup obtained when the problem size is increased linearly with the number of processing elements
95	1	The maximum number of tasks that can be executed simultaneously at any time in a parallel algorithm is called its degree of_____.	Concurrency	Parallelism	Linearity	Execution	The maximum number of tasks that can be executed simultaneously at any time in a parallel algorithm is called its degree of concurrency.
96	1	The isoefficiency due to concurrency in 2-D partitioning is:	O(p)	O(n Logp)	O(1)	O(n^2)	This is an explaination.
97	2	The total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element is known as?	Total Overhead	Overhead	Serial Runtime	Parallel Runtime	We define total overhead of a parallel system as the total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element.
98	2	Parallel computations involving matrices and vectors readily lend themselves to data _____.	Decomposition	Composition	Linearity	Parallelsim	Parallel computations involving\nmatrices and vectors readily lend themselves to data decomposition.

	marks	question	A	B	C	D	ans
99	2	Parallel 1-D with Pipelining is a_____ algorithm?	Synchronous	Asynchronous	Optimal	Cost-optimal	This is an explaination.
100	2	The serial complexity of Matrix-Matrix Multiplication is:	Õ•(n^3)	O(n^2)	O(n)	O(nlogn)	This is an explaination
101	2	What is the problem size for n x n matrix multiplication?	Ï´(n^3)	Ï´(nlogn)	Ï´(n^2)	Ï´(1)	Ï´(n^3) is the problem size.
102	2	The given equation represents which function?	Overhead Function	Parallel Model	Series Overtime	Parallel Overtime	This is an explaination.
103	2	The efficiency of a parallel program can be written as:	A	B	C	D	A
104	2	The total number of steps in the entire pipelined procedure is_____?	Î˜(n)	Î˜(n^2)	Î˜(n^3)	Î˜(1)	The total number of steps in the entire pipelined procedure is Î˜(n)
105	2	In Canon's Algorithm, the memory used is?	Î¸(n^2)	Î¸(n)	Î¸(n^3)	Î¸(nlogn)	This is an explaination.
106	2	Consider the problem of multiplying two n Ã— n dense, square\nmatrices A and B to yield the product matrix C =:	AÃ—B	A/B	A+B	A-B	Consider the problem of multiplying two n Ã— n dense, square\nmatrices A and B to yield the product matrix C = A Ã— B.
107	2	The serial runtime of multiplying a matrix of dimension n x n with a vector is?	A	B	C	D	A
108	2	_____is a measure of the fraction of time for which a processing element is usefully employed.	Efficiency	Linearity	Overtime Function	Superlinearity	Efficiency is a measure of the fraction of time for which a processing element is usefully employed.
109	2	When the work performed by a serial algorithm is greater than its parallel formulation or due to hardware features that put the serial implementation at a disadvantage.This phenomena is known as?	Superlinear Speedup	Linear Speedups	Super Linearity	Performance Metrics	This is an explaintion
110	3	The all-to-all broadcast and the computation of y[i] both take time?	Î˜(n)	Î˜(nlogn)	Î˜(n^2)	Î˜(n^3)	This is an explaination.

	marks	question	A	B	C	D	ans
111	3	If virtual processing elements are mapped appropriately onto physical processing elements, the overall communication time does not grow by more than a factor of	N/p	P/n	N+p	N*p	If virtual processing elements are mapped appropriately onto physical processing elements, the overall communication time does not grow by more than a factor of n/p
112	3	Parallel execution time can be expressed as a function of problem size, overhead function, and the number of processing elements.The Formed eqn is:	A	B	C	D	A
113	3	In 2-D partioning, the first alignment takes time=?	Ts + twn/âˆšp.\n	Ts - twn/âˆšp.\n	Ts*twn/âˆšp.\n	Ts/ twn*âˆšp.\n	Ts + twn/âˆšp.\n
114	3	Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called_____?	Scaling Down	Scaling up	Scaling	Stimulation	Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called scaling down.
115	3	Which of the following is a drawback of matrix matrix multiplication?	Memory Optimal	Efficient	Time-bound	Complex	This is an explaination
116	3	Consider the problem of sorting 1024 numbers (n = 1024, log n = 10) on 32 processing elements. The speedup expected is	P/log n	P*log n	P+logn	N*log p	Consider the problem of sorting 1024 numbers (n = 1024, log n = 10) on 32 processing elements. The speedup expected is p/logn
117	3	Consider the problem of adding n numbers on p processing elements such that p < n and both n and p are powers of 2. The overall parallel execution time of the problem is:	ê™¨((n/p) log p).	ê™¨((n*p) log p).	ê™¨((p/n) log p).	ê™¨((n) log p).	Ans-(a)-ê™¨((n/p) log p).
118	3	DNS algorithm has____ runtime?	â„¦(n)	â„¦(n^2)	â„¦(n^3)	â„¦(logn)	DNS has â„¦(n) runtime

	marks	question	A	B	C	D	ans
119	3	The serial algorithm requires_____ multiplications and additions in matrix-vector multiplication.\n	N^2	N^3	Log n	Nlog(n)	Ans-(b)-n^2. The serial algorithm requires n^2 multiplications and additions.\n\n
120	1	The time required to merge two sorted blocks of n/p elements is_____?\n\n	Î,(n/p)	Î,(n)	Î,(p/n)	Î,(nlogp)	The time required to merge two sorted blocks of n/p elements is Î,(n/p).\n\n
121	1	In Parallel DFS,the stack is split into two equal pieces such that the size of the search space represented by each stack is the same. Such a split is called?.	Half-Split	Half-Split	Parallel-Split	None	The stack is split into two equal pieces such that the size of the search space represented by each stack is the same. Such a split is called a half-split.
122	1	To avoid sending very small amounts of work, nodes beyond a specified stack depth are not given away. This depth is called the_____depth.	Cut-Off	Breakdown	Full	Series	To avoid sending very small amounts of work, nodes beyond a specified stack depth are not given away. This depth is called the cutoff depth.
123	1	In sequential sorting algorithms, the input and the sorted sequences are stored in which memory?	Process Memory	Secondary Memory	Main Memory	External Memory	In sequential sorting algorithms, the input and the sorted sequences are stored in the process's memory
124	1	Each process sends its block to the other process. Now, each process merges the two sorted blocks and retains only the appropriate half of the merged block. We refer to this operation as?	Compare-Split	Split	Compare	Exchange.	Each process sends its block to the other process. Now, each process merges the two sorted blocks and retains only the appropriate half of the merged block. We refer to this operation as compare-split.

	marks	question	A	B	C	D	ans
125	1	Each process compares the received element with its own and retains the appropriate element.We refer this operation as_____?	Compare Exchange	Exchange	Process-Exchange	All	Each process compares the received element with its own and retains the appropriate element. We refer this as compare exchange.
126	1	Which algorithm maintains the unexpanded nodes in the search graph, ordered according to their l-value?	Parallel BFS	Parallel DFS	Both a and b	None	Parallel BFS maintains the unexpanded nodes in the search graph, ordered according to their l-value.
127	1	The critical issue in parallel depth-first search algorithms is the distribution of the search space among the_____?	Processor	Space	Memory	Blocks	The critical issue in parallel depth-first search algorithms is the distribution of the search space among the processors
128	2	Enumeration Sort uses how many processes to sort n elements?	N^2	Logn	N^3	N	This is an explaination.
129	2	Which sequence is a sequence of elements <a0, a1, ..., an-1> with the property that either (1) there exists an index i, 0 â‰¤ i â‰¤n - 1, such that <a0, ..., ai > is monotonically increasing and <ai +1, ..., an-1> is monotonically decreasing, or (2) there exists a cyclic shift of indices so that (1) is satisfied.	Bitonic Sequence	Acyclic Sequence	Asymptotic Sequence	Cyclic Sequence.	A bitonic sequence is a sequence of elements <a0, a1, ..., an-1> with the property that either (1) there exists an index i, 0 i n - 1, such that <a0, ..., ai > is monotonically increasing and <ai +1, ..., an-1> is monotonically decreasing, or (2) there exists a cyclic shift of indices so that (1) is satisfied

	marks	question	A	B	C	D	ans
130	2	To make a substantial improvement over odd-even transposition sort, we need an algorithm that moves elements long distances. Which one of these is such serial sorting algorithm?	Shell Sort	Linear Sort	Quick-Sort	Bubble Sort	To make a substantial improvement over odd-even transposition sort, we need an algorithm that moves elements long distances. Shellsort is one such serial sorting algorithm.
131	2	Quick-Sort is a_____ algorithm?	Divide and Conquer	Greedy Approach	Both a and b	None	Quicksort is a Divide and Conquer algorithm.
132	2	The_____ transposition algorithm sorts n elements in n phases (n is even), each of which requires n/2 compare-exchange operations.	Odd-Even	Odd	Even	None	This is an explaination.
133	2	The average time complexity for Bucket Sort is?	O(n+k)	O(nlog(n+k))	O(n^3)	Î,(n^2)	The average time complexity for Bucket Sort is O(n + k).
134	2	A popular serial algorithm for sorting an array of n elements whose values are uniformly distributed over an interval [a, b] is which algorithm?	Bucket Sort	Quick-Sort Algo.	Linear Sort	Bubble-Sort	A popular serial algorithm for sorting an array of n elements whose values are uniformly distributed over an interval [a, b] is the bucket sort algorithm
135	2	Best Case time complexity of Bubble Sort is:	O(n)	O(n^3)	O(nlogn)	O(n^2)	Best case complexity of bubblesort is O(n).

	marks	question	A	B	C	D	ans
136	2	When more than one process tries to write to the same memory location, only one arbitrarily chosen process is allowed to write, and the remaining writes are ignored. This process is called_____ in quick sort.	CRCW-PRAM	PRAM	Partitioning	CRCW	When more than one process tries to write to the same memory location, only one arbitrarily chosen process is allowed to write, and the remaining writes are ignored.It is called CRCW PRAM quick sort algo.
137	2	Average Time Complexity in a quicksort algorithm is:	O(nlogn)	O(n)	O(n^3)	Î¸(n^2)	This is an explainatoin.
138	2	The isoefficiency function of Global Round Robin (GRR) is:	O (p^2 log p)	O (p log p)	O (log p)	O (p^2)	The isoefficiency function of GRR is O (p^2 log p)
139	2	A_____ is a device with two inputs x and y and two outputs x' and y' in a Sorting Network.	Comparator	Router	Separator	Switch.	A comparator is a device with two inputs x and y and two outputs x' and y'
140	2	If T is a DFS tree in G then the parallel implementation of the algorithm runs in _____time complexity.	O(t)	O(tlogn)	O(logt)	O(1)	If T is a DFS tree in G then the parallel implementation of the algorithm outputs a proof that can be verified in O(t) time complexity.
141	2	In the quest for fast sorting methods, a number of networks have been designed that sort n elements in time significantly smaller than___?	Î¸(nlogn)	Î¸(n)	Î¸(1)	Î¸(n^2)	In the quest for fast sorting methods, a number of networks have been designed that sort n elements in time significantly smaller than Î¸(nlogn).
142	2	The average value of the search overhead factor in parallel DFS is less than_____?	One	Two	Three	Four	The average value of the search overhead factor in parallel DFS is less than one
143	3	Parallel runtime for Ring architecture in a bitonic sort is:	Î¸(n)	Î¸(nlogn)	Î¸(n^2)	Î¸(n^3)	Parallel runtime for Ring architecture in a bitonic sort is Î¸(n)

	marks	question	A	B	C	D	ans
144	3	The Sequential Complexity of Odd-Even Transposition Algorithm is:	Î¸(n^2)	Î¸(nlogn)	Î¸(n^3)	Î¸(n)	This is an explaination.
145	3	The Algorithm represents which bubble sort:	Sequential Bubble Sort	Circular Bubble Sort	Simple Bubble Sort	Linear Bubble Sort	This is an explaination.
146	3	Enumeration Sort uses how much time to sort n elements?	Î¸(1)	Î¸(nlogn)	Î¸(n^2)	Î¸(n)	This is an explaination.
147	3	The_____algorithm relies on the binary representation of the elements to be sorted.	Radix-sort	Bubble Sort	Quick-Sort	Bucket-Sort	The radix sort algorithm relies on the binary representation of the elements to be sorted.
148	3	Parallel runtime for Mesh architecture in a bitonic sort is:	Î¸(n/logn)	Î¸(n)	Î¸(n^2)	Î¸(n^3)	This is an explaination.
149	1	The number of threads in a thread block is limited by the architecture to a total of how many threads per block?	512	502	510	412	The number of threads in a thread block is also limited by the architecture to a total of 512 threads per block
150	1	CUDA Architecture is mainly provided by which company?	NVIDIA	Intel	Apple	IBM	NVIDIA provides CUDA services.
151	1	In CUDA Architecture, what are subprograms called?	Kernel	Grid	Element	Blocks	Subprograms are called kernels.
152	1	What is the fullform of CUDA?	Compute Unified Device Architecture	Computer Unified Device Architecture	Common USB Device Architecture	Common Unified Disk Architecture	CUDA Stands for Compute Unified Device Architecture.
153	2	Which of these is not an application of CUDA Arhitecture?	Thermo Dynamics	Neural Networks	VLSI Stimulation	Fluid Dynamics	CUDA architecture has no use on Thermo Dynamics.
154	2	CUDA programming is especially well-suited to address problems that can be expressed as_____ computations.	Data parallel	Task Parallel	Both a and b	None	CUDA programming is especially well-suited to address problems that can be expressed as dataparallel computations.
155	2	CUDA C/C++ uses which keyword in programming:	global	kernel	Cuda_void	nvcc	This is an explaination.
156	2	CUDA programs are saved with_____ extension.	.cd	.cx	.cc	.cu	This is an explaination

	marks	question	A	B	C	D	ans
157	2	The Kepler K20-X chip block, contains____ streaming multiprocessors\n(SMs).	15	8	16	7	The Kepler K20X chip block diagram, containing 15 streaming multiprocessors (SMs)
158	2	The Kepler K20X architecture increases the register file size to:	64K	32K	128K	256K	The K20X architecture increases the register fi le size to 64K
159	2	The register file in a GPU is of what size?	2 MB	1 MB	3MB	1024B	Register size in a GPU is 2MB.
160	2	NVIDIAâ€™s GPU computing platform is not enabled on which of the following product families:	AMD	Tegra	Quadro	Tesla	This is an explaination.
161	2	Tesla K-40 has compute capability of:	3.5	3.2	3.4	3.1	This is an explaination.
162	2	The SIMD unit creates, manages, schedules and executes_____ threads simultaneously to create a warp.	32	16	24	8	The SIMD unit creates, manages, schedules and executes 32 threads simultaneously to create a warp
163	2	Which hardware is used by the host interface to fasten the transfer of bulk data to and fro the graphics pipeline?	Direct Memory Access	Switch	Hub	Memory Hardware	This is an Explaination
164	2	A ____ is a collection of thread blocks of the same thread dimensionality which all execute the same kernel.	Grid	Core	Element	Blcoks	A â€˜gridâ€™ is a collection of thread blocks of the same thread dimensionality which all execute the same kernel
165	2	Active Warps can be classified into how many types?	3	2	4	5	This is an explaination.
166	2	All threads in a grid share the same_____space.	Global memory	Local Memory	Synchronized Memory	All	All threads in a grid\nshare the same global memory space
167	2	CUDA was introduced in which year?	2007	2006	2008	2010	This is an explaination.

	marks	question	A	B	C	D	ans
168	3	Unlike a C function call, all CUDA kernel launches are:	Asynchronous	Synchronous	Both a and b	None	Unlike a C function call, all CUDA kernel launches are asynchronous
169	3	A warp consists of____consecutive threads and all threads in a warp are executed in Single Instruction Multiple Thread (SIMT) fashion.	32	16	64	128	A warp consists of 32 consecutive threads and all\nthreads in a warp are executed in Single Instruction Multiple Thread (SIMT) fashion
170	3	There are how many streaming multiprocessors in CUDA architecture?	16	8	12	4	This is an explaination.
171	3	In CUDA programming, if CPU is the host then device will be:	GPU	Compiler	HDD	GPGPU	This is an explaination.
172	3	Both grids and blocks use the_____ type with three unsigned integer fields.	Dim3	Dim2	Dim1	Dim4	Both grids and blocks use the dim3 type with three unsigned integer fi elds
173	3	Tesla P100 GPU based on the Pascal GPU Architecture has 56 Streaming Multiprocessors (SMs), each capable of supporting up to____active threads.	2048	512	1024	256	Tesla P100 GPU based on the Pascal GPU Architecture has 56 Streaming Multiprocessors (SMs), each capable of supporting up to 2048 active threads.
174	3	The maximum size at each level of the thread hierarchy is_____dependent.	Device	Host	Compiler	Memory	The maximum size at each level of the thread hierarchy is device dependent.
175	3	Intel I7 has the memory bus of width:	19B	180B	152B	102B	This is an explaination.
176	3	The_____ is the heart of the GPU architecture:	Streaming Multiprocessor	Multiprocessor	CUDA	Compiler	The Streaming Multiprocessor (SM) is the heart of the GPU architecture.

	marks	question	A	B	C	D	ans
177	3	A kernel is defined using the_____ declaration specification	_global	_host	_device	_void	A kernel is defi ned using the\n__global declaration specifi cation
178	3	The function printThreadInfo() is not used to print out which of the following information about each thread:	Memory Allocations	Block Index	Matrix Coordinates	Control-Index	Ans-(d)- Memory Allocations.

Which is alternative options for latency hiding?
A. Increase CPU frequency
B. Multithreading
C. Increase Bandwidth
D. Increase Memory
ANSWER: B

_____ Communication model is generally seen in tightly coupled system.
A. Message Passing
B. Shared-address space
C. Client-Server
D. Distributed Network
ANSWER: B

The principal parameters that determine the communication latency are as follows:
A. Startup time (ts) Per-hop time (th) Per-word transfer time (tw)
B. Startup time (ts) Per-word transfer time (tw)
C. Startup time (ts) Per-hop time (th)
D. Startup time (ts) Message-Packet-Size(W)
ANSWER: A

The number and size of tasks into which a problem is decomposed determines the __
A. Granularity
B. Task
C. Dependency Graph
D. Decomposition
ANSWER: A

Average Degree of Concurrency is...
A. The average number of tasks that can run concurrently over the entire duration of execution of the process.
B. The average time that can run concurrently over the entire duration of execution of the process.
C. The average in degree of task dependency graph.
D. The average out degree of task dependency graph.
ANSWER: A

Which task decomposition technique is suitable for the 15-puzzle problem?
A. Data decomposition
B. Exploratory decomposition
C. Speculative decomposition
D. Recursive decomposition
ANSWER: B

Which of the following method is used to avoid Interaction Overheads?
A. Maximizing data locality
B. Minimizing data locality
C. Increase memory size
D. None of the above.
ANSWER: A

Which of the following is not parallel algorithm model
A. The Data Parallel Model
B. The work pool model
C. The task graph model
D. The Speculative Model
ANSWER: D

Nvidia GPU based on following architecture
A. MIMD
B. SIMD
C. SISD
D. MISD
ANSWER: B

What is Critical Path?

A. The length of the longest path in a task dependency graph is called the critical path length.
B. The length of the smallest path in a task dependency graph is called the critical path length.
C. Path with loop
D. None of the mentioned.
ANSWER: A

Which decompositioin technique uses divide-andconquer strategy?
A. recursive decomposition
B. Sdata decomposition
C. exploratory decomposition
D. speculative decomposition
ANSWER: A

If there are 6 nodes in a ring topology how many message passing cycles will be required to complete broadcast process in one to all?

A. 1
B. 6
C. 3
D. 4
ANSWER: 3

If there is 4 X 4 Mesh topology network then how many ring operation will perform to complete one to all broadcast?

A. 4
B. 8
C. 16
D. 32
ANSWER: 8

Consider all to all broadcast in ring topology with 8 nodes. How many messages will be present with each node after 3rd step/cycle of communication?
A. 3
B. 4
C. 6
D. 7
ANSWER: 4

Consider Hypercube topology with 8 nodes then how many message passing cycles will require in all to all broadcast operation?

A. The longest path between any pair of finish nodes.
B. The longest directed path between any pair of start & finish node.
C. The shortest path between any pair of finish nodes.
D. The number of maximum nodes level in graph.
ANSWER: D

Scatter is _____.
A. One to all broadcast communication
B. All to all broadcast communication
C. One to all personalised communication
D. Node of the above.
ANSWER: C

If there is 4X4 Mesh Topology _____ message passing cycles will require complete all to all reduction.
A. 4
B. 6
C. 8
D. 16
ANSWER: C

Following issue(s) is/are the true about sorting techniques with parallel computing.
A. Large sequence is the issue
B. Where to store output sequence is the issue
C. Small sequence is the issue
D. None of the above
ANSWER: B

Partitioning on series done after _____
A. Local arrangement
B. Processess assignments
C. Global arrangement
D. None of the above
ANSWER: C

In Parallel DFS processes has following roles.(Select multiple choices if applicable)
A. Donor
B. Active
C. Idle
D. Passive
ANSWER: A

Suppose there are 16 elements in a series then how many phases will be required to sort the series using parallel odd-even bubble sort?
A. 8
B. 4
C. 5
D. 15
ANSWER: D

Which are different sources of Overheads in Parallel Programs?
A. Interprocess interactions
B. Process Idling
C. All mentioned options
D. Excess Computation
ANSWER: C

The ratio of the time taken to solve a problem on a parallel processors to the time required to solve the same problem on a single processor with p identical processing elements.
A. The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements.

B. The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements
C. The ratio of number of multiple processors to size of data
D. None of the above
ANSWER: B

Efficiency is a measure of the fraction of time for which a processing element is usefully employed.
A. TRUE
B. FALSE
ANSWER: A

CUDA helps do execute code in parallel mode using _____
A. CPU
B. GPU
C. ROM
D. Cash memory
ANSWER: B

In thread-function execution scenario thread is a _____
A. Work
B. Worker
C. Task
D. None of the above
ANSWER: B

In GPU Following statements are true
A. Grid contains Block
B. Block contains Threads
C. All the mentioned options.
D. SM stands for Streaming MultiProcessor
ANSWER: C

Computer system of a parallel computer is capable of_____
A. Decentralized computing
B. Parallel computing
C. Centralized computing
D. All of these
ANSWER: A

In which application system Distributed systems can run well?
A. HPC
B. Distrubuted Framework
C. HRC
D. None of the above
ANSWER: A

A pipeline is like ..... ?
A. an automobile assembly line
B. house pipeline
C. both a and b
D. a gas line
ANSWER: A

Pipeline implements ?
A. fetch instruction
B. decode instruction
C. fetch operand
D. all of above

ANSWER: D

A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ ?
A. Super-scaling
B. Pipe-lining
C. Parallel Computation
D. None of these
ANSWER: B

In a parallel execution, the performance will always improve as the number of processors will increase?
A. True
B. False
ANSWER: B

VLIW stands for ?
A. Very Long Instruction Word
B. Very Long Instruction Width
C. Very Large Instruction Word
D. Very Long Instruction Width
ANSWER: A

In VLIW the decision for the order of execution of the instructions depends on the program itself?
A. True
B. False
ANSWER: A

Which one is not a limitation of a distributed memory parallel system?
A. Higher communication time
B. Cache coherency
C. Synchronization overheads
D. None of the above
ANSWER: B

Which of these steps can create conflict among the processors?
A. Synchronized computation of local variables
B. Concurrent write
C. Concurrent read
D. None of the above
ANSWER: B

Which one is not a characteristic of NUMA multiprocessors?
A. It allows shared memory computing
B. Memory units are placed in physically different location
C. All memory units are mapped to one common virtual global memory
D. Processors access their independent local memories
ANSWER: D

Which of these is not a source of overhead in parallel computing?
A. Non-uniform load distribution
B. Less local memory requirement in distributed computing
C. Synchronization among threads in shared memory computing
D. None of the above
ANSWER: B

Systems that do not have parallel processing capabilities are?
A. SISD
B. SIMD

C. MIMD
D. All of the above
ANSWER: A

How does the number of transistors per chip increase according to Moore´s law?
A. Quadratically
B. Linearly
C. Cubicly
D. Exponentially
ANSWER: D

Parallel processing may occur?
A. in the instruction stream
B. in the data stream
C. both[A] and [B]
D. none of the above
ANSWER: C

To which class of systems does the von Neumann computer belong?
A. SIMD (Single Instruction Multiple Data)
B. MIMD (Multiple Instruction Multiple Data)
C. MISD (Multiple Instruction Single Data)
D. SISD (Single Instruction Single Data)
ANSWER: D

Fine-grain threading is considered as a _____ threading?
A. Instruction-level
B. Loop level
C. Task-level
D. Function-level
ANSWER: A

Multiprocessor is systems with multiple CPUs, which are capable of independently executing different tasks in parallel. In this category every processor and memory module has similar access time?
A. UMA
B. Microprocessor
C. Multiprocessor
D. NUMA
ANSWER: A

For inter processor communication the miss arises are called?
A. hit rate
B. coherence misses
C. comitt misses
D. parallel processing
ANSWER: B

NUMA architecture uses _____in design?
A. cache
B. shared memory
C. message passing
D. distributed memory
ANSWER: D

A multiprocessor machine which is capable of executing multiple instructions on multiple data sets?
A. SISD
B. SIMD

C. MIMD
D. MISD
ANSWER: C

In message passing, send and receive message between?
A. Task or processes
B. Task and Execution
C. Processor and Instruction
D. Instruction and decode
ANSWER: A

The First step in developing a parallel algorithm is_____?
A. To Decompose the problem into tasks that can be executed concurrently
B. Execute directly
C. Execute indirectly
D. None of Above
ANSWER: A

The number of tasks into which a problem is decomposed determines its?
A. Granularity
B. Priority
C. Modernity
D. None of above
ANSWER: A

The length of the longest path in a task dependency graph is called?
A. the critical path length
B. the critical data length
C. the critical bit length
D. None of above
ANSWER: A

The graph of tasks (nodes) and their interactions/data exchange (edges)?
A. Is referred to as a task interaction graph
B. Is referred to as a task Communication graph
C. Is referred to as a task interface graph
D. None of Above
ANSWER: A

Mappings are determined by?
A. task dependency
B. task interaction graphs
C. Both A and B
D. None of Above
ANSWER: C

Decomposition Techniques are?
A. recursive decomposition
B. data decomposition
C. exploratory decomposition
D. All of Above
ANSWER: D

The Owner Computes Rule generally states that the process assigned a particular data item is responsible for?
A. All computation associated with it
B. Only one computation
C. Only two computation
D. Only occasionally computation
ANSWER: A

A simple application of exploratory decomposition is_?
A. The solution to a 15 puzzle
B. The solution to 20 puzzle
C. The solution to any puzzle
D. None of Above
ANSWER: A

Speculative Decomposition consist of _?
A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B
ANSWER: C

task characteristics include?
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.
D. All of Above
ANSWER: D

Writing parallel programs is referred to as?
A. Parallel computation
B. Parallel processes
C. Parallel development
D. Parallel programming
ANSWER: D

Parallel Algorithm Models?
A. Data parallel model
B. Bit model
C. Data model
D. network model
ANSWER: A

The number and size of tasks into which a problem is decomposed determines the?
A. fine-granularity
B. coarse-granularity
C. sub Task
D. granularity
ANSWER: A

A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is its _____ path?
A. critical
B. easy
C. difficult
D. ambiguous
ANSWER: A

The pattern of_____ among tasks is captured by what is known as a task-interaction graph?
A. Interaction
B. communication
C. optmization
D. flow
ANSWER: A

Interaction overheads can be minimized by____?
A. Maximize Data Locality
B. Maximize Volume of data exchange
C. Increase Bandwidth
D. Minimize social media contents
ANSWER: A

Type of parallelism that is naturally expressed by independent tasks in a task-dependency graph is called _____ parallelism?
A. Task
B. Instruction
C. Data
D. Program
ANSWER: A

Speed up is defined as a ratio of?
A. s=Ts/Tp
B. S= Tp/Ts
C. Ts=S/Tp
D. Tp=S /Ts
ANSWER: A

Parallel computing means to divide the job into several _____?
A. Bit
B. Data
C. Instruction
D. Task
ANSWER: D

_____ is a method for inducing concurrency in problems that can be solved using the divide-and-conquer strategy?
A. exploratory decomposition
B. speculative decomposition
C. data-decomposition
D. Recursive decomposition
ANSWER: C

The___ time collectively spent by all the processing elements Tall = p TP?
A. total
B. Average
C. mean
D. sum
ANSWER: A

Group communication operations are built using point-to-point messaging primitives?
A. True
B. False
ANSWER: A

Communicating a message of size m over an uncongested network takes time ts + tmw?
A. True
B. False
ANSWER: A

The dual of one-to-all broadcast is ?
A. All-to-one reduction
B. All-to-one receiver

C. All-to-one Sum
D. None of Above
ANSWER: A

A hypercube has?
A. 2d nodes
B. 2d nodes
C. 2n Nodes
D. N Nodes
ANSWER: A

A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes?
A. True
B. False
ANSWER: A

In All-to-All Broadcast each processor is thesource as well as destination?
A. True
B. False
ANSWER: A

The Prefix Sum Operation can be implemented using the ?
A. All-to-all broadcast kernel.
B. All-to-one broadcast kernel.
C. One-to-all broadcast Kernel
D. Scatter Kernel
ANSWER: A

In the scatter operation ?
A. Single node send a unique message of size m to every other node
B. Single node send a same message of size m to every other node
C. Single node send a unique message of size m to next node
D. None of Above
ANSWER: A

The gather operation is exactly the inverse of the ?
A. Scatter operation
B. Broadcast operation
C. Prefix Sum
D. Reduction operation
ANSWER: A

In All-to-All Personalized Communication Each node has a distinct message of size m for every other node ?
A. True
B. False
ANSWER: A

Parallel algorithms often require a single process to send identical data to all other processes or to a subset of them. This operation is known as _____?
A. one-to-all broadcast
B. All to one broadcast
C. one-to-all reduction
D. all to one reduction
ANSWER: A

In which of the following operation, a single node sends a unique message of size m to every other node?
A. Gather
B. Scatter
C. One to all personalized communication
D. Both A and C
ANSWER: D

Gather operation is also known as _____?
A. One to all personalized communication
B. One to all broadcast
C. All to one reduction
D. All to All broadcast
ANSWER: A

one-to-all personalized communication does not involve any duplication of data?
A. True
B. False
ANSWER: A

Gather operation, or concatenation, in which a single node collects a unique message from each node?
A. True
B. False
ANSWER: A

Conventional architectures coarsely comprise of a?
A. A processor
B. Memory system
C. Data path.
D. All of Above
ANSWER: D

Data intensive applications utilize?
A. High aggregate throughput
B. High aggregate network bandwidth
C. High processing and memory system performance.
D. None of above
ANSWER: A

A pipeline is like?
A. Overlaps various stages of instruction execution to achieve performance.
B. House pipeline
C. Both a and b
D. A gas line
ANSWER: A

Scheduling of instructions is determined?
A. True Data Dependency
B. Resource Dependency
C. Branch Dependency
D. All of above
ANSWER: D

VLIW processors rely on?
A. Compile time analysis
B. Initial time analysis
C. Final time analysis

D. Mid time analysis
ANSWER: A

Memory system performance is largely captured by?
A. Latency
B. Bandwidth
C. Both a and b
D. none of above
ANSWER: C

The fraction of data references satisfied by the cache is called?
A. Cache hit ratio
B. Cache fit ratio
C. Cache best ratio
D. none of above
ANSWER: A

A single control unit that dispatches the same Instruction to various processors is?
A. SIMD
B. SPMD
C. MIMD
D. None of above
ANSWER: A

The primary forms of data exchange between parallel tasks are?
A. Accessing a shared data space
B. Exchanging messages.
C. Both A and B
D. None of Above
ANSWER: C

Switches map a fixed number of inputs to outputs?
A. True
B. False
ANSWER: A

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A. Decentralized computing
B. Parallel computing
C. Centralized computing
D. Decentralized computing
E. Distributed computing
ANSWER: A

Writing parallel programs is referred to as?
A. Parallel computation
B. Parallel processes
C. Parallel development
D. Parallel programming
ANSWER: D

Simplifies applications of three-tier architecture is _____?
A. Maintenance
B. Initiation
C. Implementation
D. Deployment
ANSWER: D

Dynamic networks of networks, is a dynamic connection that grows is called?
A. Multithreading
B. Cyber cycle
C. Internet of things
D. Cyber-physical system
ANSWER: C

In which application system Distributed systems can run well?
A. HPC
D. HTC
C. HRC
D. Both A and B
ANSWER: D

In which systems desire HPC and HTC?
A. Adaptivity
B. Transparency
C. Dependency
D. Secretive
ANSWER: B

No special machines manage the network of architecture in which resources are known as?
A. Peer-to-Peer
B. Space based
C. Tightly coupled
D. Loosely coupled
ANSWER: A

Significant characteristics of Distributed systems have of ?
A. 5 types
B. 2 types
C. 3 types
D. 4 types
ANSWER: C

Built of Peer machines are over?
A. Many Server machines
B. 1 Server machine
C. 1 Client machine
D. Many Client machines
ANSWER: D

Type HTC applications are?

A. Business
B. Engineering
C. Science
D. Media mass
ANSWER: A

Virtualization that creates one single address space architecture that of, is called?
A. Loosely coupled
B. Peer-to-Peer
C. Space-based
D. Tightly coupled
ANSWER: C

We have an internet cloud of resources In cloud computing to form?
A. Centralized computing
B. Decentralized computing
C. Parallel computing
D. All of these
ANSWER: D

Data access and storage are elements of Job throughput, of _____?
A. Flexibility
B. Adaptation
C. Efficiency
D. Dependability
ANSWER: C

Billions of job requests is over massive data sets, ability to support known as?
A. Efficiency
B. Dependability
C. Adaptation
D. Flexibility
ANSWER: C

Broader concept offers Cloud computing .to select which of the following?
A. Parallel computing
B. Centralized computing
C. Utility computing
D. Decentralized computing
ANSWER: C

Resources and clients transparency that allows movement within a system is called?
A. Mobility transparency
B. Concurrency transparency
C. Performance transparency
D. Replication transparency
ANSWER: A

Distributed program in a distributed computer running a is known as?
A. Distributed process
B. Distributed program
C. Distributed application
D. Distributed computing
ANSWER: B

Uniprocessor computing devices is called_____?
A. Grid computing

B. Centralized computing
C. Parallel computing
D. Distributed computing
ANSWER: B

Utility computing focuses on a_____ model?
A. Data
B. Cloud
C. Scalable
D. Business
ANSWER: D

What is a CPS merges technologies?
A. 5C
B. 2C
C. 3C
D. 4C
ANSWER: C

Aberration of HPC?
A. High-peak computing
B. High-peripheral computing
C. High-performance computing
D. Highly-parallel computing
ANSWER: C

Peer-to-Peer leads to the development of technologies like?
A. Norming grids
B. Data grids
C. Computational grids
D. Both A and B
ANSWER: D

Type of HPC applications of?
A. Management
B. Media mass
C. Business
D. Science
ANSWER: D

The development generations of Computer technology has gone through?
A. 6
B. 3
C. 4
D. 5
ANSWER: D

Utilization rate of resources in an execution model is known to be its?
A. Adaptation
B. Efficiency
C. Dependability
D. Flexibility
ANSWER: B

Even under failure conditions Providing Quality of Service (QoS) assurance is the responsibility of?
A. Dependability
B. Adaptation
C. Flexibility
D. Efficiency

ANSWER: A

Interprocessor communication that takes place?
A. Centralized memory
B. Shared memory
C. Message passing
D. Both A and B
ANSWER: D

Data centers and centralized computing covers many and?
A. Microcomputers
B. Minicomputers
C. Mainframe computers
D. Supercomputers
ANSWER: D

Which of the following is an primary goal of HTC paradigm_____?
A. High ratio Identification
B. Low-flux computing
C. High-flux computing
D. Computer utilities
ANSWER: C

The high-throughput service provided is measures taken by
A. Flexibility
B. Efficiency
C. Dependability
D. Adaptation
ANSWER: D

What are the sources of overhead?
A. Essential /Excess Computation
B. Inter-process Communication
C. Idling
D. All above
ANSWER: D

Which are the performance metrics for parallel systems?
A. Execution Time
B. Total Parallel Overhead
C. Speedup
D. All above
ANSWER: D

The efficiency of a parallel program can be written as: E = Ts / pTp.
True or False?
A. True
B. False
ANSWER: A

The important feature of the VLIW is _____?
A. ILP
B. Performance
C. Cost effectiveness
D. delay
ANSWER: A

What are the sources of overhead?

A. Essential /Excess Computation
B. Inter-process Communication
C. Idling
D. All above

Answer : D

Which are the performance metrics for parallel systems?

A. Execution Time
B. Total Parallel Overhead
C. Speedup
D. Efficiency
E. Cost
F. All above

Answer : F

The efficiency of a parallel program can be written as: ***E = Ts / pTp.*** True or False?

A. True
B. False

Answer : A

Overhead function or ***total overhead*** of a parallel system as the total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element. True or False?

A. True
B. False

Answer : A

What is Speedup?

A. A measure that captures the relative benefit of solving a problem in parallel. It is defined as the ratio of the time taken to solve a problem on a single processing element to the time required to solve the same problem on a parallel computer with *p* identical processing elements.
B. A measure of the fraction of time for which a processing element is usefully employed.
C. None of the above

Answer : A

In an ideal parallel system, speedup is equal to *p* and efficiency is equal to one. True or False?

A. True
B. False

Answer : A

A parallel system is said to be _____ if the cost of solving a problem on a parallel computer has the same asymptotic growth (in Θ terms) as a function of the input size as the fastest-known sequential algorithm on a single processing element.

A. Cost optimal
B. Non Cost optimal

Answer : A

Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called _____ a parallel system in terms of the number of processing elements.

A. Scaling down
B. Scaling up

Answer : B

The _____ function determines the ease with which a parallel system can maintain a constant efficiency and hence achieve speedups increasing in proportion to the number of processing elements.

A. Isoefficiency
B. Efficiency
C. Scalability
D. Total overhead

Answer : A

Minimum execution time for adding n numbers is *Tp = n/p + 2 logp* True or False ?

A. True
B. False

Answer : A

The overhead function To = pTP – TS.

A. True
B. False

Answer : A

Performance Metrics for Parallel Systems: Speedup(S) =TS/TP

A. True
B. False

Answer : A

Matrix Vector multiplication 2D Partitions requires some basic communication operations

A. one-to-one communication to align the vector along the main diagonal
B. one-to-all broadcast of each vector element among the n processes of each column
C. all-to-one reduction in each row
D. All Above

Answer : D

What are the issues in sorting?

A. Where the Input and Output Sequences are Stored

B. How Comparisons are Performed

C. All above

Answer : C

The parallel run time of the formulation for Bubble sort is

A. Tp = O(n/plogn/p) + O(n) + O(n)

B. Tp = O(n/plogn/p) + O (n/plogp) + O(ln/p)

C. Non of the above

Answer : A

What are the variants of Bubble sort?

A. Shell sort

B. Quick sort

C. Odd-Even transposition

D. Option A & C

Answer : D

What is the overall complexity of parallel algorithm for quick sort?

A. Tp = O(n/p logn/p) + O(n/p logp) + O($\log^2$p)

B. Tp = O(n/p logn/p) + O(n/p logp)

C. Tp = O(n/p logn/p) + O($\log^2$p)

Answer : A

Formally, given a weighted graph $G(V, E, w)$, the ***all-pairs shortest paths*** problem is to find the shortest paths between all pairs of vertices. True or False?

A. True
B. False

Answer : A

What is true for parallel formulation of Dijkstra's Algorithm?

A. One approach partitions the vertices among different processes and has each process compute the single-source shortest paths for all vertices assigned to it. We refer to this approach as the ***source-partitioned formulation.***
B. Another approach assigns each vertex to a set of processes and uses the parallel formulation of the single-source algorithm to solve the problem on each set of processes. We refer to this approach as the ***source-parallel formulation***.
C. Both are true
D. Non of these is true

Answer : C

Search algorithms can be used to solve discrete optimization problems. True or False ?

A. True
B. False

Answer : A

Examples of Discrete optimization problems are ;

A. planning and scheduling,
B. The optimal layout of VLSI chips,
C. Robot motion planning,
D. Test-pattern generation for digital circuits, and logistics and control.
E. All of above

Answer : E

List the important parameters of Parallel DFS

A. Work- Splitting Strategies

B. Load balancing Schemes

C. All of above

Answer : C

List the communication strategies for parallel BFS.

A. Random communication strategy

B. Ring communication strategy

C. Blackboard communication strategy

D. All of above

Answer : D

The lower bound on any comparison-based sort of *n* numbers is $\Theta(n \log n)$

A. True
B. False

Answer : A

In a compare-split operation

A. Each process sends its block of size n/p to the other process
B. Each process merges the received block with its own block and retains only the appropriate half of the merged block
C. Both A & B

Answer : C

In a typical sorting network

A. Every sorting network is made up of a series of columns
B. Each column contains a number of comparators connected in parallel
C. Both A & B

Answer : C

Bubble sort is difficult to parallelize since the algorithm has no concurrency

A. True
B. False

Answer : A

Which of the following statements are true with regard to compute capability in CUDA

A. Code compiled for hardware of one compute capability will not need to be re-compiled to run on hardware of another

B. Different compute capabilities may imply a different amount of local memory per thread

C. Compute capability is measured by the number of FLOPS a GPU accelerator can compute.

Answer : B

True or False: The threads in a thread block are distributed across SM units so that each thread is executed by one SM unit.

A. True

B. False

Answer : B

The style of parallelism supported on GPUs is best described as

A. SISD - Single Instruction Single Data

B. MISD - Multiple Instruction Single Data

C. SIMT - Single Instruction Multiple Thread

Answer : C

True or false: Functions annotated with the __global__ qualifier may be executed on the host or the device

A. True

B. Flase

Answer : A

Which of the following correctly describes a GPU kernel

A. A kernel may contain a mix of host and GPU code

B. All thread blocks involved in the same computation use the same kernel

C. A kernel is part of the GPU's internal micro-operating system, allowing it to act as in independent host

Answer : B

Which of the following is *not* a form of parallelism supported by CUDA

A. Vector parallelism - Floating point computations are executed in parallel on wide vector units

B. Thread level task parallelism - Different threads execute a different tasks

C. Block and grid level parallelism - Different blocks or grids execute different tasks

D. Data parallelism - Different threads and blocks process different parts of data in memory

Answer :A

What strategy does the GPU employ if the threads within a warp diverge in their execution?

A. Threads are moved to different warps so that divergence does not occur within a single warp

B. Threads are allowed to diverge

C. All possible execution paths are run by all threads in a warp serially so that thread instructions do not diverge

Answer : C

Which of the following does *not* result in uncoalesced (i.e. serialized) memory access on the K20 GPUs installed on Stampede

A. Aligned, but non-sequential access

B. Misaligned data access

C. Sparse memory access

Answer : A

Which of the following correctly describes the relationship between Warps, thread blocks, and CUDA cores?

A. A warp is divided into a number of thread blocks, and each thread block executes on a single CUDA core

B. A thread block may be divided into a number of warps, and each warp may execute on a single CUDA core

C. A thread block is assigned to a warp, and each thread in the warp is executed on a separate CUDA core

Answer : B

Shared memory in CUDA is accessible to:

A. All threads in a single block

B. Both the host and GPU

C. All threads associated with a single kernel

Answer : A

CUDA Architecture CPU consist of

A. CUDA Libraries

B. CUDA Runtime

C. CUDA Driver

D. All Above

Answer : D

CUDA platform works on

A. C

B. C++

C. Forton

D. All Above

Answer : D

Threads support Shared memory and Synchronization

A. True

B. False

Answer : A

Application of CUDA are

A. Fast Video Transcoding

B. Medical Imaging

C. Computational Science

D. Oil and Natural Resources exploration

E. All Above

Answer : E

GPU execute device code

A. True

B. False

Answer : A

SET 1 (120 MCQs)

---

1. Conventional architectures coarsely comprise of a_

   A. A processor
   B. Memory system
   C Data path.
   D All of Above

2. Data intensive applications utilize_

   A **High aggregate throughput**
   B High aggregate network bandwidth
   C High processing and memory system performance.
   D None of above

3. A pipeline is like_

   A Overlaps various stages of instruction execution to achieve performance.
   B House pipeline
   C Both a and b
   D A gas line

4. Scheduling of instructions is determined_

   A True Data Dependency
   B Resource Dependency
   C Branch Dependency
   D All of above

5. VLIW processors rely on_

   A **Compile time analysis**
   B Initial time analysis
   C Final time analysis
   D Mid time analysis

6. Memory system performance is largely captured by_

   A Latency
   B Bandwidth
   C Both a and b
   D none of above

7. The fraction of data references satisfied by the cache is called_

A Cache *hit ratio*
B Cache *fit ratio*
B Cache *best ratio*
C none of above

8. A single control unit that dispatches the same Instruction to various processors is__

A SIMD
B SPMD
C MIMD
D None of above

9. The primary forms of data exchange between parallel tasks are_

A Accessing a shared data space
B Exchanging messages.
C Both A and B
D None of Above

10. Switches map a fixed number of inputs to outputs.
A True
B False

11. The First step in developing a parallel algorithm is_

A. To Decompose the problem into tasks that can be executed concurrently
B. Execute directly
C. Execute indirectly
D. None of Above

12. The number of tasks into which a problem is decomposed determines its_

A. Granularity
B. Priority
C. Modernity
D. None of above

13. The length of the longest path in a task dependency graph is called_
A. the critical path length
B. the critical data length
C. the critical bit length
D. None of above
E.

14. The graph of tasks (nodes) and their interactions/data exchange (edges)_
A. Is referred to as a *task interaction graph*

B. Is referred to as a *task Communication graph*
C. Is referred to as a *task interface graph*
D. None of Above

15. Mappings are determined by_

A. task dependency
B. task interaction graphs
C. Both A and B
D. None of Above

16. Decomposition Techniques are_
A. recursive decomposition
B. data decomposition
C. exploratory decomposition
D. speculative decomposition
E. All of Above

17. The *Owner Computes Rule* generally states that the process assigned a particular data item is responsible for_

A. All computation associated with it
B. Only one computation
C. Only two computation
D. Only occasionally computation

18. A simple application of exploratory decomposition is_

A. The solution to a 15 puzzle
B. The solution to 20 puzzle
C. The solution to any puzzle
D. None of Above

19. Speculative Decomposition consist of _
A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B

20. task characteristics include:
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.
D. All of Above

21. Group communication operations are built using point-to-point messaging primitives
    A. True
    B. False

22. Communicating a message of size m over an uncongested network takes time ts + tmw

    A. True
    B. False

23. The dual of one-to-all broadcast is_

    A. *All-to-one reduction*
    B. *All-to-one receiver*
    C. *All-to-one Sum*
    D. *None of Above*

24. A hypercube has_

    A. 2^d nodes
    B. 2d nodes
    C. 2n Nodes
    D. N Nodes

25. A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes.

    A. True
    B. False

26. In All-to-All Broadcast each processor is the source as well as destination.

    A. True
    B. False

27. The Prefix Sum Operation can be implemented using the_

    A. All-to-all broadcast kernel.
    B. All-to-one broadcast kernel.
    C. One-to-all broadcast Kernel
    D. Scatter Kernel

28. In the *scatter* operation_

    A. Single node send a unique message of size m to every other node
    B. Single node send a same message of size m to every other node
    C. Single node send a unique message of size m to next node

D. None of Above

29. The gather operation is exactly the inverse of the_

A. Scatter operation
B. Broadcast operation
C. Prefix Sum
D. Reduction operation

30. In All-to-All Personalized Communication Each node has a distinct message of size m for every other node

A. True
B. False

31. Computer system of a parallel computer is capable of

A. Decentralized computing
B. Parallel computing
C. Centralized computing
D. Decentralized computing
E. Distributed computing
F. All of these
G. None of these

32. Writing parallel programs is referred to as

A. Parallel computation
B. Parallel processes
C. Parallel development
D. Parallel programming
E. Parallel computation
F. All of these
G. None of these

33. Simplifies applications of three-tier architecture is _____.
A. Maintenance
B. Initiation
C. Implementation
D. Deployment
E. All of these
F. None of these

34. Dynamic networks of networks, is a dynamic connection that grows is called

A. Multithreading
B. Cyber cycle
C. Internet of things
D. Cyber-physical system
E. All of these
F. None of these

35. In which application system Distributed systems can run well?

A. HPC
D. HTC
C. HRC
D. Both A and B
E. All of these
F. None of these

36. In which systems desire HPC and HTC.

A. Adaptivity
B. Transparency
C. Dependency
D. Secretive
E. Adaptivity
F. All of these
G. None of these

37. No special machines manage the network of architecture in which resources are known as

A. Peer-to-Peer
B. Space based
C. Tightly coupled
D. Loosely coupled
E. All of these
F. None of these

38. Significant characteristics of Distributed systems have of
A. 5 types
B. 2 types
C. 3 types
D. 4 types
E. All of these
F. None of these

39. Built of Peer machines are over

A. Many Server machines
B. 1 Server machine
C. 1 Client machine
D. Many Client machines
E. All of these
F. None of these

40. Type HTC applications are

A. Business
B. Engineering
C. Science
D. Media mass
E. All of these
F. None of these

41. Virtualization that creates one single address space architecture that of, is called

A. Loosely coupled
B. Peer-to-Peer
C. Space-based
D. Tightly coupled
E. Loosely coupled
F. All of these
G. None of these

42. We have an internet cloud of resources In cloud computing to form

A. Centralized computing
B. Decentralized computing
C. Parallel computing
D. Both A and B
E. All of these
F. None of these

43. Data access and storage are elements of Job throughput, of _____.

A. Flexibility
B. Adaptation
C. Efficiency
D. Dependability
E. All of these
F. None of these

44. Billions of job requests is over massive data sets, ability to support known as

A. Efficiency
B. Dependability
C. Adaptation
D. Flexibility
E. All of these
F. None of these

45. Broader concept offers Cloud computing .to select which of the following.

A. Parallel computing
B. Centralized computing
C. Utility computing
D. Decentralized computing
E. Parallel computing
F. All of these
G. None of these

46. Resources and clients transparency that allows movement within a system is called

A. Mobility transparency
B. Concurrency transparency
C. Performance transparency
D. Replication transparency
E. All of these
F. None of these

47. Distributed program in a distributed computer running a is known as

A. Distributed process
B. Distributed program
C. Distributed application
D. Distributed computing
E. All of these
F. None of these

48. Uniprocessor computing devices is called_____.

A. Grid computing
B. Centralized computing
C. Parallel computing
D. Distributed computing
E. All of these
F. None of these

49. Utility computing focuses on a_____ model.

A. Data
B. Cloud
C. Scalable
D. Business
E. All of these
F. None of these

50.|What is a CPS merges technologies

A. 5C
B. 2C
C. 3C
D. 4C
E. All of these
F. None of these

51. Aberration of HPC

A. High-peak computing
B. High-peripheral computing
C. High-performance computing
D. Highly-parallel computing
E. All of these
F. None of these

52. Peer-to-Peer leads to the development of technologies like

A. Norming grids
B. Data grids
C. Computational grids
D. Both A and B
E. All of these
F. None of these

53. Type of HPC applications of.

A. Management
B. Media mass
C. Business
D. Science
E. All of these
F. None of these

54. The development generations of Computer technology has gone through

A. 6

B. 3
C. 4
D. 5
E. All of these
F. None of these

55. Utilization rate of resources in an execution model is known to be its

A. Adaptation
B. Efficiency
C. Dependability
D. Flexibility
E. All of these
F. None of these

56. Even under failure conditions Providing Quality of Service (QoS) assurance is the responsibility of

A. Dependability
B. Adaptation
C. Flexibility
D. Efficiency
E. All of these
F. None of these

57. Interprocessor communication that takes place
A. Centralized memory
B. Shared memory
C. Message passing
D. Both A and B
E. All of these
F. None of these

58. Data centers and centralized computing covers many and
A. Microcomputers
B. Minicomputers
C. Mainframe computers
D. Supercomputers
E. All of these
F. None of these

59. Which of the following is an primary goal of HTC paradigm_____.
A. High ratio Identification
B. Low-flux computing
C. High-flux computing
D. Computer utilities

E. All of these
F. None of these

60. The high-throughput service provided is measures taken by
A. Flexibility
B. Efficiency
D. Adaptation
E. Dependability
F. All of these
G. None of these

61. What are the sources of overhead?
A. Essential /Excess Computation
B. Inter-process Communication
C. Idling
D. All above

62. Which are the performance metrics for parallel systems?
A. Execution Time
B. Total Parallel Overhead
C. Speedup
D. Efficiency
E. Cost
F. All above

63. The efficiency of a parallel program can be written as: ***E = Ts / pTp.*** True or False?
A. True
B. False

64. Overhead function or ***total overhead*** of a parallel system as the total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element. True or False?
A. True
B. False

65. What is Speedup?
A. A measure that captures the relative benefit of solving a problem in parallel. It is defined as the ratio of the time taken to solve a problem on a single processing element to the time required to solve the same problem on a parallel computer with *p* identical processing elements.
B. A measure of the fraction of time for which a processing element is usefully employed.
C. None of the above
Answer : A

66. In an ideal parallel system, speedup is equal to *p* and efficiency is equal to one. True or False?

A. True

B. False

67. A parallel system is said to be _____ if the cost of solving a problem on a parallel computer has the same asymptotic growth (in Q terms) as a function of the input size as the fastest-known sequential algorithm on a single processing element.

A. Cost optimal

B. Non Cost optimal

68. Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called _____ a parallel system in terms of the number of processing elements.

A. Scaling down

B. Scaling up

69. The _____ function determines the ease with which a parallel system can maintain a constant efficiency and hence achieve speedups increasing in proportion to the number of processing elements.

A. Isoefficiency

B. Efficiency

C. Scalability

D. Total overhead

70. Minimum execution time for adding n numbers is $Tp = n/p + 2 \log p$ True or False ?

A. True

B. False

71. The overhead function To = pTP − TS.

A. True

B. False

72. Performance Metrics for Parallel Systems: Speedup(S) =TS/TP

A. True

B. False

73. Matrix Vector multiplication 2D Partitions requires some basic communication operations

A. one-to-one communication to align the vector along the main diagonal

B. one-to-all broadcast of each vector element among the n processes of each column

C. all-to-one reduction in each row

D. All Above

74. What are the issues in sorting?
A. Where the Input and Output Sequences are Stored
B. How Comparisons are Performed
C. All above
Answer : C

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C. CUDA Driver
D. **All Above**

95. CUDA platform works on
A. C
B. C++
C. Forton
D. **All Above**

96. Threads support Shared memory and Synchronization
A. **True**
B. False

97. Application of CUDA is
A. Fast Video Transcoding
B. Medical Imaging
C. Computational Science
D. Oil and Natural Resources exploration
E. **All Above**

98. GPU execute device code
A. **True**
B. False

99. Hazard are eliminated through renaming by renaming all

A. Source register
B. Memory
C. Data
D. **Destination register**

100. Types of HPC application

A. Mass Media
B. Business
C. Management
D. Science

101. A distributed operating system must provide a mechanism for

A. intraprocessor communication
B. intraprocess and intraprocessor communication
C. interprocess and interprocessor communication
D. interprocessor communication

102. This is computation not performed by the serial version

A. Serial computation
B. Excess computation
C. perpendicular computation
D. parallel computing

103. The important feature of the VLIW is _____

A. ILP
B. Performance
C. Cost effectiveness
D. delay

104. The tightly coupled set of threads execution working on a single task ,that is called

A. Multithreading
B. Parallel processing
C. Recurrence
D. Serial processing

105. Parallel Algorithm Models

A. Data parallel model

B. Bit model
C. Data model
D. Network model

106. Mpi_Recv used for

A. reverse message
B. receive message
C. forward message
D. Collect message

107. Status bit is also called

A. Binary bit
B. Flag bit
C. Signed bit
D. Unsigned bit

108. For inter processor communication the miss arises are called

A. hit rate
B. coherence misses
C. comitt misses
D. parallel processing

109. The interconnection topologies are implemented using _____ as a node.

A. control unit
B. **microprocessor**
C. processing unit
D. microprocessor or processing unit

110. _____ gives the theoretical speedup in latency of the execution of a task at fixed execution time

A. Amdahl's

B. Moor's
C. metcalfe's
D. Gustafson's law

111. The number and size of tasks into which a problem is decomposed determines the

A. fine-grainularity
B. coarse-grainularity
C. sub Task
D. granularity

112. MPI_Finalize used for

A. Stop mpi environment program
B. intitalise program
C. Include header files
D. program start

113. Private data that is used by a single processor then shared data are used

A. Single processor
B. Multi processor
C. Single tasking
D. Multi tasking

114. The time lost due to the branch instruction is often referred to as _____

A. Delay
B. Branch penalty
C. Latency
D. control hazard

115. NUMA architecture uses _____in design

A. cache
B. shared memory

C. message passing
D. distributed memory

116. Divide and Conqure apporach is known for

A. Sequentional algorithm development
B. parallel algorithm develpoment
C. Task defined algorithm
D. Non defined Algorithm

117. The parallelism across branches require which scheduling

A. Global scheduling
B. Local Scheduling
C. post scheduling
D. pre scheduling

118. Parallel processing may occur

A. In the data stream
B. In instruction stream
C. In network
D. In transferring

119. Pipe-lining is a unique feature of _____.

A. CISC
B. RISC
C. ISA
D. IANA

120. In MPI programing MPI_char is the instruction for

A. Unsign Char
B. Sign character
C. Long Char
D. unsign long char

SET 2 (26 MCQs)

---

1. What is Cuda Architecture?
a.CUDA Architecture included a unified shader pipeline, allowing each and every chip to be marshaled by a program.
b.CUDA Architecture included a unified shader pipeline, allowing each and every unit on the chip to be marshaled by a program intending to perform general-purpose computations
c.CUDA Architecture included a unified shader pipeline, allowing each and every logic unit on the chip to be marshaled by a program intending to perform general-purpose computations
d.CUDA Architecture included a unified shader pipeline, allowing each and every arithmetic logic unit (ALU) on the chip to be marshaled by a program intending to perform general-purpose computations
Ans.D

2. For the following code write a kernel

```
__global__ void kernel( void ) { }
int main( void ) {
// Write a kernel here
printf( "Hello, World!\n" ); return 0; }
```

a.kernel<1, 1>(1,1);
b.kernel<<<1, 1>>>(1,1);
c.kernel<<<1, 1>>>();
d.kernel<<1, 1>>();
Ans. c

3. Find out which is the kernel from following code:

```
#include <iostream>
__global__ void add( int a, int b, int *c ) {
*c = a + b;
}
int main( void ) {
int c; int *dev_c;
HANDLE_ERROR( cudaMalloc( (void**)&dev_c, sizeof(int) ) );
add<<<1,1>>>( 2, 7, dev_c );
HANDLE_ERROR( cudaMemcpy( &c, dev_c, sizeof(int), cudaMemcpyDeviceToHost ) );
printf( "2 + 7 = %d\n", c );
cudaFree( dev_c );
return 0;
}
```

a.cudaMalloc((void**)&dev_c, sizeof(int))
b.add<<<1,1>>>(2, 7, dev_c)
c.add<<1,1>>(2, 7, dev_c);
d.add<<<1,1>>>()

Ans.b

4. From following code which particular line is responsible for copying between device to host

```
#include <iostream>
__global__ void add( int a, int b, int *c ) {
*c = a + b;
}
int main( void ) {
int c; int *dev_c;
HANDLE_ERROR( cudaMalloc( (void**)&dev_c, sizeof(int) ) );
add<<<1,1>>>( 2, 7, dev_c );
HANDLE_ERROR( cudaMemcpy( &c, dev_c, sizeof(int), cudaMemcpyDeviceToHost ) );
printf( "2 + 7 = %d\n", c );
cudaFree( dev_c );
return 0;
}
```

a. c, dev_c, sizeof(int);
b. HANDLE_ERROR(&c, dev_c, sizeof(int), cudaMemcpyDeviceToHost);
c. HANDLE_ERROR(cudaMemcpy(&c, dev_c, sizeof(int), cudaMemcpyDeviceToHost));
d. cudaMemcpy(&c, dev_c, sizeof(int), cudaMemcpyDeviceToHost) ;

Ans.c

5. What is output of the following code:

```
#include <iostream>
__global__ void add( int a, int b, int *c ) {
*c = a + b;
}
int main( void ) {
int c; int *dev_c;
HANDLE_ERROR( cudaMalloc( (void**)&dev_c, sizeof(int) ) );
add<<<1,1>>>( 2, 7, dev_c );
HANDLE_ERROR( cudaMemcpy( &c, dev_c, sizeof(int), cudaMemcpyDeviceToHost ) );
printf( "2 + 7 = %d\n", c );
cudaFree( dev_c );
return 0;
}
```

a.2
b.9
c.7
d.0

Ans. b

6.what is function of e __global__ qualifier in cuda program
a. alerts the compiler that a function should be compiled to run on a device instead of the host

b. alerts the interpreter that a function should be compiled to run on a device instead of the host
c. alerts the interpreter that a function should be interpreted to run on a device instead of the host
d. alerts the interpreter that a function should be compiled to run on a host instead of the device
ans.a

7. The on-chip memory which is local to every multithreaded Single Instruction Multiple Data (SIMD) Processor is called
a. Local Memory
b. Global Memory
c. Flash memory
d. Stack
Ans. a

8. The machine object created by the hardware, managing, scheduling, and executing is a thread of
a. DIMS instructions
b. DMM instructions
c. SIMD instructions
d. SIM instructions
Ans. c

9. The primary and essential mechanism to support the sparse matrices is
a. Gather-scatter operations
b. Gather operations
c. Scatter operations
d. Gather-scatter technique
Ans. a

10. Which of the following architectures is/are not suitable for realizing SIMD ?
a. Vector Processor
b. Array Processor
c. Von Neumann
d. All of the above
Ans . c

11. Multithreading allowing multiple-threads for sharing the functional units of a
a.Multiple processor
b.Single processor
c.Dual core
d. Corei5
Ans . b

12. Which compiler is used to compile the cude source code:
a.gcc
b.nvc++
c.nc++

d.nvcc
Ans.d

13. which command line is used to execute a cuda program :
a.nvcc hello.cu -o hello
b.nvg++ heloo.cpp -o hello
c.ncc hello.c -o hello
D.g++ hello.cu -o hello
Ans.a

14.The syntax of kernel execution configuration is as follows
a.<<< M , T >>> with a grid of M thread blocks. Each thread block has T parallel blocks
b.<<< M , T >>> with a grid of M blocks. Each thread block has T parallel threads
c.<<< M , T >>> with a grid of M thread blocks. Each thread block has T parallel threads
d.<<< M , T >>> with a grid of M thread blocks. Each thread block has T threads
Ans. c

15.what it contains threadIdx.x
A.contains the index of the thread within the block
b.contains the index of the block within the thread
c.contains the index of the thread size within the block
d.contains the index of the block size within the thread
Ans. A

16.what it contains blockDim.x
a.contains the size of block
b.contains the size of block thread
c.contains the size of thread block (number of threads in the thread block).
d.the size of thread block
Ans. c

17.memory allocation of of variable x and y in cuda:
A.float *b, *a;
cudaMallocManaged(&, N*sizeof(float));
cudaMallocManaged(&, N*sizeof(float));
B.float *x, *y;
cudaMallocManaged(&a, N*sizeof(float));
cudaMallocManaged(&b, N*sizeof(float));
c.float *a, *b;
cudaMallocManaged(&x, N*sizeof(float));
cudaMallocManaged(&y, N*sizeof(float));
d.float *x, *y;
cudaMallocManaged(&x, N*sizeof(float));
cudaMallocManaged(&y, N*sizeof(float));
Ans. D

18.which function is used for free the memory in cuda
a.cudaFree()
b.Free()
c.Cudafree()
d.CudaFree()
Ans. a

19. Which of the following is *not* a form of parallelism supported by CUDA
a.Vector parallelism - Floating point computations are executed in parallel on wide vector units
b.Thread level task parallelism - Different threads execute a different tasks
c.Block and grid level parallelism - Different blocks or grids execute different tasks
d.Data parallelism - Different threads and blocks process different parts of data in memory
Ans . a

20.The style of parallelism supported on GPUs is best described as
a.SISD - Single Instruction Single Data
b.MISD - Multiple Instruction Single Data
c.SIMT - Single Instruction Multiple Thread
d.MIMD - Multiple Instruction Multiple Data
Ans. c

21. Which of the following correctly describes a GPU kernel
a.A kernel may contain a mix of host and GPU code
b.All thread blocks involved in the same computation use the same kernel
c.A kernel is part of the GPU's internal micro-operating system, allowing it to act as in independent host
d.All thread blocks involved in the same computation use the different kernel
Ans .b

22.Shared memory in CUDA is accessible to:
a.All threads in a single block
b.Both the host and GPU
c.All threads associated with a single kernel
d.one thread in a single block
Ans.a

23.Which of the following correctly describes the relationship between Warps, thread blocks, and CUDA cores?
a.A warp is divided into a number of thread blocks, and each thread block executes on a single CUDA core
b.A thread block may be divided into a number of warps, and each warp may execute on a single CUDA core
c.A thread block is assigned to a warp, and each thread in the warp is executed on a separate CUDA core
d. A block index is same as thread index
Ans .b

24. A processor assigned with a thread block, that executes a code ,which we usually call a
A. multithreaded MIMD processor
b. multithreaded SIMD processor
c. multithreaded
D. multicore
Ans. c

25. Thread blocked altogether and being executed in the sets of 32 thread called as
a.block of thread
b.thread block
c.thread
d.block
Ans. b

26.Who developed CUDA :
a. ARM
b. INTEL
c. AMD
d. NVIDIA
Ans. d

SET 3 (30 MCQs)

Unit I

1. Conventional architectures coarsely comprise of a_

A. A processor
B. Memory system
C Data path.
D All of Above
2. Data intensive applications utilize_

A **High aggregate throughput**
B High aggregate network bandwidth
C High processing and memory system performance.
D None of above
3. A pipeline is like_

A Overlaps various stages of instruction execution to achieve performance.
B House pipeline
C Both a and b
D A gas line

4. Scheduling of instructions is determined_

A True Data Dependency
B Resource Dependency
C Branch Dependency
D All of above
5. VLIW processors rely on_

A Compile time analysis
B Initial time analysis
C Final time analysis
D Mid time analysis
6. Memory system performance is largely captured by_

A Latency
B Bandwidth
C Both a and b
D none of above

7. The fraction of data references satisfied by the cache is called_
A Cache *hit ratio*
B Cache *fit ratio*
B Cache *best ratio*
C none of above
8. A single control unit that dispatches the same Instruction to various processors is__

A SIMD
B SPMD
C MIMD
D None of above
9. The primary forms of data exchange between parallel tasks are_

A Accessing a shared data space
B Exchanging messages.
C Both A and B
D None of Above

10. Switches map a fixed number of inputs to outputs.
A True
B False

Unit 2

1. The First step in developing a parallel algorithm is_

A. To Decompose the problem into tasks that can be executed concurrently

B. Execute directly
C. Execute indirectly
D. None of Above

2. The number of tasks into which a problem is decomposed determines its_

A. Granularity
B. Priority
C. Modernity
D. None of above

3. The length of the longest path in a task dependency graph is called_
A. the critical path length
B. the critical data length
C. the critical bit length
D. None of above

4. The graph of tasks (nodes) and their interactions/data exchange (edges)_

A. Is referred to as a *task interaction graph*
B. Is referred to as a *task Communication graph*
C. Is referred to as a *task interface graph*
D. None of Above

5. Mappings are determined by_

A. task dependency
B. task interaction graphs
C. Both A and B
D. None of Above

6. Decomposition Techniques are_
A. recursive decomposition
B. data decomposition
C. exploratory decomposition
D. speculative decomposition
E. All of Above

7. The *Owner Computes Rule* generally states that the process assigned a particular data item is responsible for_

A. All computation associated with it
B. Only one computation
C. Only two computation
D. Only occasionally computation

8. A simple application of exploratory decomposition is_

A. The solution to a 15 puzzle
B. The solution to 20 puzzle
C. The solution to any puzzle
D. None of Above

9. Speculative Decomposition consist of _

A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B

10. task characteristics include:
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.

D. All of Above

Unit 3

1. Group communication operations are built using point-to-point messaging primitives
A. True
B. False

2. Communicating a message of size m over an uncongested network takes time ts + tmw

A. True
B. False

3. The dual of one-to-all broadcast is_

A. *All-to-one reduction*
B. All-to-one receiver
C. All-to-one Sum
D. None of Above

4. A hypercube has_

A. 2d nodes
B. 2d nodes
C. 2n Nodes
D. N Nodes

5. A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes.

A. True
B. False

6. In All-to-All Broadcast each processor is the source as well as destination.

A. True
B. False

7. The Prefix Sum Operation can be implemented using the_

A. All-to-all broadcast kernel.
B. All-to-one broadcast kernel.
C. One-to-all broadcast Kernel
D. Scatter Kernel

8. In the *scatter* operation_

A. Single node send a unique message of size m to every other node
B. Single node send a same message of size m to every other node
C. Single node send a unique message of size m to next node
D. None of Above

9. The gather operation is exactly the inverse of the_

A. Scatter operation
B. Broadcast operation
C. Prefix Sum
D. Reduction operation

10. In All-to-All Personalized Communication Each node has a distinct message of size m for every other node

A. True
B. False

SET 4 (MCQs)

1.Message passing system allows processes to : a) communicate with one another without resorting to shared data b) communicate with one another by resorting to shared data c) share data d) name the recipient or sender of the message
Ans-a

2. An IPC facility provides at least two operations : a) write & delete message b) delete & receive message c) send & delete message d) receive & send message
Ans- d

3.Messages sent by a process : a) have to be of a fixed size b) have to be a variable size c) can be fixed or variable sized d) None of the mentioned
Ans- c

4.The link between two processes P and Q to send and receive messages is called : a) communication link b) message-passing link c) synchronization link d) all of the mentioned
Ans- a

5.In the Zero capacity queue : a) the queue can store at least one messageb) the sender blocks until the receiver receives the message c) the sender keeps sending and the messages don't wait in the queue d) none of the mentioned
Ans- b

6.Inter process communication :

a) allows processes to communicate and synchronize their actions when using the same address space.
b) allows processes to communicate and synchronize their actions without using the same address space.
c) allows the processes to only synchronize their actions without communication.
d) None of these
Ans- b

7.In the non blocking send :
a) the sending process keeps sending until the message is received b) the sending process sends the message and resumes operation
c) the sending process keeps sending until it receives a message
d) None of these
Ans- b

8.In indirect communication between processes P and Q :
a) there is another process R to handle and pass on the messages between P and Q
b) there is another machine between the two processes to help communication
c) there is a mailbox to help communication between P and Q
d) None of these
Ans- c

9. In SIMD, elements of short vectors are processed in _____a
a) parallel
b) one by one
c)first come first serve basisd) on priority basis
Ans- b

10.Which one of the following the correct sequence
a) SIMD < SIMT < SMT
b) SIMD > SIMT > SMT
c) SIMD < SIMT > SMT
d) SIMD > SIMT < SMT
Ans- a

11.Single instruction is applied to a multiple data item to produce the ___ output(s).
a)multiple
b)different
c)same
Ans- c

12. Which of the following is NOT a characteristic of parallel computing?
a) Breaks a task into pieces
b) Uses a single processor or computer
c) Simultaneous execution
d) May use networking

Ans- b

13. Parallel computing uses _____ execution.
a) sequential
b) uniquec) simultaneous
d) none of the answers is correct.
Ans- c

14) A collection of lines that connects several devices is called .....
A. bus
B. peripheral connection wires
C. Both a and b
D. internal wires
Answer: A. bus

15) A complete microcomputer system consist of .....
A. microprocessor
B. memory
C. peripheral equipment
D. all of the above
Answer: D. all of the above

16) PC Program Counter is also called .....
A. instruction pointer
B. memory pointer
C. data counter
D. file pointer
Answer: A. instruction pointer

17) Data hazards occur when .....
A. Greater performance loss
B. Pipeline changes the order of read/write access to operands
C. Some functional unit is not fully pipelined
D. Machine size is limited
Answer: B. Pipeline changes the order of read/write access to operands

18) Which of the following bus is used to transfer data from main memory to peripheral device?
A. DMA bus
B. Output bus
C. Data bus
D.All of the above
Answer: C. Data bus

19) Micro instructions are stored in
A. computer memory
B. primary storage

C. secondary storage
D. control memory
E. cache memory
Answer: D. control memory

20. Pipeline processing implement
A. fetch instruction
B. decode instruction
C. fetch operand
D. calculate operand
E. execute instruction
F. all of the above
Answer: F. all of the above

21) Instruction pipelining has minimum stages
A. 4
B. 2
C. 3
D. 6
Answer: B. 2

22). Systems that do not have parallel processing capabilities are
A. SISD
B. SIMD
C. MIMD
D. All of the above
Answer: A. SISD

23) Who is regarded as the founder of Computer Architecture?
A. Alan TuringB. Konrad Zuse
C. John von Neumann
D. John William Mauchly
E. None of the answers above is correct
Answer: C. John von Neumann

24). What is characteristic for the organization of a computer architecture?
A. Size

B. Dynamic behaviour
C. Static behaviour
D. Speed
E. None of the answers above is correct
Answer: B. Dynamic behaviour

25). What is usually regarded as the von Neumann Bottleneck?
A. Processor/memory interface

B. Control unit
C. Arithmetic logical unitD. Instruction set
E. None of the answers above is correct
Answer: A. Processor/memory interface

26) How does the number of transistors per chip increase according to Moore ´s law?
A. Quadratically
B. Linearly
C. Cubicly
D. Exponentially
E. None of the answers above is correct
Answer: D. Exponentially

27) Which value has the speedup of a parallel program that achieves an efficiency of 75% on 32 processors?
A. 18
B. 24
C. 16
D. 20
E. None of the answers above is correct
Answer: B. 24

28). Pipelining strategy is called implement
A. instruction execution
B. instruction prefetch
C. instruction decoding
D. instruction manipulation
Answer: B. instruction prefetch

29). The concept of pipelining is most effective in improving performance if the tasks being performed in different stages :
A. require different amount of time
B. require about the same amount of time
C. require different amount of time with time difference between any two tasks being same
D. require different amount with time difference between any two tasks being different
Answer: B. require about the same amount of time

30) Which Algorithm is better choice for pipelining?
A. Small Algorithm
B. Hash Algorithm
C. Merge-Sort Algorithm
D. Quick-Sort Algorithm
Answer: C. Merge-Sort Algorithm

31) The expression 'delayed load' is used in context of
A. processor-printer communication

B. memory-monitor communication
C. pipelining
D. none of the above
Answer: C. pipelining

32) Parallel processing may occur
A. in the instruction stream
B. in the data stream
C. both[A] and [B]
D. none of the above
Answer: C. both[A] and [B]

33) The cost of a parallel processing is primarily determined by :
A. Time Complexity
B. Switching Complexity
C. Circuit Complexity
D. None of the above
Answer: C. Circuit Complexity

34) An instruction to provide small delay in program
A. LDA
B. NOP
C. BEA
D. None of the above
Answer: B. NOP

35)Characteristic of RISC (Reduced Instruction Set Computer) instruction set is
A. three instructions per cycle
B. two instructions per cycle
C. one instruction per cycle
D. none of the
Answer: C. one instruction per cycle

36) In daisy-chaining priority method, all the devices that can request an interrupt are connected in
A. parallel
B. serial
C. random
D. none of the above
Answer: B. serial

37) Which one of the following is a characteristic of CISC (Complex Instruction Set Computer)
A. Fixed format instructions
B. Variable format instructions
C. Instructions are executed by hardware
D. None of the above

Answer: B. Variable format instructions

38). During the execution of the instructions, a copy of the instructions is placed in the _____ .
A. Register
B. RAM
C. System heap
D. Cache
Answer: D. Cache

39) Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster ?
A. A
B. B
C. Both take the same time
D. Insuffient information
Answer: A. A
40)A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ .
A. Super-scaling
B. Pipe-lining
C. Parallel Computation
D. None of these
Answer: B. Pipe-lining

41) For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution ?
A. ISA
B. ANSA
C. Super-scalar
D. All of the above
Answer: C. Super-scalar

42)The clock rate of the processor can be improved by,
A. Improving the IC technology of the logic circuits
B. Reducing the amount of processing done in one step
C. By using overclocking method
D. All of the above
Answer: D. All of the above

43)An optimizing Compiler does,
A. Better compilation of the given piece of code.
B. Takes advantage of the type of processor and reduces its process time.
C. Does better memory managament.
D. Both a and c
Answer: B. Takes advantage of the type of processor and reduces its process time.

44)The ultimate goal of a compiler is to,
A. Reduce the clock cycles for a programming task.
B. Reduce the size of the object code.
C. Be versatile.
D. Be able to detect even the smallest of errors.
Answer: A. Reduce the clock cycles for a programming task.

45)To which class of systems does the von Neumann computer belong?
A. SIMD (Single Instruction Multiple Data)
B. MIMD (Multiple Instruction Multiple Data)
C. MISD (Multiple Instruction Single Data)
D. SISD (Single Instruction Single Data)
E. None of the answers above is correct.
Answer: D. SISD (Single Instruction Single Data)

46). Parallel programs: Which speedup could be achieved according to Amdahl´s law for infinite number of processors if 5% of a program is sequential and the remaining part is ideally parallel?
A. Infinite speedup
B. 5
C. 20
D. 50
E. None of the answers above is correct.
Answer: C. 20

47). Itanium processor: Which hazard can be circumvented by register rotation?
A. Control hazards
B. Data hazards
C. Structural hazards
D. None
E. None of the answers above is correct.
Answer: B. Data hazards

48 Which MIMD systems are best scalable with respect to the number of processors?
A. Distributed memory computers
B. ccNUMA systems
C. nccNUMA systems
D. Symmetric multiprocessors
E. None of the answers above is correct
Answer: A. Distributed memory computers

49). Cache coherence: For which shared (virtual) memory systems is the snooping protocol suited?
A. Crossbar connected systems
B. Systems with hypercube network
C. Systems with butterfly network

D. Bus based systems
E. None of the answers above is correct.
Answer: D. Bus based systems

50)Parallel processing may occur
A. in the instruction stream
B. in the data stream
C. both[A] and [B]
D. none of the above
Answer: C. both[A] and [B]

51). The cost of a parallel processing is primarily determined by :
A. Time Complexity
B. Switching Complexity
C. Circuit Complexity
D. None of the above
Answer: C. Circuit Complexity

Unit 2

1. The best mode of connection between devices which need to send or receive large amounts of data over a short distance is _____
a) BUS
b) Serial port
c) Parallel port
d) Isochronous port
View Answer
Answer: c
Explanation: The parallel port transfers around 8 to 16 bits of data simultaneously over the lines, hence increasing transfer rates.

8. In the output interface of the parallel port, along with the valid signal _____ is also sent.
a) Data
b) Idle signal
c) Interrupt
d) Acknowledge signal
View Answer
Answer: b
Explanation: The idle signal is used to check if the device is idle and ready to receive data.
3. Parallel computing uses _____ execution.
a) sequential
b) unique
c) simultaneous
d) none of the above
ans c

4. Heap can be used as _____
a) Priority queue
b) Stack
c) A decreasing order array
d) None of the mentioned
Answer: a

Explanation: The property of heap that the value of root must be either greater or less than both of its children makes it work like a priority queue.
6. Which of the following is true about parallel computing performance?
a. Computations use multiple processors.
b. There is an increase in speed.
c. The increase in speed is loosely tied to the number of processor or computers used.
d. All of the answers are correct.
ANS: a

7.Which of the following is NOT a characteristic of parallel computing?
a.Breaks a task into pieces
b.Uses a single processor or computer
c.Simultaneous execution
d.May use networking
ans: b

8) Decentralized computing B. Parallel computing C. Centralized computing D. Decentralized computing E. Distributed computing F. All of these G. None of these
Answer- A

9) Writing parallel programs is referred to as
A. Parallel computation B. Parallel processes C. Parallel development D. Parallel programming E. Parallel computation F. All of these G. None of these
Answer- D

10) **In which application system Distributed systems can run well?**
A. HPC D. HTC C. HRC
D. Both A and B E. All of these F. None of these
Answer- D

11) **In which systems desire HPC and HTC.**
A. Adaptivity B. Transparency C. Dependency D. Secretive E. Adaptivity F. All of these G. None of these
Answer- B

12) **No special machines manage the network of architecture in which resources are known as**
A. Peer-to-Peer B. Space based C. Tightly coupled D. Loosely coupled E. All of these F. None of these

Answer- A

13) **Virtualization that creates one single address space architecture that of, is called**
A. Loosely coupled B. Peer-to-Peer C. Space-based D. Tightly coupled E. Loosely coupled F. All of these G. None of these
Answer- C

14) **Uniprocessor computing devices is called_____.**
A. Grid computing B. Centralized computing C. Parallel computing D. Distributed computing E. All of these F. None of these
Answer- B

15) **Utility computing focuses on a_____ model.**
A. Data B. Cloud C. Scalable D. Business E. All of these F. None of these
Answer- D

16) **Aberavationn of HPC**
A. High-peak computing B. High-peripheral computing
C. High-performance computing
D. Highly-parallel computing
E. All of these
F. None of these
Answer- C

17) **Peer-to-Peer leads to the development of technologies like**
A. Norming grids
B. Data grids
C. Computational grids
D. Both A and B
E. All of these
F. None of these
Answer- D

18) **Type of HPC applications of.**
A. Management B. Media mass C. Business D. Science E. All of these F.None of these
Answer- D

20) **Utilization rate of resources in an execution model is known to be its**
A. Adaptation B. Efficiency C. Dependability D. Flexibility E. All of these F. None of these
Answer- B

21) **Interprocessor communication that takes place**
A. Centralized memory B. Shared memory C. Message passing D. Both A and B E. All of these F. None of these
Answer- D

22) **Data centers and centralized computing covers many and**
A. Microcomputers B. Minicomputers C. Mainframe computers D. Supercomputers E. All of these F. None of these
Answer- D

23) Execution of several activities at the same time. a) processing b) parallel processing c) serial processing d) multitasking
Answer: b

24) Parallel processing has single execution flow. a) True b) False
Answer: b

25) A term for simultaneous access to a resource, physical or logical. a) Multiprogramming b) Multitasking c) Threads d) Concurrency
Answer: D

26) _____ leads to concurrency. a) Serialization b) Parallelism c) Serial processing d) Distribution
Answer: b

27) A parallelism based on increasing processor word size. a) Increasing b) Count based c) Bit based d) Bit leve
Answer: d

28) A type of parallelism that uses micro architectural techniques. a) instructional b) bit level c) bit based d) increasing
Answer: A
29) MIPS stands for? a) Mandatory Instructions/sec b) Millions of Instructions/sec c) Most of Instructions/sec d) Many Instructions / sec
Answer: B

30) Several instructions execution simultaneously in _____ a) processing b) parallel processing c) serial processing d) multitasking
Answer: B

31) Computer has a built-in system clock that emits millions of regularly spaced electric pulses per _____ called clock cycles. a) second b) millisecond c) microsecond d) minute
Answer: a

32) It takes one clock cycle to perform a basic operation. a) True b) False
Answer: a

33) The operation that does not involves clock cycles is _____ a) Installation of a device b) Execute c) Fetch d) Decode
Answer: a

34). The number of clock cycles per second is referred as _____ a) Clock speed b) Clock frequency c) Clock rate d) Clock timing
Answer: a

35). CISC stands for _____ a) Complex Information Sensed CPU b) Complex Instruction Set Computer c) Complex Intelligence Sensed CPU d) Complex Instruction Set CPU
Answer: b

36). Which of the following processor has a fixed length of instructions? a) CISC b) RISC c) EPIC d) Multi-core
Answer: b

37). Processor which is complex and expensive to produce is _____ a) RISC b) EPIC c) CISC d) Multi-core
Answer: c

38). The architecture that uses a tighter coupling between the compiler and the processor is _____ a) EPIC b) Multi-core c) RISC d) CISC
Answer: a

39). MAR stands for _____ a) Memory address register b) Main address register c) Main accessible register
d) Memory accessible register
Answer: a.

40). A circuitry that processes that responds to and processes the basic instructions that are required to drive a computer system is _____ a) Memory b) ALU c) CU d) Processor
Answer: d

41) The graph of tasks (nodes) and their interactions/data exchange (edges)_
A. Is referred to as a task interaction graph
B. Is referred to as a task Communication graph
C. Is referred to as a task interface graph
D. None of Above
Answer: A

42) task characteristics include:
A)Task generation.
B)Task sizes.
C)Size of data associated with tasks.
D) All of Above
Answer: D

43). Decomposition Techniques are_
A. recursive decomposition
B. data decomposition

C. exploratory decomposition
D. speculative decomposition
E. All of Above
Answer: E

44) The *Owner Computes Rule* generally states that the process assigned a particular data item is responsible for_
A. All computation associated with it
B. Only one computation
C. Only two computation
D. Only occasionally computation
Answer: A

Unit 3

1.Which topology requires a central controller or hub?
a.Mesh
b.Star
c.Bus
d.Ring
Ans:- b

2.Which topology requires a multipoint connection?
a.Mesh
b.Star
c.Bus
d.Ring
Ans:- c

3 Multipoint topology is
a.Bus
b.Star
c.Mesh
d.Ring
Ans:- a

4.In mesh topology, every device has a dedicated topology of
a.Multipoint linking
b.Point to point linking
c.None of Above
d.Both a and b
Ans:- a

5 .Bus, ring and star topologies mostly used in the
a.LAN
b.MAN

c.WAN
d.Internetwork
Ans:- a

6 Combination of two or more topologies are called
a.Star
b.Bus
c.Ring
d.Hybrid
Ans:- d

7 The topology with highest reliability is ?
a.Bus topology
b.Star topology
c.Ring Topology
d.Mesh Topology
Ans:- d

8 .Star Topology is Based On a Central Device that can be _____ ?
a.HUB
b.Switch
c.Only a
d.Both a and b
Ans:- d

9.Which of the following is not type of the network topology?
a.Mesh
b.Bus
c.Ring
d.stub
Ans:- d

10.In a star-topology Ethernet LAN, _____ is just a point where the signals coming from different stations collide; it is the collision point.
a.An active hub
b.A passive hub
c.either (a) or (b)
d.neither (a) nor (b)
Ans:- b

11) Group communication operations are built using point-to-point messaging primitives
A. True
B. False
Ans:- A

12) A hypercube has_

A. 2d nodes
B. 2d nodes
C. 2n Nodes
D. N Nodes
Ans:- A

13)The function of multiplexing is
a. To reduce the bandwidth of the signal to be transmitted
b. To combine multiple data streams over a single data channel
c. To allow multiple data streams over multiple channels in a prescribed format
d. To match the frequencies of the signal at the transmitter as well as the receiver
Ans: b
14) A 3 GHz carrier is DSB SC modulated by a signal with maximum frequency of 2 MHz. The minimum sampling frequency required for the signal so that the signal is ideally sampled is
a. 4 MHz
b. 6 MHz
c. 6.004 GHz
d. 6 GHz
Ans: c

15) Emitter modulator amplifier for Amplitude Modulation
a. Operates in class A mode
b. Has a low efficiency
c. Output power is small
d. All of the above
Ans: d

16) Super heterodyne receivers
a. Have better sensitivity
b. Have high selectivity
c. Need extra circuitry for frequency conversion
d. All of the above
Ans: d

17) The AM spectrum consists of
a. Carrier frequency
b. Upper side band frequency
c. Lower side band frequency
d. All of the above
Ans: d

18) Standard intermediate frequency used for AM receiver is
a. 455 MHz
b. 455 KHz
c. 455 Hz
d. None of the above

Ans: b

19) In the TV receivers, the device used for tuning the receiver to the incoming signal is
a. Varactor diode
b. High pass Filter
c. Zener diode
d. Low pass filter
Ans: a

20) The modulation technique that uses the minimum channel bandwidth and transmitted power is
a. FM
b. DSB-SC
c. VSB
d. SSB
Ans: d

21) Calculate the bandwidth occupied by a DSB signal when the modulating frequency lies in the range from 100 Hz to 10KHz.
a. 28 KHz
b. 24.5 KHz
c. 38.6 KHz
d. 19.8 KHz
Ans: d

23)What is a high performance multi-core processor that can be used to accelerate a wide variety of applications using parallel computing.
1. CLU
2. GPU
3. CPU
4. DSP
ANS-2

24) What is GPU?
1. Grouped Processing Unit
2. Graphics Processing Unit
3. Graphical Performance Utility
4. Graphical Portable Unit
ANS-2

25. A code, known as GRID, which runs on GPU consisting of a set of
1. 32 Thread
2. 32 Block
3. Unit Block
4. Thread Block
ANS-4

26. Interprocessor communication that takes place
1. Centralized memory
2. Shared memory
3. Message passing
4. Both A and B
ANS-4

27. Decomposition into a large number of tasks results in coarse-grained decomposition
1. True
2. False
ANS-2

28. The fetch and execution cycles are interleaved with the help of __
1. Modification in processor architecture
2. Clock
3. Special unit
4. Control unit
ANS-2

29**. The processor of system which can read /write GPU memory is known as**
1. kernal
2. device
3. Server
4. Host
ANS-4

30. Increasing the granularity of decomposition and utilizing the resulting concurrency to perform more tasks in parallel decreses performance.
1. TRUE
2. FALSE
ANS-2

SET 5 (MCQs)

What are the sources of overhead?
A. Essential /Excess Computation
B. Inter-process Communication
C. Idling
D. All above
Answer : D

Which are the performance metrics for parallel systems?

A. Execution Time
B. Total Parallel Overhead
C. Speedup
D. Efficiency
E. Cost
F. All above
Answer : F

The efficiency of a parallel program can be written as: ***E = Ts / pTp.*** True or False?
A. True
B. False
Answer : A

Overhead function or ***total overhead*** of a parallel system as the total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element.
True or False?
A. True
B. False
Answer : A

What is Speedup?
A. A measure that captures the relative benefit of solving a problem in parallel. It is defined as the
ratio of the time taken to solve a problem on a single processing element to the time required to solve the same problem on a parallel computer with *p* identical processing elements.
B. A measure of the fraction of time for which a processing element is usefully employed.
C. None of the above
Answer : A

In an ideal parallel system, speedup is equal to *p* and efficiency is equal to one. True or False?
A. True
B. False
Answer : A

A parallel system is said to be _____ if the cost of solving a problem on a parallel computer has the same asymptotic growth (in □□terms) as a function of the input size as the fastest-known sequential algorithm on a single processing element.
A. Cost optimal
B. Non Cost optimal
Answer : A

Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called _____ a parallel system in terms of the number of

processing elements.
A. Scaling down
B. Scaling up
Answer : B

The _____ function determines the ease with which a parallel system can maintain a constant efficiency and hence achieve speedups increasing in proportion to the number of processing elements.
A. Isoefficiency
B. Efficiency
C. Scalability
D. Total overhead
Answer : A

Minimum execution time for adding n numbers is $Tp = n/p + 2 \log p$ True or False ?
A. True
B. False
Answer : A

The overhead function To = pTP − TS.
A. True
B. False
Answer : A

Performance Metrics for Parallel Systems: Speedup(S) =TS/TP
A. True
B. False
Answer : A

Matrix Vector multiplication 2D Partitions requires some basic communication operations
A. one-to-one communication to align the vector along the main diagonal
B. one-to-all broadcast of each vector element among the n processes of each column
C. all-to-one reduction in each row
D. All Above
Answer : D

What are the issues in sorting?
A. Where the Input and Output Sequences are Stored
B. How Comparisons are Performed
C. All above
Answer : C

The parallel run time of the formulation for Bubble sort is
A. Tp = O(n/plogn/p) + O(n) + O(n)
B. Tp = O(n/plogn/p) + O (n/plogp) + O(ln/p)
C. Non of the above

Answer : A

What are the variants of Bubble sort?
A. Shell sort
B. Quick sort
C. Odd-Even transposition
D. Option A & C
Answer : D

What is the overall complexity of parallel algorithm for quick sort?
A. Tp = O(n/p logn/p) + O(n/p logp) + O(log2p)
B. Tp = O(n/p logn/p) + O(n/p logp)
C. Tp = O(n/p logn/p) + O(log2p)
Answer : A

Formally, given a weighted graph $G(V, E, w)$, the ***all-pairs shortest paths*** problem is to find the shortest paths between all pairs of vertices. True or False?
A. True
B. False
Answer : A

What is true for parallel formulation of Dijkstra's Algorithm?
A. One approach partitions the vertices among different processes and has each process compute the single-source shortest paths for all vertices assigned to it. We refer to this approach as the ***source-partitioned formulation.***
B. Another approach assigns each vertex to a set of processes and uses the parallel formulation of the single-source algorithm to solve the problem on each set of processes. We refer to this approach as the ***source-parallel formulation***.
C. Both are true
D. Non of these is true
Answer : C

Search algorithms can be used to solve discrete optimization problems. True or False ?
A. True
B. False
Answer : A

Examples of Discrete optimization problems are ;
A. planning and scheduling,
B. The optimal layout of VLSI chips,
C. Robot motion planning,
D. Test-pattern generation for digital circuits, and logistics and control.
E. All of above
Answer : E

List the important parameters of Parallel DFS

A. Work- Splitting Strategies
B. Load balancing Schemes
C. All of above
Answer : C

List the communication strategies for parallel BFS.
A. Random communication strategy
B. Ring communication strategy
C. Blackboard communication strategy
D. All of above
Answer : D

The lower bound on any comparison-based sort of n numbers is $\Theta(n \log n)$
A. True
B. False
Answer : A

In a compare-split operation
A. Each process sends its block of size n/p to the other process
B. Each process merges the received block with its own block and retains only the appropriate half of the merged block
C. Both A & B
Answer : C

In a typical sorting network
A. Every sorting network is made up of a series of columns
B. Each column contains a number of comparators connected in parallel
C. Both A & B
Answer : C

Bubble sort is difficult to parallelize since the algorithm has no concurrency
A. True
B. False
Answer : A

Unit I

1. Conventional architectures coarsely comprise of a_
A. A processor
B. Memory system
C Data path.
D All of Above

2. Data intensive applications utilize_
A **High aggregate throughput**
B High aggregate network bandwidth

C High processing and memory system performance.
D None of above

3. A pipeline is like_
A Overlaps various stages of instruction execution to achieve performance.
B House pipeline
C Both a and b
D A gas line

4. Scheduling of instructions is determined_
A True Data Dependency
B Resource Dependency
C Branch Dependency
D All of above

5. VLIW processors rely on_
A **Compile time analysis**
B Initial time analysis
C Final time analysis
D Mid time analysis

6. Memory system performance is largely captured by_
A Latency
B Bandwidth
C Both a and b
D none of above

7. The fraction of data references satisfied by the cache is called_
A Cache *hit ratio*
B Cache *fit ratio*
B Cache *best ratio*
C none of above

8. A single control unit that dispatches the same Instruction to various processors is__
A SIMD
B SPMD
C MIMD
D None of above

9. The primary forms of data exchange between parallel tasks are_
A Accessing a shared data space
B Exchanging messages.
C Both A and B
D None of Above

10. Switches map a fixed number of inputs to outputs.

A True
B False

Unit 2

1. The First step in developing a parallel algorithm is_
A. To Decompose the problem into tasks that can be executed concurrently
B. Execute directly
C. Execute indirectly
D. None of Above

2. The number of tasks into which a problem is decomposed determines its_
A. Granularity
B. Priority
C. Modernity
D. None of above

3. The length of the longest path in a task dependency graph is called_
A. the critical path length
B. the critical data length
C. the critical bit length
D. None of above

4. The graph of tasks (nodes) and their interactions/data exchange (edges)_
A. Is referred to as a *task interaction graph*
B. Is referred to as a *task Communication graph*
C. Is referred to as a *task interface graph*
D. None of Above

5. Mappings are determined by_
A. task dependency
B. task interaction graphs
C. Both A and B
D. None of Above

6. Decomposition Techniques are_
A. recursive decomposition
B. data decomposition
C. exploratory decomposition
D. speculative decomposition
E. All of Above

7. The *Owner Computes Rule* generally states that the process assigned a particular data item is responsible for_
A. All computation associated with it
B. Only one computation
C. Only two computation

D. Only occasionally computation

8. A simple application of exploratory decomposition is_
A. The solution to a 15 puzzle
B. The solution to 20 puzzle
C. The solution to any puzzle
D. None of Above

9. Speculative Decomposition consist of _
A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B

10. task characteristics include:
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.
D. All of Above

Unit 3

1. Group communication operations are built using point-to-point messaging primitives
A. True
B. False

2. Communicating a message of size m over an uncongested network takes time ts + tmw
A. True
B. False

3. The dual of one-to-all broadcast is_
A. *All-to-one reduction*
B. *All-to-one receiver*
C. *All-to-one Sum*
D. *None of Above*

4. A hypercube has_
A. 2d nodes
B. 2d nodes
C. 2n Nodes
D. N Nodes

5. A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes.
A. True
B. False

6. In All-to-All Broadcast each processor is the source as well as destination.
A. True
B. False

7. The Prefix Sum Operation can be implemented using the_
A. All-to-all broadcast kernel.
B. All-to-one broadcast kernel.
C. One-to-all broadcast Kernel
D. Scatter Kernel

8. In the *scatter* operation_
A. Single node send a unique message of size m to every other node
B. Single node send a same message of size m to every other node
C. Single node send a unique message of size m to next node
D. None of Above

9. The gather operation is exactly the inverse of the_
A. Scatter operation
B. Broadcast operation
C. Prefix Sum
D. Reduction operation

10. In All-to-All Personalized Communication Each node has a distinct message of size m for every other node
A. True
B. False

1. It is _____ strength and _____ permeability.
a) High, high
b) Low, low
c) High, low
d) Low, high
View Answer
Answer: c
Explanation: It is specifically chosen so as to have particularly appropriate properties for the expected use of the structure such as high strength and low permeability.

2. High Performance concrete works out to be economical.
a) True
b) False
View Answer
Answer: a
Explanation: High Performance concrete works out to be economical, even though its initial cost is high.

3. HPC is not used in high span bridges.
a) True
b) False
View Answer
Answer: b
Explanation: Major applications of high-performance concrete in the field of Civil Engineering constructions have been in the areas of long-span bridges, high-rise buildings or structures, highway pavements, etc.

4. Concrete having 28- days' compressive strength in the range of 60 to 100 MPa.
a) HPC
b) VHPC
c) OPC
d) HSC
View Answer
Answer: a
Explanation: High Performance Concrete having 28- days' compressive strength in the range of 60 to 100 MPa

5. Concrete having 28-days compressive strength in the range of 100 to 150 MPa.
a) HPC
b) VHPC
c) OPC
d) HSC
View Answer
Answer: b
Explanation: Very high performing Concrete having 28-days compressive strength in the range of 100 to 150 MPa.

6. High-Performance Concrete is _____ as compared to Normal Strength Concrete.
a) Less brittle
b) Brittle
c) More brittle
d) Highly ductile
View Answer
Answer: c
Explanation: High-Performance Concrete is more brittle as compared to Normal Strength Concrete (NSC), especially when high strength is the main criteria

7. The choice of cement for high-strength concrete should not be based only on mortarcube tests but it should also include tests of compressive strengths of concrete at _____ days.
a) 28, 56, 91
b) 28, 60, 90
c) 30, 60, 90

d) 30, 45, 60
View Answer
Answer: a
Explanation: The choice of cement for high-strength concrete should not be based only on mortar-cube tests but it should also include tests of compressive strengths of concrete at 28, 56, and 91 days.

8. For high-strength concrete, a cement should produce a minimum 7-days mortar-cube strength of approximately ___ MPa.
a) 10
b) 20
c) 30
d) 40
View Answer
Answer: c
Explanation: For high-strength concrete, a cement should produce a minimum 7-days mortar-cube strength of approximately 30 MPa.

9. _____ mm nominal maximum size aggregates gives optimum strength.
a) 9.5 and 10.5
b) 10.5 and 12.5
c) 9.5 and 12.5
d) 11.5 and 12.5
View Answer
Answer: c

Explanation: Many studies have found that 9.5 mm to 12.5 mm nominal maximum size aggregates gives optimum strength.
10. Due to low w/c ratio _____
a) It doesn't cause any problems
b) It causes problems
c) Workability is easy
d) Strength is more
View Answer
Answer: b
Explanation: Due to the low w/c ratio, it causes problems so superplasticizers are used.

Which of the following statements are true with regard to compute capability in CUDA
A. Code compiled for hardware of one compute capability will not need to be recompiled to run on hardware of another
B. Different compute capabilities may imply a different amount of local memory per thread
C. Compute capability is measured by the number of FLOPS a GPU accelerator can compute.
Answer : B

True or False: The threads in a thread block are distributed across SM units so that each thread is executed by one SM unit.
A. True
B. False
Answer : B

The style of parallelism supported on GPUs is best described as
A. SISD - Single Instruction Single Data
B. MISD - Multiple Instruction Single Data
C. SIMT - Single Instruction Multiple Thread
Answer : C

True or false: Functions annotated with the __global__ qualifier may be executed on the host or the device
A. True
B. Flase
Answer : A

Which of the following correctly describes a GPU kernel
A. A kernel may contain a mix of host and GPU code
B. All thread blocks involved in the same computation use the same kernel
C. A kernel is part of the GPU's internal micro-operating system, allowing it to act as in independent host
Answer : B

Which of the following is *not* a form of parallelism supported by CUDA
A. Vector parallelism - Floating point computations are executed in parallel on wide vector units
B. Thread level task parallelism - Different threads execute a different tasks
C. Block and grid level parallelism - Different blocks or grids execute different tasks
D. Data parallelism - Different threads and blocks process different parts of data in memory
Answer :A

What strategy does the GPU employ if the threads within a warp diverge in their execution?
A. Threads are moved to different warps so that divergence does not occur within a single warp
B. Threads are allowed to diverge
C. All possible execution paths are run by all threads in a warp serially so that thread instructions do not diverge
Answer : C

Which of the following does *not* result in uncoalesced (i.e. serialized) memory access on the K20 GPUs installed on Stampede
A. Aligned, but non-sequential access
B. Misaligned data access

C. Sparse memory access
Answer : A

Which of the following correctly describes the relationship between Warps, thread blocks, and CUDA cores?
A. A warp is divided into a number of thread blocks, and each thread block executes on a single CUDA core
B. A thread block may be divided into a number of warps, and each warp may execute on a single CUDA core
C. A thread block is assigned to a warp, and each thread in the warp is executed on a separate CUDA core
Answer : B

Shared memory in CUDA is accessible to:
A. All threads in a single block
B. Both the host and GPU
C. All threads associated with a single kernel
Answer : A

CUDA Architecture CPU consist of
A. CUDA Libraries
B. CUDA Runtime
C. CUDA Driver
D. All Above
Answer : D

CUDA platform works on
A. C
B. C++
C. Forton
D. All Above
Answer : D

Threads support Shared memory and Synchronization
A. True
B. False
Answer : A

Application of CUDA are
A. Fast Video Transcoding
B. Medical Imaging
C. Computational Science
D. Oil and Natural Resources exploration
E. All Above
Answer : E

GPU execute device code
A. True
B. False
Answer : A

SET 6 (MCQs)

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1) Execution of several activities at the same time.
a) processing b) parallel processing c) serial processing d) multitasking
Ans: b Explanation:

2)
Parallel processing has single execution flow.
a) True b) False
Ans: b Explanation: The statement is false. Sequential programming specifically has single execution flow.

3)
A term for simultaneous access to a resource, physical or logical.
a) Multiprogramming b) Multitasking c) Threads d) Concurrency
Ans: d Explanation: Concurrency is the term used for the same. When several things are accessed simultaneously, the job is said to be concurrent.

4)
_____ leads to concurrency.
a) Serialization b) Parallelism c) Serial processing d) Distribution Ans: b Explanation: Parallelism leads naturally to Concurrency. For example, Several processes trying to print a file on a single printer.

5)
A parallelism based on increasing processor word size.
a) Increasing b) Count based c) Bit based d) Bit level
Ans: d Explanation: Bit level parallelism is based on increasing processor word size. It focuses on hardware capabilities for structuring.

6)
The measure of the "effort" needed to maintain efficiency while adding processors.
a) Maintainability b) Efficiency
c) Scalability d) Effectiveness
Ans: C Explanation: The measure of the "effort" needed to maintain efficiency while adding processors is called as scalability.

7)
Several instructions execution simultaneously in _____

a) processing b) parallel processing c) serial processing d) multitasking
Ans: b Explanation: In parallel processing, the several instructions are executed simultaneously.

8)
Conventional architectures coarsely comprise of a_
a) A processor
b) Memory system
c) Data path.
d) All of Above
Ans: d Explanation:

9) A pipeline is like_
a) Overlaps various stages of instruction execution to achieve performance.
b) House pipeline
c) Both a and b
d) A gas line
Ans: a Explanation:

10) VLIW processors rely on_
a) Compile time analysis
b) Initial time analysis
c) Final time analysis
d) Mid time analysis
Ans: a Explanation:

11)
Memory system performance is largely captured by_
a) Latency
b) Bandwidth
c) Both a and b
d) none of above
Ans: c Explanation:

12)
The fraction of data references satisfied by the cache is called_
a) Cache hit ratio
b) Cache fit ratio
c) Cache best ratio
d) none of above
Ans: a Explanation:

13)
A single control unit that dispatches the same Instruction to various processors is__
a) SIMD
b) SPMD
c) MIMD

d) None of above
Ans: a Explanation:

14)
The primary forms of data exchange between parallel tasks are_
a) Accessing a shared data space
b) Exchanging messages.
c) Both A and B
d) None of Above Ans: c Explanation:

16)
Switches map a fixed number of inputs to outputs.
a) True
b) False
Ans: a Explanation:

UNIT-2

1)
The First step in developing a parallel algorithm is_
a) To Decompose the problem into tasks that can be executed concurrently
b) Execute directly
c) Execute indirectly
d) None of Above
Ans: a Explanation:

2)
The number of tasks into which a problem is decomposed determines its_
a) Granularity
b) Priority
c) Modernity
d) None of above
Ans: A Explanation:

3)
The length of the longest path in a task dependency graph is called_
a) the critical path length
b) the critical data length
c) the critical bit length
d) None of above
Ans: a Explanation:

4)
The graph of tasks (nodes) and their interactions/data exchange (edges)_
a) Is referred to as a task interaction graph
b) Is referred to as a task Communication graph

c) Is referred to as a task interface graph
d) None of Above
Ans: a Explanation:

5)
Mappings are determined by_
a) task dependency
b) task interaction graphs
c) Both A and B
d) None of Above
Ans: c Explanation:

6)
Decomposition Techniques are_
a) recursive decomposition
b) data decomposition
c) exploratory decomposition
d) speculative decomposition
e) All of Above
Ans: E Explanation:

7)
The Owner Computes Rule generally states that the process assigned a particular data item is responsible for_
a) All computation associated with it
b) Only one computation
c) Only two computation
d) Only occasionally computation
Ans: A Explanation:

8)
A simple application of exploratory decomposition is_
a) The solution to a 15 puzzle
b) The solution to 20 puzzle
c) The solution to any puzzle
d) None of Above
Ans: A Explanation:

9)
Speculative Decomposition consist of _
a) conservative approaches
b) optimistic approaches
c) Both A and B
d) Only B
Ans: C Explanation:

10)
task characteristics include:
a) Task generation.
b) Task sizes.
c) Size of data associated with tasks.
d) All of Above
Ans: d Explanation: UNIT-3

1)
Group communication operations are built using point-to-point messaging primitives
a) True
b) False
Ans: A Explanation:

2)
Communicating a message of size m over an uncongested network takes time ts + tmw
a) True
b) False
Ans: A Explanation:

3)
The dual of one-to-all broadcast is_
a) All-to-one reduction
b) All-to-one receiver
c) All-to-one Sum
d) None of Above
Ans: A Explanation:

4)
A hypercube has_
a) 2d nodes
b) 2d nodes
c) 2n Nodes
d) N Nodes
Ans: a Explanation:

5)
A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes.
a) True
b) False
Ans: A Explanation:

6)
In All-to-All Broadcast each processor is the source as well as destination.
a) True

b) False
Ans: A Explanation:

7)
The Prefix Sum Operation can be implemented using the_
a) All-to-all broadcast kernel.
b) All-to-one broadcast kernel.
c) One-to-all broadcast Kernel
d) Scatter Kernel
Ans: A Explanation:

8)
In the scatter operation_
a) Single node send a unique message of size m to every other node
b) Single node send a same message of size m to every other node
c) Single node send a unique message of size m to next node
d) None of Above
Ans: A Explanation:

9)
The gather operation is exactly the inverse of the_
a) Scatter operation
b) Broadcast operation
c) Prefix Sum
d) Reduction operation
Ans: A Explanation:

10)
In All-to-All Personalized Communication Each node has a distinct message of size m for every other node
a) True
b) False
Ans: a Explanation:

UNIT-1

1) Conventional architectures coarsely comprise of a_____

a) processor
b) Memory system
c) Datapath.
d) All of Above
Ans: d
Explanation:

2) Data intensive applications utilize_____

a) High aggregate throughput

b) High aggregate network bandwidth

c) High processing and memory system performance.

d) None of above

Ans: a

Explanation:

3) A pipeline is like_____

a. Overlaps various stages of instruction execution to achieve performance.

b. House pipeline

c. Both a and b

d. gas line

Ans: a

Explanation:

4) Scheduling of instructions is determined ____

a) True Data Dependency

b) Resource Dependency

c) Branch Dependency

d) All of above

Ans: d

Explanation:

5) VLIW processors rely on_____

a) Compile time analysis

b) Initial time analysis

c) Final time analysis

d) Mid time analysis

Ans: a

Explanation:

6) Memory system performance is largely captured by_____

a) Latency

b) Bandwidth

c) Both a and b

d) none of above

Ans: c

Explanation:

7) The fraction of data references satisfied by the cache is called_____

a) Cache hit ratio

b) Cache fit ratio
c) Cache best ratio
d) none of above
Ans: a
Explanation:
8) A single control unit that dispatches the same Instruction to various processors is__
a) SIMD
b) SPMD
c) MIMD
d) None of above
Ans: a
Explanation:
9) The primary forms of data exchange between parallel tasks are_

a. Accessing a shared data space
b. Exchanging messages.
c. Both A and B
d. None of Above
Ans: c
Explanation:
10) Switches map a fixed number of inputs to outputs.
a) True
b) False
Ans: a
Explanation:
11) The stage in which the CPU fetches the instructions from the instruction cache in superscalar organization is
a) Prefetch stage
b) D1 (first decode) stage
c) D2 (second decode) stage
d) Final stage
Ans: a
Explanation: In the prefetch stage of pipeline, the CPU fetches the instructions from the instruction cache, which stores the instructions to be executed. In this stage, CPU also aligns the codes appropriately.

12) The CPU decodes the instructions and generates control words in
a) Prefetch stage
b) D1 (first decode) stage
c) D2 (second decode) stage
d) Final stage
Ans: b

Explanation: In D1 stage, the CPU decodes the instructions and generates control words. For simple RISC instructions, only single control word is enough for starting the execution.
13) The fifth stage of pipeline is also known as

a) read back stage
b) read forward stage
c) write back stage
d) none of the mentioned
Ans: c
Explanation: The fifth stage or final stage of pipeline is also known as "Write back (WB) stage".
14) In the execution stage the function performed is
a) CPU accesses data cache
b) executes arithmetic/logic computations
c) executes floating point operations in execution unit
d) all of the mentioned
Ans: d
Explanation: In the execution stage, known as E-stage, the CPU accesses data cache, executes arithmetic/logic computations, and floating point operations in execution unit.

15) The stage in which the CPU generates an address for data memory references in this stage is
a) prefetch stage
b) D1 (first decode) stage
c) D2 (second decode) stage
d) execution stage
Ans: c
Explanation: In the D2 (second decode) stage, CPU generates an address for data memory references in this stage. This stage is required where the control word from D1 stage is again decoded for final execution.

16) The feature of separated caches is
a) supports the superscalar organization
b) high bandwidth
c) low hit ratio
d) all of the mentioned
Ans: d
Explanation: The separated caches have low hit ratio compared to a unified cache, but have the advantage of supporting the superscalar organization and high bandwidth.
17) In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from
a) floating point unit
b) instruction cache
c) floating point register file or data cache
d) floating point register file or instruction cache
Ans: C
Explanation: In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from either floating point register file or data cache.
18) The FPU (Floating Point Unit) writes the results to the floating point register file in
a) X1 execution state
b) X2 execution state

c) write back stage
d) none of the mentioned

Ans: c
Explanation: In the two execution stages of X1 and X2, the floating point unit reads the data from the data cache and executes the floating point computation. In the "write back stage" of pipeline, the FPU (Floating Point Unit) writes the results to the floating point register file.

19) The floating point multiplier segment performs floating point multiplication in
a) single precision
b) double precision
c) extended precision
d) all of the mentioned

Ans: d
Explanation: The floating point multiplier segment performs floating point multiplication in single precision, double precision and extended precision.
20) The instruction or segment that executes the floating point square root instructions is
a) floating point square root segment
b) floating point division and square root segment
c) floating point divider segment
d) none of the mentioned

Ans: c
Explanation: The floating point divider segment executes the floating point division and square root instructions.

21) The floating point rounder segment performs rounding off operation at

a) after write back stage
b) before write back stage
c) before arithmetic operations
d) none of the mentioned
Ans: b
Explanation: The results of floating point addition or division process may be required to be rounded off, before write back stage to the floating point registers.
21) Which of the following is a floating point exception that is generated in case of integer arithmetic?
a) divide by zero
b) overflow
c) denormal operand
d) all of the mentioned
Ans: D
Explanation: In the case of integer arithmetic, the possible floating point exceptions in Pentium are:
1. divide by zero

2. overflow
3. denormal operand
4. underflow
5. invalid operation.

1. The First step in developing a parallel algorithm is_

E. To Decompose the problem into tasks that can be executed concurrently
F. Execute directly
G. Execute indirectly
H. None of Above

2. The number of tasks into which a problem is decomposed determines its_

E. Granularity
F. Priority
G. Modernity
H. None of above

3. The length of the longest path in a task dependency graph is called_
F. the critical path length
G. the critical data length
H. the critical bit length
I. None of above

4. The graph of tasks (nodes) and their interactions/data exchange (edges)_
   E. Is referred to as a *task interaction graph*
   F. Is referred to as a *task Communication graph*
   G. Is referred to as a *task interface graph*
   H. None of Above

5. Mappings are determined by_

E. task dependency
F. task interaction graphs
G. Both A and B
H. None of Above

6. Decomposition Techniques are_
F. recursive decomposition
G. data decomposition
H. exploratory decomposition
I. speculative decomposition
J. All of Above

7. The *Owner Computes Rule* generally states that the process assigned a particular data item is responsible for_

E. All computation associated with it
F. Only one computation
G. Only two computation
H. Only occasionally computation

8. A simple application of exploratory decomposition is_

E. The solution to a 15 puzzle
F. The solution to 20 puzzle
G. The solution to any puzzle
H. None of Above

9. Speculative Decomposition consist of _

E. conservative approaches
F. optimistic approaches
G. Both A and B
H. Only B

10. task characteristics include:
E. Task generation.
F. Task sizes.
G. Size of data associated with tasks.
H. All of Above

11. Choose the most accurate (**CORRECT**) statement:
a. Scalability is a measure of the capacity to increase speedup in proportion to the number of processors
b. Efficiency is the ratio of the serial run time of the best sequential algorithm for solving a problem to the time taken by the parallel algorithm to solve the same problem on *p* processors
c. Run time is the time that elapses from the moment a parallel computation starts to the moment the last processor finishes.
d. Superlinear is the fraction of time for which a processor is usefully employed
12. Parallelism can be used to increase the (parallel) size of the problem is applicable in _____.
a. Amdahl's Law
b. Gustafson-Barsis's Law
c. Newton's Law
d. Pascal's Law

13. _____ is due to load imbalance, synchronization, or serial components as parts of overheads in parallel programs.
a. Interprocess interaction
b. Synchronization
c. Idling
d. Excess computation
14. Which of the following parallel methodological design elements focuses on recognizing opportunities for parallel execution?
a. Partitioning
b. Communication
c. Aggromeration
d. Mapping
15. Considering to use weak or strong scaling is part of _____ in addressing the challenges of distributed memory programming.
a. Splitting the problem
b. Speeding up computations
c. Speeding up communication
d. Speeding up hardware
16. Domain and functional decomposition are considered in the following parallel methodological design elements, **EXCEPT**:
a. Partitioning
b. Communication
c. Agglomeration
d. Mapping
17. Synchronization is one of the common issues in parallel programming. The issues related to synchronization include the followings, **EXCEPT**:
a. Deadlock
b. Livelock
c. Fairness
d. Correctness
18. Which of the followings is the **BEST** description of Message Passing Interface (MPI)?
a. A specification of a shared memory library
b. MPI uses objects called communicators and groups to define which collection of processes may communicate with each other
c. Only communicators and not groups are accessible to the programmer only by a "handle"
d. A communicator is an ordered set of processes

SET 7 MCQs

Which is alternative options for latency hiding?
A. Increase CPU frequency
B. Multithreading
C. Increase Bandwidth

D. Increase Memory
ANSWER: B
_____ Communication model is generally seen in tightly coupled system.
A. Message Passing
B. Shared-address space
C. Client-Server
D. Distributed Network
ANSWER: B
The principal parameters that determine the communication latency are as follows:
A. Startup time (ts) Per-hop time (th) Per-word transfer time (tw)
B. Startup time (ts) Per-word transfer time (tw)
C. Startup time (ts) Per-hop time (th)
D. Startup time (ts) Message-Packet-Size(W)
ANSWER: A
The number and size of tasks into which a problem is decomposed determines the __
A. Granularity
B. Task
C. Dependency Graph
D. Decomposition
ANSWER: A
Average Degree of Concurrency is...
A. The average number of tasks that can run concurrently over the entire duration of execution of the process.
B. The average time that can run concurrently over the entire duration of execution of the process.
C. The average in degree of task dependency graph.
D. The average out degree of task dependency graph.
ANSWER: A
Which task decomposition technique is suitable for the 15-puzzle problem?
A. Data decomposition
B. Exploratory decomposition
C. Speculative decomposition
D. Recursive decomposition
ANSWER: B
Which of the following method is used to avoid Interaction Overheads?
A. Maximizing data locality
B. Minimizing data locality
C. Increase memory size
D. None of the above.
ANSWER: A
Which of the following is not parallel algorithm model

A. The Data Parallel Model
B. The work pool model
C. The task graph model
D. The Speculative Model
ANSWER: D
Nvidia GPU based on following architecture
A. MIMD
B. SIMD
C. SISD
D. MISD
ANSWER: B
What is Critical Path?
A. The length of the longest path in a task dependency graph is called the critical path length.
B. The length of the smallest path in a task dependency graph is called the critical path length.
C. Path with loop
D. None of the mentioned.
ANSWER: A
Which decompositioin technique uses divide-andconquer strategy?
A. recursive decomposition
B. Sdata decomposition
C. exploratory decomposition
D. speculative decomposition
ANSWER: A
If there are 6 nodes in a ring topology how many message passing cycles will be required to complete broadcast process in one to all?
A. 1
B. 6
C. 3
D. 4
ANSWER: 3
If there is 4 X 4 Mesh topology network then how many ring operation will perform to complete one to all broadcast?
A. 4
B. 8
C. 16
D. 32
ANSWER: 8
Consider all to all broadcast in ring topology with 8 nodes. How many messages will be present with each node after 3rd step/cycle of communication?
A. 3
B. 4
C. 6
D. 7

ANSWER: 4
Consider Hypercube topology with 8 nodes then how many message passing cycles will require in all to all broadcast operation?
A. The longest path between any pair of finish nodes.
B. The longest directed path between any pair of start & finish node.
C. The shortest path between any pair of finish nodes.
D. The number of maximum nodes level in graph.
ANSWER: D
Scatter is _____.
A. One to all broadcast communication
B. All to all broadcast communication
C. One to all personalised communication
D. Node of the above.
ANSWER: C
If there is 4X4 Mesh Topology _____ message passing cycles will require complete all to all reduction.
A. 4
B. 6
C. 8
D. 16
ANSWER: C
Following issue(s) is/are the true about sorting techniques with parallel computing.
A. Large sequence is the issue
B. Where to store output sequence is the issue
C. Small sequence is the issue
D. None of the above
ANSWER: B
Partitioning on series done after _____
A. Local arrangement
B. Processess assignments
C. Global arrangement
D. None of the above
ANSWER: C
In Parallel DFS processes has following roles.(Select multiple choices if applicable)
A. Donor
B. Active
C. Idle
D. Passive
ANSWER: A
Suppose there are 16 elements in a series then how many phases will be required to sort the series using parallel odd-even bubble sort?
A. 8
B. 4

C. 5
D. 15
ANSWER: D
Which are different sources of Overheads in Parallel Programs?
A. Interprocess interactions
B. Process Idling
C. All mentioned options
D. Excess Computation
ANSWER: C
The ratio of the time taken to solve a problem on a parallel processors to the time required to solve the same problem on a single processor with p identical processing elements.
A. The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements.
B. The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements
C. The ratio of number of multiple processors to size of data
D. None of the above
ANSWER: B
Efficiency is a measure of the fraction of time for which a processing element is usefully employed.
A. TRUE
B. FALSE
ANSWER: A
CUDA helps do execute code in parallel mode using _____
A. CPU
B. GPU
C. ROM
D. Cash memory
ANSWER: B
In thread-function execution scenario thread is a _____
A. Work
B. Worker
C. Task
D. None of the above
ANSWER: B
In GPU Following statements are true
A. Grid contains Block
B. Block contains Threads
C. All the mentioned options.
D. SM stands for Streaming MultiProcessor
ANSWER: C
Computer system of a parallel computer is capable of_____
A. Decentralized computing

B. Parallel computing
C. Centralized computing
D. All of these
ANSWER: A
In which application system Distributed systems can run well?
A. HPC
B. Distrubuted Framework
C. HRC
D. None of the above
ANSWER: A
A pipeline is like ..... ?
A. an automobile assembly line
B. house pipeline
C. both a and b
D. a gas line
ANSWER: A
Pipeline implements ?
A. fetch instruction
B. decode instruction
C. fetch operand
D. all of above
ANSWER: D
A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ ?
A. Super-scaling
B. Pipe-lining
C. Parallel Computation
D. None of these
ANSWER: B
In a parallel execution, the performance will always improve as the number of processors will increase?
A. True
B. False
ANSWER: B
VLIW stands for ?
A. Very Long Instruction Word
B. Very Long Instruction Width
C. Very Large Instruction Word
D. Very Long Instruction Width
ANSWER: A
In VLIW the decision for the order of execution of the instructions depends on the program itself?
A. True
B. False
ANSWER: A
Which one is not a limitation of a distributed memory parallel

system?
A. Higher communication time
B. Cache coherency
C. Synchronization overheads
D. None of the above
ANSWER: B
Which of these steps can create conflict among the processors?
A. Synchronized computation of local variables
B. Concurrent write
C. Concurrent read
D. None of the above
ANSWER: B
Which one is not a characteristic of NUMA multiprocessors?
A. It allows shared memory computing
B. Memory units are placed in physically different location
C. All memory units are mapped to one common virtual global memory
D. Processors access their independent local memories
ANSWER: D
Which of these is not a source of overhead in parallel computing?
A. Non-uniform load distribution
B. Less local memory requirement in distributed computing
C. Synchronization among threads in shared memory computing
D. None of the above
ANSWER: B
Systems that do not have parallel processing capabilities are?
A. SISD
B. SIMD
C. MIMD
D. All of the above
ANSWER: A
How does the number of transistors per chip increase according to
Moore ´s law?
A. Quadratically
B. Linearly
C. Cubicly
D. Exponentially
ANSWER: D
Parallel processing may occur?
A. in the instruction stream
B. in the data stream
C. both[A] and [B]
D. none of the above
ANSWER: C
To which class of systems does the von Neumann computer belong?
A. SIMD (Single Instruction Multiple Data)
B. MIMD (Multiple Instruction Multiple Data)

C. MISD (Multiple Instruction Single Data)
D. SISD (Single Instruction Single Data)
ANSWER: D
Fine-grain threading is considered as a _____ threading?
A. Instruction-level
B. Loop level
C. Task-level
D. Function-level
ANSWER: A
Multiprocessor is systems with multiple CPUs, which are capable of independently executing different tasks in parallel. In this category every processor and memory module has similar access time?
A. UMA
B. Microprocessor
C. Multiprocessor
D. NUMA
ANSWER: A
For inter processor communication the miss arises are called?
A. hit rate
B. coherence misses
C. comitt misses
D. parallel processing
ANSWER: B
NUMA architecture uses _____in design?
A. cache
B. shared memory
C. message passing
D. distributed memory
ANSWER: D
A multiprocessor machine which is capable of executing multiple instructions on multiple data sets?
A. SISD
B. SIMD
C. MIMD
D. MISD
ANSWER: C
In message passing, send and receive message between?
A. Task or processes
B. Task and Execution
C. Processor and Instruction
D. Instruction and decode
ANSWER: A
The First step in developing a parallel algorithm is_____?
A. To Decompose the problem into tasks that can be executed concurrently
B. Execute directly

C. Execute indirectly
D. None of Above
ANSWER: A
The number of tasks into which a problem is decomposed determines its?
A. Granularity
B. Priority
C. Modernity
D. None of above
ANSWER: A
The length of the longest path in a task dependency graph is called?
A. the critical path length
B. the critical data length
C. the critical bit length
D. None of above
ANSWER: A
The graph of tasks (nodes) and their interactions/data exchange (edges)?
A. Is referred to as a task interaction graph
B. Is referred to as a task Communication graph
C. Is referred to as a task interface graph
D. None of Above
ANSWER: A
Mappings are determined by?
A. task dependency
B. task interaction graphs
C. Both A and B
D. None of Above
ANSWER: C
Decomposition Techniques are?
A. recursive decomposition
B. data decomposition
C. exploratory decomposition
D. All of Above
ANSWER: D
The Owner Computes Rule generally states that the process assigned a particular data item is responsible for?
A. All computation associated with it
B. Only one computation
C. Only two computation
D. Only occasionally computation
ANSWER: A
A simple application of exploratory decomposition is_?
A. The solution to a 15 puzzle
B. The solution to 20 puzzle
C. The solution to any puzzle

D. None of Above
ANSWER: A
Speculative Decomposition consist of _?
A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B
ANSWER: C
task characteristics include?
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.
D. All of Above
ANSWER: D
Writing parallel programs is referred to as?
A. Parallel computation
B. Parallel processes
C. Parallel development
D. Parallel programming
ANSWER: D
Parallel Algorithm Models?
A. Data parallel model
B. Bit model
C. Data model
D. network model
ANSWER: A
The number and size of tasks into which a problem is decomposed determines the?
A. fine-granularity
B. coarse-granularity
C. sub Task
D. granularity
ANSWER: A
A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is its _____ path?
A. critical
B. easy
C. difficult
D. ambiguous
ANSWER: A
The pattern of_____ among tasks is captured by what is known as a task-interaction graph?
A. Interaction
B. communication
C. optmization

D. flow
ANSWER: A
Interaction overheads can be minimized by____?
A. Maximize Data Locality
B. Maximize Volume of data exchange
C. Increase Bandwidth
D. Minimize social media contents
ANSWER: A
Type of parallelism that is naturally expressed by independent tasks in a task-dependency graph is called _____ parallelism?
A. Task
B. Instruction
C. Data
D. Program
ANSWER: A
Speed up is defined as a ratio of?
A. s=Ts/Tp
B. S= Tp/Ts
C. Ts=S/Tp
D. Tp=S /Ts
ANSWER: A
Parallel computing means to divide the job into several _____?
A. Bit
B. Data
C. Instruction
D. Task
ANSWER: D
_____ is a method for inducing concurrency in problems that can be solved using the divide-and-conquer strategy?
A. exploratory decomposition
B. speculative decomposition
C. data-decomposition
D. Recursive decomposition
ANSWER: C
The___ time collectively spent by all the processing elements Tall = p TP?
A. total
B. Average
C. mean
D. sum
ANSWER: A
Group communication operations are built using point-to-point messaging primitives?
A. True
B. False
ANSWER: A

Communicating a message of size m over an uncongested network takes time ts + tmw?
A. True
B. False
ANSWER: A
The dual of one-to-all broadcast is ?
A. All-to-one reduction
B. All-to-one receiver
C. All-to-one Sum
D. None of Above
ANSWER: A
A hypercube has?
A. 2d nodes
B. 2d nodes
C. 2n Nodes
D. N Nodes
ANSWER: A
A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes?
A. True
B. False
ANSWER: A
In All-to-All Broadcast each processor is thesource as well as destination?
A. True
B. False
ANSWER: A
The Prefix Sum Operation can be implemented using the ?
A. All-to-all broadcast kernel.
B. All-to-one broadcast kernel.
C. One-to-all broadcast Kernel
D. Scatter Kernel
ANSWER: A
In the scatter operation ?
A. Single node send a unique message of size m to every other node
B. Single node send a same message of size m to every other node
C. Single node send a unique message of size m to next node
D. None of Above
ANSWER: A
The gather operation is exactly the inverse of the ?
A. Scatter operation
B. Broadcast operation
C. Prefix Sum
D. Reduction operation
ANSWER: A
In All-to-All Personalized Communication Each node has a distinct

message of size m for every other node ?
A. True
B. False
ANSWER: A
Parallel algorithms often require a single process to send identical data to all other processes or to a subset of them. This operation is known as _____?
A. one-to-all broadcast
B. All to one broadcast
C. one-to-all reduction
D. all to one reduction
ANSWER: A
In which of the following operation, a single node sends a unique message of size m to every other node?
A. Gather
B. Scatter
C. One to all personalized communication
D. Both A and C
ANSWER: D
Gather operation is also known as _____?
A. One to all personalized communication
B. One to all broadcast
C. All to one reduction
D. All to All broadcast
ANSWER: A
one-to-all personalized communication does not involve any duplication of data?
A. True
B. False
ANSWER: A
Gather operation, or concatenation, in which a single node collects a unique message from each node?
A. True
B. False
ANSWER: A
Conventional architectures coarsely comprise of a?
A. A processor
B. Memory system
C. Data path.
D. All of Above
ANSWER: D
Data intensive applications utilize?
A. High aggregate throughput
B. High aggregate network bandwidth
C. High processing and memory system performance.
D. None of above

ANSWER: A
A pipeline is like?
A. Overlaps various stages of instruction execution to achieve performance.
B. House pipeline
C. Both a and b
D. A gas line
ANSWER: A
Scheduling of instructions is determined?
A. True Data Dependency
B. Resource Dependency
C. Branch Dependency
D. All of above
ANSWER: D
VLIW processors rely on?
A. Compile time analysis
B. Initial time analysis
C. Final time analysis
D. Mid time analysis
ANSWER: A
Memory system performance is largely captured by?
A. Latency
B. Bandwidth
C. Both a and b
D. none of above
ANSWER: C
The fraction of data references satisfied by the cache is called?
A. Cache hit ratio
B. Cache fit ratio
C. Cache best ratio
D. none of above
ANSWER: A
A single control unit that dispatches the same Instruction to various processors is?
A. SIMD
B. SPMD
C. MIMD
D. None of above
ANSWER: A
The primary forms of data exchange between parallel tasks are?
A. Accessing a shared data space
B. Exchanging messages.
C. Both A and B
D. None of Above
ANSWER: C
Switches map a fixed number of inputs to outputs?

A. True
B. False
ANSWER: A
The First step in developing a parallel algorithm is?
A. To Decompose the problem into tasks that can be executed concurrently
B. Execute directly
C. Execute indirectly
D. None of Above
ANSWER: A
The number of tasks into which a problem is decomposed determines its?
A. Granularity
B. Priority
C. Modernity
D. None of above
ANSWER: A
The length of the longest path in a task dependency graph is called?
A. the critical path length
B. the critical data length
C. the critical bit length
D. None of above
ANSWER: A
The graph of tasks (nodes) and their interactions/data exchange (edges)?
A. Is referred to as a task interaction graph
B. Is referred to as a task Communication graph
C. Is referred to as a task interface graph
D. None of Above
ANSWER: A
Mappings are determined by?
A. task dependency
B. task interaction graphs
C. Both A and B
D. None of Above
ANSWER: C
Decomposition Techniques are?
A. recursive decomposition
B. data decomposition
C. exploratory decomposition
D. All of Above
ANSWER: D
The Owner Computes Rule generally states that the process assigned a particular data item are responsible for?
A. All computation associated with it
B. Only one computation

C. Only two computation
D. Only occasionally computation
ANSWER: A
A simple application of exploratory decomposition is?
A. The solution to a 15 puzzle
B. The solution to 20 puzzle
C. The solution to any puzzle
D. None of Above
ANSWER: A
Speculative Decomposition consist of ?
A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B
ANSWER: C
Task characteristics include?
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.
D. All of Above.
ANSWER: D
Group communication operations are built using point-to-point messaging primitives?
A. True
B. False
ANSWER: A
Communicating a message of size m over an uncongested network takes time ts + tmw?
A. True
B. False
ANSWER: A
The dual of one-to-all broadcast is?
A. All-to-one reduction
B. All-to-one receiver
C. All-to-one Sum
D. None of Above
ANSWER: A
A hypercube has?
A. 2d nodes
B. 3d nodes
C. 2n Nodes
D. N Nodes
ANSWER: A
A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes?
A. True

B. False
ANSWER: A
In All-to-All Broadcast each processor is the source as well as destination?
A. True
B. False
ANSWER: A
The Prefix Sum Operation can be implemented using the?
A. All-to-all broadcast kernel.
B. All-to-one broadcast kernel.
C. One-to-all broadcast Kernel
D. Scatter Kernel
ANSWER: A
In the scatter operation?
A. Single node send a unique message of size m to every other node
B. Single node send a same message of size m to every other node
C. Single node send a unique message of size m to next node
D. None of Above
ANSWER: A
The gather operation is exactly the inverse of the?
A. Scatter operation
B. Broadcast operation
C. Prefix Sum
D. Reduction operation
ANSWER: A
In All-to-All Personalized Communication Each node has a distinct message of size m for every other node?
A. True
B. False
ANSWER: A
Computer system of a parallel computer is capable of?
A. Decentralized computing
B. Parallel computing
C. Centralized computing
D. Decentralized computing
E. Distributed computing
ANSWER: A
Writing parallel programs is referred to as?
A. Parallel computation
B. Parallel processes
C. Parallel development
D. Parallel programming
ANSWER: D
Simplifies applications of three-tier architecture is _____?
A. Maintenance
B. Initiation

C. Implementation
D. Deployment
ANSWER: D
Dynamic networks of networks, is a dynamic connection that grows is called?
A. Multithreading
B. Cyber cycle
C. Internet of things
D. Cyber-physical system
ANSWER: C
In which application system Distributed systems can run well?
A. HPC
D. HTC
C. HRC
D. Both A and B
ANSWER: D
In which systems desire HPC and HTC?
A. Adaptivity
B. Transparency
C. Dependency
D. Secretive
ANSWER: B
No special machines manage the network of architecture in which resources are known as?
A. Peer-to-Peer
B. Space based
C. Tightly coupled
D. Loosely coupled
ANSWER: A
Significant characteristics of Distributed systems have of ?
A. 5 types
B. 2 types
C. 3 types
D. 4 types
ANSWER: C
Built of Peer machines are over?
A. Many Server machines
B. 1 Server machine
C. 1 Client machine
D. Many Client machines
ANSWER: D
Type HTC applications are?
A. Business
B. Engineering
C. Science
D. Media mass

ANSWER: A
Virtualization that creates one single address space architecture that of, is called?
A. Loosely coupled
B. Peer-to-Peer
C. Space-based
D. Tightly coupled
ANSWER: C
We have an internet cloud of resources In cloud computing to form?
A. Centralized computing
B. Decentralized computing
C. Parallel computing
D. All of these
ANSWER: D
Data access and storage are elements of Job throughput, of _____?
A. Flexibility
B. Adaptation
C. Efficiency
D. Dependability
ANSWER: C
Billions of job requests is over massive data sets, ability to support known as?
A. Efficiency
B. Dependability
C. Adaptation
D. Flexibility
ANSWER: C
Broader concept offers Cloud computing .to select which of the following?
A. Parallel computing
B. Centralized computing
C. Utility computing
D. Decentralized computing
ANSWER: C
Resources and clients transparency that allows movement within a system is called?
A. Mobility transparency
B. Concurrency transparency
C. Performance transparency
D. Replication transparency
ANSWER: A
Distributed program in a distributed computer running a is known as?
A. Distributed process
B. Distributed program
C. Distributed application

D. Distributed computing
ANSWER: B
Uniprocessor computing devices is called_____?
A. Grid computing
B. Centralized computing
C. Parallel computing
D. Distributed computing
ANSWER: B
Utility computing focuses on a_____ model?
A. Data
B. Cloud
C. Scalable
D. Business
ANSWER: D
What is a CPS merges technologies?
A. 5C
B. 2C
C. 3C
D. 4C
ANSWER: C
Aberration of HPC?
A. High-peak computing
B. High-peripheral computing
C. High-performance computing
D. Highly-parallel computing
ANSWER: C
Peer-to-Peer leads to the development of technologies like?
A. Norming grids
B. Data grids
C. Computational grids
D. Both A and B
ANSWER: D
Type of HPC applications of?
A. Management
B. Media mass
C. Business
D. Science
ANSWER: D
The development generations of Computer technology has gone through?
A. 6
B. 3
C. 4
D. 5
ANSWER: D
Utilization rate of resources in an execution model is known to be
its?

A. Adaptation
B. Efficiency
C. Dependability
D. Flexibility
ANSWER: B
Even under failure conditions Providing Quality of Service (QoS) assurance is the responsibility of?
A. Dependability
B. Adaptation
C. Flexibility
D. Efficiency
ANSWER: A
Interprocessor communication that takes place?
A. Centralized memory
B. Shared memory
C. Message passing
D. Both A and B
ANSWER: D
Data centers and centralized computing covers many and?
A. Microcomputers
B. Minicomputers
C. Mainframe computers
D. Supercomputers
ANSWER: D
Which of the following is an primary goal of HTC paradigm_____?
A. High ratio Identification
B. Low-flux computing
C. High-flux computing
D. Computer utilities
ANSWER: C
The high-throughput service provided is measures taken by
A. Flexibility
B. Efficiency
C. Dependability
D. Adaptation
ANSWER: D
What are the sources of overhead?
A. Essential /Excess Computation
B. Inter-process Communication
C. Idling
D. All above
ANSWER: D
Which are the performance metrics for parallel systems?
A. Execution Time
B. Total Parallel Overhead

C. Speedup
D. All above
ANSWER: D
The efficiency of a parallel program can be written as: E = Ts /
pTp. True or False?
A. True
B. False
ANSWER: A
The important feature of the VLIW is _____?
A. ILP
B. Performance
C. Cost effectiveness
D. delay
ANSWER: A

SET 8 (MCQs)

No.	Question	1	2	3	4	Ans
1	Any condition that causes a processor to stall is called as _____.	Hazard	Page fault	System error	None of the above	1
2	The time lost due to branch instruction is often referred to as _____.	Latency	Delay	Branch penalty	None of the above	3
3	_____ method is used in centralized systems to perform out of order execution.	Scorecard	Score boarding	Optimizing	Redundancy	2
4	The computer cluster architecture emerged as an alternative for ____.	ISA	Workstation	Super computers	Distributed systems	3
5	NVIDIA CUDA Warp is made up of how many threads?	512	1024	312	32	4
6	Out-of-order instructions is not possible on GPUs.	TRUE	FALSE	--	--	2
7	CUDA supports programming in	C or C++ only	Java, Python, and more	C, C++, third party wrappers for Java, Python, and more	Pascal	3
8	FADD, FMAD, FMIN, FMAX are ----- supported by Scalar Processors of NVIDIA GPU.	32-bit IEEE floating point instructions	32-bit integer instructions	both	none of the above	1
9	Each streaming multiprocessor (SM) of CUDA herdware has ------ scalar processors (SP).	1024	128	512	8	4
10	Each NVIDIA GPU has ------ Streaming Multiprocessors	8	1024	512	16	4
11	CUDA provides ------- warp and thread scheduling. Also, the overhead of thread creation is on the order of ----.	“programming-overhead”, 2 clock	“zero-overhead”, 1 clock	64, 2 clock	32, 1 clock	2
12	Each warp of GPU receives a single instruction and “broadcasts” it to all of its threads. It is a ---- operation.	SIMD (Single instruction multiple data)	SIMT (Single instruction multiple thread)	SISD (Single instruction single data)	SIST (Single instruction single thread)	2

13	Limitations of CUDA Kernel	recursion, call stack, static variable declaration	No recursion, no call stack, no static variable declarations	recursion, no call stack, static variable declaration	No recursion, call stack, no static variable declarations	**2**
14	What is Unified Virtual Machine	It is a technique that allow both CPU and GPU to read from single virtual machine, simultaneously .	It is a technique for managing separate host and device memory spaces.	It is a technique for executing device code on host and host code on device.	It is a technique for executing general purpose programs on device instead of host.	**1**
15	_____ became the first language specifically designed by a GPU Company to facilitate general purpose computing on ____.	Python, GPUs.	C, CPUs.	CUDA C, GPUs.	Java, CPUs.	**3**
16	The CUDA architecture consists of --------- for parallel computing kernels and functions.	RISC instruction set architecture	CISC instruction set architecture	ZISC instruction set architecture	PTX instruction set architecture	**4**
17	CUDA stands for --------, designed by NVIDIA.	Common Union Discrete Architecture	Complex Unidentified Device Architecture	Compute Unified Device Architecture	Complex Unstructured Distributed Architecture	**3**
18	The host processor spawns multithread tasks (or kernels as they are known in CUDA) onto the GPU device. State true or false.	TRUE	FALSE	---	---	**1**
19	The NVIDIA G80 is a ---- CUDA core device, the NVIDIA G200 is a ---- CUDA core device, and the NVIDIA Fermi is a ---- CUDA core device.	128, 256, 512	32, 64, 128	64, 128, 256	256, 512, 1024	**1**
20	NVIDIA 8-series GPUs offer -------- .	50-200 GFLOPS	200-400 GFLOPS	400-800 GFLOPS	800-1000 GFLOPS	**1**

21	IADD, IMUL24, IMAD24, IMIN, IMAX are ---------- supported by Scalar Processors of NVIDIA GPU.	32-bit IEEE floating point instructions	32-bit integer instructions	both	none of the above	**2**
22	CUDA Hardware programming model supports: a) fully generally data-parallel archtecture; b) General thread launch; c) Global load-store; d) Parallel data cache; e) Scalar architecture; f) Integers, bit operation	a,c,d,f	b,c,d,e	a,d,e,f	a,b,c,d,e,f	**4**
23	In CUDA memory model there are following memory types available: a) Registers; b) Local Memory; c) Shared Memory; d) Global Memory; e) Constant Memory; f) Texture Memory.	a, b, d, f	a, c, d, e, f	a, b, c, d, e, f	b, c, e, f	**3**
24	What is the equivalent of general C program with CUDA C: int main(void) { printf("Hello, World!\n"); return 0; }	int main (void) { kernel <<<1,1>>>(); printf("Hello, World!\n"); return 0; }	__global__ void kernel(void) { } int main (void) { kernel <<<1,1>>>(); printf("Hello, World!\n"); return 0; }	__global__ void kernel(void) { kernel <<<1,1>>>(); printf("Hello, World!\n"); return 0; }	__global__ int main (void) { kernel <<<1,1>>>(); printf("Hello, World!\n"); return 0; }	**2**
25	Which function runs on Device (i.e. GPU): a) __global__ void kernel (void) { } b) int main (void) { ... return 0; }	a	b	both a,b	---	**1**
26	A simple kernel for adding two integers: __global__ void add(int *a, int *b, int *c) { *c = *a + *b; } where __global__ is a CUDA C keyword which indicates that:	add() will execute on device, add() will be called from host	add() will execute on host, add() will be called from device	add() will be called and executed on host	add() will be called and executed on device	**1**
27	If variable a is host variable and dev_a is a device (GPU) variable, to allocate memory to dev_a select correct statement:	cudaMalloc(&dev_a, sizeof(int))	malloc(&dev_a, sizeof(int))	cudaMalloc((void**) &dev_a, sizeof(int))	malloc((void**) &dev_a, sizeof(int))	**3**

28	If variable a is host variable and dev_a is a device (GPU) variable, to copy input from variable a to variable dev_a select correct statement:	memcpy(dev_a, &a, size);	cudaMemcpy(dev_a, &a, size, cudaMemcpyHostToDevice);	memcpy((void*) dev_a, &a, size);	cudaMemcpy((void*) &dev_a, &a, size, cudaMemcpyDeviceToHost);	**2**
29	Triple angle brackets mark in a statement inside main function, what does it indicates?	a call from host code to device code	a call from device code to host code	less than comparison	greater than comparison	**1**
30	What makes a CUDA code runs in parallel	__global__ indicates parallel execution of code	main() function indicates parallel execution of code	Kernel name outside triple angle bracket indicates excecution of kernel N times in parallel	first parameter value inside triple angle bracket (N) indicates excecution of kernel N times in parallel	**4**
31	**Item Text**	**1**	**2**	**3**	**4**	**Ans**
32	Which of the following statements is **NOT TRUE** for Internal Sorting algorithms	Usually deal with small number of elements	No of elements must be able to fit in process's main memory	Use auxilliary memory like tape or hard disk	Ususally are of type compare-exchange	**3**
33						
34	In sorting networks for INCREASING COMPARATOR with input x,y select the correct output X', Y' from the following options	X' = min { x , y } and Y' = min { x , y }	X' = max { x , y } and Y' = min { x , y }	X' = min { x , y } and Y' = max{ x , y }	X' = max { x , y } and Y' = max { x , y }	**3**
35						
36	In sorting networks for DECREASING COMPARATOR with input x,y select the correct output X', Y' from the following options	X' = min { x , y } and Y' = min { x , y }	X' = max { x , y } and Y' = min { x , y }	X' = min { x , y } and Y' = max{ x , y }	X' = max { x , y } and Y' = max { x , y }	**2**
37						
38	Which of the following is TRUE for **Bitonic Sequence** a) Monotonically increasing b) Monotonically Decreasing c) With cyclic shift of indices d) First increasing then decreasing	a) and b)	a) and b) and d)	a) and b) and c)	a) and b) and c) and d)	**4**

39						
40	Which of the following is **NOT a BITONIC Sequence**	{8, 6, 4, 2, 3, 5, 7, 9}	{0, 4, 8, 9, 2, 1}	{3, 5, 7, 9, 8, 6, 4, 2}	{1, 2, 4, 7, 6, 0, 1}	**4**
41						
42	The procedure of sorting a bitonic sequence using bitonic splits is called	Bitonic Merge	Bitonic Split	Bitonic Divide	Bitonic Series	**1**
43						
44	While mapping Bitonic sort on Hypercube, Compare-exchange operations take place between wires whose labels differ in	One Bit	Two bits	Three Bits	Four bits	**1**
45						
46	Which of following is **NOT A WAY** of mapping the input wires of the bitonic sorting network to a MESH of processes	Row Major Mapping	Column Major Mapping	Row Major Snakelike mapping	Row Major Shuffled Mapping	**2**
47						
48	Which is the sorting algorithm in below given steps - 1. procedure X_SORT(n) 2. begin 3. for i := n - 1 downto 1 do 4. for j := 1 to i do 5. compare-exchange(aj, aj + 1); 6. end X_SORT	Selection Sort	Bubble Sort	Parallel Selcetion Sort	Parallel Bubble Sort	**2**
49						
50	The **odd-even transposition** algorithm sorts n elements in n phases (n is even), each of which requires ----------compare-exchange operations	2n	n^2	n/2	n	**3**
51						

52	What is TRUE about SHELL SORT	Moves elements only one position at a time	Moves elements long distance	During second phase algorithm switches to odd even transposition sort	both 2 and 3	**4**
53						
54	Which is the fastest sorting algorithm	Bubble Sort	Odd-Even Transposition Sort	Shell Sort	Quick Sort	**4**
55						
56	Quicksort's performance is greatly affected by the way it partitions a sequence.	TRUE	FALSE			**1**
57						
58	Pivot in Quick sort can be selected as	Always First Element	Always Last element	Always Middle index Element	Randomly Selected Element	**4**
59						
60	Quick sort uses Recursive Decomposition	TRUE	FALSE			**1**
61						
62	In first step of parallelizing quick sort for n elements to get subarrays, which of the following statement is TRUE	Only one process is used	n processes are used	two processes are used	None of the above	**1**
63						
64	In Binary tree representation created by execution of Quick sort, Pivot is at	Leaf Node	Root of tree	Any internal node	None of the above	**2**
65						
66	What is the worst case time complexity of a quick sort algorithm?	O(N)	O(N log N)	$O(N^2)$	O(log N)	**3**
67						
68	What is the average running time of a quick sort algorithm?	O(N)	O(N log N)	$O(N^2)$	O(log N)	**2**
69						
70	Odd-even transposition sort is a variation of	Quick Sort	Shell Sort	Bubble Sort	Selection Sort	**3**
71						

72	What is the average case time complexity of odd-even transposition sort?	O(N log N)	O(N)	O(log N)	$O(N^2)$	**4**
73						
74	Shell sort is an improvement on	Quick Sort	Bubble Sort	Insertion sort	Selection Sort	**3**
75						
76	In parallel Quick Sort Pivot is sent to processes by	Broadcast	Multicast	Selective Multicast	Unicast	**1**
77						
78	In parallel Quick Sort each process divides the unsorted list into	n Lists	2 Lists	4 Lists	n-1 Lists	**2**
79						
80	Time Complexity of DFS is? (V – number of vertices, E – number of edges)	O(V + E)	O(V)	O(E)	O(V*E)	**1**
81						
82	A person wants to visit some places. He starts from a vertex and then wants to visit every vertex till it finishes from one vertex, backtracks and then explore other vertex from same vertex. What algorithm he should use?	BFS	DFS	Prim's	Kruskal's	**2**
83						
84	Given an array of n elements and p processes, in the message-passing version of the parallel quicksort, each process stores ---------elements of array	n*p	n-p	p/n	n/p	**4**
85						
86	In parallel quick sort Pivot selecton strategy is crucial for	Maintaing load balance	Maintaining uniform distribution of elements in process groups	Effective Pivot selection in next level	all of the above	**4**
87						

88	In execution of the hypercube formulation of quicksort for d = 3, split along ----------dimention to partition sequence into two big blocks, one greater than pivot and other smaller than pivot as shown in diagram	first	scond	third	None of above	**3**
89						
90	Which Parallel formulation of Quick sort is possible	Shared-Address-Space Parallel Formulation	Message Passing formulation	Hypercube Formulation	All of the above	**4**
91						
92	Which formulation of Dijkstra's algorithm exploits more parallelism	source-partitioned formulation	source-parallel formulation	Partitioned-Parallel Formulation	All of above	**2**
93						
94	In Dijkstra's all pair shortest path each process compute the single-source shortest paths for all vertices assigned to it in SOURCE PARTITIONED FORMULATION	TRUE	FALSE			**1**
95						
96	A complete graph is a graph in which each pair of vertices is adjacent	TRUE	FALSE			**1**
97						
98	The space required to store the adjacency matrix of a graph with n vertices is	in order of n	in order of n log n	in order of n squared	in order of n/2	**3**
99						
100	Graph can be represented by	Identity Matrix	Adjacency Matrix	Sprse list	Sparse matrix	**2**
101						
102	to solve the all-pairs shortest paths problem which algorithm/s is/are used a) Floyd's algorithm b) Dijkstra's single-source shortest paths c) Prim's Algorithm d) Kruskal's Algorithm	a) and c)	a) and b)	b) and c)	c) and d)	**2**

103						
104	Simple backtracking is a depth-first search method that terminates upon finding the first solution.	TRUE	FALSE			**1**
105						
106	Best-first search (BFS) algorithms can search both graphs and trees.	TRUE	FALSE			**1**
107						
108	A* algorithm is a	BFS algorithm	DFS Algorithm	Prim's Algorithm	Kruskal's Algorithm	**1**
109						
110	identify Load-Balancing Scheme/s	Asynchronous Round Robin	Global Round Robin	Random Polling	All above methods	**4**
111						
112	important component of best-first search (BFS) algorithms is	Open List	Closed List	Node List	Mode List	**1**
113	**Question**	**a**	**b**	**c**	**d**	**Ans**
114	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
115	The kernel code is dentified by the _____qualifier with void return type	_host_	__global__	_device_	void	**b**
116	The kernel code is only callable by the host	TRUE	FALSE			**a**
117	The kernel code is executable on the device and host	TRUE	FALSE			**b**
118	Calling a kernel is typically referred to as _____.	kernel thread	kernel initialization	kernel termination	kernel invocation	**d**
119	Host codes in a CUDA application can Initialize a device	TRUE	FALSE			**a**

120	Host codes in a CUDA application can Allocate GPU memory	TRUE	FALSE			**a**
121	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
122	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
123	The kernel code is dentified by the _____qualifier with void return type	_host_	__global__	_device_	void	**b**
124	Host codes in a CUDA application can not Invoke kernels	TRUE	FALSE			**b**
125	CUDA offers the Chevron Syntax to configure and execute a kernel.	TRUE	FALSE			**a**
126	the BlockPerGrid and ThreadPerBlock parameters are related to the _____ model supported by CUDA.	host	kernel	thread abstractio n	none of above	**c**
127	_____ is Callable from the device only	_host_	__global__	_device_	none of above	**c**
128	_____ is Callable from the host	_host_	__global__	_device_	none of above	**b**
129	_____ is Callable from the host	_host_	__global__	_device_	none of above	**a**
130	CUDA supports _____ in which code in a single thread is executed by all other threads.	tread division	tread termination	thread abstraction	none of above	**c**
131	In CUDA, a single invoked kernel is referred to as a _____.	block	tread	grid	none of above	**c**
132	A grid is comprised of _____ of threads.	block	bunch	host	none of above	**a**
133	A block is comprised of multiple _____.	treads	bunch	host	none of above	**a**
134	a solution of the problem in representing the parallelismin algorithm is	CUD	PTA	CDA	CUDA	**d**
135	_____ is Callable from the host	_host_	__global__	_device_	none of above	**b**
13	_____ is Callable from the host	_host_	__global__	_device_	none of above	**a**

6						
137	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
138	The kernel code is dentified by the _____qualifier with void return type	_host_	__global__	_device_	void	**b**
139	Host codes in a CUDA application can not Reset a device	TRUE	FALSE			**b**
140	Host codes in a CUDA application can not Invoke kernels	TRUE	FALSE			**b**
141	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
142	Calling a kernel is typically referred to as _____.	kernel thread	kernel initialization	kernel termination	kernel invocation	**d**
143	In CUDA, a single invoked kernel is referred to as a _____.	block	tread	grid	none of above	**c**
144	A grid is comprised of _____ of threads.	block	bunch	host	none of above	**a**
145	A block is comprised of multiple _____.	treads	bunch	host	none of above	**a**
146	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
147	_____ is Callable from the host	_host_	__global__	_device_	none of above	**a**
148	In CUDA, a single invoked kernel is referred to as a _____.	block	tread	grid	none of above	**c**
149	the BlockPerGrid and ThreadPerBlock parameters are related to the _____ model supported by CUDA.	host	kernel	thread abstraction	none of above	**c**
150	Host codes in a CUDA application can Transfer data to and from the device	TRUE	FALSE			**a**
151	Host codes in a CUDA application can not Deallocate memory on the GPU	TRUE	FALSE			**b**
152	Host codes in a CUDA application can not Reset a device	TRUE	FALSE			**b**

153	Calling a kernel is typically referred to as _____.	kernel thread	kernel initialization	kernel termination	kernel invocation	**d**

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Class : BE Computer Div: A + B Subject : High Performance Computing
Academic Year : 2020-21 Sem : I Exam Date: 23/07/2020

Q. No.	*Question Description*	*Options*	*Correct Answer*	*Marks*	*CO*	*PO*	*PSO*	*BTL*
1	Select different aspects of parallelism	A. data intensive applications utilize high aggregate throughput B. server applications utilize high aggregate network bandwidth C. scientific applications typically utilize high processing and memory system performance D. all of the above	**D**	**2**	**1**	**1**	**3**	**4**
2	Select correct answer: DRAM access times have only improved at the rate of roughly ____% per year over this interval.	A. 10 B. 20 C. 40 D. 50	**A**	**2**	**1**	**1**	**3**	**4**
3	Justify, why to use parallel computing?	A. Real world is massively parallel B. Save time and/or time C. Solve larger / more complex problems D. Provide concurrency E. All of the above	**E**	**2**	**1**	**3**	**3**	**5**
4	Analyze, if the second instruction has data dependencies with the first, but the third instruction does not, the first	A. In-order B. Out-of-order C. Both of the above D. None of the above	**B**	**2**	**1**	**3**	**3**	**4**

	and third instructions can be co-scheduled. Which type if this issue is?							
5	Select the parameters which captures Memory system performance	A. Latency B. Bandwidth C. Both of the above D. None of the above	**C**	**2**	**1**	**3**	**3**	**4**
6	Consider the example of a fire-hose. If the water comes out of the hose five seconds after the hydrant is turned on. Once the water starts flowing, if the hydrant delivers water at the rate of 15 gallons/second. Analyze the bandwidth and latency.	A. Bandwidth: 5 gallons/second and Latency: 15 seconds B. Bandwidth: 5*15 gallons/second and Latency: 15 seconds C. Bandwidth: 15 gallons/second and Latency: 5 seconds D. Bandwidth: 3 gallons/second and Latency: 5 seconds	**C**	**2**	**1**	**4**	**3**	**5**
7	Select alternate approaches for Hiding Memory Latency	A. Prefeching B. Multithreading C. spatial locality D. all of the above	**D**	**2**	**1**	**3**	**3**	**4**
8	Select which clause in OpenMP is similar to the private, except values of variables are initialized to corresponding values before the	A. Private B. Firstprivate C. Shared D. All of the above	**B**	**2**	**1**	**5**	**3**	**4**

	parallel directive.							
9	The time which includes all overheads that are determined by the length of the message like bandwidth of links, error checking and correction, etc. is called as	A. Startup time (ts) B. Per-hop time (th) C. Per-word transfer time (tw) D. All of the above	**C**	**2**	**1**	**1**	**3**	**1**
10	Select in which routing technique, Message is divided into packets?	A. Store-and-forward routing B. Packet routing C. cut-through-routing D. in both 2 and 3	**D**	**2**	**1**	**3**	**3**	**4**
11	Which of the following is an efficient method of cache updating?	A. Snoopy writes B. Write through C. Write within D. Buffered write	**A**	**2**	**1**	**1**	**3**	**1**
12	Select which protocol is used for maintaining coherence of multiple processors?	A. Data coherence protocols B. Commit coherence protocols C. Recurrence D. Cache coherence protocols	**D**	**2**	**1**	**3**	**3**	**4**
13	From inter-processor communication, the misses arises are often called	A. Coherence misses B. Commit misses C. Parallel processing D. Hit rate	**A**	**2**	**1**	**1**	**3**	**1**
14	As per Flynn's Classification, where Parallel processing may occur?	A. in the instruction stream B. in the data stream C. both of the above D. none of the above	**C**	**2**	**1**	**1**	**3**	**1**

15	Which of the following projects of Blue Gene is not in development?	A. Blue Gene / L B. Blue Gene / M C. Blue Gene / P D. Blue Gene / Q	**B**	**2**	**1**	**1**	**3**	**1**

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Unit Test II Date: 26/08/2020

Class : BE Computer Div: A + B Subject : High Performance Computing
Academic Year : 2020-21 Sem : I Exam Date: 26/08/2020

Q. No.	*Question Description*	*Options 28*	*Correct Answer*	*Marks*	*CO*	*PO*	*PSO*	*BTL*
1	Task interaction graphs represent _____ dependencies, whereas task dependency graphs represent _____ dependencies.	A. control, data B. task, data C. process, control D. data, control	**D**	**2**	**2**	**1**	**3**	**4**
2	Select correct answer. Which graph represents tasks as nodes and their interactions/data exchange as edges?	A. task dependency graph B. process dependency graph C. process interaction graph D. task interaction graph	**D**	**2**	**2**	**1**	**3**	**4**
3	The average number of tasks that can be processed in parallel over the execution of the program is called as _____	A. average degree of concurrency B. degree of concurrency C. critical path length D. maximum concurrency	**A**	**2**	**2**	**1**	**3**	**4**
4	The number of tasks that can be executed in	A. average concurrency B. degree of concurrency C. critical path length	**B**	**2**	**2**	**1**	**3**	**4**

	parallel is the _____ of a decomposition.	D. maximum concurrency						
5	A decomposition can be illustrated in the form of a directed graph with nodes corresponding to tasks and edges indicating that the result of one task is required for processing the next. Such graph is called as _____	A. process dependency graph B. task dependency graph C. task interaction graph D. process interaction graph	**B**	**2**	**2**	**1**	**3**	**4**
6	In which case, the owner computes rule implies that the output is computed by the process to which the output data is assigned?	A. input data decomposition B. output data decomposition C. Both of the above D. None of the above	**B**	**2**	**2**	**4**	**3**	**5**
7	Select relevant task characteristics from the options given below:	A. Task generation B. Task sizes C. Size of data associated with tasks D. All of the above	**D**	**2**	**2**	**1**	**3**	**4**
8	A classic example of game playing - each 15 puzzle board is the example of _____	A. Static Task Generation B. Dynamic Task Generation C. None of the above D. All of the above	**B**	**2**	**2**	**3**	**3**	**4**
9	Analyze task interaction pattern	A. static regular interaction pattern B. static irregular interaction pattern	**B**	**2**	**2**	**3**	**3**	**5**

	of the multiplication of a sparse matrix with a vector.	C. dynamic regular interaction pattern D. dynamic irregular interaction pattern						
10	Select the methods for containing Interaction Overheads.	A. Maximize data locality B. Minimize volume of data exchange C. Minimize frequency of interactions D. Minimize contention and hot-spots E. All of the above	**E**	**2**	**2**	**3**	**3**	**4**
11	Which model is equally suitable to shared-address-space or message-passing paradigms, since the interaction is naturally two ways.	A. Work pool model B. Master slave model C. Data parallel model D. Producer consumer or pipeline model	**B**	**2**	**2**	**1**	**3**	**4**
12	In which type of the model, tasks are dynamically assigned to the processes for balancing the load?	A. Work pool model B. Master slave model C. Data parallel model D. Producer consumer or pipeline model	**A**	**2**	**2**	**3**	**3**	**4**
13	Select the appropriate stage of GPU Pipeline which receives commands from CPU and also pulls geometry information from system memory.	A. pixel processing B. vertex processing C. memory interface D. host interface	**D**	**2**	**2**	**12**	**3**	**4**
14	Select the hardware specifications	A. GPU Clock Speed B. Size of memory bus C. Amount of available memory	**E**	**2**	**2**	**12**	**3**	**1**

	which most affect the GPU cards speed.	D. Memory Clock Rate E. All of the above						
15	Select the appropriate stage of GPU Pipeline where computations include texture mapping and math operations.	A. pixel processing B. vertex processing C. memory interface D. host interface	**A**	**2**	**2**	**12**	**3**	**1**

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Unit Test III Date: 14/10/2020

Class : BE Computer Div: A Subject : High Performance Computing
Academic Year : 2020-21 Sem : I Exam Date: 14/10/2020

Q. No.	*Question Description*	*Options 28*	*Correct Answer*	*Marks*	*CO*	*PO*	*PSO*	*BTL*
1	In all-to-one reduction, data items must be combined piece-wise and the result made available at a _____ processor.	A. First B. Last C. Target D. N-1	**C**	**2**	**3**	**1**	**3**	**4**
2	Analyze the Cost of Scatter and Gather .	A. T=tw log p + ts m (p-1) B. T=ts log p + tw m (p-1) C. T=ts log p - tw m (p-1) D. T=tw log p - ts m (p-1)	**B**	**2**	**3**	**4**	**3**	**4**
3	All-to-all personalized communication is also known as _____.	A. partial exchange B. total exchange C. both of the above D. none of the above	**B**	**2**	**3**	**1**	**3**	**1**
4	All-to-all personalized communication is performed independently in each row with clustered messages of size _____ on a mesh.	A. m B. p C. m√p D. p√m	**C**	**2**	**3**	**1**	**3**	**4**
5	In All-to-All Personalized Communication on a Ring, the size of the message reduces by _____ at each step	A. m B. p C. m-1 D. p-1	**A**	**2**	**3**	**1**	**3**	**1**

6	All-to-All Broadcast and Reduction algorithm on a Ring terminates in _____steps.	A. p B. p+1 C. p-1 D. p*p	**C**	**2**	**3**	**1**	**3**	**1**
7	In All-to-all Broadcast on a Mesh, operation performs in which sequence?	A. rowwise, rowwise B. rowwise, columnwise C. columnwise, rowwise D. columnwise, columnwise	**B**	**2**	**3**	**1**	**3**	**3**
8	In the _____ operation, a single node sends a unique message of size m to every other node.	A. Scatter B. gather	**A**	**2**	**3**	**3**	**3**	**1**
9	In the _____ operation, a single node collects a unique message from each node.	A. Scatter B. gather	**B**	**2**	**3**	**3**	**3**	**1**
10	Messages get smaller in _____and stay constant in _____.	A. broadcast, gather B. gather, broadcast C. scatter , broadcast D. scatter, gather	**C**	**2**	**3**	**1**	**3**	**4**
11	The time taken by all-to-all broadcast on a ring is _____.	A. T= $2t_s(\sqrt{p} - 1) + t_w m(p-1)$ B. T= $(t_s + t_w m)(p-1)$ C. T= $t_s \log_p + t_w m(p-1)$ D. T= $2t_s(\sqrt{p} - 1) - t_w m(p-1)$	**B**	**2**	**3**	**4**	**3**	**4**
12	The time taken by all-to-all broadcast on a mesh is _____.	A. T= $2t_s(\sqrt{p} - 1) + t_w m(p-1)$ B. T= $(t_s + t_w m)(p-1)$ C. T= $t_s \log_p + t_w m(p-1)$ D. T= $2t_s(\sqrt{p} - 1) - t_w m(p-1)$	**A**	**2**	**3**	**4**	**3**	**4**
13	The time taken by all-to-all broadcast on a hypercube is _____.	A. T= $2t_s(\sqrt{p} - 1) + t_w m(p-1)$ B. T= $(t_s + t_w m)(p-1)$ C. T= $t_s \log_p + t_w m(p-1)$ D. T= $2t_s(\sqrt{p} - 1) - t_w m(p-1)$	**C**	**2**	**3**	**4**	**3**	**4**
14	_____ is a special permutation in which	A. Left shift B. Right shift	**C**	**2**	**3**	**1**	**3**	**1**

	node *i* sends a data packet to node *(i + q)* mod *p* in a *p*-node ensemble *(0 ≤ q ≤ p)*.	C. Circular shift D. Linear shift						
15	The prefix-sum operation can be implemented using the _____kernel	A. all-to-all reduction B. all-to-all broadcast C. one-to-all broadcast D. all-to-one broadcast	**B**	**2**	**3**	**1**	**3**	**1**

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Unit Test IV Date: 09/11/2020

Class : BE Computer Div: A Subject : High Performance Computing
Academic Year : 2020-21 Sem : I Exam Date: 11/11/2020

Q. No.	*Question Description*	*Options 28*	*Correct Answer*	*Marks*	*CO*	*PO*	*PSO*	*BTL*
1	Select the parameters on which the parallel runtime of a program depends.	A. Input size B. Number of processors C. Communication parameters of the machine D. All of the above	**D**	**2**	**4**	**1**	**3**	**4**
2	The time that elapses from the moment the first processor starts to the moment the last processor finishes execution is called as _____.	A. Serial runtime B. Parallel runtime C. Overhead runtime D. Excess runtime	**B**	**2**	**4**	**4**	**3**	**4**
3	Select how the overhead function (T_o) is calculated.	A. $T_o = T_P - T_S$ B. $T_o = p*n\ T_P - T_S$ C. $T_o = p\ T_P - T_S$ D. $T_o = T_P - pT_S$	**C**	**2**	**4**	**1**	**3**	**1**
4	What is is the ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with ***p*** identical processing elements?	A. Efficiency B. Overall time C. Speedup D. Scaleup	**C**	**2**	**4**	**1**	**3**	**4**
5	The parallel time for odd-even sort (efficient	A. 3.75 B. 3.5	**B**	**2**	**4**	**1**	**3**	**1**

	parallelization of bubble sort) is 50 seconds. The serial time for bubblesort is 175 seconds. Evaluate the speedup of bubble sort.	C. 0.33 D. 0.26						
6	Consider the problem of adding ***n*** numbers by using ***n*** processing elements. The serial time taken is Θ (***n***) and parallel time is Θ (**log *n***). Evaluate the efficiency.	A. E = Θ (***n* / log *n***) B. E = Θ (***n* log *n***) C. E = Θ (**log *n* / *n***) D. E = Θ (**1 / log *n***)	**D**	**2**	**4**	**1**	**3**	**1**
7	What will be the efficiency of cost optimal parallel systems?	A. ***E*** = *O*(n). B. ***E*** = *O*(1). C. ***E*** = *O*(p). D. ***E*** = *O*(n log n).	**B**	**2**	**4**	**1**	**3**	**3**
8	Which law states that the maximum speedup of a parallel program is limited by the sequential fraction of the initial sequential program?	A. Amdahl's Law B. Flynn's Law C. Moore's Law D. Van Neumann's Law	**A**	**2**	**4**	**3**	**3**	**1**
9	Arrange the steps for the Matrix-Vector 2-D partitioning: i) result vector is computed by performing an all-to-one reduction along the columns. ii) Alignment of the vector *x* along the principal diagonal of the matrix. iii) Copy the vector	A. i, ii, iii B. ii, iii, i C. iii, i, ii D. ii, i, iii	**B**	**2**	**4**	**3**	**3**	**1**

	elements from each diagonal process to all the processes in the corresponding column using *n* simultaneous broadcasts among all processors in the column.							
10	Arrange the communication sequence in Matrix-Vector 2-D partitioning: i) all-to-one reduction in each row ii) one-to-all broadcast of each vector element among the *n* processes of each column iii) one-to-one communication to align the vector along the main diagonal	A. i, ii, iii B. ii, iii, i C. iii, ii, i D. ii, i, iii	**C**	**2**	**4**	**1**	**3**	**4**
11	Parallel time in Rowwise 1-D Partitioning of Matrix-Vector Multiplication where p=n is ____.	A. $\Theta(1)$ B. $\Theta(n \log n)$ C. $\Theta(n^2)$ D. $\Theta(n)$	**D**	**2**	**4**	**4**	**3**	**4**
12	What are the sources of overhead in parallel programs?	A. Interprocess interaction B. Idling C. Excess computation D. All of the above	**D**	**2**	**4**	**4**	**3**	**4**
13	What are the performance metrics of parallel systems?	A. Execution time B. Total parallel overhead C. Speedup	**E**	**2**	**4**	**4**	**3**	**4**

		D. Efficiency E. All of the above						
14	The isoefficiency function determines the ease with which a parallel system can maintain a constant efficiency. True of false?	A. True B. False	**A**	**2**	**4**	**1**	**3**	**1**
15	Which matrix-matrix multiplication algorithm uses a 3-D partitioning?	A. Cannon's algorithm B. DNS algorithm C. Both of the above D. None of the above	**B**	**2**	**4**	**1**	**3**	**1**

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Prelim Exam Date: 29/12/2020

Class : BE Computer Div: A & B Subject : High Performance Computing
Academic Year : 2020-21 Sem : I Exam Date: 31/12/2020

Q. No.	*Question Description*	*Options*	*Correct Answer*	*Marks*	*CO*	*PO*	*PSO*	*BTL*
1	Which of the following is the type of parallelism?	**a. Bit level parallelism** **b. Instruction level parallelism** **c. Loop level parallelism** **d. All of the above**	**D**	**1**	1	**1,12**	**1**	**2**
2	Which of the parallelism is used by VLIW	**a. Bit level parallelism** **b. Instruction level parallelism** **c. Loop level parallelism** **d. Task level Parallelism**	**B**	1	1	**1,12**	**1**	**2**
3	Tendency of a software process to access information items whose addresses are near one another known as	**a. Spatial Locality** **b. Temporal locality** **c. Permanent Locality** **d. Sequential Locality**	**a**	1	1	**1**	**1**	**1**
4	Parallel Computers are classified based on Flynn's taxonomy which among the following options does not come under this	**a. SISD** **b. SIMD** **c. MIMD** **d. SIPD**	**d**	1	1	**1,12**	**1**	**1**
5	Which among the following is the popular multistage network	**a. Hypercube** **b. Omega**	**b**	1	1	**1**	**1**	**2**

		c. Gamma **d. K-D Mesh**						
6	The multicore architecture that consists of dedicated application specific processor cores that would target the issue of running variety of applications to be executed on a computer.	**a. Homogeneous core architecture.** **b. Heterogeneous core architecture.** **c. Polaris core architecture** **d. None of the above**	**b**	1	1	**1**	**1**	**3**
7	Decomposition of computation into a small number of large task is	**a. Fine grained granularity** **b. course grained granularity** **c. coarse grained granularity** **d. task grained granularity**	**C**	1	2	**1**	**3**	**1**
8	Which among the following is the type of decomposition	**a. Data-decomposition** **b. Hybrid decomposition** **c. Speculative decomposition** **d. All of the above**	**D**	1	2	**1,12**	**3**	**2**
9	The 15-puzzle problem uses which type of decomposition	**a. Data decomposition** **b. Exploratory decomposition** **c. Speculative decomposition** **d. Recursive decomposition**	**B**	1	2	**1,4,12**	**3**	**2**

10	An interaction pattern is considered to be _____if it has some structure that can be exploited for efficient implementation	**a. Structured interaction** **b. unstructured interaction** **c. Regular interaction** **d. Irregular interaction**	**C**	1	2	**1,12**	**3**	**2**
11	The mapping in which is tasks are distributed to processes during execution is called as___	**a. Dynamic mapping** **b. Static mapping** **c. Pre-execution mapping** **d. In-process mapping**	**a**	1	2	**1**	**1**	**1**
12	The parallel algorithm model in which mapping of tasks is done dynamically where pointer to tasks is stored in physically shared list/priority queue/hash table/tree is called	**a. The data parallel model** **b. Producer consumer model** **c. The task graph model** **d. Work pool model**	**d**	1	2	**1,2**	**1**	**2**
13	The world's first GPU is marketed by NVDIA in 1999 is	**a. GEForce 356** **b. GEForce 256** **c. GEForce 3800** **d. GEForce 956**	**B**	1	6	**5**	**3**	**1**
14	The operation in which data from all processes are combined at a single destination process is	**a. All to one reduction** **b. All to all reduction** **c. one to all reduction** **d. None of the above**	**A**	1	3	**1**	**1**	**2**
15	In scatter operation a single node sends a unique message to every node is also called as	a. One-to-one personalized communication b. One-to-all broadcast	**C**	1	3	**1**	**1**	**2**

		communication c. One-to-all personalized communication **d.** all-to-all personalized communication						
16	Single port communication node can communicate on all the channels connected to it and provides apparent speedup	a. True **b.** False	**B**	1	3	**1**	**1**	**1**
17	Symmetric multiprocessors architecture are sometimes known as	**a. Uniform memory access** **b. Static memory access** **c. Variable memory access** **d. All of the above**	**A**	1	3	**1**	**1**	**1**
18	Heuristic is way of trying	**a. To discover something or an idea embedded in a program** **b. To search and measure how far a node in a search tree seems to be from a goal** **c. To compare two nodes in a search tree to see if one is better than another** **d. All of the mentioned**	**a**	1	4	**1,2**	**3**	**2**
19	A * algorithm is based on	**a. Breadth-First search** **b. Depth-first Search** **c. Best first search** **d. Hill climbing**	**C**	1	5	**1,2**	**1**	**2**

20	Best – First search can be implemented using the following data structure	**a. Queue** **b. Stack** **c. Priority Queue** **d. Circular Queue**	**C**	1	5	**1,2**	**1**	**1**
21	_____is a measure of the fraction of time for which a processing element is usefully employed	**a. Scalability** **b. Efficiency** **c. Speedup** **d. isoefficiency**	**B**	1	5	**1,2**	**1**	**2**
22	The ___of a parallel system is a measure of its capacity to increase speedup in proportion to the number of processing elements	**A. speedup** **B. Cost** **C. Efficiency** **D. Scalability**	**D**	1	3	**1,12**	**1**	**2**
23	___helps us determine the best algorithm/architecture combination for a particular problem without explicitly analyzing all possible combinations under all possible co	**a. Isoefficiency Metric of scalability** **b. Efficiency matric of scalability** **c. Cost metric of scalability** **d. None of the above**	**A**	1	3	**1,3**	**1**	**2**
24	It is defined as a ratio of the time taken to solve a problem on a single processing element to the time computer with p identical processing elements	**a. Total parallel overhead** **b. Efficiency** **c. Cost** **d. speedup**	**D**	1	3	**1,12**	**1**	**1**
25	In Practice a speedup greater than p is sometimes observed. It is called as_____	**a. scalability effect** **b. superscalar effect**	**C**	1	3	**1,2,12**	**1**	**1**

		c. super linearity effect **d. speedup effect**						
26	Odd-even transposition sort is not cost -optimal, because time product is	**a. theta(n^2)** **b. theta(n^logn)** **c. O(n^3)** **d. O(n+logn)**	**A**	1	5	**1,2, 5**	**3**	**3**
27	The quicksort algorithm, which has an average complexity of	**a. O(n^3)** **b. O(n+logn)** **c. theta(n^logn)** **d. theta(n^2)**	**C**	1	5	**1,2, 5**	**1**	**3**
28	Parallel code executes in many concurrent Device (GPU) threads across multiple parallel processing elements, called	**a. Synchronising multiprocessor** **b. Streaming multiprocessor** **c. Scalable multiprocessor** **d. Summative multiprocessor**	**B**	1	6	**1,2, 12**	**1**	**2**
29	____partitions the vertices among different processes and has each process compute the single-source shortest path for all vertices assigned to it	**a. Source parallel formulation** **b. Single partitioned formulation** **c. Source partitioned formulation** **d. Shortest path partitioned formulation**	**C**	1	5	**1,2, 12**	**3**	**2**
30	A processor, assigned with a thread block that executes	**a. Multithreaded DIMS**	**B**	1	2	**1**	**1**	**1**

	code, which we usually call a	**processor** **b. Multithreaded SIMD processor** **c. Multithreaded queue** **d. Multithreaded stack**						
31	Processor of system, which can read/write GPU memory, is known as	**a. Server** **b. Kernel** **c. Guest** **d. Host**	**D**	1	6	**1**	**1**	**1**
32	CUDA stands for	**a. Compute uniform device architecture** **b. Computing universal device architecture** **c. Computer unicode device architecture** **d. Compute unified device architecture**	**D**	1	6	**1,2, 5**	**2**	**1**
33	The device that are being used primarily for database, file server and mostly for web application are known as	**a. Servers** **b. Desktops** **c. Tablets** **d. Supercomputers**	**A**	1	1	**1**	**1**	**1**
34	GPU are designed for running a large number of complex tasks	**a. True** **b. False**	**B**	1	6	**1,2**	**1**	**1**
35	The parallel algorithm design contains a number of processes where one process may send the identical data to all other processes is called as	a. All to one broadcast b. All to all broadcast c. One to all broadcast **d.** None of these	**C**	1	3	**1**	**1**	**2**
36	The efficient utilization can be done by devising a	a. Recursive doubling b. Recursive		1	3	**1**	**1**	**1**

	broadcasting algorithm with the method known as	c. Scatter and Gather **d.** None of these	a					
37	The balanced tree is mapped neutrally from the hypercube algorithm for one-to-all broadcast where intermediate are the _____and each leaf nodes are the _____	a. switching nodes, processing nodes **b.** processing nodes, switching nodes	a	1	3	**1,12**	**1**	**2**
38	Finding prefix-sum operation is also called as scan operation	a. True **b.** False	a	1	3	**1,12**	**1**	**1**
39	All to all personalized communication is also called as	a. Scan operation b. Total exchange method c. None of these	B	1	3	**1,12**	**1**	**2**
40	On which network broadcast and reduction operations performed in two steps: 1. Operations along with row 2. Operations along with column	a. Ring b. Hypercube c. Linear array **d.** Mesh	d	1	3	**1,12**	**1**	**2**
41	Gather operation is also called as all to one reduction	a. True **b.** False	b	1	3	**1,8**	**1**	**1**
42	The method which is used in various parallel algorithm like Fourier transform, matrix transpose, some parallel database join operations is called as	a. All-to-all personalized communication b. All-to-all Broadcast c. Total exchange method d. Both a & c	d	1	3	**1,12**	**1**	**1**
43	Consider a sequence in which numbers are originally arranged<2,4,5,6,1>, then sequence of Prefix sum will be	a. <2,6,11,17,18 > b. <6,15,21,22 > c. None of these	a	1	3	**4**	**2**	**3**
44	Select the parameters on which the parallel runtime of a program depends.	A. nput size B. umber of processors C.	**D**	**1**	**4**	**1**	**3**	**4**

		ommunication parameters of the machine D. ll of the above						
45	The time that elapses from the moment the first processor starts to the moment the last processor finishes execution is called as _____.	A. Serial runtime B. Parallel runtime C. Overhead runtime D. Excess runtime	**B**	1	**4**	**4**	**3**	**4**
46	Select how the overhead function (T_o) is calculated.	A. $T_o = T_P - T_S$ B. $T_o = p*n\ T_P - T_S$ C. $T_o = p\ T_P - T_S$ D. $T_o = T_P - pT_S$	**C**	**1**	**4**	**1**	**3**	**1**
47	The parallel time for odd-even sort (efficient parallelization of bubble sort) is 50 seconds. The serial time for bubble sort is 175 seconds. Evaluate the speedup of bubble sort.	A. 3.75 B. 3.5 C. 0.33 D. 0.26	**B**	**1**	**4**	**1**	**3**	**1**
48	Consider the problem of adding n numbers by using n processing elements. The serial time taken is $\Theta(n)$ and parallel time is $\Theta(\log n)$. Evaluate the efficiency.	A. $E = \Theta(n / \log n)$ B. $E = \Theta(n \log n)$ C. $E = \Theta(\log n / n)$ **D.** $E = \Theta(1 / \log n)$	**D**	**1**	**4**	**1**	**3**	**1**
49	What will be the efficiency of cost optimal parallel systems?	A. $E = O(n)$. B. $E = O(1)$.	**B**	**1**	**4**	**1**	**3**	**3**

		C. $E = O(p)$. **D.** $E = O(n \log n)$.						
50	Which law states that the maximum speedup of a parallel program is limited by the sequential fraction of the initial sequential program?	A. Amdahl's Law B. Flynn's Law C. Moore's Law **D.** Van Neumann's Law	**A**	**1**	**4**	**3**	**3**	**1**
51	Arrange the steps for the Matrix-Vector 2-D partitioning i) result vector is computed by performing an all-to-one reduction along the columns. ii)Alignment of the vector *x* along the principal diagonal of the matrix. iii)Copy the vector elements from each diagonal process to all the processes in the corresponding column using *n* simultaneous broadcasts among all processors in the column.	A. i, ii, iii B. ii, iii, i C. iii, i, ii D. ii, i, iii	**B**	**1**	**4**	**3**	**3**	**1**
52	Arrange the communication sequence in Matrix-Vector 2-D partitioning: i) all-to-one reduction in each row ii) one-to-all broadcast of each vector element among the *n* processes of each column iii) one-to-one	A. i, ii, iii B. ii, iii, i C. iii, ii, i D. ii, i, iii	**C**	**1**	**4**	**1**	**3**	**4**

	communication to align the vector along the main diagonal							
53	Parallel time in Rowwise 1-D Partitioning of Matrix-Vector Multiplication where p=n is ____.	A. $\Theta(1)$ B. $\Theta(n \log n)$ C. $\Theta(n^2)$ D. $\Theta(n)$	**D**	**1**	**4**	**4**	**3**	**4**
54	NVIDIA thought that 'unifying theme' of every forms of parallelism is the	**a. CDA thread** **b. PTA thread** **c. CUDA thread** **d. CUD thread**	**c**	1	6	1,2, 12	**1**	**2**
55	Thread being blocked altogether and being executed in sets of 32 threads, called a	**a. Thread block** **b. 32 thread** **c. 32 block** **d. Unit block**	**a**	1	6	**1,2, 12**	**1**	**2**
56	Length of a vector operation in a real program is often	**a. Known** **b. Unknown** **c. Visible** **d. Invisible**	**a**	1	6	**1,2, 12, 6**	**1**	**3**
57	A code, known as grid which runs on a GPU consisting of a set of	**a. 32 thread** **b. Unit block** **c. 32 block** **d. Thread block**	**d**	1	6	**1,1 2,5**	**1**	**1**
58	NVDIA unvield the industrys first directX 10 GPU is___	**a. GTX 1050**	**b**	1	6	**1,1 2,5**	**1**	**1**

		b. GeForce 8800 GTX **c. GeForce GTX 1080** **d. GTX 1060**				**1**		
59	The number of instructions being executed defines the	**a. Instruction count** **b. Hit time** **c. Clock rate** **d. All above**	**A**	1	2	**1**	**1**	**1**
60	In CUDA Programming kernel is launch using which pair of brackets?	**a. <<<>>>** **b. {{{}}}** **c. ((()))** **d. [[[]]]**	**d**	1	6	**1,2, 12, 5**	**3**	**2**
61	In CUDA programming the transfer of data between host and device special function used is ___	**a. Memcopy()** **b. Memorycpy()** **c. cudaMemcopy()** **d. cudaMemorycpy()**	**c**	1	6	**1,2, 12, 5**	**1**	**1**
62	Streaming multiprocessor in CUDA, divides the thread in a block is called as___	**a. WRAP** **b. Packet** **c. Grid** **d. Thread block**	**a**	1	6	**1,1 2,5**	**1**	**2**
63	Sources of overheads in parallel program are	**a. Idling** **b. Interprocess communication** **c. Excess computation** **d. All of the above**	**d**	1	3	**1,1 2,2**	**1**	**2**
64	What are the sources of overhead in parallel	A. Interprocess interaction	**D**	**1**	**4**	**4**	**3**	**4**

	programs?	B. Idling C. Excess computation D. All of the above						
65	What are the performance metrics of parallel systems?	A. Execution time B. Total parallel overhead C. Speedup D. Efficiency E. All of the above	**E**	1	**4**	**4**	**3**	**4**
66	The isoefficiency function determines the ease with which a parallel system can maintain a constant efficiency. True of false?	A. True B. False	**A**	**1**	**4**	**1**	**3**	**1**
67	Which matrix-matrix multiplication algorithm uses a 3-D partitioning?	A. Cannon's algorithm B. DNS algorithm C. Both of the above D. None of the above	**B**	**1**	**4**	**1**	**3**	**1**
68	A solution representing a parallelism in an algorithm is	**A. CDA** **B. PTA** **C. CUDA** **D. CUD**	**c**	1	6	**1**	**1**	**2**
69	Blocking optimization is used to improve temporal locality, for reduce	**A. Hit miss** **B. Misses**	**B**	1	5	**1**	**1**	**2**

		C. Hit rate **D. Cache misses**						
70	Data are allocated to disks in the RAID at the	**A. Block level** **B. Cache level** **C. Low level** **D. High level**	**A**	1	6	**1**	**1**	**1**
71	In CUDA C programming serial code is executed by__and parallel code is executed by__	**a. CPU, CPU** **b. GPU,CPU** **c. GPU,GPU** **d. CPU,GPU**	**d**	1	6	**1,2, 12, 5**	**2**	**2**
72	Kernel function is qualified by the qualifier	**a. __local__** **b. __universal__** **c. __global__** **d. A or C**	**C**	1	6	**1,3**	**1**	**1**

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UNIT ONE	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
1	A pipeline is like	an automobile assembly line	house pipeline	both a and b	a gas line	**a**
2	Data hazards occur when	Greater performance loss	Pipeline changes the order of read/ write access to operands	Some functional unit is not fully pipelined	Machine size is limited	**b**
3	Systems that do not have parallel processing capabilities are	SISD	SIMD	MIMD	All of the above	**a**
4	How does the number of transistors per chip increase according to Moore ´s law?	Quadratically	Linearly	Cubicly	Exponentially	**d**
5	Parallel processing may occur	in the instruction stream	B. in the data stream	both[A] and [B]	none of the above	**c**
6	Execution of several activities at the same time.	processing	parallel processing	serial processing	multitasking	**b**
7	Cache memory works on the principle of	Locality of data	Locality of memory	Locality of reference	Locality of reference & memory	**c**

8	SIMD represents an organization that _____.	refers to a computer system capable of processing several programs at the same time.	represents organization of single computer containing a control unit, processor unit and a memory unit.	includes many processing units under the supervision of a common control unit	none of the above.	**c**
9	A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ .	Super-scaling	Pipe-lining	Parallel Computation	None of these	**b**
10	General MIMD configuration usually called	a multiprocessor	a vector processor	array processor	none of the above.	**a**
11	A Von Neumann computer uses which one of the following?	SISD	SIMD	MISD	MIMD.	**a**
12	MIMD stands for	Multiple instruction multiple data	Multiple instruction memory data	Memory instruction multiple data	Multiple information memory data	**a**
13	MIPS stands for:	Memory Instruction Per Second	Major Instruction Per Second	Main Information Per Second	Million Instruction Per Second	**d**
14	M.J. Flynn's parallel processing classification is based on:	Multiple Instructions	Multiple data	Both (a) and (b)	None of the above	**c**
15	VLIW stands for:	Vector Large Instruction Word	Very Long Instruction Word	Very Large Integrated Word	Very Low Integrated Word	**b**

16	The major disadvantage of pipeline is:	High cost individual dedicated	Initial setup time	If branch instruction is encountered the pipe has to be flushed	All of the above	**c**
17	A topology that involves Tokens.	Star	Ring	Bus	Daisy Chaining	**b**
18	multipoint topology is	bus	star	mesh	ring	**a**
19	In super-scalar mode, all the similar instructions are grouped and executed together.	TRUE	False			**a**
20	Which mechanism performs an analysis on the code to determine which data items may become unsafe for caching, and they mark those items accordingly?	Directory protocol	Snoopy protocol	Server based cache coherence	Compiler based cache coherence	**d**
21	How many processors can be organized in 5-dimensional binary hypercube system?	25	10	32	20	**c**
22	Multiprocessors are classified as _____.	SIMD	MIMD	SISD	MISD	**b**
23	Which of the following is not one of the interconnection structures?	Crossbar switch	Hypercube system	Single port memory	Time-shared common bus	**c**
24	Which combinational device is used in crossbar switch for selecting proper memory from multiple addresses?	Multiplexer	Decoder	Encoder	Demultiplexer	**a**

25	How many switch points are there in crossbar switch network that connects 9 processors to 6 memory modules?	50	63	60	54	**d**
26	In a three-cube structure, node 101 cannot communicate directly with node?	1	11	100	111	**b**
27	Which method is used as an alternative way of snooping-based coherence protocol?	Directory protocol	Memory protocol	Compiler based protocol	None of above	**a**
28	snoopy cache protocol are used in ----------based system	bus	mesh	star	hypercube	**a**
29	superscalar architecture contains ----------execution units for instruction execution	multiple	single	none of the above		**a**
30	time taken by header of a message between two directly connected nodes is called as----------	startup time	per hop time	per word transfer time	packaging time	**b**
31	the number of switch requirement for a network with n input and n output is ----------	n	n2	n3	n4	**b**
32	which of the following is not static network	bus	ring	mesh	crossbar switch	**d**
33	In super-scalar processors, _____ mode of execution is used.	In-order	Post order	Out of order	None of the mentioned	**c**
34	_____ have been developed specifically for pipelined systems.	Utility software	Speed up utilities	Optimizing compilers	None of the above	**c**

35	Which of the following is a combination of several processors on a single chip?	Multicore architecture	RISC architecture	CISC architecture	Subword parallelism	**a**
36	The important feature of the VLIW is	ILP	Cost effectiveness	performance	None of the mentioned	**a**
37	The parallel execution of operations in VLIW is done according to the schedule determined by	sk scheduler	Interpreter	Compiler	Encoder	**c**
38	The VLIW processors are much simpler as they do not require of	Computational register	Complex logic circuits	SSD slots	Scheduling hardware	**d**
39	The VLIW architecture follows ..... approach to achieve parallelism.	MISD	SISD	SIMD	MIMD	**d**
40	Which of the following is not a Pipeline Conflicts?	Timing Variations	Branching	Load Balancing	Data Dependency	**c**

UNIT TWO	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
1	Task dependency graph is ----------	directed	undirected	directed acyclic	undirected acyclic	**c**
2	In task dependency graph longest directed path between any pair of start and finish node is called as ----------	total work	critical path	task path	task length	**b**
3	which of the following is not a granularity type	course grain	large grain	medium grain	fine grain	**b**
4	which of the following is a an example of data decomposition	matrix multiplication	merge sort	quick sort	15 puzzal	**a**
5	which problems can be handled by recursive decomposition	backtracking	greedy method	divide and conquer problem	branch and bound	**c**
6	In this decomposition problem decomposition goes hand in hand with its execution	data decomposition	recursive decomposition	explorative decomposition	speculative decomposition	**c**
7	which of the following is not an example of explorative decomposition	n queens problem	15 puzzal problem	tic tac toe	quick sort	**d**
8	Topological sort can be applied to which of the following graphs?	a) Undirected Cyclic Graphs	b) Directed Cyclic Graphs	c) Undirected Acyclic Graphs	d) Directed Acyclic Graphs	**d**

9	In most of the cases, topological sort starts from a node which has _____	a) Maximum Degree	b) Minimum Degree	c) Any degree	d) Zero Degree	**d**
10	Which of the following is not an application of topological sorting?	a) Finding prerequisite of a task	b) Finding Deadlock in an Operating System	c) Finding Cycle in a graph	d) Ordered Statistics	**d**
11	In ----------task are defined before starting the execution of the algorithm	dynamic task	static task	regular task	one way task	**b**
12	which of the following is not the array distribution method of data partitioning	block	cyclic	block cyclic	chunk	**d**
13	blocking optimization is used to improve temmporal locality for reduce	hit miss	misses	hit rate	cache misses	**b**
14	CUDA thought that 'unifying theme' of every form of parallelism is	CDA thread	PTA thread	CUDA thread	CUD thread	**c**
15	Topological sort of a Directed Acyclic graph is?	a) Always unique	b) Always Not unique	c) Sometimes unique and sometimes not unique	d) Always unique if graph has even number of vertices	**c**
16	threads being block altogether and being executed in the sets of 32 threads called a	thread block	32 thread	32 block	unit block	**a**
17	True or False: The threads in a thread block are distributed across SM units so that each thread is executed by one SM unit.	TRUE	FALSE			**a**

18	When the topological sort of a graph is unique?	a) When there exists a hamiltonian path in the graph	b) In the presence of multiple nodes with indegree 0	c) In the presence of single node with indegree 0	d) In the presence of single node with outdegree 0	**a**
19	What is a high performance multi-core processor that can be used to accelerate a wide variety of applications using parallel computing.	CPU	DSP	GPU	CLU	**c**
20	A good mapping does not depends on which following factor	knowledge of task sizes	the size of data associated with tasks	characteristics of inter-task interactions	task overhead	**d**
21	CUDA is a parallel computing platform and programming model	TRUE	FALSE			**a**
22	Which of the following is *not* a form of parallelism supported by CUDA	Vector parallelism - Floating point computations are executed in parallel on wide vector units	Thread level task parallelism - Different threads execute a different tasks	Block and grid level parallelism - Different blocks or grids execute different tasks	Data parallelism - Different threads and blocks process different parts of data in memory	**a**
23	The style of parallelism supported on GPUs is best described as	MISD - Multiple Instruction Single Data	SIMT - Single Instruction Multiple Thread	SISD - Single Instruction Single Data	MIMD	**b**
24	True or false: Functions annotated with the __global__ qualifier may be executed on the host or the device	TRUE	FALSE			**a**

25	Which of the following correctly describes a GPU kernel	A kernel may contain a mix of host and GPU code	All thread blocks involved in the same computation use the same kernel	A kernel is part of the GPU's internal micro-operating system, allowing it to act as in independent host	kernel may contain only host code	**b**
26	a code known as grid which runs on GPU consisting of a set of	32 thread	unit block	32 block	thread block	**d**
27	which of the following is not an parallel algorithm model	data parallel model	task graph model	task model	work pool model	**c**
28	Having load before the store in a running program order, then interchanging this order, results in a	WAW hazards	Destination registers	WAR hazards	Registers	**c**
29	model based on the passing of stream of data through process arranged in a succession is called as	producer consumer model	hybrid model	task graph model	work pool model	**a**
30	When instruction i and instruction j are tends to write the same register or the memory location, it is called	Input dependence	Output dependence	Ideal pipeline	Digital call	**b**
31	Multithreading allowing multiple-threads for sharing the functional units of a	Multiple processor	Single processor	Dual core	Corei5	**b**
32	Allowing multiple instructions for issuing in a clock cycle, is the goal of	Single-issue processors	Dual-issue processors	Multiple-issue processors	No-issue processors	**c**

33	OpenGL stands for:	A. Open General Liability	B. Open Graphics Library	C. Open Guide Line	D. Open Graphics Layer	**b**
34	which of the following is not an advantage of OpenGL	There is more detailed documentation for OpenGL while other API's don't have such detailed documentation.	OpenGL is portable.	OpenGL is more functional than any other API.	It is not a cross-platform API,	**d**
35	work pool model uses ---------- approach for task assignment	static	dynamic	centralized	decentralized	**b**
36	which of the following is false regarding data parallel model	all task perform same computations	degree of parallelism increase with size of problem	matrix multiplication is example of data parallel	dynamic mapping is done	**d**
37	which of the following are methods for containing interaction overheads	maximizing data locality	minimize volumn of data exchange	min frequency of interactions	all the above	**d**
38	which of the following are classes of dynamic mapping centralized method	self scheduling	chunk scheduling	both a and b	none of the above	**c**
39	which of the following is not scheme for static mapping	block distribution	block cyclic distributions	cyclic distributions	self scheduling	**d**

UNIT THREE	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
e.g 1	**Write down question**	**Option a**	**Option b**	**Option c**	**Option d**	**a/b/c/d**
1	Group communication operations are built using which primitives?	one to all	all to all	point to point	None of these	**c**
2	___ can be performed in an identical fashion by inverting the process.	Recursive Doubling	Reduction	Broadcast	None of these	**b**
3	Broadcast and reduction operations on a mesh is performed	along the rows	along the columns	both a and b concurrently	None of these	**c**
4	Cost Analysis on a ring is	(ts + twm)(p - 1)	(ts - twm)(p + 1)	(tw + tsm)(p - 1)	(tw - tsm)(p + 1)	**a**
5	Cost Analysis on a mesh is	2ts(sqrt(p) + 1) + twm(p - 1)	2tw(sqrt(p) + 1) + tsm(p - 1)	2tw(sqrt(p) - 1) + tsm(p - 1)	2ts(sqrt(p) - 1) + twm(p - 1)	**d**
6	Communication between two directly link nodes	Cut-through routing	Store-and-forward routing	Nearest neighbour communication	None	**c**
7	All-to-one communication (reduction) is the dual of _____ broadcast.	all-to-all	one-to-all	one-to-one	all-to-one	**b**
8	Which is known as Reduction?	all-to-one	all-to-all	one-to-one	one-to-all	**a**

9	Which is known as Broadcast?	one-to-one	one-to-all	all-to-all	all-to-one	**b**
10	The dual of all-to-all broadcast is	all-to-all reduction	all-to-one reduction	Both	None	**a**
11	All-to-all broadcast algorithm for the 2D mesh is based on the	Linear Array Algorithm	Ring algorithm	Both	None	**b**
12	In the first phase of 2D Mesh All to All, the message size is ___	p	m*sqrt(p)	m	p*sqrt(m)	**c**
13	In the second phase of 2D Mesh All to All, the message size is ___	m	p*sqrt(m)	p	m*sqrt(p)	**d**
14	In All to All on Hypercube, The size of the message to be transmitted at the next step is ____ by concatenating the received message with their current data	doubled	tripled	halfed	no change	**a**
15	The all-to-all broadcast on Hypercube needs ____ steps	p	sqrt(p) - 1	log p	None	**c**
16	One-to-All Personalized Communication operation is commonly called ___	gather operation	concatenation	scatter operation	None	**c**
17	The dual of the scatter operation is the	concatenation	gather operation	Both	None	**c**

18	In Scatter Operation on Hypercube, on each step, the size of the messages communicated is ____	tripled	halved	doubled	no change	**b**
19	Which is also called "Total Exchange" ?	All-to-all broadcast	All-to-all personalized communication	all-to-one reduction	None	**b**
20	All-to-all personalized communication can be used in ____	Fourier transform	matrix transpose	sample sort	all of the above	**d**
21	In collective communication operations, collective means	involve group of processors	involve group of algorithms	involve group of variables	none of these	**a**
22	efficiency of data parallel algorithm depends on the	efficient implementation of the algorithm	efficient implementation of the operation	both	none	**b**
23	All processes participate in a single _____ interaction operation.	global	local	wide	variable	**a**
24	subsets of processes in _____ interaction.	global	local	wide	variable	**b**
25	Goal of good algorithm is to implement commonly used _____ pattern.	communication	interaction	parallel	regular	**a**
26	Reduction can be used to find the sum, product, maximum, minimum of _____ of numbers.	tuple	list	sets	all of above	**c**
27	source ____ is bottleneck.	process	algorithm	list	tuple	**a**

28	only connections between single pairs of nodes are used at a time is	good utilization	poor utilization	massive utilization	medium utilization	**b**
29	all processes that have the data can send it again is	recursive doubling	naive approach	reduction	all	**a**
30	The ____ do not snoop the messages going through them.	nodes	variables	tuple	list	**a**
31	accumulate results and send with the same pattern is...	broadcast	naive approach	recursive doubling	reduction symmetric	**d**
32	every node on the linear array has the data and broadcast on the columns with the linear array algorithm in _____	parallel	vertical	horizontal	all	**a**
33	using different links every time and forwarding in parallel again is	better for congestion	better for reduction	better for communication	better for algorithm	**a**
34	In a balanced binary tree processing nodes is equal to	leaves	number of elemnts	branch	none	**a**
35	In one -to- all broadcast there is	divide and conquer type algorithm	sorting type algorithm	searching type algorithm	simple algorithm	**a**
36	For sake of simplicity, the number of nodes is a power of	1	2	3	4	**b**
37	Nides with zero in i least significant bits participate in _____	algorithm	broadcast	communication	searching	**c**

38	every node has to know when to communicate that is	call the procedure	call for broadcast	call for communication	call the congestion	**a**
39	the procedure is disturbed and require only point-to-point _____	synchronization	communication	both	none	**a**
40	Renaming relative to the source is _____ the source.	XOR	XNOR	AND	NAND	**a**

UNIT FOUR	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
e.g 1	**Write down question**	**Option a**	**Option b**	**Option c**	**Option d**	**a/b/c/d**
1	mathematically efficiency is	e=s/p	e=p/s	e*s=p/2	e=p+e/e	**a**
2	Cost of a parallel system is sometimes referred to____ of product	work	processor time	both	none	**c**
3	Scaling Characteristics of Parallel Programs Ts is	increase	constant	decreases	none	**b**
4	Speedup tends to saturate and efficiency _____ as a consequence of Amdahl's law.	increase	constant	decreases	none	**c**
5	Speedup obtained when the problem size is _____ linearly with the number of processing elements.	increase	constant	decreases	depend on problem size	**a**
6	The n × n matrix is partitioned among n processors, with each processor storing complete ___ of the matrix.	row	column	both	depend on processor	**a**
7	cost-optimal parallel systems have an efficiency of ___	1	n	logn	complex	**a**
8	The n × n matrix is partitioned among n2 processors such that each processor owns a _____ element.	n	2n	single	double	**c**
9	how many basic communication operations are used in matrix vector multiplication	1	2	3	4	**c**
10	In DNS algorithm of matrix multiplication it used	1d partition	2d partition	3d partition	both a,b	**c**

11	In the Pipelined Execution, steps contain	normalization	communicatio n	elimination	all	**d**
12	the cost of the parallel algorithm is higher than the sequential run time by a factor of __	3/2	2/3	3*2	2/3+3/2	**a**
13	The load imbalance problem in Parallel Gaussian Elimination: can be alleviated by using a ____ mapping	acyclic	cyclic	both	none	**b**
14	A parallel algorithm is evaluated by its runtime in function of	the input size,	the number of processors,	the communicatio n parameters.	all	**d**
15	For a problem consisting of W units of work, p__W processors can be used optimally.	<=	>=	<	>	**a**
16	C(W)__Θ(W) for optimality (necessary condition).	>	<	<=	equals	**d**
17	many interactions in oractical parallel programs occur in _____ pattern	well defined	zig-zac	reverse	straight	**a**
18	efficient implementation of basic communication operation can improve	performance	communicatio n	algorithm	all	**a**
19	efficient use of basic communication operations can reduce	development effort and	software quality	both	none	**a**
20	Group communication operations are built using_____ Messenging primitives.	point-to-point	one-to-all	all-to-one	none	**a**
21	one processor has a piece of data and it need to send to everyone is	one -to-all	all-to-one	point -to-point	all of above	**a**
22	the dual of one -to-all is	all-to-one reduction	one -to-all reduction	pnoint -to-point reducntion	none	**a**

23	Data items must be combined piece-wise and the result made available at	target processor finally	target variable finatlalyrget receiver			**a**
24	wimpleat way to send p-1 messages from source to the other p-1 processors	Algorithm	communicatio n	concurrency	receiver	**c**
25	In a eight node ring, node ____ is source of broadcast	1	2	8	0	**d**
26	The processors compute _____ product of the vector element and the loval matrix	local	global	both	none	**a**
27	one to all broadcast use	recursive doubling	simple algorithm	both	none	**a**
28	In a broadcast and reduction on a balanced binary tree reduction is done in _____	recursive order	straight order	vertical order	parallel order	**a**
29	if "X" is the message to broadcast it initially resides at the source node	1	2	8	0	**d**
30	logical operators used in algorithm are	XOR	AND	both	none	**c**
31	Generalization of broadcast in Which each processor is	Source as well as destination	only source	only destination	none	**a**
32	The algorithm terminates in _____ steps	p	p+1	p+2	p-1	**d**
33	Each node first sends to one of its neighbours the data it need to....	broadcast	identify	verify	none	**a**
34	The second communication phase is a columnwise _____ broadcast of consolidated	All-to-all	one -to-all	all-to-one	point-to-poi nt	**a**

35	All nodes collects _____ message corresponding to √p nodes to their respectively	√p	p	p+1	p-1	**a**
36	It is not possible to port ____ for higher dimensional network	Algorithm	hypercube	both	none	**a**
37	If we port algorithm to higher dimemsional network it would cause	error	contention	recursion	none	**b**
38	In the scatter operation ____ node send message to every other node	single	double	triple	none	**a**
39	The gather Operation is exactly the inverse of _____	scatter operation	recursion operation	execution	none	**a**
40	Similar communication pattern to all-to-all broadcast except in the_____	reverse order	parallel order	straight order	vertical order	**a**

UNIT FIVE	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
e.g 1	**Write down question**	**Option a**	**Option b**	**Option c**	**Option d**	**a/b/c/d**
1	In _____, the number of elements to be sorted is small enough to fit into the process's main memory.	internal sorting	internal searching	external sorting	external searching	**a**
2	_____ algorithms use auxiliary storage (such as tapes and hard disks) for sorting because the number of elements to be sorted is too large to fit into memory.	internal sorting	internal searching	External sorting	external searching	**c**
3	_____ can be comparison-based or noncomparison-based.	searching	Sorting	both a and b	none of above	**b**
4	The fundamental operation of comparison-based sorting is _____.	compare-exchange	searching	Sorting	swapping	**a**
5	The complexity of bubble sort is Θ(n2).	TRUE	FALSE			**a**
6	Bubble sort is difficult to parallelize since the algorithm has no concurrency.	TRUE	FALSE			**a**
7	Quicksort is one of the most common sorting algorithms for sequential computers because of its simplicity, low overhead, and optimal average complexity.	TRUE	FALSE			**a**
8	The performance of quicksort depends critically on the quality of the _____-.	non-pivote	pivot	center element	len of array	**b**

9	the complexity of quicksort is O(nlog n).	TRUE	FALSE			**a**
10	DFS begins by expanding the initial node and generating its successors. In each subsequent step, DFS expands one of the most recently generated nodes.	TRUE	FALSE			
11	The main advantage of _____ is that its storage requirement is linear in the depth of the state space being searched.	BFS	DFS	a and b	none of above	**b**
12	_____ algorithms use a heuristic to guide search.	BFS	DFS	a and b	none of above	**a**
13	If the heuristic is admissible, the BFS finds the optimal solution.	TRUE	FALSE			**a**
14	The search overhead factor of the parallel system is defined as the ratio of the work done by the parallel formulation to that done by the sequential formulation	TRUE	FALSE			**a**
15	The critical issue in parallel depth-first search algorithms is the distribution of the search space among the processors.	TRUE	FALSE			**a**
16	Graph search involves a closed list, where the major operation is a _____	sorting	searching	lookup	none of above	**c**
17	_____ algorithms use auxiliary storage (such as tapes and hard disks) for sorting because the number of elements to be sorted is too large to fit into memory.	internal sorting	internal searching	External sorting	external searching	**c**
18	_____ can be comparison-based or noncomparison-based.	searching	Sorting	both a and b	none of above	**b**

19	If the heuristic is admissible, the BFS finds the optimal solution.	TRUE	FALSE			**a**
20	The search overhead factor of the parallel system is defined as the ratio of the work done by the parallel formulation to that done by the sequential formulation	TRUE	FALSE			**a**
21	Breadth First Search is equivalent to which of the traversal in the Binary Trees?	Pre-order Traversal	Post-order Traversal	Level-order Traversal	In-order Traversal	**c**
22	Time Complexity of Breadth First Search is? (V – number of vertices, E – number of edges)	O(V + E)	O(V)	O(E)	O(V*E)	**a**
23	Which of the following is not an application of Breadth First Search?	When the graph is a Binary Tree	When the graph is a Linked List	When the graph is a n-ary Tree	When the graph is a Ternary Tree	**b**
24	In BFS, how many times a node is visited?	Once	Twice	Equivalent to number of indegree of the node	Thrice	**c**
25	Is Best First Search a searching algorithm used in graphs.	TRUE	FALSE			**a**
26	The critical issue in parallel depth-first search algorithms is the distribution of the search space among the processors.	TRUE	FALSE			**a**
27	Graph search involves a closed list, where the major operation is a _____	sorting	searching	lookup	none of above	**c**

28	The fundamental operation of comparison-based sorting is _____.	compare-exchange	searching	Sorting	swapping	**a**
29	The complexity of bubble sort is Θ(n2).	TRUE	FALSE			**a**
30	DFS begins by expanding the initial node and generating its successors. In each subsequent step, DFS expands one of the most recently generated nodes.	TRUE	FALSE			
31	The main advantage of _____ is that its storage requirement is linear in the depth of the state space being searched.	BFS	DFS	a and b	none of above	**b**
32	Breadth First Search is equivalent to which of the traversal in the Binary Trees?	Pre-order Traversal	Post-order Traversal	Level-order Traversal	In-order Traversal	**c**
33	Time Complexity of Breadth First Search is? (V – number of vertices, E – number of edges)	O(V + E)	O(V)	O(E)	O(V*E)	**a**
34	Which of the following is not an application of Breadth First Search?	When the graph is a Binary Tree	When the graph is a Linked List	When the graph is a n-ary Tree	When the graph is a Ternary Tree	**b**
35	In BFS, how many times a node is visited?	Once	Twice	Equivalent to number of indegree of the node	Thrice	**c**
36	Is Best First Search a searching algorithm used in graphs.	TRUE	FALSE			**a**

37	Which of the following is not a stable sorting algorithm in its typical implementation.	Insertion Sort	Merge Sort	Quick Sort	Bubble Sort	**c**
38	Which of the following is not true about comparison based sorting algorithms?	The minimum possible time complexity of a comparison based sorting algorithm is O(nLogn) for a random input array	Any comparison based sorting algorithm can be made stable by using position as a criteria when two elements	Counting Sort is not a comparison based sorting algortihm	Heap Sort is not a comparison based sorting algorithm.	**d**
39	In _____, the number of elements to be sorted is small enough to fit into the process's main memory.	internal sorting	internal searching	external sorting	external searching	**a**

UNIT SIX	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
e.g 1	**Write down question**	**Option a**	**Option b**	**Option c**	**Option d**	**a/b/c/d**
1	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
2	The kernel code is dentified by the _____qualifier with void return type	_host_	__global__	_device_	void	**b**
3	The kernel code is only callable by the host	TRUE	FALSE			**a**
4	The kernel code is executable on the device and host	TRUE	FALSE			**b**
5	Calling a kernel is typically referred to as _____.	kernel thread	kernel initialization	kernel termination	kernel invocation	**d**
6	Host codes in a CUDA application can Initialize a device	TRUE	FALSE			**a**
7	Host codes in a CUDA application can Allocate GPU memory	TRUE	FALSE			**a**
8	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
9	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
10	The kernel code is dentified by the _____qualifier with void return type	_host_	__global__	_device_	void	**b**
11	Host codes in a CUDA application can not Invoke kernels	TRUE	FALSE			**b**

12	CUDA offers the Chevron Syntax to configure and execute a kernel.	TRUE	FALSE			**a**
13	the BlockPerGrid and ThreadPerBlock parameters are related to the _____ model supported by CUDA.	host	kernel	thread abstraction	none of above	**c**
14	_____ is Callable from the device only	_host_	__global__	_device_	none of above	**c**
15	_____ is Callable from the host	_host_	__global__	_device_	none of above	**b**
16	_____ is Callable from the host	_host_	__global__	_device_	none of above	**a**
17	CUDA supports _____ in which code in a single thread is executed by all other threads.	tread division	tread termination	thread abstraction	none of above	**c**
18	In CUDA, a single invoked kernel is referred to as a _____.	block	tread	grid	none of above	**c**
19	A grid is comprised of _____ of threads.	block	bunch	host	none of above	**a**
20	A block is comprised of multiple _____.	treads	bunch	host	none of above	**a**
21	a solution of the problem in representing the parallelismin algorithm is	CUD	PTA	CDA	CUDA	**d**
22	_____ is Callable from the host	_host_	__global__	_device_	none of above	**b**
23	_____ is Callable from the host	_host_	__global__	_device_	none of above	**a**
24	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
25	The kernel code is dentified by the _____qualifier with void return type	_host_	__global__	_device_	void	**b**

26	Host codes in a CUDA application can not Reset a device	TRUE	FALSE			**b**
27	Host codes in a CUDA application can not Invoke kernels	TRUE	FALSE			**b**
28	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
29	Calling a kernel is typically referred to as _____.	kernel thread	kernel initialization	kernel termination	kernel invocation	**d**
30	In CUDA, a single invoked kernel is referred to as a _____.	block	tread	grid	none of above	**c**
31	A grid is comprised of _____ of threads.	block	bunch	host	none of above	**a**
32	A block is comprised of multiple _____.	treads	bunch	host	none of above	**a**
33	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
34	_____ is Callable from the host	_host_	__global__	_device_	none of above	**a**
35	In CUDA, a single invoked kernel is referred to as a _____.	block	tread	grid	none of above	**c**
36	the BlockPerGrid and ThreadPerBlock parameters are related to the _____ model supported by CUDA.	host	kernel	thread abstract ion	none of above	**c**
37	Host codes in a CUDA application can Transfer data to and from the device	TRUE	FALSE			**a**
38	Host codes in a CUDA application can not Deallocate memory on the GPU	TRUE	FALSE			**b**

39	Host codes in a CUDA application can not Reset a device	TRUE	FALSE			**b**
40	Calling a kernel is typically referred to as _____.	kernel thread	kernel initialization	kernel termination	kernel invocation	**d**

1.Following is true about one to all broadcast

A.In one to all broadcast initially there will be P(Number of processors) copies of messages and after broadcast finally there will be simgle copy

B.In one to all broadcast initially there will be single copy of message and after broadcast finally there will P(Number of processors) copies.

Submit

Answer

“In one to all broadcast initially there will be single copy of message and after broadcast finally there will P(Number of processors) copies.”

2.If total 8 nodes are in ring topology after one to all message broadcasting how many source nodes will be present?

2

4

8

1

Submit

Answer

8

3.Current source node selects _____ node as next source node in linear/ring one to all message broadcast

A.nearest node

B.longest node

Submit

Answer

longest node

4.In All-to-one reduction after reduction the final copy of massage is avilible on which node?

A.Source Node

B.Destination Node

C.Both of the above

D.None of these

Answer

Destination Node

5.If there is 4 by 4 mesh topology network present(as per shown in the video) then in how many broadcast cycles will be required to reach message to all 16 nodes?

2

8

4

16

Submit

Answer

4

6.If there are 8 nodes in a ring topology how many message passing cycles will be required to complete reduction process

1

2

3

4

Submit

Answer

3

7.In One to all broadcast using Hypercube topology how source node selects next destination node?

Node which is having lowest binary code (label)

Node which is having highet binary code (label)

To all connected node at a time

None of the above

Submit

Answer

Node which is having highet binary code (label)

8.If there are 8 nodes connected in ring topology then ___ number of message passing cycles will be required to complete all to all broadcast in parallel mode.

3

4

8

7

Submit

Answer

7

9.Consider all to all broadcast in ring topology with 8 nodes.How many messages will be present with each node after 3rd step/cycle of communication?

3

4

7

None of the above

Submit

Answer

4

10.If there are 16 messages in 4x4 mesh then total how many message passsing cycles will be required to complete all to all broadcast operation?

4

5

6

8

Submit

Answer

6

11.If there are P messages in mxm mesh then total how many message passsing cycles will be required to complete all to all broadcast operation?

2 √P - 2

2 √P - 1

2 √P

None of the above

Submit

Answer

2 √P - 2

12.How many massage passing cycles required for all-to-all broadcasting in 8 nodes hypercube?

4

3

2

8

Submit

Answer

3

13.In scatter opreation after massage broadcasting every node avail with same massage copy.

True

False

Submit

Answer

False

14.CUDA helps do execute code in parallel mode using __

CPU

GPU

ROM

Cash memory

Submit

Answer

GPU

15.In thread-function execution scenario thread is a ___

Work

Worker

Task

None of the above

Submit

Answer

Worker

16.In GPU Following statements are true

Block contains Grid

Grid contains Block

Block contains Threads

SM stands for Streaming MultiMedia

SM stands for Streaming MultiProcessor

Submit

Answer

“Grid contains Block”, “Block contains Threads”, “SM stands for Streaming MultiProcessor

17.Following issue(s) is/are the true about sorting techniques with parallel computing.

Large sequence is the issue

Where to store output sequence is the issue

Where to store input sequence is the issue

None of the above

Submit

Answer

“Where to store output sequence is the issue”, “Where to store input sequence is the issue”

18.Partitioning on series done after __

Local arrangement

Processess assignments

Global arrangement

None of the above

Submit

Answer

Global arrangement

19.In Parallel DFS processes has following roles.(Select multiple choices if applicable)

Donor

Active

Idle

Recipient

Submit

Answer

“Donor”, “Recipient”

20.Suppose there are 16 elements in a series then how many phases will be required to sort the series using parallel odd-even bubble sort?

8

4

5

15

Submit

Answer

15

21.Which are different sources of Overheads in Parallel Programs?

Interprocess interactions

Process Idling

Large amount of DATA

Excess Computation

Submit

Answer

“Interprocess interactions”, “Process Idling”, “Excess Computation”

1 / 1 points
1 / 1 attempts

22,Speedup (S) is….

The ratio of the time taken to solve a problem on a parallel processors to the time required to solve the same problem on a single processor with p identical processing elements

The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements

The ratio of number of multiple processors to size of data

None of the above

Submit

Answer

The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements

1 / 1 points
1 / 1 attempts

23.Efficiency is a measure of the fraction of time for which a processing element is usefully employed.

TRUE

FALSE

Submit

Answer

TRUE

	marks	question	A	B	C	D	ans
0	1	Interconnection Networks can be classified as?	Both	Dynamic	Static	Direct Network	Both Static and Dynamic.
1	1	Parallel Computers are used to solve which types of problems.	Both	Algorithmic Problems	Optimization Problems	None	This is an explaination.
2	1	How many clocks control all the stages in a pipeline?	One	Three	Four	Five	One clock Is used to control all the stages.
3	1	Main memory in parallel computing is____?	Shared	Parallel	Fixed	None	Main memory is shared in parallel computing.
4	1	Which of these is not a class of parallel computing architetcture?	Application Checkpointing	Distributed Computing	Symmetric Multiprocessing	Multicore Computing	Ans- (d)- Application checkpoiting. is not a class of parallel computer architecture.
5	1	Parallel Computing software solutions and Techniques includes:	All	Automatic Parallelization	Parallel Programming languages.	Application Checkpointing	Parallel computing software solutionincludes all of the following.. This is an explanation
6	2	The Processors are connected to the memory through a set of?	Switches	Cables	Buses	Registers	The Processors are connected thru. the switches.
7	2	Superscalar Architetcure has how many execution units?	Two	One	Three	Four	This is an explaination.
8	2	What is used to hold the intermediate output in a pipeline	Intermediate Register	Cache	RAM	ROM	The Intermediate Registers are used to hold the output.
9	2	Which oranization performs sequencing of Human Genome?	International Human Genome Sequencing and Consortium	International Sequencing and Consortium for Human Genome	Human Genome Sequencing and Constrium, Org.	Genome Sequencing for Humans and Consortium, Org.	This is an explaination.
10	2	There are how many stages in RISC Processor?	Five	Three	Two	Six	Ans(c)- Five stages are there in a RISC processor.
11	2	Over the last decade, The DRAM access time has improved at what rate per year?	0.1	0.2	0.15	None of the above	The DRAM acess time rate has improved at a rate of 10% over the last decade.

	marks	question	A	B	C	D	ans
12	2	Which memory acts as low-latency high bandwidth storage?	Cache	Register	DRAM	EPROM	Cache acts as low latency high bandwidth storage .This is an explanation.
13	2	Which processor architecture is this?	SIMD	MIMD	MISD	MIMD	This is an explaination.
14	2	Which core processor is this?	Quad-Core	Dual-Core	Octa-Core	Single-Core	This diagram shows Quad-Core.
15	2	Which of these is not a scalable design principle?	Data Caching	Decomposition	Simplification	Parsimony	Data Caching is not a prinicple of scable design.
16	2	The distance between any two nodes in Bus Based network is?	O(1)	O(n Logn)	O(N)	O(n^2)	O(1) is the ditance between any two nodes.
17	2	Early SIMD computers include:	All	MPP	CM-2	Illiac IV	All of these are early staged SIMD parallel computers.
18	2	This is which configuration in Omega networks.	Pass-through	Cross-Over	Shuffle	None	This is called Pass-through configuration.
19	2	Automatic Parallelization technique doesnâ€™t ncludes:	Share Memory	Analyse	Schedule	Parse	Parallelization includes parse, analyse schedule and code generation.
20	2	The Pentuim 4 or P4 processor has how many stage pipeline?	20	15	18	10	The P4 processor has 20 staged pipeline. This is an explanation.
21	3	Which protocol is not used to remove concurrent writes?	Identify	Priority	Common	Sum	Sum, Prioirity and common are used to remove concurrent writes.
22	3	EREW PRAM stands for?	Exclusive Read and Exclusive Write	Erasable Read and Erasable Write PRAM	Easily Read and Easily Write	None	EREW stands for Exclusive Read and Exclsuive Write PRAM.
23	3	During each clock cycle, multiple instructions are piped into the processor in_____?	Parallel	Series	Both a and b	None	Multiple Instuctiion are piped in parallel. This is an explanation.
24	3	Which Interconnection Network uses this equation.	Multistage Networks	Cross-Bar	Dynamic Networks	Bus-Staged	Multistaged Network uses this eqn.

	marks	question	A	B	C	D	ans
25	3	How many types of parallel computing are available from both proprietary and open source parallel computing vendors?	4	2	3	6	There are generally four types of parallel computing, available from both proprietary and open source parallel computing vendors.
26	3	If a piece of data is repeatedly used, the effective latency of this memory system can be reduced by the cache. The fraction of data references satisfied by the cache is called?	Hit Ratio	Memory ratio	Hit Fraction	Memory Fraction.	If a piece of data is repeatedly used, the effective latency of this memory system can be reduced by the cache. The fraction of data references satisfied by the cache is called the cache hit ratio.
27	3	Superscalar Architetcure can create problem in?	Scheduling	Phasing	Data Extraction	Data-Compiling	SuperScalar Architecture can cause problems in CPU scheduling.
28	3	In cut-through routing, a message is broken into fixed size units called?	Flits	Flow Digits	Control Digits	All	In cut-through routing, a message is broken into fixed size units called flits.
29	3	The total communication time for cut-through routing is?	A	B	C	D	This is an explaination.
30	1	The Disadvantage of GPU Pipeline is?	Load-balancing	Data balancing	Process balancing	All of the above	This is an explaination.
31	1	Examples of GPU Processors are:	Both	AMD Processors	NVIDIA	None	Both AMD and NVIDIA.
32	1	Simultaneous execution of different programs on a data stream is called?	Stream Parallelism	Data Execution	Data-paralleism	None	Simultaneous execution of different programs on a data stream is called Stream Parallelism.
33	1	Early GPU controllers were known as?	Video Shifters	GPU Shifters	GPU Controllers	Video-Movers	This is an Explaination.
34	1	_____development is a critical component of problem solving using computers?	Algorithm	Code	Pseudocode	Problem	Algorithm development is a critical component of problem solving using computers

	marks	question	A	B	C	D	ans
35	1	GPU stands for?	Graphics Processsing Unit	Graphical Processing Unit	Gaming Processing Unit	Graph Processing Unit	This is an Explaination.
36	1	What leads to concurrency?	Parallelism	Serial Processing	Decomposition	All	Parallelism leads naturally to Concurrency. For example, Several processes trying to print a file on a single printer.
37	2	The process of determining which screen-space pixel locations are covered by each\ntriangle is known as?	Rasterization	Pixelisation	Fragmentation	Space-Determining Process	Rasterization is the process of determining which screen-space pixel locations are covered by each\ntriangle.
38	2	The programmable units of the GPU follow which programming model?	SPMD	MISD	MIMD	SIMD	The programmable units of the GPU follow a single program multiple-data (SPMD) programming model.
39	2	Which space can ease the programming effort, especially if the distribution of data is different in different phases of the algorithm?	Shared Address	Parallel Address	Data- Address	Series-Address	Shared Address space can ease the programming effort, especially if the distribution of data is different in different phases of the algorithm.
40	2	Which are the hardware units that physically perform computations?	Processsor	ALU	CPU	CU	Processors are the hardware units that physically perform computations
41	2	Examples of Graphics API are?	All	DirectX	CUDA	Open-CL	All of the these are examples of Graphics API
42	2	The mechanism by which tasks are assigned to processes for execution is called___?	Mapping	Computation	Process	None	The mechanism by which tasks are assigned to processes for execution is called mapping.

	marks	question	A	B	C	D	ans
43	2	A decomposition into a large number of small tasks is called_____ granularity.	Fine- grained	Coarse-grained	Vector-granied	All	A decomposition into a large number of small tasks is called fine-grained granularity.
44	2	Identical operations being applied concurrently on different data items is called?	Data-Parallelism	Parallelism	Data Serialsm	Concurrency	Identical operations being applied concurrently on different data items is called Data Parallelism.
45	2	System which do not have parallel processsing capabiities?	SISD	SIMD	MISD	MIMD	This is the explainantion.
46	2	The time and the location in the program of a static one-way interaction is known as ?	Priori	Polling	Decomposition	Execution	The time and the location in the program of a static one-way interaction is known a priori.
47	2	Memory access in RISC architecture is limited to which instructions?	STA and LDA	CALL and RET	Push and POP	MOV and JMP	This is the explaination.
48	2	Which Algorithms can be implemented in both shared-address-space and message-passing paradigms?	Data-Parallel Algo.	Quick-Sort Algo.	Data Algorithm	Bubble Sort Algo.	Data Parallel algorithms can be implemented in both shared-address-space and message-passing paradigms
49	2	Which type of Distribution is this?	Randomized Block Distribution	Block-Cyclic Distribution	Cyclic Distribution	None	This figure shows Randomized Block Distribution.
50	2	An abstraction used to express such dependencies among tasks and their relative order of execution is known as_____?	Task-Dependency Graph.	Dependency Graph.	Time-Dependency Graph	None	An abstraction used to express such dependencies among tasks and their relative order of execution is known as a task-dependency graph.

	marks	question	A	B	C	D	ans
51	3	Which is the simplest way to distribute an array and assign uniform contiguous portions of the array to different processes?	Block Distrbution	Array Distrbution	Process Distribution	All	Block distributions are some of the simplest ways to distribute an array and assign uniform contiguous portions of the array to different processes
52	3	An example of a decomposition with a regular interaction pattern is?	Image-dethering problem.	Travelling Salesman Problem	Time-complexity Problens	8 Queen problem.	An example of a decomposition with a regular interaction pattern is the problem of image dithering.
53	3	A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is	Critical-path	Process-path	Granularity.	Concurrency	A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is critical path.
54	3	The shared-address-space programming paradigms can handle which interactions?	Both	Two way	One way	None	The shared-address-space programming paradigms can handle both one-way and two-way interactions.
55	3	Which distribution can result in an almost perfect load balance due to the extreme fine-grained underlying decomposition.	Cyclic Distribution.	Array Distribution	Block-Cyclic Distribution	Block Distribution.	Cyclic Distribution can result in an almost perfect load balance due to the extreme fine-grained underlying decomposition.
56	3	Data sharing interactions can be categorized as_____interactions?	Both	Read-Write	Read only	None	Data sharing interactions can be categorized as either read-only or read-write interactions

	marks	question	A	B	C	D	ans
57	3	What is the way of structuring a parallel algorithm by selecting a decomposition and mapping technique and applying the appropriate strategy to minimize interactions called?	Algorithm Model	Parallel Model	Data Model	Mapping Model	Algo. Model is a way of structuring a parallel algorithm by selecting a decomposition and mapping technique and applying the appropriate strategy to minimize interactions.
58	3	Which Algorithm is this?	Serial column based Algo.	Column-Algorithm	Bubble Sort Algo.	None.	This is Serial Column based algorithm.
59	3	Algorithms based on the task graph model include:	All	Matrix-Factorization	Parallel QuickSort	Quicksort	This is an Explaination.
60	1	Which model permits simultaneous communication on all the channels connected to a node?	All-port communication	One-port communication	Dual-port communication	Quad-port communication	All-port communication model permits simultaneous communication on all the channels connected to a node.
61	1	A process sends the same m-word message to every other process, but different processes may broadcast different messages. It is called?	All to All Broadcast	One to All Broadcast	All to All Reduction	None	This is an Explaination.
62	1	The Matrix is transposed using which operation?	All to All personalized communication	One-to-all personalized communication	All-to-one personalized communication	One to one personalized communication.	This is an Explaination.
63	1	Each node in a two-dimensional wraparound mesh has how many ports?	Four	Two	Three	One	Each node in a two-dimensional wraparound mesh has four ports
64	1	Circular shift is a member of a broader class of global communication operations known as?	Permutation	Combination.	Both a and b	None	This is ann explaination.
65	1	We define_____ as the operation in which node i sends a data packet to node (i + q) mod p in a p-node ensemble (0 < q < p).	Circular q-shift	Linear shift	Circular shift	Linear q-shift.	We define a circular q-shift as the operation in which node i sends a data packet to node (i + q) mod p in a p-node ensemble (0 < q < p).

	marks	question	A	B	C	D	ans
66	1	Parallel algorithms often require a single process to send identical data to all other processes or to a subset of them. This operation is known as?	One to All Broadcast	One to One Broadcast	All to One Broadcast	None	Parallel algorithms often require a single process to send identical data to all other processes or to a subset of them. This operation is known as One to All Broadcast.
67	1	In which Communication each node sends a distinct message of size m to every other node?	All to All personalized communication	One to One personalized communication	All-to-one personalized communication	One-to-all personalized communication.	This is an Explaination.
68	1	All to All personalized communication operation is not used in a which of these parallel algorithms?	Quick Sort	Matrix-Transpose	Fourier Transformation	Database Join operation	This is an Explaination.
69	1	The Dual of one-to-all broadcast is?	All to one Reduction	All to one Broadcast	One to Many Reduction	All to All Broadcast	The dual of one to all Broadcast is called all to one reduction.
70	1	Reduction on a linear array can be performed by_____ the direction and the sequence of communication?	Reversing	Forwarding	Escaping	Widening	Reduction on a linear array can be performed by simply reversing the direction and the sequence of communication
71	2	This equation is used to solve which topology operations in all to all communications?	Hypercube	Mesh	Ring	Linear-Array	This is an Explaination.
72	2	\nThe communication pattern of all-to-all broadcast can be used to perform_____?	Third Variation of Reduction	Second Variation of Reduction	First Variation of Reduction	Fifth Variation of Reduction	This is an Explaination.
73	2	A single node sends a unique message of size m to every other node. This operation is known as_____?	Scatter	Reduction	Gather	Concatenate	In the scatter operation, a single node sends a unique message of size m to every other node.
74	2	The Algorithm represents which broadcast?	All to All Broadcast	All to All Broadcast	All to All Reduction	One to One Reduction	This is an explaination.
75	2	The message can be broadcast in how many steps?	Log(p)	Log(p^2)	One	Sin(p)	The message can be broadcast in log p steps.
76	2	This equation is used to solve which operations?	All to All personalized communication	One-to-all personalized communication	One to one personalized communication	All-to-one personalized communication.	This is an Explaination.

	marks	question	A	B	C	D	ans
77	2	There are how many computations for n^2 words of data transferred among the nodes?	N^3	Tan n	E^n	Log n	There are n^3 computations for n^2 words of data transferred among the nodes.
78	2	Scatter Operation is also known as?	One-to-all personalized communication	One-to-one personalized communication	All-to-one personalized communication	All-to-all personalized communication.	Scatter opeartion is also known as One-to-all personalized communication.
79	2	A Hypercube with 2d nodes can be regarded as a d-dimensional mesh with____ nodes in each dimension.	Two	One	Three	Four	A hypercube with 2d nodes can be regarded as a d-dimensional mesh with two nodes in each dimension
80	2	One-to-all broadcast and all-to-one reduction are used in several important parallel algorithms including?	All	Gausiian Elimination	Shortest path Algo.	Matrix- Vector multiplication	This is an Explaination.
81	2	Each node of the distributed-memory parallel computer is a_____ shared-memory multiprocessor.	NUMA	UMA	CCMA	None	Each node of the distributed-memory parallel computer is a NUMA shared-memory multiprocessor.
82	2	To perform a q-shift, we expand q as a sum of distinct powers of_____?	2	3	e	Log p	To perform a q-shift, we expand q as a sum of distinct powers of 2 .
83	3	In which implementation of circular shift, the entire row to data set is shifted by	Mesh	Hypercube	Ring	Linear	This is an Explaination
84	3	On a p-node hypercube with all-port communication, the coefficients of tw in the expressions for the communication times of one-to-all and all-to-all broadcast and personalized communication are all smaller than their single-port counterparts by a factor of?	Log(p)	Cos(p)	Sin(p)	E^p	On a p-node hypercube with all-port communication, the coefficients of tw in the expressions for the communication times of one-to-all and all-to-all broadcast and personalized communication are all smaller than their single-port counterparts by a factor of log p.

	marks	question	A	B	C	D	ans
85	3	The Equation represents which analysis in All to All Broadcasts?	Cost Analysis	Time Analysis	Data Model Analysis	Space-Time Analysis	Ans-(c) Cost Analysis.
86	3	On a p-node hypercube, the size of each message exchanged in the i th of the log p steps is?	A	B	C	D	A
87	3	Which broadcast is applied on this 3D hypercube?	One to All Broadcast	One to One Broadcast	All to One Broadcast	All to one Reduction	This figure shows One to All Broadcast being applied on 3D hypercube.
88	3	The Equation represents which analysis in One to All Broadcasts?	Cost Analysis	Time Analysis	Data Analysis	Space Analysis	This is an explaination.
89	3	The time for circular shift on a hypercube can be improved by almost a factor of _____ for large messages.	Log p	Cos(p)	e^p	Sin p	The time for circular shift on a hypercube can be improved by almost a factor of log p for large messages.
90	1	The execution time of parallel algorithm doesnâ€™t depends upon?	Processor	Input Size	Relative computation	Communication speed	The execution time of a parallel algorithm depends not only on input size but also on the number of processing elements used, and their relative computation and interprocess communication speeds.
91	1	Processing elements in a parallel system may become idle due to many reasons such as:	Both	Synchronization	Load Imbalance	The processing element doesnâ€™t become idle.	Both synchronization and load imbalance
92	1	If the scaled-speedup curve is close to linear with respect to the number of processing elements, then the parallel system is considered as?	Scalable	Iso-scalable	Non-Scalable	Scale-Efficient	If the scaled-speedup curve is close to linear with respect to the number of processing elements, then the parallel system is considered scalable

	marks	question	A	B	C	D	ans
93	1	Which system is the combination of an algorithm and the parallel architecture on which it is implemented?	Parallel System	Data- Parallel System	Architecture System	Series System	A parallel system is the combination of an algorithm and the parallel architecture on which it is implemented
94	1	What is defined as the speedup obtained when the problem size is increased linearly with the number of processing elements?	Scalable Speedup	Unscalable Speedup	Superlinearity Speedup	Isoefficiency Speedup	Scalable Speedup defined as the speedup obtained when the problem size is increased linearly with the number of processing elements
95	1	The maximum number of tasks that can be executed simultaneously at any time in a parallel algorithm is called its degree of_____.	Concurrency	Parallelism	Linearity	Execution	The maximum number of tasks that can be executed simultaneously at any time in a parallel algorithm is called its degree of concurrency.
96	1	The isoefficiency due to concurrency in 2-D partitioning is:	O(p)	O(n Logp)	O(1)	O(n^2)	This is an explaination.
97	2	The total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element is known as?	Total Overhead	Overhead	Serial Runtime	Parallel Runtime	We define total overhead of a parallel system as the total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element.
98	2	Parallel computations involving matrices and vectors readily lend themselves to data _____.	Decomposition	Composition	Linearity	Parallelsim	Parallel computations involving\nmatrices and vectors readily lend themselves to data decomposition.

	marks	question	A	B	C	D	ans
99	2	Parallel 1-D with Pipelining is a_____ algorithm?	Synchronous	Asynchronous	Optimal	Cost-optimal	This is an explaination.
100	2	The serial complexity of Matrix-Matrix Multiplication is:	Õ•(n^3)	O(n^2)	O(n)	O(nlogn)	This is an explaination
101	2	What is the problem size for n x n matrix multiplication?	Ï´(n^3)	Ï´(nlogn)	Ï´(n^2)	Ï´(1)	Ï´(n^3) is the problem size.
102	2	The given equation represents which function?	Overhead Function	Parallel Model	Series Overtime	Parallel Overtime	This is an explaination.
103	2	The efficiency of a parallel program can be written as:	A	B	C	D	A
104	2	The total number of steps in the entire pipelined procedure is_____?	Î˜(n)	Î˜(n^2)	Î˜(n^3)	Î˜(1)	The total number of steps in the entire pipelined procedure is Î˜(n)
105	2	In Canon's Algorithm, the memory used is?	Î¸(n^2)	Î¸(n)	Î¸(n^3)	Î¸(nlogn)	This is an explaination.
106	2	Consider the problem of multiplying two n Ã— n dense, square\nmatrices A and B to yield the product matrix C =:	AÃ—B	A/B	A+B	A-B	Consider the problem of multiplying two n Ã— n dense, square\nmatrices A and B to yield the product matrix C = A Ã— B.
107	2	The serial runtime of multiplying a matrix of dimension n x n with a vector is?	A	B	C	D	A
108	2	_____is a measure of the fraction of time for which a processing element is usefully employed.	Efficiency	Linearity	Overtime Function	Superlinearity	Efficiency is a measure of the fraction of time for which a processing element is usefully employed.
109	2	When the work performed by a serial algorithm is greater than its parallel formulation or due to hardware features that put the serial implementation at a disadvantage.This phenomena is known as?	Superlinear Speedup	Linear Speedups	Super Linearity	Performance Metrics	This is an explaintion
110	3	The all-to-all broadcast and the computation of y[i] both take time?	Î˜(n)	Î˜(nlogn)	Î˜(n^2)	Î˜(n^3)	This is an explaination.

	marks	question	A	B	C	D	ans
111	3	If virtual processing elements are mapped appropriately onto physical processing elements, the overall communication time does not grow by more than a factor of	N/p	P/n	N+p	N*p	If virtual processing elements are mapped appropriately onto physical processing elements, the overall communication time does not grow by more than a factor of n/p
112	3	Parallel execution time can be expressed as a function of problem size, overhead function, and the number of processing elements.The Formed eqn is:	A	B	C	D	A
113	3	In 2-D partioning, the first alignment takes time=?	Ts + twn/âˆšp.\n	Ts - twn/âˆšp.\n	Ts*twn/âˆšp.\n	Ts/ twn*âˆšp.\n	Ts + twn/âˆšp.\n
114	3	Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called_____?	Scaling Down	Scaling up	Scaling	Stimulation	Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called scaling down.
115	3	Which of the following is a drawback of matrix matrix multiplication?	Memory Optimal	Efficient	Time-bound	Complex	This is an explaination
116	3	Consider the problem of sorting 1024 numbers (n = 1024, log n = 10) on 32 processing elements. The speedup expected is	P/log n	P*log n	P+logn	N*log p	Consider the problem of sorting 1024 numbers (n = 1024, log n = 10) on 32 processing elements. The speedup expected is p/logn
117	3	Consider the problem of adding n numbers on p processing elements such that p < n and both n and p are powers of 2. The overall parallel execution time of the problem is:	ê™¨((n/p) log p).	ê™¨((n*p) log p).	ê™¨((p/n) log p).	ê™¨((n) log p).	Ans-(a)-ê™¨((n/p) log p).
118	3	DNS algorithm has____ runtime?	â„¦(n)	â„¦(n^2)	â„¦(n^3)	â„¦(logn)	DNS has â„¦(n) runtime

	marks	question	A	B	C	D	ans
119	3	The serial algorithm requires_____ multiplications and additions in matrix-vector multiplication.\n	N^2	N^3	Log n	Nlog(n)	Ans-(b)-n^2. The serial algorithm requires n^2 multiplications and additions.\n\n
120	1	The time required to merge two sorted blocks of n/p elements is_____?\n\n	Î,(n/p)	Î,(n)	Î,(p/n)	Î,(nlogp)	The time required to merge two sorted blocks of n/p elements is Î,(n/p).\n\n
121	1	In Parallel DFS,the stack is split into two equal pieces such that the size of the search space represented by each stack is the same. Such a split is called?.	Half-Split	Half-Split	Parallel-Split	None	The stack is split into two equal pieces such that the size of the search space represented by each stack is the same. Such a split is called a half-split.
122	1	To avoid sending very small amounts of work, nodes beyond a specified stack depth are not given away. This depth is called the_____depth.	Cut-Off	Breakdown	Full	Series	To avoid sending very small amounts of work, nodes beyond a specified stack depth are not given away. This depth is called the cutoff depth.
123	1	In sequential sorting algorithms, the input and the sorted sequences are stored in which memory?	Process Memory	Secondary Memory	Main Memory	External Memory	In sequential sorting algorithms, the input and the sorted sequences are stored in the process's memory
124	1	Each process sends its block to the other process. Now, each process merges the two sorted blocks and retains only the appropriate half of the merged block. We refer to this operation as?	Compare-Split	Split	Compare	Exchange.	Each process sends its block to the other process. Now, each process merges the two sorted blocks and retains only the appropriate half of the merged block. We refer to this operation as compare-split.

	marks	question	A	B	C	D	ans
125	1	Each process compares the received element with its own and retains the appropriate element.We refer this operation as_____?	Compare Exchange	Exchange	Process-Exchange	All	Each process compares the received element with its own and retains the appropriate element. We refer this as compare exchange.
126	1	Which algorithm maintains the unexpanded nodes in the search graph, ordered according to their l-value?	Parallel BFS	Parallel DFS	Both a and b	None	Parallel BFS maintains the unexpanded nodes in the search graph, ordered according to their l-value.
127	1	The critical issue in parallel depth-first search algorithms is the distribution of the search space among the_____?	Processor	Space	Memory	Blocks	The critical issue in parallel depth-first search algorithms is the distribution of the search space among the processors
128	2	Enumeration Sort uses how many processes to sort n elements?	N^2	Logn	N^3	N	This is an explaination.
129	2	Which sequence is a sequence of elements <a0, a1, ..., an-1> with the property that either (1) there exists an index i, 0 â‰¤ i â‰¤n - 1, such that <a0, ..., ai > is monotonically increasing and <ai +1, ..., an-1> is monotonically decreasing, or (2) there exists a cyclic shift of indices so that (1) is satisfied.	Bitonic Sequence	Acyclic Sequence	Asymptotic Sequence	Cyclic Sequence.	A bitonic sequence is a sequence of elements <a0, a1, ..., an-1> with the property that either (1) there exists an index i, 0 i n - 1, such that <a0, ..., ai > is monotonically increasing and <ai +1, ..., an-1> is monotonically decreasing, or (2) there exists a cyclic shift of indices so that (1) is satisfied

	marks	question	A	B	C	D	ans
130	2	To make a substantial improvement over odd-even transposition sort, we need an algorithm that moves elements long distances. Which one of these is such serial sorting algorithm?	Shell Sort	Linear Sort	Quick-Sort	Bubble Sort	To make a substantial improvement over odd-even transposition sort, we need an algorithm that moves elements long distances. Shellsort is one such serial sorting algorithm.
131	2	Quick-Sort is a_____ algorithm?	Divide and Conquer	Greedy Approach	Both a and b	None	Quicksort is a Divide and Conquer algorithm.
132	2	The_____ transposition algorithm sorts n elements in n phases (n is even), each of which requires n/2 compare-exchange operations.	Odd-Even	Odd	Even	None	This is an explaination.
133	2	The average time complexity for Bucket Sort is?	O(n+k)	O(nlog(n+k))	O(n^3)	Î,(n^2)	The average time complexity for Bucket Sort is O(n + k).
134	2	A popular serial algorithm for sorting an array of n elements whose values are uniformly distributed over an interval [a, b] is which algorithm?	Bucket Sort	Quick-Sort Algo.	Linear Sort	Bubble-Sort	A popular serial algorithm for sorting an array of n elements whose values are uniformly distributed over an interval [a, b] is the bucket sort algorithm
135	2	Best Case time complexity of Bubble Sort is:	O(n)	O(n^3)	O(nlogn)	O(n^2)	Best case complexity of bubblesort is O(n).

	marks	question	A	B	C	D	ans
136	2	When more than one process tries to write to the same memory location, only one arbitrarily chosen process is allowed to write, and the remaining writes are ignored. This process is called_____ in quick sort.	CRCW-PRAM	PRAM	Partitioning	CRCW	When more than one process tries to write to the same memory location, only one arbitrarily chosen process is allowed to write, and the remaining writes are ignored.It is called CRCW PRAM quick sort algo.
137	2	Average Time Complexity in a quicksort algorithm is:	O(nlogn)	O(n)	O(n^3)	Î¸(n^2)	This is an explainatoin.
138	2	The isoefficiency function of Global Round Robin (GRR) is:	O (p^2 log p)	O (p log p)	O (log p)	O (p^2)	The isoefficiency function of GRR is O (p^2 log p)
139	2	A_____ is a device with two inputs x and y and two outputs x' and y' in a Sorting Network.	Comparator	Router	Separator	Switch.	A comparator is a device with two inputs x and y and two outputs x' and y'
140	2	If T is a DFS tree in G then the parallel implementation of the algorithm runs in _____time complexity.	O(t)	O(tlogn)	O(logt)	O(1)	If T is a DFS tree in G then the parallel implementation of the algorithm outputs a proof that can be verified in O(t) time complexity.
141	2	In the quest for fast sorting methods, a number of networks have been designed that sort n elements in time significantly smaller than___?	Î¸(nlogn)	Î¸(n)	Î¸(1)	Î¸(n^2)	In the quest for fast sorting methods, a number of networks have been designed that sort n elements in time significantly smaller than Î¸(nlogn).
142	2	The average value of the search overhead factor in parallel DFS is less than_____?	One	Two	Three	Four	The average value of the search overhead factor in parallel DFS is less than one
143	3	Parallel runtime for Ring architecture in a bitonic sort is:	Î¸(n)	Î¸(nlogn)	Î¸(n^2)	Î¸(n^3)	Parallel runtime for Ring architecture in a bitonic sort is Î¸(n)

	marks	question	A	B	C	D	ans
144	3	The Sequential Complexity of Odd-Even Transposition Algorithm is:	Î¸(n^2)	Î¸(nlogn)	Î¸(n^3)	Î¸(n)	This is an explaination.
145	3	The Algorithm represents which bubble sort:	Sequential Bubble Sort	Circular Bubble Sort	Simple Bubble Sort	Linear Bubble Sort	This is an explaination.
146	3	Enumeration Sort uses how much time to sort n elements?	Î¸(1)	Î¸(nlogn)	Î¸(n^2)	Î¸(n)	This is an explaination.
147	3	The_____algorithm relies on the binary representation of the elements to be sorted.	Radix-sort	Bubble Sort	Quick-Sort	Bucket-Sort	The radix sort algorithm relies on the binary representation of the elements to be sorted.
148	3	Parallel runtime for Mesh architecture in a bitonic sort is:	Î¸(n/logn)	Î¸(n)	Î¸(n^2)	Î¸(n^3)	This is an explaination.
149	1	The number of threads in a thread block is limited by the architecture to a total of how many threads per block?	512	502	510	412	The number of threads in a thread block is also limited by the architecture to a total of 512 threads per block
150	1	CUDA Architecture is mainly provided by which company?	NVIDIA	Intel	Apple	IBM	NVIDIA provides CUDA services.
151	1	In CUDA Architecture, what are subprograms called?	Kernel	Grid	Element	Blocks	Subprograms are called kernels.
152	1	What is the fullform of CUDA?	Compute Unified Device Architecture	Computer Unified Device Architecture	Common USB Device Architecture	Common Unified Disk Architecture	CUDA Stands for Compute Unified Device Architecture.
153	2	Which of these is not an application of CUDA Arhitecture?	Thermo Dynamics	Neural Networks	VLSI Stimulation	Fluid Dynamics	CUDA architecture has no use on Thermo Dynamics.
154	2	CUDA programming is especially well-suited to address problems that can be expressed as_____ computations.	Data parallel	Task Parallel	Both a and b	None	CUDA programming is especially well-suited to address problems that can be expressed as dataparallel computations.
155	2	CUDA C/C++ uses which keyword in programming:	global	kernel	Cuda_void	nvcc	This is an explaination.
156	2	CUDA programs are saved with_____ extension.	.cd	.cx	.cc	.cu	This is an explaination

	marks	question	A	B	C	D	ans
157	2	The Kepler K20-X chip block, contains____ streaming multiprocessors\n(SMs).	15	8	16	7	The Kepler K20X chip block diagram, containing 15 streaming multiprocessors (SMs)
158	2	The Kepler K20X architecture increases the register file size to:	64K	32K	128K	256K	The K20X architecture increases the register fi le size to 64K
159	2	The register file in a GPU is of what size?	2 MB	1 MB	3MB	1024B	Register size in a GPU is 2MB.
160	2	NVIDIAâ€™s GPU computing platform is not enabled on which of the following product families:	AMD	Tegra	Quadro	Tesla	This is an explaination.
161	2	Tesla K-40 has compute capability of:	3.5	3.2	3.4	3.1	This is an explaination.
162	2	The SIMD unit creates, manages, schedules and executes_____ threads simultaneously to create a warp.	32	16	24	8	The SIMD unit creates, manages, schedules and executes 32 threads simultaneously to create a warp
163	2	Which hardware is used by the host interface to fasten the transfer of bulk data to and fro the graphics pipeline?	Direct Memory Access	Switch	Hub	Memory Hardware	This is an Explaination
164	2	A ____ is a collection of thread blocks of the same thread dimensionality which all execute the same kernel.	Grid	Core	Element	Blcoks	A â€˜gridâ€™ is a collection of thread blocks of the same thread dimensionality which all execute the same kernel
165	2	Active Warps can be classified into how many types?	3	2	4	5	This is an explaination.
166	2	All threads in a grid share the same_____space.	Global memory	Local Memory	Synchronized Memory	All	All threads in a grid\nshare the same global memory space
167	2	CUDA was introduced in which year?	2007	2006	2008	2010	This is an explaination.

	marks	question	A	B	C	D	ans
168	3	Unlike a C function call, all CUDA kernel launches are:	Asynchronous	Synchronous	Both a and b	None	Unlike a C function call, all CUDA kernel launches are asynchronous
169	3	A warp consists of____consecutive threads and all threads in a warp are executed in Single Instruction Multiple Thread (SIMT) fashion.	32	16	64	128	A warp consists of 32 consecutive threads and all\nthreads in a warp are executed in Single Instruction Multiple Thread (SIMT) fashion
170	3	There are how many streaming multiprocessors in CUDA architecture?	16	8	12	4	This is an explaination.
171	3	In CUDA programming, if CPU is the host then device will be:	GPU	Compiler	HDD	GPGPU	This is an explaination.
172	3	Both grids and blocks use the_____ type with three unsigned integer fields.	Dim3	Dim2	Dim1	Dim4	Both grids and blocks use the dim3 type with three unsigned integer fi elds
173	3	Tesla P100 GPU based on the Pascal GPU Architecture has 56 Streaming Multiprocessors (SMs), each capable of supporting up to____active threads.	2048	512	1024	256	Tesla P100 GPU based on the Pascal GPU Architecture has 56 Streaming Multiprocessors (SMs), each capable of supporting up to 2048 active threads.
174	3	The maximum size at each level of the thread hierarchy is_____dependent.	Device	Host	Compiler	Memory	The maximum size at each level of the thread hierarchy is device dependent.
175	3	Intel I7 has the memory bus of width:	19B	180B	152B	102B	This is an explaination.
176	3	The_____ is the heart of the GPU architecture:	Streaming Multiprocessor	Multiprocessor	CUDA	Compiler	The Streaming Multiprocessor (SM) is the heart of the GPU architecture.

	marks	question	A	B	C	D	ans
177	3	A kernel is defined using the_____ declaration specification	_global	_host	_device	_void	A kernel is defi ned using the\n__global declaration specifi cation
178	3	The function printThreadInfo() is not used to print out which of the following information about each thread:	Memory Allocations	Block Index	Matrix Coordinates	Control-Index	Ans-(d)- Memory Allocations.

UNIT 1

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1. Which is the type of Microcomputer Memory

Address
Contents
Both a and b
none
Ans:
Both a and b

2. A collection of lines that connects several devices is called

Bus
Peripheral connection wires
Both a and b
internal wires
Ans:
Bus

3. Conventional architectures coarsely comprise of a

Processor
Memory System
Data path
All of the above
Ans:
All of the above

4. VLIW processors rely on

Compile time analysis
Initial time analysis
Final time analysis
id time analysis
Ans:
Compile time analysis

5. HPC is not used in high span bridges

True
False
Ans:
False

6. The access time of memory is …… the time required for performing any single CPU operation.

longer than
shorter than

negligible than
same as
Ans:
longer than

7. Data intensive applications utilize_

High aggregate throughput
High aggregate network bandwidth
high processing and memory system performance
none of above
Ans:
High aggregate throughput

8. Memory system performance is largely captured by_

Latency
bandwidth
both a and b
none of above
Ans:
both a and b

9. A processor performing fetch or decoding of different instruction during the execution of another instruction is called __ .

Super-scaling
Pipe-lining
Parallel Computation
none of above
Ans:
Pipe-lining

10. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution ?

ISA
ANSA
Super-scalar
All of the above
Ans:
Super-scalar

high performance computing mcq sppu
11. HPC works out to be economical.

True
false
Ans:
True

12. High Performance Computing of the Computer System tasks are done by

Node Cluster
Network Cluster
Beowulf Cluster
Stratified Cluster
Ans:
Beowulf Cluster

13. Octa Core Processors are the processors of the computer system that contains

2 Processors
4 Processors
6 Processors
8 Processors
Ans:
8 Processors

14. Parallel computing uses _ execution

sequential
unique
simultaneous
None of above
Ans:
simultaneous

15. Which of the following is NOT a characteristic of parallel computing?

Breaks a task into pieces
Uses a single processor or computer
Simultaneous execution
May use networking
Ans:
Uses a single processor or computer

16. Which of the following is true about parallel computing performance?

Computations use multiple processors
There is an increase in speed
The increase in speed is loosely tied to the number of processor or computers used
All of the **Ans:**s are correct.
Ans:
All of the **Ans:**s are correct.

17. __ leads to concurrency.

Serialization
Parallelism
Serial processing
Distribution

Ans:
Parallelism

18. MIPS stands for?

Mandatory Instructions/sec
Millions of Instructions/sec
Most of Instructions/sec
Many Instructions / sec
Ans:
Millions of Instructions/sec

19. Which MIMD systems are best scalable with respect to the number of processors

Distributed memory computers
ccNUMA systems
Symmetric multiprocessors
None of above
Ans:
Distributed memory computers

high performance computing mcq questions
20. To which class of systems does the von Neumann computer belong?

SIMD (Single Instruction Multiple Data)
MIMD (Multiple Instruction Multiple Data)
MISD (Multiple Instruction Single Data)
SISD (Single Instruction Single Data)
Ans:
SISD (Single Instruction Single Data)

21. Which of the architecture is power efficient?

CISC
RISC
ISA
IANA
Ans:
RISC

22. Pipe-lining is a unique feature of _.

RISC
CISC
ISA
IANA
Ans:
RISC

23. The computer architecture aimed at reducing the time of execution of instructions is __.

RISC
CISC
ISA
IANA
Ans:
RISC

24. Type of microcomputer memory is

processor memory
primary memory
secondary memory
All of above
Ans:
All of above

25. A pipeline is like_

Overlaps various stages of instruction execution to achieve performance.
House pipeline
Both a and b
A gas line
Ans:
Overlaps various stages of instruction execution to achieve performance.

High Performance Computing mcq pdf
High Performance Computing mcq pdf unit 1Download
26. Scheduling of instructions is determined_

True Data Dependency
Resource Dependency
Branch Dependency
All of above
Ans:
All of above

27. The fraction of data references satisfied by the cache is called_

Cache hit ratio
Cache fit ratio
Cache best ratio
none of above
Ans:
Cache hit ratio

28. A single control unit that dispatches the same Instruction to various processors is__

SIMD
SPMD
MIMD
none of above

Ans:
SIMD

29. The primary forms of data exchange between parallel tasks are_

Accessing a shared data space
Exchanging messages.
Both A and B
none of above
Ans:
Both A and B

30. Switches map a fixed number of inputs to outputs.

True
False
Ans:
True

UNIT 2

---

1. The First step in developing a parallel algorithm is_

To Decompose the problem into tasks that can be executed concurrently
Execute directly
Execute indirectly
None of Above
Ans:
To Decompose the problem into tasks that can be executed concurrently

2. The number of tasks into which a problem is decomposed determines its_

Granularity
Priority
Modernity
None of Above
Ans:
Granularity

3. The length of the longest path in a task dependency graph is called_

the critical path length
the critical data length
the critical bit length
None of Above
Ans:
he critical path length

4. The graph of tasks (nodes) and their interactions/data exchange (edges)_

Is referred to as a task interaction graph
Is referred to as a task Communication graph
Is referred to as a task interface graph
None of Above
Ans:
Is referred to as a task interaction graph

5. Mappings are determined by_

task dependency
task interaction graphs
Both A and B
None of Above
Ans:
Both A and B

6. Decomposition Techniques are_

recursive decomposition
data decomposition
exploratory decomposition
speculative decomposition
All of above
Ans:
All of above

7. The Owner Computes rule generally states that the process assigned a particular data item is responsible for _

All computation associated with it
Only one computation
Only two computation
Only occasionally computation
Ans:
All computation associated with it

8. A simple application of exploratory decomposition is_

The solution to a 15 puzzle
The solution to 20 puzzle
The solution to any puzzle
None of Above
Ans:
The solution to a 15 puzzle

9. Speculative Decomposition consist of _

conservative approaches
optimistic approaches
Both A and B
only B

Ans:
Both A and B

hpc mcq questions
10. task characteristics include:

Task generation.
Task sizes.
Size of data associated with tasks.
All of above
Ans:
All of above

11. What is a high performance multi-core processor that can be used to accelerate a wide variety of applications using parallel computing.

CLU
GPU
CPU
DSP
Ans:
GPU

12. What is GPU?

Grouped Processing Unit
Graphics Processing Unit
Graphical Performance Utility
Graphical Portable Unit
Ans:
Graphics Processing Unit

13. A code, known as GRID, which runs on GPU consisting of a set of

32 Thread
32 Block
Unit Block
Thread Block
Ans:
Thread Block

14. Interprocessor communication that takes place

Centralized memory
Shared memory
Message passing
Both A and B
Ans:
Both A and B

15. Decomposition into a large number of tasks results in coarse-grained decomposition

True
False
Ans:
False

16. Relevant task characteristics include

Task generation.
Task sizes
Size of data associated with tasks
Overhead
both A and B
Ans:
both A and B

17. The fetch and execution cycles are interleaved with the help of __

Modification in processor architecture
Clock
Special unit
Control unit
Ans:
Clock

18. The processor of system which can read /write GPU memory is known as

kernal
device
Server
Host
Ans:
Host

19. Increasing the granularity of decomposition and utilizing the resulting concurrency to perform more tasks in parallel decreses performance.

TRUE
FALSE
Ans:
FALSE

Parallel computing mcq with answers
20. If there is dependency between tasks it implies their is no need of interaction between them.

TRUE
FALSE
Ans:
FALSE

21. Parallel quick sort is example of task parallel model

TRUE
FALSE
Ans:
TRUE

22. True Data Dependency is

The result of one operation is an input to the next.
Two operations require the same resource.
Ans:
The result of one operation is an input to the next.

23. What is Granularity ?

The size of database
The size of data item
The size of record
The size of file
Ans:
The size of data item

24. In coarse-grained parallelism, a program is split into …… task and …… Size

Large tasks , Smaller Size
Small Tasks , Larger Size
Small Tasks , Smaller Size
Equal task, Equal Size
Ans:
Large tasks , Smaller Size

UNIT 3

---

1. The primary and essential mechanism to support the sparse matrices is

Gather-scatter operations
Gather operations
Scatter operations
Gather-scatter technique
Ans:
Gather-scatter operations

2. In the gather operation, a single node collects a ———

Unique message from each node
Unique message from only one node
Different message from each node
None of Above

Ans:
Unique message from each node

3. In the scatter operation, a single node sends a ————

Unique message of size m to every other node
Different message of size m to every other node
Different message of different size m to every other node
All of Above
Ans:
Unique message of size m to every other node

4. Is All to all Bradcasting is same as All to all personalized communication?

Yes
No
Ans:
No

5. Is scatter operation is same as Broadcast?

Yes
No
Ans:
No

6. All-to-all personalized communication is also known as

Total Exchange
Personal Message
Scatter
Gather
Ans:
Total Exchange

7. By which way, scatter operation is different than broadcast

Message size
Number of nodes
Same
None of above
Ans:
Message size

8. The gather operation is exactly the _ of the scatter operation

Inverse
Reverse
Multiple
Same
Ans:

Inverse

9. The gather operation is exactly the inverse of the_

Scatter operation
Broadcast operation
Prefix Sum
Reduction operation
Ans:
Scatter operation

hpc mcq questions
10. The dual of one-to-all broadcast is all-to-one reduction. True or False?

TRUE
FALSE
Ans:
TRUE

11. A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes.

TRUE
FALSE
Ans:
TRUE

12. Group communication operations are built using point-to-point messaging primitives

TRUE
FALSE
Ans:
TRUE

13. Communicating a message of size m over an uncongested network takes time ts + tmw

True
False
Ans:
True

14. Parallel programs: Which speedup could be achieved according to Amdahl´s law for infinite number of processors if 5% of a program is sequential and the remaining part is ideally parallel?

Infinite speedup
5
20
None of above
Ans:
20

15. Shift register that performs a circular shift is called

Invalid Counter
Valid Counter
Ring
Undefined
Ans:
Ring

16. 8 bit information can be stored in

2 Registers
4 Registers
6 Registers
8 Registers
Ans:
8 Registers

17. The result of prefix expression * / b + – d a c d, where a = 3, b = 6, c = 1, d = 5 is

0
5
10
8
Ans:
10

18. The height of a binary tree is the maximum number of edges in any root to leaf path. The maximum number of nodes in a binary tree of height h is?

2h – 1
2h – 1 – 1
2h + 1 – 1
2 * (h+1)
Ans:
2h + 1 – 1

19. A hypercube has_

2^d nodes
2d nodes
2n Nodes
N Nodes
Ans:
2^d nodes

Parallel computing mcq with answers
20. The Prefix Sum Operation can be implemented using the_

All-to-all broadcast kernel
All-to-one broadcast kernel
One-to-all broadcast Kernel

Scatter Kernel
Ans:
All-to-all broadcast kernel

21.In the scatter operation_

Single node send a unique message of size m to every other node
Single node send a same message of size m to every other node
Single node send a unique message of size m to next node
None of Above
Ans:
Single node send a unique message of size m to every other node

22. In All-to-All Personalized Communication Each node has a distinct message of size m for every other node

True
False
Ans:
True

23. A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes.

True
False
Ans:
True

24. In All-to-All Broadcast each processor is thesource as well as destination.

True
False
Ans:
True

UNIT 4

---

1. mathematically efficiency is

e=s/p
e=p/s
e*s=p/2
e=p+e/e
Ans:
e=s/p

2. Cost of a parallel system is sometimes referred to____ of product

work
processor time
both
none
Ans:
both

3. Scaling Characteristics of Parallel Programs Ts is

increase
constant
decreases
none
Ans:
constant

4. Speedup tends to saturate and efficiency _ as a consequence of Amdahl's law.

increase
constant
decreases
none
Ans:
decreases

5. Speedup obtained when the problem size is _____ linearly with the number of processing elements.

increase
constant
decreases
depend on problem size
Ans:
increase

6. The n × n matrix is partitioned among n processors, with each processor storing complete ___ _ of the matrix.

row
column
both
depend on processor
Ans:
row

7. cost-optimal parallel systems have an efficiency of _____

1
n
logn
complex
Ans:

1

8. The n × n matrix is partitioned among n2 processors such that each processor owns a _ element

n
2n
single
double
Ans:
single

9. how many basic communication operations are used in matrix vector multiplication

1
2
3
4
Ans:
3

10. In DNS algorithm of matrix multiplication it used

1d partition
2d partition
3d partition
both a,b
Ans:
3d partition

high performance computing mcq sppu
11. In the Pipelined Execution, steps contain

normalization
communication
elimination
all
Ans:
all

12. the cost of the parallel algorithm is higher than the sequential run time by a factor of __

3/2
2/3
3*2
2/3+3/2
Ans:
3/2

13. The load imbalance problem in Parallel Gaussian Elimination: can be alleviated by using a __

mapping

acyclic
cyclic
both
none
Ans:
acyclic

14. A parallel algorithm is evaluated by its runtime in function of

the input size,
the number of processors,
the communication parameters.
all
Ans:
all

15. For a problem consisting of W units of work, p__W processors can be used optimally

<=
>=
<
>
Ans:
16. C(W)__Θ(W) for optimality (necessary condition).

>
<
<=
equals
Ans:
equals

17. many interactions in oractical parallel programs occur in ____ pattern

well defined
zig-zac
reverse
straight
Ans:
well defined

18. efficient implementation of basic communication operation can improve

performance
communication
algorithm
all
Ans:
performance

19. efficient use of basic communication operations can reduce

development effort
software quality
both
none
Ans:
development effort

high performance computing mcq questions
20. Group communication operations are built using _____ Messenging primitives.

point-to-point
one-to-all
all-to-one
none
Ans:
point-to-point

21. one processor has a piece of data and it need to send to everyone is

one -to-all
all-to-one
point -to-point
all of above
Ans:
one -to-all

22. wimpleat way to send p-1 messages from source to the other p-1 processors

Algorithm
communication
concurrency
receiver
Ans:
concurrency

23. In a eight node ring, node __ is source of broadcast

1
2
8
0
Ans:
0

24. The processors compute __ product of the vector element and the local matrix

local
global
both
none

Ans:
local

25. one to all broadcast use

recursive doubling
simple algorithm
both
none
Ans:
recursive doubling

26. In a broadcast and reduction on a balanced binary tree reduction is done in __

recursive order
straight order
vertical order
parallel order
Ans:
recursive order

27. if “X” is the message to broadcast it initially resides at the source node

1
2
8
0
Ans:
0

28. logical operators used in algorithm are

XOR
AND
both
none
Ans:
both

29. Generalization of broadcast in Which each processor is

Source as well as destination
only source
only destination
none
Ans:
Source as well as destination

30. The algorithm terminates in _ steps

p

p+1
p+2
p-1
Ans:
p-1

30. Each node first sends to one of its neighbours the data it need to….

broadcast
identify
verify
none
Ans:
broadcast

30. The second communication phase is a columnwise __ broadcast of consolidated

All-to-all
one -to-all
all-to-one
point-to-point
Ans:
All-to-all

30. All nodes collects _ message corresponding to √p nodes to their respectively

√p
p
p+1
p-1
Ans:
√p

30. It is not possible to port __ for higher dimensional network

Algorithm
hypercube
both
none
Ans:
Algorithm

30. If we port algorithm to higher dimemsional network it would cause

error
contention
recursion
none
Ans:
contention

30. In the scatter operation __ node send message to every other node

single
double
triple
none
Ans:
single

30. The gather Operation is exactly the inverse of _

scatter operation
recursion operation
execution
none
Ans:
scatter operation

30. Similar communication pattern to all-to-all broadcast except in the_____

reverse order
parallel order
straight order
vertical order
Ans:
reverse order

UNIT 5

---

1. In _, the number of elements to be sorted is small enough to fit into the process's main memory.

internal sorting
internal searching
external sorting
external searching
Ans:
internal sorting

2. __ algorithms use auxiliary storage (such as tapes and hard disks) for sorting because the number of elements to be sorted is too large to fit into memory.

internal sorting
internal searching
External sorting
external searching
Ans:
External sorting

3. __ can be comparison-based or noncomparison-based.

searching
Sorting
both a and b
none of above
Ans:
Sorting

4. The fundamental operation of comparison-based sorting is __

compare-exchange
searching
Sorting
swapping
Ans:
compare-exchange

5. The complexity of bubble sort is Θ(n^2)

TRUE
FALSE
Ans:
TRUE

6. Bubble sort is difficult to parallelize since the algorithm has no concurrency.

TRUE
FALSE
Ans:
TRUE

7. Quicksort is one of the most common sorting algorithms for sequential computers because of its simplicity, low overhead, and optimal average complexity.

TRUE
FALSE
Ans:
TRUE

8. The performance of quicksort depends critically on the quality of the __

non-pivote
pivot
center element
len of array
Ans:
pivot

9. the complexity of quicksort is O(nlog n)

TRUE

FALSE
Ans:
TRUE

10. DFS begins by expanding the initial node and generating its successors. In each subsequent step, DFS expands one of the most recently generated nodes.

TRUE
FALSE
Ans:
TRUE

high performance computing mcq sppu
11. The main advantage of __ is that its storage requirement is linear in the depth of the state space being searched.

BFS
DFS
a and b
none of above
Ans:
DFS

12. _ algorithms use a heuristic to guide search.

BFS
DFS
a and b
none of above
Ans:
BFS

13. If the heuristic is admissible, the BFS finds the optimal solution.

TRUE
FALSE
Ans:
TRUE

14. The search overhead factor of the parallel system is defined as the ratio of the work done by the parallel formulation to that done by the sequential formulation

TRUE
FALSE
Ans:
TRUE

15. The critical issue in parallel depth-first search algorithms is the distribution of the search space among the processors.

TRUE

FALSE
Ans:
TRUE

16. Graph search involves a closed list, where the major operation is a _

sorting
searching
lookup
none of above
Ans:
lookup

17. Breadth First Search is equivalent to which of the traversal in the Binary Trees?

Pre-order Traversal
Post-order Traversal
Level-order Traversal
In-order Traversal
Ans:
Level-order Traversal

18. Time Complexity of Breadth First Search is? (V – number of vertices, E – number of edges)

O(V + E)
O(V)
O(E)
O(V*E)
Ans:
O(V + E)

19. Which of the following is not an application of Breadth First Search?

When the graph is a Binary Tree
When the graph is a Linked List
When the graph is a n-ary Tree
When the graph is a Ternary Tree
Ans:
When the graph is a Linked List

high performance computing mcq questions
20. In BFS, how many times a node is visited?

Once
Twice
Equivalent to number of indegree of the node
Thrice
Ans:
Equivalent to number of indegree of the node

21. Is Best First Search a searching algorithm used in graphs.

TRUE
FALSE
Ans:
TRUE

22. The critical issue in parallel depth-first search algorithms is the distribution of the search space among the processors.

TRUE
FALSE
Ans:
TRUE

23. Graph search involves a closed list, where the major operation is a _

sorting
searching
lookup
none of above
Ans:
lookup

24. Which of the following is not a stable sorting algorithm in its typical implementation.

Insertion Sort
Merge Sort
Quick Sort
Bubble Sort
Ans:
Quick Sort

25. Which of the following is not true about comparison based sorting algorithms?

The minimum possible time complexity of a comparison based sorting algorithm is O(nLogn) for a random input array
Any comparison based sorting algorithm can be made stable by using position as a criteria when two elements are compared
Counting Sort is not a comparison based sorting algortihm
Heap Sort is not a comparison based sorting algorithm.
Ans:
Heap Sort is not a comparison based sorting algorithm.

UNIT 6

---

1. A CUDA program is comprised of two primary components: a host and a _

GPU kernel
CPU kernel

OS
none of above
Ans:
GPU kernel

2.The kernel code is dentified by the _____qualifier with void return type

host
__global__
device
void
Ans:
__global__

3. The kernel code is only callable by the host

TRUE
FALSE
Ans:
TRUE

4. The kernel code is executable on the device and host

TRUE
FALSE
Ans:
FALSE

5. Calling a kernel is typically referred to as _

kernel thread
kernel initialization
kernel termination
kernel invocation
Ans:
kernel invocation

6. Host codes in a CUDA application can Initialize a device

TRUE
FALSE
Ans:
TRUE

7. Host codes in a CUDA application can Allocate GPU memory

TRUE
FALSE
Ans:
TRUE

8. Host codes in a CUDA application can not Invoke kernels

TRUE
FALSE
Ans:
FALSE

9. CUDA offers the Chevron Syntax to configure and execute a kernel.

TRUE
FALSE
Ans:
TRUE

10. the BlockPerGrid and ThreadPerBlock parameters are related to the __ model supported by CUDA.

host
kernel
thread abstraction
none of above
Ans:
thread abstraction

high performance computing mcq sppu
11. _ is Callable from the device only

host
__global__
device
none of above
Ans:
device

12. __ is Callable from the host

__global__
device
none of above
Ans:
__global__

13. CUDA supports __ in which code in a single thread is executed by all other threads.

tread division
tread termination
thread abstraction
none of above
Ans:
thread abstraction

14. In CUDA, a single invoked kernel is referred to as a _

block
tread
grid
none of above
Ans:
grid

15. A grid is comprised of __ of threads.

block
bunch
host
none of above
Ans:
block

16. Host codes in a CUDA application can not Reset a device

TRUE
FALSE
Ans:
FALSE

17. A block is comprised of multiple _

treads
bunch
host
none of above
Ans:
treads

18. a solution of the problem in representing the parallelism in algorithm is

CUD
PTA
CDA
CUDA
Ans:
CUDA

19. Host codes in a CUDA application can Transfer data to and from the device

TRUE
FALSE
Ans:
TRUE

20. Host codes in a CUDA application can not Deallocate memory on the GPU

TRUE
FALSE
Ans:
FALSE

Question 1 : The need for parallel processor to increase speedup

1. Moores Law
2. Minsky conjecture
3. Flynns Law
4. Amdhals Law

ANSWER
Amdhals Law

Question 2 : Which of the following interrupt is non maskable

1. INTR
2. RST 7.5
3. RST 6.5
4. TRAP

ANSWER

Question 3 : In which system desire HPC

1. Adaptivity
2. Transparency
3. Dependency
4. Secretivte

ANSWER
Transparency

Question 4 : When every caches hierarchy level is subset of level which futher away from the processor

1. Synchronous
2. Atomic synschronous
3. Distrubutors

4. Multilevel inclusion

ANSWER
Multilevel inclusion

Question 5 : . _____ leads to concurrency

1. Serialization
2. cloud computing
3. Distribution
4. Parallelism

ANSWER
Parallelism

Question 6 : The problem where process concurrency becomes an issue is called as _____

1. Reader-write problem
2. Bankers problem
3. Bakery problem
4. Philosophers problem

ANSWER
Reader-write problem

Question 7 : Interprocess communication that take place

1. Centralized memory
2. Message passing
3. shared memory
4. cache memory

ANSWER
shared memory

Question 8 : Speedup can be as low as____

1. 1
2. 2
3. 0
4. 3

ANSWER
0

Question 9 : A type of parallelism that uses micro architectural techniques.

1. bit based
2. bit level
3. increasing
4. instructional

ANSWER
instructional

Question 10 : MPI_Comm_size

1. Returns number of processes
2. Returns number of line
3. Returns size of program
4. Returns value of instruction

ANSWER
Returns number of processes

Question 11 : High performance computing of the computer system tasks are done by

1. node clusters
2. network clusters
3. Beowulf clusters
4. compute nodes

ANSWER
compute nodes

Question 12 : MPI_Comm_rank

1. returns rank
2. returns processes
3. returns value
4. Returns value of instruction

ANSWER
returns rank

Question 13 : A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ .

1. Super-scaling
2. Pipe-lining
3. Parallel Computation
4. distributed

ANSWER
Pipe-lining

Question 14 : Any condition that causes a processor to stall is called as _____

1. page fault
2. system error
3. Hazard
4. execuation error

ANSWER
Hazard

Question 15 : Characteristic of RISC (Reduced Instruction Set Computer) instruction set is

1. one word instruction
2. two word instruction
3. three word instruction
4. four word instruction

ANSWER
one word instruction

Question 16 : The disadvantage of using a parallel mode of communication is _____

1. Leads to erroneous data transfer
2. It is costly
3. Security of data
4. complexity of network

ANSWER
It is costly

Question 17 : A microprogram sequencer

1. generates the address of next micro instruction to be executed.
2. generates the control signals to execute a microinstruction.
3. sequentially averages all microinstructions in the control memory.
4. enables the efficient handling of a micro program subroutine.

ANSWER

Question 18 : The___ time collectively spent by all the processing elements Tall = p TP

1. total
2. Average
3. mean
4. sum

ANSWER
total

Question 19 : In a distributed computing environment, distributed shared memory is used which is_____

1. Logical combination of virtual memories on the nodes
2. Logical combination of physical memories on the nodes
3. Logical combination of the secondary memories on all the nodes
4. Logical combinatin of files

ANSWER

Question 20 : The average number of steps taken to execute the set of instructions can be made to be less than one by following _____ .

1. Sequentional
2. super-scaling
3. pipe-lining
4. ISA

ANSWER
super-scaling

Question 21 : The main difference between the VLIW and the other approaches to improve performance is _____

1. increase in performance
2. Lack of complex hardware design
3. Cost effectiveness
4. latency

ANSWER
Lack of complex hardware design

Question 22 : CISC stands for

1. Complete Instruction Sequential Compilation
2. Complete Instruction Sequential Compiler
3. Complete Instruction Serial Compilation
4. Complex Instruction set computer

ANSWER
complex

Question 23 : Speedup, in theory, should be _____ bounded by p

1. lower
2. upper
3. left
4. right

ANSWER
upper

Question 24 : Virtualization that creates one single address space architecture that of, is called

1. Loosely coupled
2. Space based
3. Tightly coupled
4. peer-to-peer

ANSWER
Space based

Question 25 : MPI_Init

1. Close MPI environment
2. Initialize MPI environment
3. start programing
4. Call processes

ANSWER
start programing

Question 26 : Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called

1. relative address mode
2. index addressing mode
3. register mode
4. implied mode

ANSWER

Question 27 : The straight-forward model used for the memory consistency, is called

1. Sequential consistency
2. Random consistency
3. Remote node
4. Host node

ANSWER

Question 28 : Which MIMD systems are best scalable with respect to the number of processors

1. Distributed memory
2. ccNUMA
3. nccNUMA
4. Symmetric multiprocessor

ANSWER
Distributed memory

Question 29 : Memory management on a multiprocessor must deal with all of found on

1. Uniprocessor Computer

2. Computer
3. Processor
4. System

ANSWER

Question 30 : The___ time collectively spent by all the processing elements Tall = p TP

1. total
2. sum
3. average
4. product

ANSWER
total

Question 31 : Hazard are eliminated through renaming by renaming all

1. Source register
2. Memory
3. Data
4. Destination register

ANSWER
Destination register

Question 32 : The situation wherein the data of operands are not available is called _____

1. stock
2. Deadlock
3. data hazard
4. structural hazard

ANSWER
data hazard

Question 33 : types of HPC application

1. Mass Media
2. Business
3. Management

4. Science

ANSWER
Science

Question 34 : A distributed operating system must provide a mechanism for

1. intraprocessor communication
2. intraprocess and intraprocessor communication
3. interprocess and interprocessor communication
4. interprocessor communication

ANSWER

Question 35 : This is computation not performed by the serial version

1. Serial computation
2. Excess computation
3. serial computation
4. parallel computing

ANSWER

Question 36 : The important feature of the VLIW is _____

1. ILP
2. Performance
3. Cost effectiveness
4. delay

ANSWER
ILP

Question 37 : The tightly coupled set of threads execution working on a single task ,that is called

1. Multithreading
2. Parallel processing
3. Recurrence
4. Serial processing

ANSWER
Multithreading

Question 38 : Parallel Algorithm Models

1. Data parallel model
2. Bit model
3. Data model
4. network model

ANSWER
Data parallel model

Question 39 : Mpi_Recv used for

1. reverse message
2. receive message
3. forward message
4. Collect message

ANSWER
receive message

Question 40 : Status bit is also called

1. Binary bit
2. Flag bit
3. Signed bit
4. Unsigned bit

ANSWER

Question 41 : For inter processor communication the miss arises are called

1. hit rate
2. coherence misses
3. comitt misses
4. parallel processing

ANSWER
coherence misses

Question 42 : The interconnection topologies are implemented using _____ as a node.

1. control unit
2. microprocessor
3. processing unit
4. microprocessor or processing unit

ANSWER

Question 43 : _____ gives the theoretical speedup in latency of the execution of a task at fixed execution time

1. Amdahl's
2. Moor's
3. metcalfe's
4. Gustafson's law

ANSWER
Gustafson's law

Question 44 : The number and size of tasks into which a problem is decomposed determines the

1. fine-grainularity
2. coarse-grainularity
3. sub Task
4. granularity

ANSWER
granularity

Question 45 : MPI_Finalize used for

1. Stop mpi environment program
2. intitalise program
3. Include header files
4. program start

ANSWER
Stop mpi environment program

Question 46 : Private data that is used by a single processor then shared data are used

1. Single processor
2. Multi processor
3. Single tasking
4. Multi tasking

ANSWER
Single processor

Question 47 : The time lost due to the branch instruction is often referred to as _____

1. Delay
2. Branch penalty
3. Latency
4. control hazard

ANSWER
Branch penalty

Question 48 : NUMA architecture uses _____in design

1. cache
2. shared memory
3. message passing
4. distributed memory

ANSWER
distributed memory

Question 49 : Divide and Conqure apporach is known for

1. Sequentional algorithm development
2. parallel algorithm develpoment
3. Task defined algorithm
4. Non defined Algorithm

ANSWER
Sequentional algorithm development

Question 50 : The parallelism across branches require which scheduling

1. Global scheduling
2. Local Scheduling
3. post scheduling
4. pre scheduling

ANSWER
Global scheduling

Question 51 : Parallel processing may occur

1. In the data stream
2. In instruction stream
3. In network
4. In transferring

ANSWER
In the data strea

Question 52 : Pipe-lining is a unique feature of _____.

1. CISC
2. RISC
3. ISA
4. IANA

ANSWER
RISC

Question 53 : In MPI programing MPI_char is the instruction for

1. Unsign Char
2. Sign character
3. Long Char
4. unsign long char

ANSWER
Sign Char

Question 54 : To increase the speed of memory access in pipelining, we make use of _____

1. Special memory locations
2. Special purpose registers

3. Cache
4. Buffer

ANSWER
buffer

Question 55 : If the value V(x) of the target operand is contained in the address field itself, the addressing mode is

1. Immediate
2. Direct
3. Indirect
4. Implied

ANSWER

Question 56 : In a multi-processor configuration two coprocessors are connected to host 8086 processor. The instruction sets of the two coprocessors

1. must be same
2. may overlap
3. must be disjoint
4. must be the same as that of host

ANSWER

Question 57 : A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is its _____ path

1. critical
2. easy
3. difficult
4. ambiguous

ANSWER
critical

Question 58 : MPI_send used for

1. collect message

2. transfer message
3. send message
4. receive message

ANSWER
send message

Question 59 : What is usually regarded as the von Neumann Bottleneck

1. Instruction set
2. Arithmetic logical unit
3. Processor/memory interface
4. Control unit

ANSWER
Arithmetic logical unit

Question 60 : An interface between the user or an application program, and the system resources is

1. Microprocessor
2. Microcontroller
3. Multimicroprocessor
4. operating system

ANSWER

Question 61 : The computer architecture aimed at reducing the time of execution of instructions is _____.

1. CISC
2. RISC
3. SPARC
4. ISA

ANSWER
RISC

Question 62 : parallel computer is capable of

1. Decentalized computing

2. Parallel computing
3. Distributed computing
4. centralized computing

ANSWER

Question 63 : Design of _____processor is complex

1. parallel
2. pipeline
3. serial
4. distributed

ANSWER
pipeline

Question 64 : The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called

1. Data transfer instructions
2. Program control instructions
3. Input-output instructions
4. Logical instructions

ANSWER

Question 65 : The pattern of_____ among tasks is captured by what is known as a task-interaction graph

1. interaction
2. communication
3. optmization
4. flow

ANSWER
interaction

Question 66 : In vector processor a single instruction, can ask for _____ data operations

1. multiple
2. single

3. two
4. four

ANSWER
multiple

Question 67 : The cost of a parallel processing is primarily determined by

1. switching complexity
2. circuit complexity
3. Time Complexity
4. space complexity

ANSWER
Time Complexity

Question 68 : Interaction overheads can be minimized by____

1. Maximize Data Locality
2. Maximize Volume of data exchange
3. Increase Bandwidth
4. Minimize social media contents

ANSWER
Maximize Data Locality

Question 69 : This is computation not performed by the serial version

1. Excess Computation
2. serial computation
3. Parallel Computing
4. cluster computation

ANSWER
Excess Computation

Question 70 : The cost of dynamic networks is often determined by the number of _____ nodes in the network.

1. Packet
2. Ring
3. Static

4. Switching

ANSWER
Switching

Question 71 : The contention for the usage of a hardware device is called _____

1. data hazard
2. Stalk
3. Deadlock
4. structural hazard

ANSWER
structural hazard

Question 72 : Which Algorithm is better choice for pipelining

1. Small Algorithm
2. Hash Algorithm
3. Merge-Sort Algorithm
4. Quick-Sort Algorithm

ANSWER
Merge-Sort Algorithm

Question 73 : In MPI programing MPI_Reduce is the instruction for

1. Full operation
2. Limited operation
3. reduction operation
4. selected operation

ANSWER
reduction operation

Question 74 : The stalling of the processor due to the unavailability of the instructions is called as _____

1. Input hazard
2. data hazard
3. structural hazard
4. control hazard

ANSWER
control hazard

Question 75 : _____processors rely on compile time analysis to identify and bundle together instructions that can be executed concurrently

1. VILW
2. LVIW
3. VLIW
4. VLWI

ANSWER
VLIW

Question 76 : type of parallelism that is naturally expressed by independent tasks in a task-dependency graph is called _____ parallelism.

1. Task
2. Instruction
3. Data
4. Program

ANSWER
Task

Question 77 : NSM has launched its first supercomputer at

1. BHU
2. IITB
3. IITKG
4. IITM

ANSWER
BHU

Question 78 : Writing parallel programs is referred to as

1. Parallel computation
2. parallel development
3. parallel programing
4. Parallel processing

ANSWER
Parallel computation

Question 79 : A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ .

1. Super-scaling
2. Pipe-lining
3. Parallel computation
4. serial computation

ANSWER
Pipe-lining

Question 80 : Zero address instruction format is used for

1. RISC architecture
2. CISC architecture
3. Von-Neuman architecture
4. Stack-organized architecture

ANSWER

Question 81 : An interface between the user or an application program, and the system resources are

1. microprocessor
2. microcontroller
3. multi-microprocessor
4. operating system

ANSWER

Question 82 : The main objective in building the multi-microprocessor is

1. greater throughput
2. enhanced fault tolerance
3. greater throughput and enhanced fault tolerance
4. zero throughput

ANSWER

Question 83 : UMA architecture uses _____in design

1. cache
2. shared memory
3. message passing
4. distributed memory

ANSWER
shared memory

Question 84 : To which class of systems does the von Neumann computer belong

1. SIMD
2. MIMD
3. MISD
4. SISD

ANSWER
SISD

Question 85 : characteristic of CISC (Complex Instruction Set Computer)

1. Variable format instruction
2. Fixed format instructions
3. Instruction are executed by hardware
4. unsign long char

ANSWER
Variable format instruction

Question 86 : A _____ computation performs one multiply-add on a single pair of vector elements

1. dot product
2. cross product
3. multiply
4. add

ANSWER

dot

Question 87 : Data parallelism is parallelism inherent in

1. program loops
2. Serial program
3. parallel program
4. long programs

ANSWER
parallel program

Question 88 : What is the execution time per stage of a pipeline that has 5 equal stages and a mean overhead of 12 cycles

1. 2 cycles
2. 3 cycles
3. 5 cycles
4. 4 cycles

ANSWER
3 cycles

Question 89 : This algorithm is a called greedy because

1. the greedy algorithm never considers the same solution again
2. the greedy algorithm always give same solution again
3. the greedy algorithm never considers the optimal solution
4. the greedy algorithm never considers whole program

ANSWER
the greedy algorithm never considers the same solution again

Question 90 : If n is a power of two, we can perform this operation in ____ steps by propagating partial sums up a logical binary tree of processors.

1. logn
2. nlogn
3. n
4. n^2

ANSWER

logn

Question 91 : A multiprocessor machine which is capable of executing multiple instructions on multiple data sets

1. SISD
2. SIMD
3. MIMD
4. MISD

ANSWER
MIMD

Question 92 : Tree networks suffer from a communication bottleneck at higher levels of the tree. This network, also called a _____ tree.

1. fat
2. binary
3. order static
4. heap tree

ANSWER
FAT

Question 93 : Multiple application independently running are typically called

1. Multiprograming
2. multiithreading
3. Multitasking
4. Synchronization

ANSWER
Multiprograming

Question 94 : Each of the clock cycle from the previous section of execution becomes

1. Previous stage
2. stall
3. previous cycle
4. pipe stage

ANSWER

pipe stage

Question 95 : The main objective in building the multimicroprocessor is

1. greater throughput
2. enhanced fault tolerance
3. greater throughput and enhanced fault tolerance
4. none of the mentioned

ANSWER

Question 96 : Wating until there is no data hazards then

1. stall
2. write operand
3. Read operand
4. Branching

ANSWER
Read operand

Question 97 : In message passing, send and receive message between

1. Task or processes
2. Task and Execution
3. Processor and Instruction
4. Instruction and decode

ANSWER
Task or processes

Question 98 : We denote the serial runtime by TS and the parallel____by TP

1. runtime
2. clock time
3. processor time
4. clock frequency

ANSWER
runtime

Question 99 : Uniprocessor computing devices is called_____.

1. Grid computing
2. Centralized computing
3. Parallel computing
4. Distributed computing

ANSWER
Centralized computing

Question 100 : The tighhtly copuled set of threads execution working on a single task is called

1. Serial processing
2. parallel processing
3. Multithreading
4. Recurrent

ANSWER
Multithreading

Question 101 : what is WAR

1. Write before read
2. write after write
3. write after read
4. write with read

ANSWER
write after read

Question 102 : Partitioning refer to decomposing of the computational activity as

1. Small Task
2. Large Task
3. Full program
4. group of program

ANSWER
Small Task

Question 103 : Speed up is defined as a ratio of

1. s=Ts/Tp
2. S= Tp/Ts
3. Ts=S/Tp
4. Tp=S /Ts

ANSWER
s=Ts/Tp

Question 104 : A processor that continuously tries to acquire the locks, spinning around a loop till it reaches its success, is known as

1. Spin locks
2. Store locks
3. Link locks
4. Store operational

ANSWER

Question 105 : Pipelining strategy is called implement

1. Instruction execution
2. Instruction prefetch
3. Instruction manipulation
4. instruction decoding

ANSWER
Instruction prefetch

Question 106 : Parallel computing means to divide the job into several _____

1. Bit
2. Data
3. Instruction
4. Task

ANSWER
Task

Question 107 : if a piece of data is repeatedly used, the effective latency of this memory system can be reduced by the _____.

1. RAM
2. ROM
3. Cache
4. HDD

ANSWER
Cache

Question 108 : Processing of multiple tasks simultaneously on multiple processors is called

1. Parallel processong
2. Distributed processing
3. Uni- processing
4. Multi-processing

ANSWER
Multi-processing

Question 109 : The instuction execution sequence ,that holds the instruction result known as

1. Data buffer
2. control buffer
3. reorder buffer
4. ordered buffer

ANSWER
reorder buffer

Question 110 : A multiprocessor operating system must take care of

1. authorized data access and data protection
2. unauthorized data access and data protection
3. authorized data access
4. data protection

ANSWER

Question 111 : The expression 'delayed load' is used in context of

1. prefetching
2. pipelining

3. processor-printer communication
4. memory-monitor communication

ANSWER
pipelining

Question 112 : _____ is a method for inducing concurrency in problems that can be solved using the divide-and-conquer strategy.

1. exploratory decomposition
2. speculative decomposition
3. data-decomposition
4. Recursive decomposition

ANSWER
data-decomposition

Question 113 : If no node having a copy of a cache block, this technique is known as

1. Uniform memory access
2. Cached
3. Un-cached
4. Commit

ANSWER

1: Computer system of a parallel computer is capable of

A. Decentralized computing
B. Parallel computing
C. Centralized computing
D. Decentralized computing
E. Distributed computing
F. All of these
G. None of these

Ans :
A
2: Writing parallel programs is referred to as

A. Parallel computation
B. Parallel processes

C. Parallel development
D. Parallel programming
E. Parallel computation
F. All of these
G. None of these
Ans :
D

3: Simplifies application's of three-tier architecture is _____.
A. Maintenance
B. Initiation
C.Implementation
D. Deployment
E. All of these
F. None of these
Ans :
D

4: Dynamic networks of networks, is a dynamic connection that grows is called

A. Multithreading
B. Cyber cycle
C. Internet of things
D. Cyber-physical system
E. All of these
F. None of these
Ans :
C

5: In which application system Distributed systems can run well?

A. HPC
D. HTC
C. HRC
D. Both A and B
E. All of these
F. None of these
Ans :
D

6: In which systems desire HPC and HTC.

A. Adaptivity
B. Transparency
C. Dependency
D. Secretive
E. Adaptivity
F. All of these
G. None of these

Ans :
B

7: No special machines manage the network of architecture in which resources are known as

A. Peer-to-Peer
B. Space based
C. Tightly coupled
D. Loosely coupled
E. All of these
F. None of these

Ans :
A
8: Significant characteristics of Distributed systems have of

A. 5 types
B. 2 types
C. 3 types
D. 4 types
E. All of these
F. None of these

Ans :
C
9: Built of Peer machines are over

A. Many Server machines
B. 1 Server machine
C. 1 Client machine
D. Many Client machines
E. All of these
F. None of these

Ans :
D
10: Type HTC applications are

A. Business
B. Engineering
C. Science
D. Media mass
E. All of these
F. None of these

Ans :

A
11: Virtualization that creates one single address space architecture that of, is called

A. Loosely coupled
B. Peer-to-Peer
C. Space-based
D. Tightly coupled
E. Loosely coupled
F. All of these
G. None of these

Ans :
C
12: We have an internet cloud of resources In cloud computing to form

A. Centralized computing
B. Decentralized computing
C. Parallel computing
D. Both A and B
E. All of these
F. None of these

Ans :
E
13: Data access and storage are elements of Job throughput, of _____.

A. Flexibility
B. Adaptation
C. Efficiency
D. Dependability
E. All of these
F. None of these

Ans :
C
14: Billions of job requests is over massive data sets, ability to support known as

A. Efficiency
B. Dependability
C. Adaptation
D. Flexibility
E. All of these
F. None of these

Ans :
C
15: Broader concept offers Cloud computing .to select which of the following.

A. Parallel computing
B. Centralized computing
C. Utility computing
D. Decentralized computing
E. Parallel computing
F. All of these
G. None of these

Ans :
C
16: Resources and clients transparency that allows movement within a system is called

A.Mobility transparency
B. Concurrency transparency
C. Performance transparency
D. Replication transparency
E. All of these
F. None of these

Ans :
A
17: Distributed program in a distributed computer running a is known as

A. Distributed process
B. Distributed program
C. Distributed application
D. Distributed computing
E. All of these
F. None of these

Ans :
B
18: Uniprocessor computing devices is called_____.

A. Grid computing
B. Centralized computing
C. Parallel computing
D. Distributed computing
E. All of these
F. None of these

Ans :
B
19: Utility computing focuses on a_____ model.

A. Data

B. Cloud
C. Scalable
D. Business
E. All of these
F. None of these

Ans :
D
20: what is a CPS merges technologies

A. 5C
B. 2C
C. 3C
D. 4C
E. All of these
F. None of these

Ans :
C
21: Aberavationn of HPC

A. High-peak computing
B. High-peripheral computing

C. High-performance computing

D. Highly-parallel computing

E. All of these

F. None of these

Ans :
C

22: Peer-to-Peer leads to the development of technologies like

A. Norming grids

B. Data grids

C. Computational grids

D. Both A and B

E. All of these
F. None of these

Ans :
D
23: Type of HPC applications of.

A. Management
B. Media mass
C. Business
D. Science
E. All of these
F.None of these

Ans :
D
24: The development generations of Computer technology has gone through

A. 6
B. 3
C. 4
D. 5
E. All of these
F. None of these

Ans :
D

25: Utilization rate of resources in an execution model is known to be its

A. Adaptation
B. Efficiency
C. Dependability
D. Flexibility
E. All of these
F. None of these

Ans :
B
26: Even under failure conditions Providing Quality of Service (QoS) assurance is the responsibility of

A. Dependability
B. Adaptation
C. Flexibility
D. Efficiency
E. All of these
F. None of these

Ans :
A
27: Interprocessor communication that takes place

A. Centralized memory
B. Shared memory
C. Message passing
D. Both A and B
E. All of these
F. None of these

Ans :
D

28: Data centers and centralized computing covers many and

A. Microcomputers
B. Minicomputers
C. Mainframe computers
D. Supercomputers
E. All of these
F. None of these

Ans :
D
29: Which of the following is an primary goal of HTC paradigm_____.

A. High ratio Identification
B. Low-flux computing
C. High-flux computing
D. Computer utilities
E. All of these
F. None of these

Ans :
C
30: The high-throughput service provided is measures taken by

A. Flexibility
B. Efficiency
D. Adaptation
E. Dependability
F. All of these
G. None of these

Ans :
D

A modem is very helpful to link up two computers with the help of?

(A). telephone line

(B). dedicated line

(C). All of these

(D). None of these

Ans : (C)

A whole micro-computer system consists of which of the following?

(A). microprocessor

(B). memory

(C). peripheral equipment

(D). all of these

(E). None of these

Ans : (D).

Which of the following program is a micro-program written in 0 and 1?

(A). binary micro-program

(B). binary microinstruction

(C). symbolic microinstruction

(D). Symbolic microinstruction

(E). None of these

Ans : A

A pipeline is similar to which of the following?

(A). a gas line

(B). house pipeline

(C). both a and b

(D). an automobile assembly line

(E). None of these

Ans : D

A processor performing fetching or decoding of instructions during the execution of another instruction is commonly known as?

(A). Super-scaling

(B). Parallel Computation

(C). Pipe-lining

(D). None of these

Ans : D

An optimizing compiler performs which of the following?

(A). Better compilation of the given code.

(B). better memory management.

(C). Takes the benefit of processor type and decreases its process time.

(D). Both a and c

(E). None of these

Ans : C

Which of the following wires is a collection of lines that connects several devices?

(A). internal wires

(B). peripheral connection wires

(C). Both a and b

(D). bus

(E). None of these

Ans : (D).

Which of the following is an instruction to give a small delay in the program?

(A). NOP

(B). LDA

(C). BEA

(D). None of these

Ans : A

How to define a peripheral?

(A). any physical device connected to the computer

(B). tape drive connected to a computer

(C). any drives installed in the computer

(D). None of these

Ans : A

UNIT ONE	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
1	A pipeline is like	an automobile assembly line	house pipeline	both a and b	a gas line	**a**
2	Data hazards occur when	Greater performance loss	Pipeline changes the order of read/ write access to operands	Some functional unit is not fully pipelined	Machine size is limited	**b**
3	Systems that do not have parallel processing capabilities are	SISD	SIMD	MIMD	All of the above	**a**
4	How does the number of transistors per chip increase according to Moore ´s law?	Quadratically	Linearly	Cubicly	Exponentially	**d**
5	Parallel processing may occur	in the instruction stream	B. in the data stream	both[A] and [B]	none of the above	**c**
6	Execution of several activities at the same time.	processing	parallel processing	serial processing	multitasking	**b**
7	Cache memory works on the principle of	Locality of data	Locality of memory	Locality of reference	Locality of reference & memory	**c**

8	SIMD represents an organization that _____.	refers to a computer system capable of processing several programs at the same time.	represents organization of single computer containing a control unit, processor unit and a memory unit.	includes many processing units under the supervision of a common control unit	none of the above.	**c**
9	A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ .	Super-scaling	Pipe-lining	Parallel Computation	None of these	**b**
10	General MIMD configuration usually called	a multiprocessor	a vector processor	array processor	none of the above.	**a**
11	A Von Neumann computer uses which one of the following?	SISD	SIMD	MISD	MIMD.	**a**
12	MIMD stands for	Multiple instruction multiple data	Multiple instruction memory data	Memory instruction multiple data	Multiple information memory data	**a**
13	MIPS stands for:	Memory Instruction Per Second	Major Instruction Per Second	Main Information Per Second	Million Instruction Per Second	**d**
14	M.J. Flynn's parallel processing classification is based on:	Multiple Instructions	Multiple data	Both (a) and (b)	None of the above	**c**
15	VLIW stands for:	Vector Large Instruction Word	Very Long Instruction Word	Very Large Integrated Word	Very Low Integrated Word	**b**

16	The major disadvantage of pipeline is:	High cost individual dedicated	Initial setup time	If branch instruction is encountered the pipe has to be flushed	All of the above	**c**
17	A topology that involves Tokens.	Star	Ring	Bus	Daisy Chaining	**b**
18	multipoint topology is	bus	star	mesh	ring	**a**
19	In super-scalar mode, all the similar instructions are grouped and executed together.	TRUE	False			**a**
20	Which mechanism performs an analysis on the code to determine which data items may become unsafe for caching, and they mark those items accordingly?	Directory protocol	Snoopy protocol	Server based cache coherence	Compiler based cache coherence	**d**
21	How many processors can be organized in 5-dimensional binary hypercube system?	25	10	32	20	**c**
22	Multiprocessors are classified as _____.	SIMD	MIMD	SISD	MISD	**b**
23	Which of the following is not one of the interconnection structures?	Crossbar switch	Hypercube system	Single port memory	Time-shared common bus	**c**
24	Which combinational device is used in crossbar switch for selecting proper memory from multiple addresses?	Multiplexer	Decoder	Encoder	Demultiplexer	**a**

25	How many switch points are there in crossbar switch network that connects 9 processors to 6 memory modules?	50	63	60	54	**d**
26	In a three-cube structure, node 101 cannot communicate directly with node?	1	11	100	111	**b**
27	Which method is used as an alternative way of snooping-based coherence protocol?	Directory protocol	Memory protocol	Compiler based protocol	None of above	**a**
28	snoopy cache protocol are used in ----------based system	bus	mesh	star	hypercube	**a**
29	superscalar architecture contains ----------execution units for instruction execution	multiple	single	none of the above		**a**
30	time taken by header of a message between two directly connected nodes is called as----------	startup time	per hop time	per word transfer time	packaging time	**b**
31	the number of switch requirement for a network with n input and n output is ----------	n	n2	n3	n4	**b**
32	which of the following is not static network	bus	ring	mesh	crossbar switch	**d**
33	In super-scalar processors, _____ mode of execution is used.	In-order	Post order	Out of order	None of the mentioned	**c**
34	_____ have been developed specifically for pipelined systems.	Utility software	Speed up utilities	Optimizing compilers	None of the above	**c**

35	Which of the following is a combination of several processors on a single chip?	Multicore architecture	RISC architecture	CISC architecture	Subword parallelism	**a**
36	The important feature of the VLIW is	ILP	Cost effectiveness	performance	None of the mentioned	**a**
37	The parallel execution of operations in VLIW is done according to the schedule determined by	sk scheduler	Interpreter	Compiler	Encoder	**c**
38	The VLIW processors are much simpler as they do not require of	Computational register	Complex logic circuits	SSD slots	Scheduling hardware	**d**
39	The VLIW architecture follows ..... approach to achieve parallelism.	MISD	SISD	SIMD	MIMD	**d**
40	Which of the following is not a Pipeline Conflicts?	Timing Variations	Branching	Load Balancing	Data Dependency	**c**

UNIT TWO	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
1	Task dependency graph is ----------	directed	undirected	directed acyclic	undirected acyclic	**c**
2	In task dependency graph longest directed path between any pair of start and finish node is called as ----------	total work	critical path	task path	task length	**b**
3	which of the following is not a granularity type	course grain	large grain	medium grain	fine grain	**b**
4	which of the following is a an example of data decomposition	matrix multiplication	merge sort	quick sort	15 puzzal	**a**
5	which problems can be handled by recursive decomposition	backtracking	greedy method	divide and conquer problem	branch and bound	**c**
6	In this decomposition problem decomposition goes hand in hand with its execution	data decomposition	recursive decomposition	explorative decomposition	speculative decomposition	**c**
7	which of the following is not an example of explorative decomposition	n queens problem	15 puzzal problem	tic tac toe	quick sort	**d**
8	Topological sort can be applied to which of the following graphs?	a) Undirected Cyclic Graphs	b) Directed Cyclic Graphs	c) Undirected Acyclic Graphs	d) Directed Acyclic Graphs	**d**

9	In most of the cases, topological sort starts from a node which has _____	a) Maximum Degree	b) Minimum Degree	c) Any degree	d) Zero Degree	**d**
10	Which of the following is not an application of topological sorting?	a) Finding prerequisite of a task	b) Finding Deadlock in an Operating System	c) Finding Cycle in a graph	d) Ordered Statistics	**d**
11	In ----------task are defined before starting the execution of the algorithm	dynamic task	static task	regular task	one way task	**b**
12	which of the following is not the array distribution method of data partitioning	block	cyclic	block cyclic	chunk	**d**
13	blocking optimization is used to improve temmporal locality for reduce	hit miss	misses	hit rate	cache misses	**b**
14	CUDA thought that 'unifying theme' of every form of parallelism is	CDA thread	PTA thread	CUDA thread	CUD thread	**c**
15	Topological sort of a Directed Acyclic graph is?	a) Always unique	b) Always Not unique	c) Sometimes unique and sometimes not unique	d) Always unique if graph has even number of vertices	**c**
16	threads being block altogether and being executed in the sets of 32 threads called a	thread block	32 thread	32 block	unit block	**a**
17	True or False: The threads in a thread block are distributed across SM units so that each thread is executed by one SM unit.	TRUE	FALSE			**a**

18	When the topological sort of a graph is unique?	a) When there exists a hamiltonian path in the graph	b) In the presence of multiple nodes with indegree 0	c) In the presence of single node with indegree 0	d) In the presence of single node with outdegree 0	**a**
19	What is a high performance multi-core processor that can be used to accelerate a wide variety of applications using parallel computing.	CPU	DSP	GPU	CLU	**c**
20	A good mapping does not depends on which following factor	knowledge of task sizes	the size of data associated with tasks	characteristics of inter-task interactions	task overhead	**d**
21	CUDA is a parallel computing platform and programming model	TRUE	FALSE			**a**
22	Which of the following is *not* a form of parallelism supported by CUDA	Vector parallelism - Floating point computations are executed in parallel on wide vector units	Thread level task parallelism - Different threads execute a different tasks	Block and grid level parallelism - Different blocks or grids execute different tasks	Data parallelism - Different threads and blocks process different parts of data in memory	**a**
23	The style of parallelism supported on GPUs is best described as	MISD - Multiple Instruction Single Data	SIMT - Single Instruction Multiple Thread	SISD - Single Instruction Single Data	MIMD	**b**
24	True or false: Functions annotated with the __global__ qualifier may be executed on the host or the device	TRUE	FALSE			**a**

25	Which of the following correctly describes a GPU kernel	A kernel may contain a mix of host and GPU code	All thread blocks involved in the same computation use the same kernel	A kernel is part of the GPU's internal micro-operating system, allowing it to act as in independent host	kernel may contain only host code	**b**
26	a code known as grid which runs on GPU consisting of a set of	32 thread	unit block	32 block	thread block	**d**
27	which of the following is not an parallel algorithm model	data parallel model	task graph model	task model	work pool model	**c**
28	Having load before the store in a running program order, then interchanging this order, results in a	WAW hazards	Destination registers	WAR hazards	Registers	**c**
29	model based on the passing of stream of data through process arranged in a succession is called as	producer consumer model	hybrid model	task graph model	work pool model	**a**
30	When instruction i and instruction j are tends to write the same register or the memory location, it is called	Input dependence	Output dependence	Ideal pipeline	Digital call	**b**
31	Multithreading allowing multiple-threads for sharing the functional units of a	Multiple processor	Single processor	Dual core	Corei5	**b**
32	Allowing multiple instructions for issuing in a clock cycle, is the goal of	Single-issue processors	Dual-issue processors	Multiple-issue processors	No-issue processors	**c**

33	OpenGL stands for:	A. Open General Liability	B. Open Graphics Library	C. Open Guide Line	D. Open Graphics Layer	**b**
34	which of the following is not an advantage of OpenGL	There is more detailed documentation for OpenGL while other API's don't have such detailed documentation.	OpenGL is portable.	OpenGL is more functional than any other API.	It is not a cross-platform API,	**d**
35	work pool model uses ---------- approach for task assignment	static	dynamic	centralized	decentralized	**b**
36	which of the following is false regarding data parallel model	all task perform same computations	degree of parallelism increase with size of problem	matrix multiplication is example of data parallel	dynamic mapping is done	**d**
37	which of the following are methods for containing interaction overheads	maximizing data locality	minimize volumn of data exchange	min frequency of interactions	all the above	**d**
38	which of the following are classes of dynamic mapping centralized method	self scheduling	chunk scheduling	both a and b	none of the above	**c**
39	which of the following is not scheme for static mapping	block distribution	block cyclic distributions	cyclic distributions	self scheduling	**d**

UNIT THREE	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
e.g 1	**Write down question**	**Option a**	**Option b**	**Option c**	**Option d**	**a/b/c/d**
1	Group communication operations are built using which primitives?	one to all	all to all	point to point	None of these	**c**
2	___ can be performed in an identical fashion by inverting the process.	Recursive Doubling	Reduction	Broadcast	None of these	**b**
3	Broadcast and reduction operations on a mesh is performed	along the rows	along the columns	both a and b concurrently	None of these	**c**
4	Cost Analysis on a ring is	(ts + twm)(p - 1)	(ts - twm)(p + 1)	(tw + tsm)(p - 1)	(tw - tsm)(p + 1)	**a**
5	Cost Analysis on a mesh is	2ts(sqrt(p) + 1) + twm(p - 1)	2tw(sqrt(p) + 1) + tsm(p - 1)	2tw(sqrt(p) - 1) + tsm(p - 1)	2ts(sqrt(p) - 1) + twm(p - 1)	**d**
6	Communication between two directly link nodes	Cut-through routing	Store-and-forward routing	Nearest neighbour communication	None	**c**
7	All-to-one communication (reduction) is the dual of _____ broadcast.	all-to-all	one-to-all	one-to-one	all-to-one	**b**
8	Which is known as Reduction?	all-to-one	all-to-all	one-to-one	one-to-all	**a**

9	Which is known as Broadcast?	one-to-one	one-to-all	all-to-all	all-to-one	**b**
10	The dual of all-to-all broadcast is	all-to-all reduction	all-to-one reduction	Both	None	**a**
11	All-to-all broadcast algorithm for the 2D mesh is based on the	Linear Array Algorithm	Ring algorithm	Both	None	**b**
12	In the first phase of 2D Mesh All to All, the message size is ___	p	m*sqrt(p)	m	p*sqrt(m)	**c**
13	In the second phase of 2D Mesh All to All, the message size is ___	m	p*sqrt(m)	p	m*sqrt(p)	**d**
14	In All to All on Hypercube, The size of the message to be transmitted at the next step is ____ by concatenating the received message with their current data	doubled	tripled	halfed	no change	**a**
15	The all-to-all broadcast on Hypercube needs ____ steps	p	sqrt(p) - 1	log p	None	**c**
16	One-to-All Personalized Communication operation is commonly called ___	gather operation	concatenation	scatter operation	None	**c**
17	The dual of the scatter operation is the	concatenation	gather operation	Both	None	**c**

18	In Scatter Operation on Hypercube, on each step, the size of the messages communicated is ____	tripled	halved	doubled	no change	**b**
19	Which is also called "Total Exchange" ?	All-to-all broadcast	All-to-all personalized communication	all-to-one reduction	None	**b**
20	All-to-all personalized communication can be used in ____	Fourier transform	matrix transpose	sample sort	all of the above	**d**
21	In collective communication operations, collective means	involve group of processors	involve group of algorithms	involve group of variables	none of these	**a**
22	efficiency of data parallel algorithm depends on the	efficient implementation of the algorithm	efficient implementation of the operation	both	none	**b**
23	All processes participate in a single _____ interaction operation.	global	local	wide	variable	**a**
24	subsets of processes in _____ interaction.	global	local	wide	variable	**b**
25	Goal of good algorithm is to implement commonly used _____ pattern.	communication	interaction	parallel	regular	**a**
26	Reduction can be used to find the sum, product, maximum, minimum of _____ of numbers.	tuple	list	sets	all of above	**c**
27	source ____ is bottleneck.	process	algorithm	list	tuple	**a**

28	only connections between single pairs of nodes are used at a time is	good utilization	poor utilization	massive utilization	medium utilization	**b**
29	all processes that have the data can send it again is	recursive doubling	naive approach	reduction	all	**a**
30	The ____ do not snoop the messages going through them.	nodes	variables	tuple	list	**a**
31	accumulate results and send with the same pattern is...	broadcast	naive approach	recursive doubling	reduction symmetric	**d**
32	every node on the linear array has the data and broadcast on the columns with the linear array algorithm in _____	parallel	vertical	horizontal	all	**a**
33	using different links every time and forwarding in parallel again is	better for congestion	better for reduction	better for communication	better for algorithm	**a**
34	In a balanced binary tree processing nodes is equal to	leaves	number of elemnts	branch	none	**a**
35	In one -to- all broadcast there is	divide and conquer type algorithm	sorting type algorithm	searching type algorithm	simple algorithm	**a**
36	For sake of simplicity, the number of nodes is a power of	1	2	3	4	**b**
37	Nides with zero in i least significant bits participate in _____	algorithm	broadcast	communication	searching	**c**

38	every node has to know when to communicate that is	call the procedure	call for broadcast	call for communication	call the congestion	**a**
39	the procedure is disturbed and require only point-to-point _____	synchronization	communication	both	none	**a**
40	Renaming relative to the source is _____ the source.	XOR	XNOR	AND	NAND	**a**

UNIT FOUR	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
e.g 1	**Write down question**	**Option a**	**Option b**	**Option c**	**Option d**	**a/b/c/d**
1	mathematically efficiency is	e=s/p	e=p/s	e*s=p/2	e=p+e/e	**a**
2	Cost of a parallel system is sometimes referred to____ of product	work	processor time	both	none	**c**
3	Scaling Characteristics of Parallel Programs Ts is	increase	constant	decreases	none	**b**
4	Speedup tends to saturate and efficiency _____ as a consequence of Amdahl's law.	increase	constant	decreases	none	**c**
5	Speedup obtained when the problem size is _____ linearly with the number of processing elements.	increase	constant	decreases	depend on problem size	**a**
6	The n × n matrix is partitioned among n processors, with each processor storing complete ___ of the matrix.	row	column	both	depend on processor	**a**
7	cost-optimal parallel systems have an efficiency of ___	1	n	logn	complex	**a**
8	The n × n matrix is partitioned among n2 processors such that each processor owns a _____ element.	n	2n	single	double	**c**
9	how many basic communication operations are used in matrix vector multiplication	1	2	3	4	**c**
10	In DNS algorithm of matrix multiplication it used	1d partition	2d partition	3d partition	both a,b	**c**

11	In the Pipelined Execution, steps contain	normalization	communicatio n	elimination	all	**d**
12	the cost of the parallel algorithm is higher than the sequential run time by a factor of __	3/2	2/3	3*2	2/3+3/2	**a**
13	The load imbalance problem in Parallel Gaussian Elimination: can be alleviated by using a ____ mapping	acyclic	cyclic	both	none	**b**
14	A parallel algorithm is evaluated by its runtime in function of	the input size,	the number of processors,	the communicatio n parameters.	all	**d**
15	For a problem consisting of W units of work, p__W processors can be used optimally.	<=	>=	<	>	**a**
16	C(W)__Θ(W) for optimality (necessary condition).	>	<	<=	equals	**d**
17	many interactions in oractical parallel programs occur in _____ pattern	well defined	zig-zac	reverse	straight	**a**
18	efficient implementation of basic communication operation can improve	performance	communicatio n	algorithm	all	**a**
19	efficient use of basic communication operations can reduce	development effort and	software quality	both	none	**a**
20	Group communication operations are built using_____ Messenging primitives.	point-to-point	one-to-all	all-to-one	none	**a**
21	one processor has a piece of data and it need to send to everyone is	one -to-all	all-to-one	point -to-point	all of above	**a**
22	the dual of one -to-all is	all-to-one reduction	one -to-all reduction	pnoint -to-point reducntion	none	**a**

23	Data items must be combined piece-wise and the result made available at	target processor finally	target variable finatlalyrget receiver			**a**
24	wimpleat way to send p-1 messages from source to the other p-1 processors	Algorithm	communicatio n	concurrency	receiver	**c**
25	In a eight node ring, node ____ is source of broadcast	1	2	8	0	**d**
26	The processors compute _____ product of the vector element and the loval matrix	local	global	both	none	**a**
27	one to all broadcast use	recursive doubling	simple algorithm	both	none	**a**
28	In a broadcast and reduction on a balanced binary tree reduction is done in _____	recursive order	straight order	vertical order	parallel order	**a**
29	if "X" is the message to broadcast it initially resides at the source node	1	2	8	0	**d**
30	logical operators used in algorithm are	XOR	AND	both	none	**c**
31	Generalization of broadcast in Which each processor is	Source as well as destination	only source	only destination	none	**a**
32	The algorithm terminates in _____ steps	p	p+1	p+2	p-1	**d**
33	Each node first sends to one of its neighbours the data it need to....	broadcast	identify	verify	none	**a**
34	The second communication phase is a columnwise _____ broadcast of consolidated	All-to-all	one -to-all	all-to-one	point-to-poi nt	**a**

35	All nodes collects _____ message corresponding to √p nodes to their respectively	√p	p	p+1	p-1	**a**
36	It is not possible to port ____ for higher dimensional network	Algorithm	hypercube	both	none	**a**
37	If we port algorithm to higher dimemsional network it would cause	error	contention	recursion	none	**b**
38	In the scatter operation ____ node send message to every other node	single	double	triple	none	**a**
39	The gather Operation is exactly the inverse of _____	scatter operation	recursion operation	execution	none	**a**
40	Similar communication pattern to all-to-all broadcast except in the_____	reverse order	parallel order	straight order	vertical order	**a**

UNIT FIVE	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
e.g 1	**Write down question**	**Option a**	**Option b**	**Option c**	**Option d**	**a/b/c/d**
1	In _____, the number of elements to be sorted is small enough to fit into the process's main memory.	internal sorting	internal searching	external sorting	external searching	**a**
2	_____ algorithms use auxiliary storage (such as tapes and hard disks) for sorting because the number of elements to be sorted is too large to fit into memory.	internal sorting	internal searching	External sorting	external searching	**c**
3	_____ can be comparison-based or noncomparison-based.	searching	Sorting	both a and b	none of above	**b**
4	The fundamental operation of comparison-based sorting is _____.	compare-exchange	searching	Sorting	swapping	**a**
5	The complexity of bubble sort is Θ(n2).	TRUE	FALSE			**a**
6	Bubble sort is difficult to parallelize since the algorithm has no concurrency.	TRUE	FALSE			**a**
7	Quicksort is one of the most common sorting algorithms for sequential computers because of its simplicity, low overhead, and optimal average complexity.	TRUE	FALSE			**a**
8	The performance of quicksort depends critically on the quality of the _____-.	non-pivote	pivot	center element	len of array	**b**

9	the complexity of quicksort is O(nlog n).	TRUE	FALSE			**a**
10	DFS begins by expanding the initial node and generating its successors. In each subsequent step, DFS expands one of the most recently generated nodes.	TRUE	FALSE			
11	The main advantage of _____ is that its storage requirement is linear in the depth of the state space being searched.	BFS	DFS	a and b	none of above	**b**
12	_____ algorithms use a heuristic to guide search.	BFS	DFS	a and b	none of above	**a**
13	If the heuristic is admissible, the BFS finds the optimal solution.	TRUE	FALSE			**a**
14	The search overhead factor of the parallel system is defined as the ratio of the work done by the parallel formulation to that done by the sequential formulation	TRUE	FALSE			**a**
15	The critical issue in parallel depth-first search algorithms is the distribution of the search space among the processors.	TRUE	FALSE			**a**
16	Graph search involves a closed list, where the major operation is a _____	sorting	searching	lookup	none of above	**c**
17	_____ algorithms use auxiliary storage (such as tapes and hard disks) for sorting because the number of elements to be sorted is too large to fit into memory.	internal sorting	internal searching	External sorting	external searching	**c**
18	_____ can be comparison-based or noncomparison-based.	searching	Sorting	both a and b	none of above	**b**

19	If the heuristic is admissible, the BFS finds the optimal solution.	TRUE	FALSE			**a**
20	The search overhead factor of the parallel system is defined as the ratio of the work done by the parallel formulation to that done by the sequential formulation	TRUE	FALSE			**a**
21	Breadth First Search is equivalent to which of the traversal in the Binary Trees?	Pre-order Traversal	Post-order Traversal	Level-order Traversal	In-order Traversal	**c**
22	Time Complexity of Breadth First Search is? (V – number of vertices, E – number of edges)	O(V + E)	O(V)	O(E)	O(V*E)	**a**
23	Which of the following is not an application of Breadth First Search?	When the graph is a Binary Tree	When the graph is a Linked List	When the graph is a n-ary Tree	When the graph is a Ternary Tree	**b**
24	In BFS, how many times a node is visited?	Once	Twice	Equivalent to number of indegree of the node	Thrice	**c**
25	Is Best First Search a searching algorithm used in graphs.	TRUE	FALSE			**a**
26	The critical issue in parallel depth-first search algorithms is the distribution of the search space among the processors.	TRUE	FALSE			**a**
27	Graph search involves a closed list, where the major operation is a _____	sorting	searching	lookup	none of above	**c**

28	The fundamental operation of comparison-based sorting is _____.	compare-exchange	searching	Sorting	swapping	**a**
29	The complexity of bubble sort is Θ(n2).	TRUE	FALSE			**a**
30	DFS begins by expanding the initial node and generating its successors. In each subsequent step, DFS expands one of the most recently generated nodes.	TRUE	FALSE			
31	The main advantage of _____ is that its storage requirement is linear in the depth of the state space being searched.	BFS	DFS	a and b	none of above	**b**
32	Breadth First Search is equivalent to which of the traversal in the Binary Trees?	Pre-order Traversal	Post-order Traversal	Level-order Traversal	In-order Traversal	**c**
33	Time Complexity of Breadth First Search is? (V – number of vertices, E – number of edges)	O(V + E)	O(V)	O(E)	O(V*E)	**a**
34	Which of the following is not an application of Breadth First Search?	When the graph is a Binary Tree	When the graph is a Linked List	When the graph is a n-ary Tree	When the graph is a Ternary Tree	**b**
35	In BFS, how many times a node is visited?	Once	Twice	Equivalent to number of indegree of the node	Thrice	**c**
36	Is Best First Search a searching algorithm used in graphs.	TRUE	FALSE			**a**

37	Which of the following is not a stable sorting algorithm in its typical implementation.	Insertion Sort	Merge Sort	Quick Sort	Bubble Sort	**c**
38	Which of the following is not true about comparison based sorting algorithms?	The minimum possible time complexity of a comparison based sorting algorithm is O(nLogn) for a random input array	Any comparison based sorting algorithm can be made stable by using position as a criteria when two elements	Counting Sort is not a comparison based sorting algortihm	Heap Sort is not a comparison based sorting algorithm.	**d**
39	In _____, the number of elements to be sorted is small enough to fit into the process's main memory.	internal sorting	internal searching	external sorting	external searching	**a**

UNIT SIX	SUB : 410241 HPC					
Sr. No.	**Questions**	**a**	**b**	**c**	**d**	**Answer**
e.g 1	**Write down question**	**Option a**	**Option b**	**Option c**	**Option d**	**a/b/c/d**
1	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
2	The kernel code is dentified by the _____qualifier with void return type	_host_	__global__	_device_	void	**b**
3	The kernel code is only callable by the host	TRUE	FALSE			**a**
4	The kernel code is executable on the device and host	TRUE	FALSE			**b**
5	Calling a kernel is typically referred to as _____.	kernel thread	kernel initialization	kernel termination	kernel invocation	**d**
6	Host codes in a CUDA application can Initialize a device	TRUE	FALSE			**a**
7	Host codes in a CUDA application can Allocate GPU memory	TRUE	FALSE			**a**
8	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
9	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
10	The kernel code is dentified by the _____qualifier with void return type	_host_	__global__	_device_	void	**b**
11	Host codes in a CUDA application can not Invoke kernels	TRUE	FALSE			**b**

12	CUDA offers the Chevron Syntax to configure and execute a kernel.	TRUE	FALSE			**a**
13	the BlockPerGrid and ThreadPerBlock parameters are related to the _____ model supported by CUDA.	host	kernel	thread abstract ion	none of above	**c**
14	_____ is Callable from the device only	_host_	__global__	_device_	none of above	**c**
15	_____ is Callable from the host	_host_	__global__	_device_	none of above	**b**
16	_____ is Callable from the host	_host_	__global__	_device_	none of above	**a**
17	CUDA supports _____ in which code in a single thread is executed by all other threads.	tread division	tread termination	thread abstraction	none of above	**c**
18	In CUDA, a single invoked kernel is referred to as a _____.	block	tread	grid	none of above	**c**
19	A grid is comprised of _____ of threads.	block	bunch	host	none of above	**a**
20	A block is comprised of multiple _____.	treads	bunch	host	none of above	**a**
21	a solution of the problem in representing the parallelismin algorithm is	CUD	PTA	CDA	CUDA	**d**
22	_____ is Callable from the host	_host_	__global__	_device_	none of above	**b**
23	_____ is Callable from the host	_host_	__global__	_device_	none of above	**a**
24	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
25	The kernel code is dentified by the _____qualifier with void return type	_host_	__global__	_device_	void	**b**

26	Host codes in a CUDA application can not Reset a device	TRUE	FALSE			**b**
27	Host codes in a CUDA application can not Invoke kernels	TRUE	FALSE			**b**
28	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
29	Calling a kernel is typically referred to as _____.	kernel thread	kernel initialization	kernel termination	kernel invocation	**d**
30	In CUDA, a single invoked kernel is referred to as a _____.	block	tread	grid	none of above	**c**
31	A grid is comprised of _____ of threads.	block	bunch	host	none of above	**a**
32	A block is comprised of multiple _____.	treads	bunch	host	none of above	**a**
33	A CUDA program is comprised of two primary components: a host and a _____.	GPU kernel	CPU kernel	OS	none of above	**a**
34	_____ is Callable from the host	_host_	__global__	_device_	none of above	**a**
35	In CUDA, a single invoked kernel is referred to as a _____.	block	tread	grid	none of above	**c**
36	the BlockPerGrid and ThreadPerBlock parameters are related to the _____ model supported by CUDA.	host	kernel	thread abstract ion	none of above	**c**
37	Host codes in a CUDA application can Transfer data to and from the device	TRUE	FALSE			**a**
38	Host codes in a CUDA application can not Deallocate memory on the GPU	TRUE	FALSE			**b**

39	Host codes in a CUDA application can not Reset a device	TRUE	FALSE			**b**
40	Calling a kernel is typically referred to as _____.	kernel thread	kernel initialization	kernel termination	kernel invocation	**d**

UNIT FIVE SUB : 410241 HPC

Questions	Option 1	Option 2	Option 3	Option 4	Ans
Which of the following statements is **NOT TRUE** for Internal Sorting algorithms	Usually deal with small number of elements	No of elements must be able to fit in process's main memory	Use auxilliary memory like tape or hard disk	Ususally are of type compare-exchange	**3**
In sorting networks for INCREASING COMPARATOR with input x,y select the correct output X', Y' from the following options	X' = min { x , y } and Y' = min { x , y }	X' = max { x , y } and Y' = min { x , y }	X' = min { x , y } and Y' = max{ x , y }	X' = max { x , y } and Y' = max { x , y }	**3**
In sorting networks for DECREASING COMPARATOR with input x,y select the correct output X', Y' from the following options	X' = min { x , y } and Y' = min { x , y }	X' = max { x , y } and Y' = min { x , y }	X' = min { x , y } and Y' = max{ x , y }	X' = max { x , y } and Y' = max { x , y }	**2**
Which of the following is TRUE for **Bitonic Sequence** a) Monotonically increasing b) Monotonically Decreasing c) With cyclic shift of indices d) First increasing then decreasing	a) and b)	a) and b) and d)	a) and b) and c)	a) and b) and c) and d)	**4**
Which of the following is **NOT a BITONIC Sequence**	{8, 6, 4, 2, 3, 5, 7, 9}	{0, 4, 8, 9, 2, 1}	{3, 5, 7, 9, 8, 6, 4, 2}	{1, 2, 4, 7, 6, 0, 1}	**4**
The procedure of sorting a bitonic sequence using bitonic splits is called	Bitonic Merge	Bitonic Split	Bitonic Divide	Bitonic Series	**1**

UNIT FIVE SUB : 410241 HPC

Questions	Option 1	Option 2	Option 3	Option 4	Ans
Which of the following statements is **NOT TRUE** for Internal Sorting algorithms	Usually deal with small number of elements	No of elements must be able to fit in process's main memory	Use auxilliary memory like tape or hard disk	Ususally are of type compare-exchange	**3**
While mapping Bitonic sort on Hypercube, Compare-exchange operations take place between wires whose labels differ in	One Bit	Two bits	Three Bits	Four bits	**1**
Which of following is **NOT A WAY** of mapping the input wires of the bitonic sorting network to a MESH of processes	Row Major Mapping	Column Major Mapping	Row Major Snakelike mapping	Row Major Shuffled Mapping	**2**
Which is the sorting algorithm in below given steps - 1. procedure X_SORT(n) 2. begin 3. for i := n - 1 downto 1 do 4. for j := 1 to i do 5. compare-exchange(aj, aj + 1); 6. end X_SORT	Selection Sort	Bubble Sort	Parallel Selcetion Sort	Parallel Bubble Sort	**2**
The **odd-even transposition** algorithm sorts n elements in n phases (n is even), each of which requires ----------compare-exchange operations	2n	n2	n/2	n	**3**

UNIT FIVE SUB : 410241 HPC					
Questions	**Option 1**	**Option 2**	**Option 3**	**Option 4**	**Ans**
Which of the following statements is **NOT TRUE** for Internal Sorting algorithms	Usually deal with small number of elements	No of elements must be able to fit in process's main memory	Use auxilliary memory like tape or hard disk	Ususally are of type compare-exchange	**3**
What is TRUE about SHELL SORT	Moves elements only one position at a time	Moves elements long distance	During second phase algorithm switches to odd even transposition sort	both 2 and 3	**4**
Which is the fastest sorting algorithm	Bubble Sort	Odd-Even Transposition Sort	Shell Sort	Quick Sort	**4**
Quicksort's performance is greatly affected by the way it partitions a sequence.	TRUE	FALSE			**1**
Pivot in Quick sort can be selected as	Always First Element	Always Last element	Always Middle index Element	Randomly Selected Element	**4**
Quick sort uses Recursive Decomposition	TRUE	FALSE			**1**
In first step of parallelizing quick sort for n elements to get subarrays, which of the following statement is TRUE	Only one process is used	n processes are used	two processes are used	None of the above	**1**

UNIT FIVE SUB : 410241 HPC

Questions	Option 1	Option 2	Option 3	Option 4	Ans
Which of the following statements is **NOT TRUE** for Internal Sorting algorithms	Usually deal with small number of elements	No of elements must be able to fit in process's main memory	Use auxilliary memory like tape or hard disk	Ususally are of type compare-exchange	3
In Binary tree representation created by execution of Quick sort, Pivot is at	Leaf Node	Root of tree	Any internal node	None of the above	2
What is the worst case time complexity of a quick sort algorithm?	O(N)	O(N log N)	O(N2)	O(log N)	3
What is the average running time of a quick sort algorithm?	O(N)	O(N log N)	O(N2)	O(log N)	2
Odd-even transposition sort is a variation of	Quick Sort	Shell Sort	Bubble Sort	Selection Sort	3
What is the average case time complexity of odd-even transposition sort?	O(N log N)	O(N)	O(log N)	O(N2)	4
Shell sort is an improvement on	Quick Sort	Bubble Sort	Insertion sort	Selection Sort	3
In parallel Quick Sort Pivot is sent to processes by	Broadcast	Multicast	Selective Multicast	Unicast	1

UNIT FIVE SUB : 410241 HPC

Questions	Option 1	Option 2	Option 3	Option 4	Ans
Which of the following statements is **NOT TRUE** for Internal Sorting algorithms	Usually deal with small number of elements	No of elements must be able to fit in process's main memory	Use auxilliary memory like tape or hard disk	Ususally are of type compare-exchange	**3**
In parallel Quick Sort each process divides the unsorted list into	n Lists	2 Lists	4 Lists	n-1 Lists	**2**
Time Complexity of DFS is? (V – number of vertices, E – number of edges)	O(V + E)	O(V)	O(E)	O(V*E)	**1**
A person wants to visit some places. He starts from a vertex and then wants to visit every vertex till it finishes from one vertex, backtracks and then explore other vertex from same vertex. What algorithm he should use?	BFS	DFS	Prim's	Kruskal's	**2**
Given an array of n elements and p processes, in the message-passing version of the parallel quicksort, each process stores ---------elements of array	n*p	n-p	p/n	n/p	**4**
In parallel quick sort Pivot selecton strategy is crucial for	Maintaing load balance	Maintaining uniform distribution of elements in process groups	Effective Pivot selection in next level	all of the above	**4**

UNIT FIVE SUB : 410241 HPC

Questions	Option 1	Option 2	Option 3	Option 4	Ans
Which of the following statements is **NOT TRUE** for Internal Sorting algorithms	Usually deal with small number of elements	No of elements must be able to fit in process's main memory	Use auxilliary memory like tape or hard disk	Ususally are of type compare-exchange	**3**
In execution of the hypercube formulation of quicksort for d = 3, split along ----------dimention to partition sequence into two big blocks, one greater than pivot and other smaller than pivot as shown in diagram	first	scond	third	None of above	**3**
Which Parallel formulation of Quick sort is possible	Shared-Address-Space Parallel Formulation	Message Passing formulation	Hypercube Formulation	All of the above	**4**
Which formulation of Dijkstra's algorithm exploits more parallelism	source-partitioned formulation	source-parallel formulation	Partitioned-Parallel Formulation	All of above	**2**
In Dijkstra's all pair shortest path each process compute the single-source shortest paths for all vertices assigned to it in SOURCE PARTITIONED FORMULATION	TRUE	FALSE			**1**

UNIT FIVE SUB : 410241 HPC

Questions	Option 1	Option 2	Option 3	Option 4	Ans
Which of the following statements is **NOT TRUE** for Internal Sorting algorithms	Usually deal with small number of elements	No of elements must be able to fit in process's main memory	Use auxilliary memory like tape or hard disk	Ususally are of type compare-exchange	3
A complete graph is a graph in which each pair of vertices is adjacent	TRUE	FALSE			1
The space required to store the adjacency matrix of a graph with n vertices is	in order of n	in order of n log n	in order of n squared	in order of n/2	3
Graph can be represented by	Identity Matrix	Adjacency Matrix	Sprse list	Sparse matrix	2
to solve the all-pairs shortest paths problem which algorithm/s is/are used a) Floyd's algorithm b) Dijkstra's single-source shortest paths c) Prim's Algorithm d) Kruskal's Algorithm	a) and c)	a) and b)	b) and c)	c) and d)	2
Simple backtracking is a depth-first search method that terminates upon finding the first solution.	TRUE	FALSE			1
Best-first search (BFS) algorithms can search both graphs and trees.	TRUE	FALSE			1

UNIT FIVE SUB : 410241 HPC					
Questions	**Option 1**	**Option 2**	**Option 3**	**Option 4**	**Ans**
Which of the following statements is **NOT TRUE** for Internal Sorting algorithms	Usually deal with small number of elements	No of elements must be able to fit in process's main memory	Use auxilliary memory like tape or hard disk	Ususally are of type compare-exchange	**3**
A* algorithm is a	BFS algorithm	DFS Algorithm	Prim's Algorithm	Kruskal's Algorithm	**1**
identify Load-Balancing Scheme/s	Asynchronous Round Robin	Global Round Robin	Random Polling	All above methods	**4**
important component of best-first search (BFS) algorithms is	Open List	Closed List	Node List	Mode List	**1**

UNIT SIX	SUB : 410241 HPC					
Sr. No.	**Questions**	**Option 1**	**Option 2**	**Option 3**	**Option 4**	**Ans**
1	Any condition that causes a processor to stall is called as _____.	Hazard	Page fault	System error	None of the above	**1**
2	The time lost due to branch instruction is often referred to as _____.	Latency	Delay	Branch penalty	None of the above	**3**
3	_____ method is used in centralized systems to perform out of order execution.	Scorecard	Score boarding	Optimizing	Redundancy	**2**
4	The computer cluster architecture emerged as an alternative for ____.	ISA	Workstation	Super computers	Distributed systems	**3**
5	NVIDIA CUDA Warp is made up of how many threads?	512	1024	312	32	**4**
6	Out-of-order instructions is not possible on GPUs.	TRUE	FALSE	--	--	**2**
7	CUDA supports programming in	C or C++ only	Java, Python, and more	C, C++, third party wrappers for Java, Python, and more	Pascal	**3**
8	FADD, FMAD, FMIN, FMAX are ----- supported by Scalar Processors of NVIDIA GPU.	32-bit IEEE floating point instructions	32-bit integer instructions	both	none of the above	**1**

9	Each streaming multiprocessor (SM) of CUDA herdware has ------ scalar processors (SP).	1024	128	512	8	**4**
10	Each NVIDIA GPU has ------ Streaming Multiprocessors	8	1024	512	16	**4**
11	CUDA provides ------- warp and thread scheduling. Also, the overhead of thread creation is on the order of ----.	“programming-overhead”, 2 clock	“zero-overhead”, 1 clock	64, 2 clock	32, 1 clock	**2**
12	Each warp of GPU receives a single instruction and “broadcasts” it to all of its threads. It is a ---- operation.	SIMD (Single instruction multiple data)	SIMT (Single instruction multiple thread)	SISD (Single instruction single data)	SIST (Single instruction single thread)	**2**
13	Limitations of CUDA Kernel	recursion, call stack, static variable declaration	No recursion, no call stack, no static variable declarations	recursion, no call stack, static variable declaration	No recursion, call stack, no static variable declarations	**2**
14	What is Unified Virtual Machine	It is a technique that allow both CPU and GPU to read from single virtual machine, simultaneously.	It is a technique for managing separate host and device memory spaces.	It is a technique for executing device code on host and host code on device.	It is a technique for executing general purpose programs on device instead of host.	**1**
15	_____ became the first language specifically designed by a GPU Company to facilitate general purpose computing on ____.	Python, GPUs.	C, CPUs.	CUDA C, GPUs.	Java, CPUs.	**3**

16	The CUDA architecture consists of --------- for parallel computing kernels and functions.	RISC instruction set architecture	CISC instruction set architecture	ZISC instruction set architecture	PTX instruction set architecture	**4**
17	CUDA stands for --------, designed by NVIDIA.	Common Union Discrete Architecture	Complex Unidentified Device Architecture	Compute Unified Device Architecture	Complex Unstructured Distributed Architecture	**3**
18	The host processor spawns multithread tasks (or kernels as they are known in CUDA) onto the GPU device. State true or false.	TRUE	FALSE	---	---	**1**
19	The NVIDIA G80 is a ---- CUDA core device, the NVIDIA G200 is a ---- CUDA core device, and the NVIDIA Fermi is a ---- CUDA core device.	128, 256, 512	32, 64, 128	64, 128, 256	256, 512, 1024	**1**
20	NVIDIA 8-series GPUs offer -------- .	50-200 GFLOPS	200-400 GFLOPS	400-800 GFLOPS	800-1000 GFLOPS	**1**
21	IADD, IMUL24, IMAD24, IMIN, IMAX are ---------- supported by Scalar Processors of NVIDIA GPU.	32-bit IEEE floating point instructions	32-bit integer instructions	both	none of the above	**2**
22	CUDA Hardware programming model supports: a) fully generally data-parallel archtecture; b) General thread launch; c) Global load-store; d) Parallel data cache; e) Scalar architecture; f) Integers, bit operation	a,c,d,f	b,c,d,e	a,d,e,f	a,b,c,d,e,f	**4**

23	In CUDA memory model there are following memory types available: a) Registers; b) Local Memory; c) Shared Memory; d) Global Memory; e) Constant Memory; f) Texture Memory.	a, b, d, f	a, c, d, e, f	a, b, c, d, e, f	b, c, e, f	**3**
24	What is the equivalent of general C program with CUDA C: int main(void) { printf("Hello, World!\n"); return 0; }	int main (void) { kernel <<<1,1>>>(); printf("Hello, World!\n"); return 0; }	__global__ void kernel(void) { } int main (void) { kernel <<<1,1>>>(); printf("Hello, World!\n"); return 0; }	__global__ void kernel(void) { kernel <<<1,1>>>(); printf("Hello, World!\n"); return 0; }	__global__ int main (void) { kernel <<<1,1>>>(); printf("Hello, World!\n"); return 0; }	**2**
25	Which function runs on Device (i.e. GPU): a) __global__ void kernel (void) { } b) int main (void) { ... return 0; }	a	b	both a,b	---	**1**
26	A simple kernel for adding two integers: __global__ void add(int *a, int *b, int *c) { *c = *a + *b; } where __global__ is a CUDA C keyword which indicates that:	add() will execute on device, add() will be called from host	add() will execute on host, add() will be called from device	add() will be called and executed on host	add() will be called and executed on device	**1**
27	If variable a is host variable and dev_a is a device (GPU) variable, to allocate memory to dev_a select correct statement:	cudaMalloc(&dev_a, sizeof(int))	malloc(&dev_a, sizeof(int))	cudaMalloc((void **) &dev_a, sizeof(int))	malloc((void**) &dev_a, sizeof(int))	**3**

28	If variable a is host variable and dev_a is a device (GPU) variable, to copy input from variable a to variable dev_a select correct statement:	memcpy(dev_a, &a, size);	cudaMemcpy(dev_a, &a, size, cudaMemcpyHostToDevice);	memcpy((void*) dev_a, &a, size);	cudaMemcpy((void*) &dev_a, &a, size, cudaMemcpyDeviceToHost);	**2**
29	Triple angle brackets mark in a statement inside main function, what does it indicates?	a call from host code to device code	a call from device code to host code	less than comparison	greater than comparison	**1**
30	What makes a CUDA code runs in parallel	__global__ indicates parallel execution of code	main() function indicates parallel execution of code	Kernel name outside triple angle bracket indicates excecution of kernel N times in parallel	first parameter value inside triple angle bracket (N) indicates excecution of kernel N times in parallel	**4**

Name of the Teacher: Dr. Prasad S.Halgaonkar

Class: BE **Subject: High Performance Computing**
AY: 2020-21 **SEM: I**

UNIT-1

1)	Conventional architectures coarsely comprise of a_____
	a) processor b) Memory system c) Datapath. d) All of Above
Ans:	**d**
Explanation:	
2)	Data intensive applications utilize_____
	a) High aggregate throughput b) High aggregate network bandwidth c) High processing and memory system performance. d) None of above
Ans:	**a**
Explanation:	
3)	A pipeline is like_____
	a. Overlaps various stages of instruction execution to achieve performance. b. House pipeline c. Both a and b d. gas line
Ans:	**a**
Explanation:	
4)	Scheduling of instructions is determined ____
	a) True Data Dependency b) Resource Dependency c) Branch Dependency d) All of above
Ans:	**d**
Explanation:	
5)	VLIW processors rely on_____

	a) Compile time analysis b) Initial time analysis c) Final time analysis d) Mid time analysis
Ans:	**a**
Explanation:	
6)	Memory system performance is largely captured by_____
	a) Latency b) Bandwidth c) Both a and b d) none of above
Ans:	**c**
Explanation:	
7)	The fraction of data references satisfied by the cache is called_____
	a) Cache hit ratio b) Cache fit ratio c) Cache best ratio *d)* none of above
Ans:	**a**
Explanation:	
8)	A single control unit that dispatches the same Instruction to various processors is__
	a) SIMD b) SPMD c) MIMD d) None of above
Ans:	**a**
Explanation:	
9)	The primary forms of data exchange between parallel tasks are_
	a. Accessing a shared data space b. Exchanging messages. c. Both A and B d. None of Above
Ans:	**c**
Explanation:	
10)	Switches map a fixed number of inputs to outputs.
	a) True b) False

Ans:	**a**
Explanation:	
11)	The stage in which the CPU fetches the instructions from the instruction cache in superscalar organization is
	a) **Prefetch stage** b) D1 (first decode) stage c) D2 (second decode) stage d) Final stage
Ans:	**a**
Explanation:	In the prefetch stage of pipeline, the CPU fetches the instructions from the instruction cache, which stores the instructions to be executed. In this stage, CPU also aligns the codes appropriately.
12)	The CPU decodes the instructions and generates control words in
	a) Prefetch stage b) D1 (first decode) stage c) D2 (second decode) stage d) Final stage
Ans:	**b**
Explanation:	In D1 stage, the CPU decodes the instructions and generates control words. For simple RISC instructions, only single control word is enough for starting the execution.
13)	The fifth stage of pipeline is also known as
	a) read back stage b) read forward stage c) write back stage d) none of the mentioned
Ans:	**c**
Explanation:	The fifth stage or final stage of pipeline is also known as "Write back (WB) stage".
14)	In the execution stage the function performed is
	a) CPU accesses data cache b) executes arithmetic/logic computations c) executes floating point operations in execution unit d) all of the mentioned
Ans:	**d**
Explanation:	In the execution stage, known as E-stage, the CPU accesses data cache, executes arithmetic/logic computations, and floating point operations in execution unit.
15)	The stage in which the CPU generates an address for data memory references in this stage is
	a) prefetch stage b) D1 (first decode) stage c) D2 (second decode) stage d) execution stage
Ans:	**c**

Explanation:	In the D2 (second decode) stage, CPU generates an address for data memory references in this stage. This stage is required where the control word from D1 stage is again decoded for final execution.
16)	The feature of separated caches is
	a) supports the superscalar organization b) high bandwidth c) low hit ratio d) all of the mentioned
Ans:	**d**
Explanation:	The separated caches have low hit ratio compared to a unified cache, but have the advantage of supporting the superscalar organization and high bandwidth.
17)	In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from
	a) floating point unit b) instruction cache c) floating point register file or data cache d) floating point register file or instruction cache
Ans:	**C**
Explanation:	In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from either floating point register file or data cache.
18)	The FPU (Floating Point Unit) writes the results to the floating point register file in
	a) X1 execution state b) X2 execution state c) write back stage d) none of the mentioned
Ans:	**c**
Explanation:	In the two execution stages of X1 and X2, the floating point unit reads the data from the data cache and executes the floating point computation. In the "write back stage" of pipeline, the FPU (Floating Point Unit) writes the results to the floating point register file.
19)	The floating point multiplier segment performs floating point multiplication in
	a) single precision b) double precision c) extended precision d) all of the mentioned
Ans:	**d**
Explanation:	The floating point multiplier segment performs floating point multiplication in single precision, double precision and extended precision.
20)	The instruction or segment that executes the floating point square root instructions is
	a) floating point square root segment b) floating point division and square root segment c) floating point divider segment d) none of the mentioned

Ans:	**c**
Explanation:	The floating point divider segment executes the floating point division and square root instructions.
21)	The floating point rounder segment performs rounding off operation at
	a) after write back stage b) before write back stage c) before arithmetic operations d) none of the mentioned
Ans:	b
Explanation:	The results of floating point addition or division process may be required to be rounded off, before write back stage to the floating point registers.
21)	Which of the following is a floating point exception that is generated in case of integer arithmetic?
	a) divide by zero b) overflow c) denormal operand d) all of the mentioned
Ans:	D
Explanation:	In the case of integer arithmetic, the possible floating point exceptions in Pentium are: 1. divide by zero 2. overflow 3. denormal operand 4. underflow 5. invalid operation.

Name and Sign of Subject Teacher

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DEPARTMENT OF COMPUTER ENGINEERING

Name of the Teacher: Dr. Prasad S.Halgaonkar

Class: BE **Subject: High Performance Computing**
AY: 2020-21 **SEM: I**

UNIT-2

Note: Correct Answers are in Bold Fonts

1. The First step in developing a parallel algorithm is_

   A. To Decompose the problem into tasks that can be executed concurrently
   B. Execute directly
   C. Execute indirectly
   D. None of Above

2. The number of tasks into which a problem is decomposed determines its_

   A. Granularity
   B. Priority
   C. Modernity
   D. None of above

3. The length of the longest path in a task dependency graph is called_
   A. the critical path length
   B. the critical data length
   C. the critical bit length
   D. None of above

4. The graph of tasks (nodes) and their interactions/data exchange (edges)_
   A. Is referred to as a *task interaction graph*
   B. Is referred to as a *task Communication graph*
   C. Is referred to as a *task interface graph*
   D. None of Above

5. Mappings are determined by_

   A. task dependency
   B. task interaction graphs
   C. Both A and B
   D. None of Above

6. Decomposition Techniques are_
   A. recursive decomposition
   B. data decomposition
   C. exploratory decomposition

D. speculative decomposition
E. All of Above

7. The *Owner Computes Rule* generally states that the process assigned a particular data item is responsible for_

A. All computation associated with it
B. Only one computation
C. Only two computation
D. Only occasionally computation

8. A simple application of exploratory decomposition is_

A. The solution to a 15 puzzle
B. The solution to 20 puzzle
C. The solution to any puzzle
D. None of Above

9. Speculative Decomposition consist of _

A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B

10. task characteristics include:
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.
D. All of Above

11. Choose the most accurate (**CORRECT**) statement:
a. Scalability is a measure of the capacity to increase speedup in proportion to the number of processors
b. Efficiency is the ratio of the serial run time of the best sequential algorithm for solving a problem to the time taken by the parallel algorithm to solve the same problem on *p* processors
c. Run time is the time that elapses from the moment a parallel computation starts to the moment the last processor finishes.
d. Superlinear is the fraction of time for which a processor is usefully employed

12. Parallelism can be used to increase the (parallel) size of the problem is applicable in _____.
a. Amdahl's Law
b. Gustafson-Barsis's Law
c. Newton's Law

d. Pascal's Law

13. _____ is due to load imbalance, synchronization, or serial components as parts of overheads in parallel programs.
    a. Interprocess interaction
    b. Synchronization
    c. Idling
    d. Excess computation
14. Which of the following parallel methodological design elements focuses on recognizing opportunities for parallel execution?
    a. Partitioning
    b. Communication
    c. Aggromeration
    d. Mapping
15. Considering to use weak or strong scaling is part of _____ in addressing the challenges of distributed memory programming.
    a. Splitting the problem
    b. Speeding up computations
    c. Speeding up communication
    d. Speeding up hardware
16. Domain and functional decomposition are considered in the following parallel methodological design elements, **EXCEPT**:
    a. Partitioning
    b. Communication
    c. Agglomeration
    d. Mapping
17. Synchronization is one of the common issues in parallel programming. The issues related to synchronization include the followings, **EXCEPT**:
    a. Deadlock
    b. Livelock
    c. Fairness
    d. Correctness
18. Which of the followings is the **BEST** description of Message Passing Interface (MPI)?
    a. A specification of a shared memory library
    b. MPI uses objects called communicators and groups to define which collection of processes may communicate with each other
    c. Only communicators and not groups are accessible to the programmer only by a "handle"
    d. A communicator is an ordered set of processes

Name and Sign of Subject Teacher

Name of the Teacher: Mr. B A Chaugule **Class: BE** **Subject: High Performance Computing** **AY: 2020-21** **SEM: I**	
UNIT-1	
1)	Execution of several activities at the same time.
	a) processing b) parallel processing c) serial processing d) multitasking
Ans:	**b**
Explanation:	
2)	Parallel processing has single execution flow.
	a) True b) False
Ans:	**b**
Explanation:	The statement is false. Sequential programming specifically has single execution flow.
3)	A term for simultaneous access to a resource, physical or logical.
	a) Multiprogramming b) Multitasking c) Threads d) Concurrency
Ans:	**d**
Explanation:	Concurrency is the term used for the same. When several things are accessed simultaneously, the job is said to be concurrent.
4)	_____ leads to concurrency.
	a) Serialization b) Parallelism c) Serial processing d) Distribution
Ans:	**b**
Explanation:	Parallelism leads naturally to Concurrency. For example, Several processes trying to print a file on a single printer.
5)	A parallelism based on increasing processor word size.
	a) Increasing b) Count based c) Bit based d) Bit level
Ans:	**d**
Explanation:	Bit level parallelism is based on increasing processor word size. It focuses on hardware capabilities for structuring.
6)	The measure of the "effort" needed to maintain efficiency while adding processors.
	a) Maintainability b) Efficiency

	c) Scalability d) Effectiveness
Ans:	**C**
Explanation:	The measure of the "effort" needed to maintain efficiency while adding processors is called as scalability.
7)	Several instructions execution simultaneously in _____
	a) processing b) parallel processing c) serial processing d) multitasking
Ans:	**b**
Explanation:	In parallel processing, the several instructions are executed simultaneously.
8)	Conventional architectures coarsely comprise of a_
	a) A processor b) Memory system c) Data path. d) All of Above
Ans:	**d**
Explanation:	
9)	A pipeline is like_
	a) Overlaps various stages of instruction execution to achieve performance. b) House pipeline c) Both a and b d) A gas line
Ans:	**a**
Explanation:	
10)	VLIW processors rely on_
	a) Compile time analysis b) Initial time analysis c) Final time analysis d) Mid time analysis
Ans:	**a**
Explanation:	
11)	Memory system performance is largely captured by_
	a) Latency b) Bandwidth c) Both a and b d) none of above
Ans:	**c**
Explanation:	
12)	The fraction of data references satisfied by the cache is called_
	a) Cache hit ratio b) Cache fit ratio

	c) Cache best ratio d) none of above
Ans:	**a**
Explanation:	
13)	A single control unit that dispatches the same Instruction to various processors is__
	a) SIMD b) SPMD c) MIMD d) None of above
Ans:	**a**
Explanation:	
14)	The primary forms of data exchange between parallel tasks are_
	a) Accessing a shared data space b) Exchanging messages. c) Both A and B d) None of Above
Ans:	**c**
Explanation:	
16)	Switches map a fixed number of inputs to outputs.
	a) True b) False
Ans:	**a**
Explanation:	
UNIT-2	
1)	The First step in developing a parallel algorithm is_
	a) To Decompose the problem into tasks that can be executed concurrently b) Execute directly c) Execute indirectly d) None of Above
Ans:	**a**
Explanation:	
2)	The number of tasks into which a problem is decomposed determines its_
	a) Granularity b) Priority c) Modernity d) None of above
Ans:	**A**
Explanation:	
3)	The length of the longest path in a task dependency graph is called_
	a) the critical path length b) the critical data length c) the critical bit length

	d) None of above
Ans:	**a**
Explanation:	
4)	The graph of tasks (nodes) and their interactions/data exchange (edges)_
	a) Is referred to as a task interaction graph b) Is referred to as a task Communication graph c) Is referred to as a task interface graph d) None of Above
Ans:	**a**
Explanation:	
5)	Mappings are determined by_
	a) task dependency b) task interaction graphs c) Both A and B d) None of Above
Ans:	**c**
Explanation:	
6)	Decomposition Techniques are_
	a) recursive decomposition b) data decomposition c) exploratory decomposition d) speculative decomposition e) All of Above
Ans:	**E**
Explanation:	
7)	The Owner Computes Rule generally states that the process assigned a particular data item is responsible for_
	a) All computation associated with it b) Only one computation c) Only two computation d) Only occasionally computation
Ans:	**A**
Explanation:	
8)	A simple application of exploratory decomposition is_
	a) The solution to a 15 puzzle b) The solution to 20 puzzle c) The solution to any puzzle d) None of Above
Ans:	**A**
Explanation:	
9)	Speculative Decomposition consist of _

	a) conservative approaches b) optimistic approaches c) Both A and B d) Only B
Ans:	**C**
Explanation:	
10)	task characteristics include:
	a) Task generation. b) Task sizes. c) Size of data associated with tasks. d) All of Above
Ans:	**d**
Explanation:	
UNIT-3	
1)	Group communication operations are built using point-to-point messaging primitives
	a) True b) False
Ans:	**A**
Explanation:	
2)	Communicating a message of size m over an uncongested network takes time ts + tmw
	a) True b) False
Ans:	**A**
Explanation:	
3)	The dual of one-to-all broadcast is_
	a) All-to-one reduction b) All-to-one receiver c) All-to-one Sum d) None of Above
Ans:	**A**
Explanation:	
4)	A hypercube has_
	a) 2d nodes b) 2d nodes c) 2n Nodes d) N Nodes
Ans:	**a**
Explanation:	
5)	A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes.

	a) True b) False
Ans:	**A**
Explanation:	
6)	In All-to-All Broadcast each processor is the source as well as destination.
	a) True b) False
Ans:	**A**
Explanation:	
7)	The Prefix Sum Operation can be implemented using the_
	a) All-to-all broadcast kernel. b) All-to-one broadcast kernel. c) One-to-all broadcast Kernel d) Scatter Kernel
Ans:	**A**
Explanation:	
8)	In the scatter operation_
	a) Single node send a unique message of size m to every other node b) Single node send a same message of size m to every other node c) Single node send a unique message of size m to next node d) None of Above
Ans:	**A**
Explanation:	
9)	The gather operation is exactly the inverse of the_
	a) Scatter operation b) Broadcast operation c) Prefix Sum d) Reduction operation
Ans:	**A**
Explanation:	
10)	In All-to-All Personalized Communication Each node has a distinct message of size m for every other node
	a) True b) False
Ans:	**a**
Explanation:	

Name and Sign of Subject Teacher

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Date: 23/07/2020

Class : BE Computer Div: A + B Subject : High Performance Computing
Academic Year : 2020-21 Sem : I Exam Date: 23/07/2020

Q. No.	*Question Description*	*Options*	*Correct Answer*	*Marks*	*CO*	*PO*	*PSO*	*BTL*
1	Select different aspects of parallelism	A. data intensive applications utilize high aggregate throughput B. server applications utilize high aggregate network bandwidth C. scientific applications typically utilize high processing and memory system performance D. all of the above	**D**	**2**	**1**	**1**	**3**	**4**
2	Select correct answer: DRAM access times have only improved at the rate of roughly ____% per year over this interval.	A. 10 B. 20 C. 40 D. 50	**A**	**2**	**1**	**1**	**3**	**4**
3	Justify, why to use parallel computing?	A. Real world is massively parallel B. Save time and/or time C. Solve larger / more complex problems D. Provide concurrency E. All of the above	**E**	**2**	**1**	**3**	**3**	**5**
4	Analyze, if the second instruction has data dependencies with the first, but the third instruction does not, the first	A. In-order B. Out-of-order C. Both of the above D. None of the above	**B**	**2**	**1**	**3**	**3**	**4**

	and third instructions can be co-scheduled. Which type if this issue is?							
5	Select the parameters which captures Memory system performance	A. Latency B. Bandwidth C. Both of the above D. None of the above	**C**	**2**	**1**	**3**	**3**	**4**
6	Consider the example of a fire-hose. If the water comes out of the hose five seconds after the hydrant is turned on. Once the water starts flowing, if the hydrant delivers water at the rate of 15 gallons/second. Analyze the bandwidth and latency.	A. Bandwidth: 5 gallons/second and Latency: 15 seconds B. Bandwidth: 5*15 gallons/second and Latency: 15 seconds C. Bandwidth: 15 gallons/second and Latency: 5 seconds D. Bandwidth: 3 gallons/second and Latency: 5 seconds	**C**	**2**	**1**	**4**	**3**	**5**
7	Select alternate approaches for Hiding Memory Latency	A. Prefeching B. Multithreading C. spatial locality D. all of the above	**D**	**2**	**1**	**3**	**3**	**4**
8	Select which clause in OpenMP is similar to the private, except values of variables are initialized to corresponding values before the	A. Private B. Firstprivate C. Shared D. All of the above	**B**	**2**	**1**	**5**	**3**	**4**

	parallel directive.							
9	The time which includes all overheads that are determined by the length of the message like bandwidth of links, error checking and correction, etc. is called as	A. Startup time (ts) B. Per-hop time (th) C. Per-word transfer time (tw) D. All of the above	**C**	**2**	**1**	**1**	**3**	**1**
10	Select in which routing technique, Message is divided into packets?	A. Store-and-forward routing B. Packet routing C. cut-through-routing D. in both 2 and 3	**D**	**2**	**1**	**3**	**3**	**4**
11	Which of the following is an efficient method of cache updating?	A. Snoopy writes B. Write through C. Write within D. Buffered write	**A**	**2**	**1**	**1**	**3**	**1**
12	Select which protocol is used for maintaining coherence of multiple processors?	A. Data coherence protocols B. Commit coherence protocols C. Recurrence D. Cache coherence protocols	**D**	**2**	**1**	**3**	**3**	**4**
13	From inter-processor communication, the misses arises are often called	A. Coherence misses B. Commit misses C. Parallel processing D. Hit rate	**A**	**2**	**1**	**1**	**3**	**1**
14	As per Flynn's Classification, where Parallel processing may occur?	A. in the instruction stream B. in the data stream C. both of the above D. none of the above	**C**	**2**	**1**	**1**	**3**	**1**

15	Which of the following projects of Blue Gene is not in development?	A. Blue Gene / L B. Blue Gene / M C. Blue Gene / P D. Blue Gene / Q	**B**	**2**	**1**	**1**	**3**	**1**

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Unit Test II Date: 26/08/2020

Class : BE Computer Div: A + B Subject : High Performance Computing
Academic Year : 2020-21 Sem : I Exam Date: 26/08/2020

Q. No.	*Question Description*	*Options 28*	*Correct Answer*	*Marks*	*CO*	*PO*	*PSO*	*BTL*
1	Task interaction graphs represent _____ dependencies, whereas task dependency graphs represent _____ dependencies.	A. control, data B. task, data C. process, control D. data, control	**D**	**2**	**2**	**1**	**3**	**4**
2	Select correct answer. Which graph represents tasks as nodes and their interactions/data exchange as edges?	A. task dependency graph B. process dependency graph C. process interaction graph D. task interaction graph	**D**	**2**	**2**	**1**	**3**	**4**
3	The average number of tasks that can be processed in parallel over the execution of the program is called as _____	A. average degree of concurrency B. degree of concurrency C. critical path length D. maximum concurrency	**A**	**2**	**2**	**1**	**3**	**4**
4	The number of tasks that can be executed in	A. average concurrency B. degree of concurrency C. critical path length	**B**	**2**	**2**	**1**	**3**	**4**

	parallel is the _____ of a decomposition.	D. maximum concurrency						
5	A decomposition can be illustrated in the form of a directed graph with nodes corresponding to tasks and edges indicating that the result of one task is required for processing the next. Such graph is called as _____	A. process dependency graph B. task dependency graph C. task interaction graph D. process interaction graph	**B**	**2**	**2**	**1**	**3**	**4**
6	In which case, the owner computes rule implies that the output is computed by the process to which the output data is assigned?	A. input data decomposition B. output data decomposition C. Both of the above D. None of the above	**B**	**2**	**2**	**4**	**3**	**5**
7	Select relevant task characteristics from the options given below:	A. Task generation B. Task sizes C. Size of data associated with tasks D. All of the above	**D**	**2**	**2**	**1**	**3**	**4**
8	A classic example of game playing - each 15 puzzle board is the example of _____	A. Static Task Generation B. Dynamic Task Generation C. None of the above D. All of the above	**B**	**2**	**2**	**3**	**3**	**4**
9	Analyze task interaction pattern	A. static regular interaction pattern B. static irregular interaction pattern	**B**	**2**	**2**	**3**	**3**	**5**

	of the multiplication of a sparse matrix with a vector.	C. dynamic regular interaction pattern D. dynamic irregular interaction pattern						
10	Select the methods for containing Interaction Overheads.	A. Maximize data locality B. Minimize volume of data exchange C. Minimize frequency of interactions D. Minimize contention and hot-spots E. All of the above	**E**	**2**	**2**	**3**	**3**	**4**
11	Which model is equally suitable to shared-address-space or message-passing paradigms, since the interaction is naturally two ways.	A. Work pool model B. Master slave model C. Data parallel model D. Producer consumer or pipeline model	**B**	**2**	**2**	**1**	**3**	**4**
12	In which type of the model, tasks are dynamically assigned to the processes for balancing the load?	A. Work pool model B. Master slave model C. Data parallel model D. Producer consumer or pipeline model	**A**	**2**	**2**	**3**	**3**	**4**
13	Select the appropriate stage of GPU Pipeline which receives commands from CPU and also pulls geometry information from system memory.	A. pixel processing B. vertex processing C. memory interface D. host interface	**D**	**2**	**2**	**12**	**3**	**4**
14	Select the hardware specifications	A. GPU Clock Speed B. Size of memory bus C. Amount of available memory	**E**	**2**	**2**	**12**	**3**	**1**

	which most affect the GPU cards speed.	D. Memory Clock Rate E. All of the above						
15	Select the appropriate stage of GPU Pipeline where computations include texture mapping and math operations.	A. pixel processing B. vertex processing C. memory interface D. host interface	**A**	**2**	**2**	**12**	**3**	**1**

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Unit Test III Date: 14/10/2020

Class : BE Computer Div: A Subject : High Performance Computing
Academic Year : 2020-21 Sem : I Exam Date: 14/10/2020

Q. No.	*Question Description*	*Options 28*	*Correct Answer*	*Marks*	*CO*	*PO*	*PSO*	*BTL*
1	In all-to-one reduction, data items must be combined piece-wise and the result made available at a _____ processor.	A. First B. Last C. Target D. N-1	**C**	**2**	**3**	**1**	**3**	**4**
2	Analyze the Cost of Scatter and Gather .	A. T=tw log p + ts m (p-1) B. T=ts log p + tw m (p-1) C. T=ts log p - tw m (p-1) D. T=tw log p - ts m (p-1)	**B**	**2**	**3**	**4**	**3**	**4**
3	All-to-all personalized communication is also known as _____.	A. partial exchange B. total exchange C. both of the above D. none of the above	**B**	**2**	**3**	**1**	**3**	**1**
4	All-to-all personalized communication is performed independently in each row with clustered messages of size _____ on a mesh.	A. m B. p C. m√p D. p√m	**C**	**2**	**3**	**1**	**3**	**4**
5	In All-to-All Personalized Communication on a Ring, the size of the message reduces by _____ at each step	A. m B. p C. m-1 D. p-1	**A**	**2**	**3**	**1**	**3**	**1**

6	All-to-All Broadcast and Reduction algorithm on a Ring terminates in _____steps.	A. p B. p+1 C. p-1 D. p*p	**C**	**2**	**3**	**1**	**3**	**1**
7	In All-to-all Broadcast on a Mesh, operation performs in which sequence?	A. rowwise, rowwise B. rowwise, columnwise C. columnwise, rowwise D. columnwise, columnwise	**B**	**2**	**3**	**1**	**3**	**3**
8	In the _____ operation, a single node sends a unique message of size m to every other node.	A. Scatter B. gather	**A**	**2**	**3**	**3**	**3**	**1**
9	In the _____ operation, a single node collects a unique message from each node.	A. Scatter B. gather	**B**	**2**	**3**	**3**	**3**	**1**
10	Messages get smaller in _____and stay constant in _____.	A. broadcast, gather B. gather, broadcast C. scatter , broadcast D. scatter, gather	**C**	**2**	**3**	**1**	**3**	**4**
11	The time taken by all-to-all broadcast on a ring is _____.	A. T= $2t_s(\sqrt{p} - 1) + t_w m(p-1)$ B. T= $(t_s + t_w m)(p-1)$ C. T= $t_s \log_p + t_w m(p-1)$ D. T= $2t_s(\sqrt{p} - 1) - t_w m(p-1)$	**B**	**2**	**3**	**4**	**3**	**4**
12	The time taken by all-to-all broadcast on a mesh is _____.	A. T= $2t_s(\sqrt{p} - 1) + t_w m(p-1)$ B. T= $(t_s + t_w m)(p-1)$ C. T= $t_s \log_p + t_w m(p-1)$ D. T= $2t_s(\sqrt{p} - 1) - t_w m(p-1)$	**A**	**2**	**3**	**4**	**3**	**4**
13	The time taken by all-to-all broadcast on a hypercube is _____.	A. T= $2t_s(\sqrt{p} - 1) + t_w m(p-1)$ B. T= $(t_s + t_w m)(p-1)$ C. T= $t_s \log_p + t_w m(p-1)$ D. T= $2t_s(\sqrt{p} - 1) - t_w m(p-1)$	**C**	**2**	**3**	**4**	**3**	**4**
14	_____ is a special permutation in which	A. Left shift B. Right shift	**C**	**2**	**3**	**1**	**3**	**1**

	node *i* sends a data packet to node *(i + q)* mod *p* in a *p*-node ensemble *(0 ≤ q ≤ p)*.	C. Circular shift D. Linear shift						
15	The prefix-sum operation can be implemented using the _____kernel	A. all-to-all reduction B. all-to-all broadcast C. one-to-all broadcast D. all-to-one broadcast	**B**	**2**	**3**	**1**	**3**	**1**

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Unit Test IV Date: 09/11/2020

Class : BE Computer Div: A Subject : High Performance Computing
Academic Year : 2020-21 Sem : I Exam Date: 11/11/2020

Q. No.	*Question Description*	*Options 28*	*Correct Answer*	*Marks*	*CO*	*PO*	*PSO*	*BTL*
1	Select the parameters on which the parallel runtime of a program depends.	A. Input size B. Number of processors C. Communication parameters of the machine D. All of the above	**D**	**2**	**4**	**1**	**3**	**4**
2	The time that elapses from the moment the first processor starts to the moment the last processor finishes execution is called as _____.	A. Serial runtime B. Parallel runtime C. Overhead runtime D. Excess runtime	**B**	**2**	**4**	**4**	**3**	**4**
3	Select how the overhead function (T_o) is calculated.	A. $T_o = T_P - T_S$ B. $T_o = p*n\ T_P - T_S$ C. $T_o = p\ T_P - T_S$ D. $T_o = T_P - pT_S$	**C**	**2**	**4**	**1**	**3**	**1**
4	What is is the ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with ***p*** identical processing elements?	A. Efficiency B. Overall time C. Speedup D. Scaleup	**C**	**2**	**4**	**1**	**3**	**4**
5	The parallel time for odd-even sort (efficient	A. 3.75 B. 3.5	**B**	**2**	**4**	**1**	**3**	**1**

	parallelization of bubble sort) is 50 seconds. The serial time for bubblesort is 175 seconds. Evaluate the speedup of bubble sort.	C. 0.33 D. 0.26						
6	Consider the problem of adding ***n*** numbers by using ***n*** processing elements. The serial time taken is Θ (***n***) and parallel time is Θ (**log *n***). Evaluate the efficiency.	A. E = Θ (***n*** / **log *n***) B. E = Θ (***n*** **log *n***) C. E = Θ (**log *n* / *n***) D. E = Θ (**1 / log *n***)	**D**	**2**	**4**	**1**	**3**	**1**
7	What will be the efficiency of cost optimal parallel systems?	A. ***E*** = *O*(n). B. ***E*** = *O*(1). C. ***E*** = *O*(p). D. ***E*** = *O*(n log n).	**B**	**2**	**4**	**1**	**3**	**3**
8	Which law states that the maximum speedup of a parallel program is limited by the sequential fraction of the initial sequential program?	A. Amdahl's Law B. Flynn's Law C. Moore's Law D. Van Neumann's Law	**A**	**2**	**4**	**3**	**3**	**1**
9	Arrange the steps for the Matrix-Vector 2-D partitioning: i) result vector is computed by performing an all-to-one reduction along the columns. ii) Alignment of the vector *x* along the principal diagonal of the matrix. iii) Copy the vector	A. i, ii, iii B. ii, iii, i C. iii, i, ii D. ii, i, iii	**B**	**2**	**4**	**3**	**3**	**1**

	elements from each diagonal process to all the processes in the corresponding column using *n* simultaneous broadcasts among all processors in the column.							
10	Arrange the communication sequence in Matrix-Vector 2-D partitioning: i) all-to-one reduction in each row ii) one-to-all broadcast of each vector element among the *n* processes of each column iii) one-to-one communication to align the vector along the main diagonal	A. i, ii, iii B. ii, iii, i C. iii, ii, i D. ii, i, iii	**C**	**2**	**4**	**1**	**3**	**4**
11	Parallel time in Rowwise 1-D Partitioning of Matrix-Vector Multiplication where p=n is ____.	A. $\Theta(1)$ B. $\Theta(n \log n)$ C. $\Theta(n^2)$ D. $\Theta(n)$	**D**	**2**	**4**	**4**	**3**	**4**
12	What are the sources of overhead in parallel programs?	A. Interprocess interaction B. Idling C. Excess computation D. All of the above	**D**	**2**	**4**	**4**	**3**	**4**
13	What are the performance metrics of parallel systems?	A. Execution time B. Total parallel overhead C. Speedup	**E**	**2**	**4**	**4**	**3**	**4**

		D. Efficiency E. All of the above						
14	The isoefficiency function determines the ease with which a parallel system can maintain a constant efficiency. True of false?	A. True B. False	**A**	**2**	**4**	**1**	**3**	**1**
15	Which matrix-matrix multiplication algorithm uses a 3-D partitioning?	A. Cannon's algorithm B. DNS algorithm C. Both of the above D. None of the above	**B**	**2**	**4**	**1**	**3**	**1**

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Prelim Exam Date: 29/12/2020

Class : BE Computer Div: A & B Subject : High Performance Computing
Academic Year : 2020-21 Sem : I Exam Date: 31/12/2020

Q. No.	*Question Description*	*Options*	*Correct Answer*	*Marks*	*CO*	*PO*	*PSO*	*BTL*
1	Which of the following is the type of parallelism?	**a. Bit level parallelism** **b. Instruction level parallelism** **c. Loop level parallelism** **d. All of the above**	**D**	**1**	1	**1,12**	**1**	**2**
2	Which of the parallelism is used by VLIW	**a. Bit level parallelism** **b. Instruction level parallelism** **c. Loop level parallelism** **d. Task level Parallelism**	**B**	1	1	**1,12**	**1**	**2**
3	Tendency of a software process to access information items whose addresses are near one another known as	**a. Spatial Locality** **b. Temporal locality** **c. Permanent Locality** **d. Sequential Locality**	**a**	1	1	**1**	**1**	**1**
4	Parallel Computers are classified based on Flynn's taxonomy which among the following options does not come under this	**a. SISD** **b. SIMD** **c. MIMD** **d. SIPD**	**d**	1	1	**1,12**	**1**	**1**
5	Which among the following is the popular multistage network	**a. Hypercube** **b. Omega**	**b**	1	1	**1**	**1**	**2**

		c. Gamma **d. K-D Mesh**						
6	The multicore architecture that consists of dedicated application specific processor cores that would target the issue of running variety of applications to be executed on a computer.	**a. Homogeneous core architecture.** **b. Heterogeneous core architecture.** **c. Polaris core architecture** **d. None of the above**	**b**	1	1	**1**	**1**	**3**
7	Decomposition of computation into a small number of large task is	**a. Fine grained granularity** **b. course grained granularity** **c. coarse grained granularity** **d. task grained granularity**	**C**	1	2	**1**	**3**	**1**
8	Which among the following is the type of decomposition	**a. Data-decomposition** **b. Hybrid decomposition** **c. Speculative decomposition** **d. All of the above**	**D**	1	2	**1,12**	**3**	**2**
9	The 15-puzzle problem uses which type of decomposition	**a. Data decomposition** **b. Exploratory decomposition** **c. Speculative decomposition** **d. Recursive decomposition**	**B**	1	2	**1,4,12**	**3**	**2**

10	An interaction pattern is considered to be _____if it has some structure that can be exploited for efficient implementation	**a. Structured interaction** **b. unstructured interaction** **c. Regular interaction** **d. Irregular interaction**	**C**	1	2	**1,12**	**3**	**2**
11	The mapping in which is tasks are distributed to processes during execution is called as___	**a. Dynamic mapping** **b. Static mapping** **c. Pre-execution mapping** **d. In-process mapping**	**a**	1	2	**1**	**1**	**1**
12	The parallel algorithm model in which mapping of tasks is done dynamically where pointer to tasks is stored in physically shared list/priority queue/hash table/tree is called	**a. The data parallel model** **b. Producer consumer model** **c. The task graph model** **d. Work pool model**	**d**	1	2	**1,2**	**1**	**2**
13	The world's first GPU is marketed by NVDIA in 1999 is	**a. GEForce 356** **b. GEForce 256** **c. GEForce 3800** **d. GEForce 956**	**B**	1	6	**5**	**3**	**1**
14	The operation in which data from all processes are combined at a single destination process is	**a. All to one reduction** **b. All to all reduction** **c. one to all reduction** **d. None of the above**	**A**	1	3	**1**	**1**	**2**
15	In scatter operation a single node sends a unique message to every node is also called as	a. One-to-one personalized communication b. One-to-all broadcast	**C**	1	3	**1**	**1**	**2**

		communication c. One-to-all personalized communication **d.** all-to-all personalized communication						
16	Single port communication node can communicate on all the channels connected to it and provides apparent speedup	a. True **b.** False	**B**	1	3	**1**	**1**	**1**
17	Symmetric multiprocessors architecture are sometimes known as	**a. Uniform memory access** **b. Static memory access** **c. Variable memory access** **d. All of the above**	**A**	1	3	**1**	**1**	**1**
18	Heuristic is way of trying	**a. To discover something or an idea embedded in a program** **b. To search and measure how far a node in a search tree seems to be from a goal** **c. To compare two nodes in a search tree to see if one is better than another** **d. All of the mentioned**	**a**	1	4	**1,2**	**3**	**2**
19	A * algorithm is based on	**a. Breadth-First search** **b. Depth-first Search** **c. Best first search** **d. Hill climbing**	**C**	1	5	**1,2**	**1**	**2**

20	Best – First search can be implemented using the following data structure	**a. Queue** **b. Stack** **c. Priority Queue** **d. Circular Queue**	**C**	1	5	**1,2**	**1**	**1**
21	_____is a measure of the fraction of time for which a processing element is usefully employed	**a. Scalability** **b. Efficiency** **c. Speedup** **d. isoefficiency**	**B**	1	5	**1,2**	**1**	**2**
22	The ___of a parallel system is a measure of its capacity to increase speedup in proportion to the number of processing elements	**A. speedup** **B. Cost** **C. Efficiency** **D. Scalability**	**D**	1	3	**1,12**	**1**	**2**
23	___helps us determine the best algorithm/architecture combination for a particular problem without explicitly analyzing all possible combinations under all possible co	**a. Isoefficiency Metric of scalability** **b. Efficiency matric of scalability** **c. Cost metric of scalability** **d. None of the above**	**A**	1	3	**1,3**	**1**	**2**
24	It is defined as a ratio of the time taken to solve a problem on a single processing element to the time computer with p identical processing elements	**a. Total parallel overhead** **b. Efficiency** **c. Cost** **d. speedup**	**D**	1	3	**1,12**	**1**	**1**
25	In Practice a speedup greater than p is sometimes observed. It is called as_____	**a. scalability effect** **b. superscalar effect**	**C**	1	3	**1,2, 12**	**1**	**1**

		c. super linearity effect **d. speedup effect**						
26	Odd-even transposition sort is not cost -optimal, because time product is	**a. theta(n^2)** **b. theta(n^logn)** **c. O(n^3)** **d. O(n+logn)**	**A**	1	5	**1,2, 5**	**3**	**3**
27	The quicksort algorithm, which has an average complexity of	**a. O(n^3)** **b. O(n+logn)** **c. theta(n^logn)** **d. theta(n^2)**	**C**	1	5	**1,2, 5**	**1**	**3**
28	Parallel code executes in many concurrent Device (GPU) threads across multiple parallel processing elements, called	**a. Synchronising multiprocessor** **b. Streaming multiprocessor** **c. Scalable multiprocessor** **d. Summative multiprocessor**	**B**	1	6	**1,2, 12**	**1**	**2**
29	____partitions the vertices among different processes and has each process compute the single-source shortest path for all vertices assigned to it	**a. Source parallel formulation** **b. Single partitioned formulation** **c. Source partitioned formulation** **d. Shortest path partitioned formulation**	**C**	1	5	**1,2, 12**	**3**	**2**
30	A processor, assigned with a thread block that executes	**a. Multithreaded DIMS**	**B**	1	2	**1**	**1**	**1**

	code, which we usually call a	**processor** **b. Multithreaded SIMD processor** **c. Multithreaded queue** **d. Multithreaded stack**						
31	Processor of system, which can read/write GPU memory, is known as	**a. Server** **b. Kernel** **c. Guest** **d. Host**	**D**	1	6	**1**	**1**	**1**
32	CUDA stands for	**a. Compute uniform device architecture** **b. Computing universal device architecture** **c. Computer unicode device architecture** **d. Compute unified device architecture**	**D**	1	6	**1,2, 5**	**2**	**1**
33	The device that are being used primarily for database, file server and mostly for web application are known as	**a. Servers** **b. Desktops** **c. Tablets** **d. Supercomputers**	**A**	1	1	**1**	**1**	**1**
34	GPU are designed for running a large number of complex tasks	**a. True** **b. False**	**B**	1	6	**1,2**	**1**	**1**
35	The parallel algorithm design contains a number of processes where one process may send the identical data to all other processes is called as	a. All to one broadcast b. All to all broadcast c. One to all broadcast **d.** None of these	**C**	1	3	**1**	**1**	**2**
36	The efficient utilization can be done by devising a	a. Recursive doubling b. Recursive		1	3	**1**	**1**	**1**

	broadcasting algorithm with the method known as	c. Scatter and Gather **d.** None of these	a					
37	The balanced tree is mapped neutrally from the hypercube algorithm for one-to-all broadcast where intermediate are the _____and each leaf nodes are the _____	a. switching nodes, processing nodes **b.** processing nodes, switching nodes	a	1	3	**1,12**	**1**	**2**
38	Finding prefix-sum operation is also called as scan operation	a. True **b.** False	a	1	3	**1,12**	**1**	**1**
39	All to all personalized communication is also called as	a. Scan operation b. Total exchange method c. None of these	B	1	3	**1,12**	**1**	**2**
40	On which network broadcast and reduction operations performed in two steps: 1. Operations along with row 2. Operations along with column	a. Ring b. Hypercube c. Linear array **d.** Mesh	d	1	3	**1,12**	**1**	**2**
41	Gather operation is also called as all to one reduction	a. True **b.** False	b	1	3	**1,8**	**1**	**1**
42	The method which is used in various parallel algorithm like Fourier transform, matrix transpose, some parallel database join operations is called as	a. All-to-all personalized communication b. All-to-all Broadcast c. Total exchange method d. Both a & c	d	1	3	**1,12**	**1**	**1**
43	Consider a sequence in which numbers are originally arranged<2,4,5,6,1>, then sequence of Prefix sum will be	a. <2,6,11,17,18 > b. <6,15,21,22 > c. None of these	a	1	3	**4**	**2**	**3**
44	Select the parameters on which the parallel runtime of a program depends.	A. nput size B. umber of processors C.	**D**	**1**	**4**	**1**	**3**	**4**

		ommunication parameters of the machine D. ll of the above						
45	The time that elapses from the moment the first processor starts to the moment the last processor finishes execution is called as _____.	A. Serial runtime B. Parallel runtime C. Overhead runtime D. Excess runtime	**B**	1	**4**	**4**	**3**	**4**
46	Select how the overhead function (T_o) is calculated.	A. $T_o = T_P - T_S$ B. $T_o = p*n\ T_P - T_S$ C. $T_o = p\ T_P - T_S$ D. $T_o = T_P - pT_S$	**C**	**1**	**4**	**1**	**3**	**1**
47	The parallel time for odd-even sort (efficient parallelization of bubble sort) is 50 seconds. The serial time for bubble sort is 175 seconds. Evaluate the speedup of bubble sort.	A. 3.75 B. 3.5 C. 0.33 D. 0.26	**B**	**1**	**4**	**1**	**3**	**1**
48	Consider the problem of adding n numbers by using n processing elements. The serial time taken is $\Theta(n)$ and parallel time is $\Theta(\log n)$. Evaluate the efficiency.	A. $E = \Theta(n / \log n)$ B. $E = \Theta(n \log n)$ C. $E = \Theta(\log n / n)$ **D.** $E = \Theta(1 / \log n)$	**D**	**1**	**4**	**1**	**3**	**1**
49	What will be the efficiency of cost optimal parallel systems?	A. $E = O(n)$. B. $E = O(1)$.	**B**	**1**	**4**	**1**	**3**	**3**

		C. ***E*** = *O*(p). **D.** ***E*** = *O*(n log n).						
50	Which law states that the maximum speedup of a parallel program is limited by the sequential fraction of the initial sequential program?	A. Amdahl's Law B. Flynn's Law C. Moore's Law **D.** Van Neumann's Law	**A**	**1**	**4**	**3**	**3**	**1**
51	Arrange the steps for the Matrix-Vector 2-D partitioning i) result vector is computed by performing an all-to-one reduction along the columns. ii)Alignment of the vector *x* along the principal diagonal of the matrix. iii)Copy the vector elements from each diagonal process to all the processes in the corresponding column using *n* simultaneous broadcasts among all processors in the column.	A. i, ii, iii B. ii, iii, i C. iii, i, ii D. ii, i, iii	**B**	**1**	**4**	**3**	**3**	**1**
52	Arrange the communication sequence in Matrix-Vector 2-D partitioning: i) all-to-one reduction in each row ii) one-to-all broadcast of each vector element among the *n* processes of each column iii) one-to-one	A. i, ii, iii B. ii, iii, i C. iii, ii, i D. ii, i, iii	**C**	**1**	**4**	**1**	**3**	**4**

	communication to align the vector along the main diagonal							
53	Parallel time in Rowwise 1-D Partitioning of Matrix-Vector Multiplication where p=n is ____.	A. *Θ(1)* B. *Θ(n log n)* C. *Θ(n^2)* D. *Θ(n)*	**D**	**1**	**4**	**4**	**3**	**4**
54	NVIDIA thought that 'unifying theme' of every forms of parallelism is the	**a. CDA thread** **b. PTA thread** **c. CUDA thread** **d. CUD thread**	**c**	1	6	1,2, 12	**1**	**2**
55	Thread being blocked altogether and being executed in sets of 32 threads, called a	**a. Thread block** **b. 32 thread** **c. 32 block** **d. Unit block**	**a**	1	6	**1,2, 12**	**1**	**2**
56	Length of a vector operation in a real program is often	**a. Known** **b. Unknown** **c. Visible** **d. Invisible**	**a**	1	6	**1,2, 12, 6**	**1**	**3**
57	A code, known as grid which runs on a GPU consisting of a set of	**a. 32 thread** **b. Unit block** **c. 32 block** **d. Thread block**	**d**	1	6	**1,1 2,5**	**1**	**1**
58	NVDIA unvield the industrys first directX 10 GPU is___	**a. GTX 1050**	**b**	1	6	**1,1 2,5**	**1**	**1**

		b. GeForce 8800 GTX **c. GeForce GTX 1080** **d. GTX 1060**				**1**		
59	The number of instructions being executed defines the	**a. Instruction count** **b. Hit time** **c. Clock rate** **d. All above**	**A**	1	2	**1**	**1**	**1**
60	In CUDA Programming kernel is launch using which pair of brackets?	**a. <<<>>>** **b. {{{}}}** **c. ((()))** **d. [[[]]]**	**d**	1	6	**1,2, 12, 5**	**3**	**2**
61	In CUDA programming the transfer of data between host and device special function used is ___	**a. Memcopy()** **b. Memorycpy()** **c. cudaMemcopy()** **d. cudaMemorycpy()**	**c**	1	6	**1,2, 12, 5**	**1**	**1**
62	Streaming multiprocessor in CUDA, divides the thread in a block is called as___	**a. WRAP** **b. Packet** **c. Grid** **d. Thread block**	**a**	1	6	**1,1 2,5**	**1**	**2**
63	Sources of overheads in parallel program are	**a. Idling** **b. Interprocess communication** **c. Excess computation** **d. All of the above**	**d**	1	3	**1,1 2,2**	**1**	**2**
64	What are the sources of overhead in parallel	A. Interprocess interaction	**D**	**1**	**4**	**4**	**3**	**4**

	programs?	B. Idling C. Excess computation D. All of the above						
65	What are the performance metrics of parallel systems?	A. Execution time B. Total parallel overhead C. Speedup D. Efficiency E. All of the above	**E**	1	**4**	**4**	**3**	**4**
66	The isoefficiency function determines the ease with which a parallel system can maintain a constant efficiency. True of false?	A. True B. False	**A**	**1**	**4**	**1**	**3**	**1**
67	Which matrix-matrix multiplication algorithm uses a 3-D partitioning?	A. Cannon's algorithm B. DNS algorithm C. Both of the above D. None of the above	**B**	**1**	**4**	**1**	**3**	**1**
68	A solution representing a parallelism in an algorithm is	**A. CDA** **B. PTA** **C. CUDA** **D. CUD**	**c**	1	6	**1**	**1**	**2**
69	Blocking optimization is used to improve temporal locality, for reduce	**A. Hit miss** **B. Misses**	**B**	1	5	**1**	**1**	**2**

		C. Hit rate **D. Cache misses**						
70	Data are allocated to disks in the RAID at the	**A. Block level** **B. Cache level** **C. Low level** **D. High level**	**A**	1	6	**1**	**1**	**1**
71	In CUDA C programming serial code is executed by__and parallel code is executed by__	**a. CPU, CPU** **b. GPU,CPU** **c. GPU,GPU** **d. CPU,GPU**	**d**	1	6	**1,2, 12, 5**	**2**	**2**
72	Kernel function is qualified by the qualifier	**a. __local__** **b. __universal__** **c. __global__** **d. A or C**	**C**	1	6	**1,3**	**1**	**1**

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Unit I

1. Conventional architectures coarsely comprise of a_

   A. A processor
   B. Memory system
   C Data path.
   D All of Above

2. Data intensive applications utilize_

   A **High aggregate throughput**
   B High aggregate network bandwidth
   C High processing and memory system performance.
   D None of above

3. A pipeline is like_

   A Overlaps various stages of instruction execution to achieve performance.
   B House pipeline
   C Both a and b
   D A gas line

4. Scheduling of instructions is determined_

   A True Data Dependency
   B Resource Dependency
   C Branch Dependency
   D All of above

5. VLIW processors rely on_

   A **Compile time analysis**
   B Initial time analysis
   C Final time analysis
   D Mid time analysis

6. Memory system performance is largely captured by_

   A Latency
   B Bandwidth
   C Both a and b
   D none of above

7. The fraction of data references satisfied by the cache is called_

A Cache *hit ratio*
B Cache *fit ratio*
B Cache *best ratio*
C none of above

8. A single control unit that dispatches the same Instruction to various processors is__

A SIMD
B SPMD
C MIMD
D None of above

9. The primary forms of data exchange between parallel tasks are_

A Accessing a shared data space
B Exchanging messages.
C Both A and B
D None of Above

10. Switches map a fixed number of inputs to outputs.
A True
B False

Unit 2

1. The First step in developing a parallel algorithm is_

A. To Decompose the problem into tasks that can be executed concurrently
B. Execute directly
C. Execute indirectly
D. None of Above

2. The number of tasks into which a problem is decomposed determines its_

A. Granularity
B. Priority
C. Modernity
D. None of above

3. The length of the longest path in a task dependency graph is called_
A. the critical path length
B. the critical data length
C. the critical bit length
D. None of above

4. The graph of tasks (nodes) and their interactions/data exchange (edges)_

A. Is referred to as a *task interaction graph*
B. Is referred to as a *task Communication graph*
C. Is referred to as a *task interface graph*
D. None of Above

5. Mappings are determined by_

A. task dependency
B. task interaction graphs
C. Both A and B
D. None of Above

6. Decomposition Techniques are_
A. recursive decomposition
B. data decomposition
C. exploratory decomposition
D. speculative decomposition
E. All of Above

7. The *Owner Computes Rule* generally states that the process assigned a particular data item is responsible for_

A. All computation associated with it
B. Only one computation
C. Only two computation
D. Only occasionally computation

8. A simple application of exploratory decomposition is_

A. The solution to a 15 puzzle
B. The solution to 20 puzzle
C. The solution to any puzzle
D. None of Above

9. Speculative Decomposition consist of _

A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B

10. task characteristics include:
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.
D. All of Above

Unit 3

1. Group communication operations are built using point-to-point messaging primitives
   A. True
   B. False

2. Communicating a message of size m over an uncongested network takes time ts + tmw

   A. True
   B. False

3. The dual of one-to-all broadcast is_

   A. *All-to-one reduction*
   B. *All-to-one receiver*
   C. *All-to-one Sum*
   D. *None of Above*

4. A hypercube has_

   A. 2^d nodes
   B. 2d nodes
   C. 2n Nodes
   D. N Nodes

5. A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes.

   A. True
   B. False

6. In All-to-All Broadcast each processor is the source as well as destination.

   A. True
   B. False

7. The Prefix Sum Operation can be implemented using the_

   A. All-to-all broadcast kernel.
   B. All-to-one broadcast kernel.
   C. One-to-all broadcast Kernel
   D. Scatter Kernel

8. In the *scatter* operation_

A. **Single node send a unique message of size m to every other node**
B. Single node send a same message of size m to every other node
C. Single node send a unique message of size m to next node
D. None of Above

9. The gather operation is exactly the inverse of the_

A. **Scatter operation**
B. Broadcast operation
C. Prefix Sum
D. Reduction operation

10. In All-to-All Personalized Communication Each node has a distinct message of size m for every other node

A. **True**
B. False

1. It is _____ strength and _____ permeability.
a) High, high
b) Low, low
c) High, low
d) Low, high
View Answer
Answer: c
Explanation: It is specifically chosen so as to have particularly appropriate properties for the expected use of the structure such as high strength and low permeability.

2. High Performance concrete works out to be economical.
a) True
b) False
View Answer
Answer: a
Explanation: High Performance concrete works out to be economical, even though its initial cost is high.

3. HPC is not used in high span bridges.
a) True
b) False
View Answer
Answer: b
Explanation: Major applications of high-performance concrete in the field of Civil Engineering constructions have been in the areas of long-span bridges, high-rise buildings or structures, highway pavements, etc.

4. Concrete having 28- days' compressive strength in the range of 60 to 100 MPa.
a) HPC

b) VHPC
c) OPC
d) HSC
View Answer
Answer: a
Explanation: High Performance Concrete having 28- days' compressive strength in the range of 60 to 100 MPa.

5. Concrete having 28-days compressive strength in the range of 100 to 150 MPa.
a) HPC
b) VHPC
c) OPC
d) HSC
View Answer
Answer: b
Explanation: Very high performing Concrete having 28-days compressive strength in the range of 100 to 150 MPa.

6. High-Performance Concrete is _____ as compared to Normal Strength Concrete.
a) Less brittle
b) Brittle
c) More brittle
d) Highly ductile
View Answer
Answer: c
Explanation: High-Performance Concrete is more brittle as compared to Normal Strength Concrete (NSC), especially when high strength is the main criteria.

7. The choice of cement for high-strength concrete should not be based only on mortar-cube tests but it should also include tests of compressive strengths of concrete at _____ days.
a) 28, 56, 91
b) 28, 60, 90
c) 30, 60, 90
d) 30, 45, 60
View Answer
Answer: a
Explanation: The choice of cement for high-strength concrete should not be based only on mortar-cube tests but it should also include tests of compressive strengths of concrete at 28, 56, and 91 days.

8. For high-strength concrete, a cement should produce a minimum 7-days mortar-cube strength of approximately ___ MPa.
a) 10
b) 20

c) 30
d) 40
View Answer
Answer: c
Explanation: For high-strength concrete, a cement should produce a minimum 7-days mortar-cube strength of approximately 30 MPa.

9. _____ mm nominal maximum size aggregates gives optimum strength.
a) 9.5 and 10.5
b) 10.5 and 12.5
c) 9.5 and 12.5
d) 11.5 and 12.5
View Answer
Answer: c
Explanation: Many studies have found that 9.5 mm to 12.5 mm nominal maximum size aggregates gives optimum strength.

10. Due to low w/c ratio _____
a) It doesn't cause any problems
b) It causes problems
c) Workability is easy
d) Strength is more
View Answer
Answer: b
Explanation: Due to the low w/c ratio, it causes problems so superplasticizers are used.

	marks	question	A	B	C	D	ans
0	1	Interconnection Networks can be classified as?	Both	Dynamic	Static	Direct Network	Both Static and Dynamic.
1	1	Parallel Computers are used to solve which types of problems.	Both	Algorithmic Problems	Optimization Problems	None	This is an explaination.
2	1	How many clocks control all the stages in a pipeline?	One	Three	Four	Five	One clock Is used to control all the stages.
3	1	Main memory in parallel computing is____?	Shared	Parallel	Fixed	None	Main memory is shared in parallel computing.
4	1	Which of these is not a class of parallel computing architetcture?	Application Checkpointing	Distributed Computing	Symmetric Multiprocessing	Multicore Computing	Ans- (d)- Application checkpoiting. is not a class of parallel computer architecture.
5	1	Parallel Computing software solutions and Techniques includes:	All	Automatic Parallelization	Parallel Programming languages.	Application Checkpointing	Parallel computing software solutionincludes all of the following.. This is an explanation
6	2	The Processors are connected to the memory through a set of?	Switches	Cables	Buses	Registers	The Processors are connected thru. the switches.
7	2	Superscalar Architetcure has how many execution units?	Two	One	Three	Four	This is an explaination.
8	2	What is used to hold the intermediate output in a pipeline	Intermediate Register	Cache	RAM	ROM	The Intermediate Registers are used to hold the output.
9	2	Which oranization performs sequencing of Human Genome?	International Human Genome Sequencing and Consortium	International Sequencing and Consortium for Human Genome	Human Genome Sequencing and Constrium, Org.	Genome Sequencing for Humans and Consortium, Org.	This is an explaination.
10	2	There are how many stages in RISC Processor?	Five	Three	Two	Six	Ans(c)- Five stages are there in a RISC processor.
11	2	Over the last decade, The DRAM access time has improved at what rate per year?	0.1	0.2	0.15	None of the above	The DRAM acess time rate has improved at a rate of 10% over the last decade.

	marks	question	A	B	C	D	ans
12	2	Which memory acts as low-latency high bandwidth storage?	Cache	Register	DRAM	EPROM	Cache acts as low latency high bandwidth storage .This is an explanation.
13	2	Which processor architecture is this?	SIMD	MIMD	MISD	MIMD	This is an explaination.
14	2	Which core processor is this?	Quad-Core	Dual-Core	Octa-Core	Single-Core	This diagram shows Quad-Core.
15	2	Which of these is not a scalable design principle?	Data Caching	Decomposition	Simplification	Parsimony	Data Caching is not a prinicple of scable design.
16	2	The distance between any two nodes in Bus Based network is?	O(1)	O(n Logn)	O(N)	O(n^2)	O(1) is the ditance between any two nodes.
17	2	Early SIMD computers include:	All	MPP	CM-2	Illiac IV	All of these are early staged SIMD parallel computers.
18	2	This is which configuration in Omega networks.	Pass-through	Cross-Over	Shuffle	None	This is called Pass-through configuration.
19	2	Automatic Parallelization technique doesnâ€™t ncludes:	Share Memory	Analyse	Schedule	Parse	Parallelization includes parse, analyse schedule and code generation.
20	2	The Pentuim 4 or P4 processor has how many stage pipeline?	20	15	18	10	The P4 processor has 20 staged pipeline. This is an explanation.
21	3	Which protocol is not used to remove concurrent writes?	Identify	Priority	Common	Sum	Sum, Prioirity and common are used to remove concurrent writes.
22	3	EREW PRAM stands for?	Exclusive Read and Exclusive Write	Erasable Read and Erasable Write PRAM	Easily Read and Easily Write	None	EREW stands for Exclusive Read and Exclsuive Write PRAM.
23	3	During each clock cycle, multiple instructions are piped into the processor in_____?	Parallel	Series	Both a and b	None	Multiple Instuctiion are piped in parallel. This is an explanation.
24	3	Which Interconnection Network uses this equation.	Multistage Networks	Cross-Bar	Dynamic Networks	Bus-Staged	Multistaged Network uses this eqn.

	marks	question	A	B	C	D	ans
25	3	How many types of parallel computing are available from both proprietary and open source parallel computing vendors?	4	2	3	6	There are generally four types of parallel computing, available from both proprietary and open source parallel computing vendors.
26	3	If a piece of data is repeatedly used, the effective latency of this memory system can be reduced by the cache. The fraction of data references satisfied by the cache is called?	Hit Ratio	Memory ratio	Hit Fraction	Memory Fraction.	If a piece of data is repeatedly used, the effective latency of this memory system can be reduced by the cache. The fraction of data references satisfied by the cache is called the cache hit ratio.
27	3	Superscalar Architetcure can create problem in?	Scheduling	Phasing	Data Extraction	Data-Compiling	SuperScalar Architecture can cause problems in CPU scheduling.
28	3	In cut-through routing, a message is broken into fixed size units called?	Flits	Flow Digits	Control Digits	All	In cut-through routing, a message is broken into fixed size units called flits.
29	3	The total communication time for cut-through routing is?	A	B	C	D	This is an explaination.
30	1	The Disadvantage of GPU Pipeline is?	Load-balancing	Data balancing	Process balancing	All of the above	This is an explaination.
31	1	Examples of GPU Processors are:	Both	AMD Processors	NVIDIA	None	Both AMD and NVIDIA.
32	1	Simultaneous execution of different programs on a data stream is called?	Stream Parallelism	Data Execution	Data-paralleism	None	Simultaneous execution of different programs on a data stream is called Stream Parallelism.
33	1	Early GPU controllers were known as?	Video Shifters	GPU Shifters	GPU Controllers	Video-Movers	This is an Explaination.
34	1	_____development is a critical component of problem solving using computers?	Algorithm	Code	Pseudocode	Problem	Algorithm development is a critical component of problem solving using computers

	marks	question	A	B	C	D	ans
35	1	GPU stands for?	Graphics Processsing Unit	Graphical Processing Unit	Gaming Processing Unit	Graph Processing Unit	This is an Explaination.
36	1	What leads to concurrency?	Parallelism	Serial Processing	Decomposition	All	Parallelism leads naturally to Concurrency. For example, Several processes trying to print a file on a single printer.
37	2	The process of determining which screen-space pixel locations are covered by each\ntriangle is known as?	Rasterization	Pixelisation	Fragmentation	Space-Determining Process	Rasterization is the process of determining which screen-space pixel locations are covered by each\ntriangle.
38	2	The programmable units of the GPU follow which programming model?	SPMD	MISD	MIMD	SIMD	The programmable units of the GPU follow a single program multiple-data (SPMD) programming model.
39	2	Which space can ease the programming effort, especially if the distribution of data is different in different phases of the algorithm?	Shared Address	Parallel Address	Data- Address	Series-Address	Shared Address space can ease the programming effort, especially if the distribution of data is different in different phases of the algorithm.
40	2	Which are the hardware units that physically perform computations?	Processsor	ALU	CPU	CU	Processors are the hardware units that physically perform computations
41	2	Examples of Graphics API are?	All	DirectX	CUDA	Open-CL	All of the these are examples of Graphics API
42	2	The mechanism by which tasks are assigned to processes for execution is called___?	Mapping	Computation	Process	None	The mechanism by which tasks are assigned to processes for execution is called mapping.

	marks	question	A	B	C	D	ans
43	2	A decomposition into a large number of small tasks is called_____ granularity.	Fine- grained	Coarse-grained	Vector-granied	All	A decomposition into a large number of small tasks is called fine-grained granularity.
44	2	Identical operations being applied concurrently on different data items is called?	Data-Parallelism	Parallelism	Data Serialsm	Concurrency	Identical operations being applied concurrently on different data items is called Data Parallelism.
45	2	System which do not have parallel processsing capabiities?	SISD	SIMD	MISD	MIMD	This is the explainantion.
46	2	The time and the location in the program of a static one-way interaction is known as ?	Priori	Polling	Decomposition	Execution	The time and the location in the program of a static one-way interaction is known a priori.
47	2	Memory access in RISC architecture is limited to which instructions?	STA and LDA	CALL and RET	Push and POP	MOV and JMP	This is the explaination.
48	2	Which Algorithms can be implemented in both shared-address-space and message-passing paradigms?	Data-Parallel Algo.	Quick-Sort Algo.	Data Algorithm	Bubble Sort Algo.	Data Parallel algorithms can be implemented in both shared-address-space and message-passing paradigms
49	2	Which type of Distribution is this?	Randomized Block Distribution	Block-Cyclic Distribution	Cyclic Distribution	None	This figure shows Randomized Block Distribution.
50	2	An abstraction used to express such dependencies among tasks and their relative order of execution is known as_____?	Task-Dependency Graph.	Dependency Graph.	Time-Dependency Graph	None	An abstraction used to express such dependencies among tasks and their relative order of execution is known as a task-dependency graph.

	marks	question	A	B	C	D	ans
51	3	Which is the simplest way to distribute an array and assign uniform contiguous portions of the array to different processes?	Block Distrbution	Array Distrbution	Process Distribution	All	Block distributions are some of the simplest ways to distribute an array and assign uniform contiguous portions of the array to different processes
52	3	An example of a decomposition with a regular interaction pattern is?	Image-dethering problem.	Travelling Salesman Problem	Time-complexity Problens	8 Queen problem.	An example of a decomposition with a regular interaction pattern is the problem of image dithering.
53	3	A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is	Critical-path	Process-path	Granularity.	Concurrency	A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is critical path.
54	3	The shared-address-space programming paradigms can handle which interactions?	Both	Two way	One way	None	The shared-address-space programming paradigms can handle both one-way and two-way interactions.
55	3	Which distribution can result in an almost perfect load balance due to the extreme fine-grained underlying decomposition.	Cyclic Distribution.	Array Distribution	Block-Cyclic Distribution	Block Distribution.	Cyclic Distribution can result in an almost perfect load balance due to the extreme fine-grained underlying decomposition.
56	3	Data sharing interactions can be categorized as_____interactions?	Both	Read-Write	Read only	None	Data sharing interactions can be categorized as either read-only or read-write interactions

	marks	question	A	B	C	D	ans
57	3	What is the way of structuring a parallel algorithm by selecting a decomposition and mapping technique and applying the appropriate strategy to minimize interactions called?	Algorithm Model	Parallel Model	Data Model	Mapping Model	Algo. Model is a way of structuring a parallel algorithm by selecting a decomposition and mapping technique and applying the appropriate strategy to minimize interactions.
58	3	Which Algorithm is this?	Serial column based Algo.	Column-Algorithm	Bubble Sort Algo.	None.	This is Serial Column based algorithm.
59	3	Algorithms based on the task graph model include:	All	Matrix-Factorization	Parallel QuickSort	Quicksort	This is an Explaination.
60	1	Which model permits simultaneous communication on all the channels connected to a node?	All-port communication	One-port communication	Dual-port communication	Quad-port communication	All-port communication model permits simultaneous communication on all the channels connected to a node.
61	1	A process sends the same m-word message to every other process, but different processes may broadcast different messages. It is called?	All to All Broadcast	One to All Broadcast	All to All Reduction	None	This is an Explaination.
62	1	The Matrix is transposed using which operation?	All to All personalized communication	One-to-all personalized communication	All-to-one personalized communication	One to one personalized communication.	This is an Explaination.
63	1	Each node in a two-dimensional wraparound mesh has how many ports?	Four	Two	Three	One	Each node in a two-dimensional wraparound mesh has four ports
64	1	Circular shift is a member of a broader class of global communication operations known as?	Permutation	Combination.	Both a and b	None	This is ann explaination.
65	1	We define_____ as the operation in which node i sends a data packet to node (i + q) mod p in a p-node ensemble (0 < q < p).	Circular q-shift	Linear shift	Circular shift	Linear q-shift.	We define a circular q-shift as the operation in which node i sends a data packet to node (i + q) mod p in a p-node ensemble (0 < q < p).

	marks	question	A	B	C	D	ans
66	1	Parallel algorithms often require a single process to send identical data to all other processes or to a subset of them. This operation is known as?	One to All Broadcast	One to One Broadcast	All to One Broadcast	None	Parallel algorithms often require a single process to send identical data to all other processes or to a subset of them. This operation is known as One to All Broadcast.
67	1	In which Communication each node sends a distinct message of size m to every other node?	All to All personalized communication	One to One personalized communication	All-to-one personalized communication	One-to-all personalized communication.	This is an Explaination.
68	1	All to All personalized communication operation is not used in a which of these parallel algorithms?	Quick Sort	Matrix-Transpose	Fourier Transformation	Database Join operation	This is an Explaination.
69	1	The Dual of one-to-all broadcast is?	All to one Reduction	All to one Broadcast	One to Many Reduction	All to All Broadcast	The dual of one to all Broadcast is called all to one reduction.
70	1	Reduction on a linear array can be performed by_____ the direction and the sequence of communication?	Reversing	Forwarding	Escaping	Widening	Reduction on a linear array can be performed by simply reversing the direction and the sequence of communication
71	2	This equation is used to solve which topology operations in all to all communications?	Hypercube	Mesh	Ring	Linear-Array	This is an Explaination.
72	2	\nThe communication pattern of all-to-all broadcast can be used to perform_____?	Third Variation of Reduction	Second Variation of Reduction	First Variation of Reduction	Fifth Variation of Reduction	This is an Explaination.
73	2	A single node sends a unique message of size m to every other node. This operation is known as_____?	Scatter	Reduction	Gather	Concatenate	In the scatter operation, a single node sends a unique message of size m to every other node.
74	2	The Algorithm represents which broadcast?	All to All Broadcast	All to All Broadcast	All to All Reduction	One to One Reduction	This is an explaination.
75	2	The message can be broadcast in how many steps?	Log(p)	Log(p^2)	One	Sin(p)	The message can be broadcast in log p steps.
76	2	This equation is used to solve which operations?	All to All personalized communication	One-to-all personalized communication	One to one personalized communication	All-to-one personalized communication.	This is an Explaination.

	marks	question	A	B	C	D	ans
77	2	There are how many computations for n^2 words of data transferred among the nodes?	N^3	Tan n	E^n	Log n	There are n^3 computations for n^2 words of data transferred among the nodes.
78	2	Scatter Operation is also known as?	One-to-all personalized communication	One-to-one personalized communication	All-to-one personalized communication	All-to-all personalized communication.	Scatter opeartion is also known as One-to-all personalized communication.
79	2	A Hypercube with 2d nodes can be regarded as a d-dimensional mesh with____ nodes in each dimension.	Two	One	Three	Four	A hypercube with 2d nodes can be regarded as a d-dimensional mesh with two nodes in each dimension
80	2	One-to-all broadcast and all-to-one reduction are used in several important parallel algorithms including?	All	Gausiian Elimination	Shortest path Algo.	Matrix- Vector multiplication	This is an Explaination.
81	2	Each node of the distributed-memory parallel computer is a_____ shared-memory multiprocessor.	NUMA	UMA	CCMA	None	Each node of the distributed-memory parallel computer is a NUMA shared-memory multiprocessor.
82	2	To perform a q-shift, we expand q as a sum of distinct powers of_____?	2	3	e	Log p	To perform a q-shift, we expand q as a sum of distinct powers of 2 .
83	3	In which implementation of circular shift, the entire row to data set is shifted by	Mesh	Hypercube	Ring	Linear	This is an Explaination
84	3	On a p-node hypercube with all-port communication, the coefficients of tw in the expressions for the communication times of one-to-all and all-to-all broadcast and personalized communication are all smaller than their single-port counterparts by a factor of?	Log(p)	Cos(p)	Sin(p)	E^p	On a p-node hypercube with all-port communication, the coefficients of tw in the expressions for the communication times of one-to-all and all-to-all broadcast and personalized communication are all smaller than their single-port counterparts by a factor of log p.

	marks	question	A	B	C	D	ans
85	3	The Equation represents which analysis in All to All Broadcasts?	Cost Analysis	Time Analysis	Data Model Analysis	Space-Time Analysis	Ans-(c) Cost Analysis.
86	3	On a p-node hypercube, the size of each message exchanged in the i th of the log p steps is?	A	B	C	D	A
87	3	Which broadcast is applied on this 3D hypercube?	One to All Broadcast	One to One Broadcast	All to One Broadcast	All to one Reduction	This figure shows One to All Broadcast being applied on 3D hypercube.
88	3	The Equation represents which analysis in One to All Broadcasts?	Cost Analysis	Time Analysis	Data Analysis	Space Analysis	This is an explaination.
89	3	The time for circular shift on a hypercube can be improved by almost a factor of _____ for large messages.	Log p	Cos(p)	e^p	Sin p	The time for circular shift on a hypercube can be improved by almost a factor of log p for large messages.
90	1	The execution time of parallel algorithm doesnâ€™t depends upon?	Processor	Input Size	Relative computation	Communication speed	The execution time of a parallel algorithm depends not only on input size but also on the number of processing elements used, and their relative computation and interprocess communication speeds.
91	1	Processing elements in a parallel system may become idle due to many reasons such as:	Both	Synchronization	Load Imbalance	The processing element doesnâ€™t become idle.	Both synchronization and load imbalance
92	1	If the scaled-speedup curve is close to linear with respect to the number of processing elements, then the parallel system is considered as?	Scalable	Iso-scalable	Non-Scalable	Scale-Efficient	If the scaled-speedup curve is close to linear with respect to the number of processing elements, then the parallel system is considered scalable

	marks	question	A	B	C	D	ans
93	1	Which system is the combination of an algorithm and the parallel architecture on which it is implemented?	Parallel System	Data- Parallel System	Architecture System	Series System	A parallel system is the combination of an algorithm and the parallel architecture on which it is implemented
94	1	What is defined as the speedup obtained when the problem size is increased linearly with the number of processing elements?	Scalable Speedup	Unscalable Speedup	Superlinearity Speedup	Isoefficiency Speedup	Scalable Speedup defined as the speedup obtained when the problem size is increased linearly with the number of processing elements
95	1	The maximum number of tasks that can be executed simultaneously at any time in a parallel algorithm is called its degree of_____.	Concurrency	Parallelism	Linearity	Execution	The maximum number of tasks that can be executed simultaneously at any time in a parallel algorithm is called its degree of concurrency.
96	1	The isoefficiency due to concurrency in 2-D partitioning is:	O(p)	O(n Logp)	O(1)	O(n^2)	This is an explaination.
97	2	The total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element is known as?	Total Overhead	Overhead	Serial Runtime	Parallel Runtime	We define total overhead of a parallel system as the total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element.
98	2	Parallel computations involving matrices and vectors readily lend themselves to data _____.	Decomposition	Composition	Linearity	Parallelsim	Parallel computations involving\nmatrices and vectors readily lend themselves to data decomposition.

	marks	question	A	B	C	D	ans
99	2	Parallel 1-D with Pipelining is a_____ algorithm?	Synchronous	Asynchronous	Optimal	Cost-optimal	This is an explaination.
100	2	The serial complexity of Matrix-Matrix Multiplication is:	Õ•(n^3)	O(n^2)	O(n)	O(nlogn)	This is an explaination
101	2	What is the problem size for n x n matrix multiplication?	Ï´(n^3)	Ï´(nlogn)	Ï´(n^2)	Ï´(1)	Ï´(n^3) is the problem size.
102	2	The given equation represents which function?	Overhead Function	Parallel Model	Series Overtime	Parallel Overtime	This is an explaination.
103	2	The efficiency of a parallel program can be written as:	A	B	C	D	A
104	2	The total number of steps in the entire pipelined procedure is_____?	Î˜(n)	Î˜(n^2)	Î˜(n^3)	Î˜(1)	The total number of steps in the entire pipelined procedure is Î˜(n)
105	2	In Canon's Algorithm, the memory used is?	Î¸(n^2)	Î¸(n)	Î¸(n^3)	Î¸(nlogn)	This is an explaination.
106	2	Consider the problem of multiplying two n Ã— n dense, square\nmatrices A and B to yield the product matrix C =:	AÃ—B	A/B	A+B	A-B	Consider the problem of multiplying two n Ã— n dense, square\nmatrices A and B to yield the product matrix C = A Ã— B.
107	2	The serial runtime of multiplying a matrix of dimension n x n with a vector is?	A	B	C	D	A
108	2	_____is a measure of the fraction of time for which a processing element is usefully employed.	Efficiency	Linearity	Overtime Function	Superlinearity	Efficiency is a measure of the fraction of time for which a processing element is usefully employed.
109	2	When the work performed by a serial algorithm is greater than its parallel formulation or due to hardware features that put the serial implementation at a disadvantage.This phenomena is known as?	Superlinear Speedup	Linear Speedups	Super Linearity	Performance Metrics	This is an explaintion
110	3	The all-to-all broadcast and the computation of y[i] both take time?	Î˜(n)	Î˜(nlogn)	Î˜(n^2)	Î˜(n^3)	This is an explaination.

	marks	question	A	B	C	D	ans
111	3	If virtual processing elements are mapped appropriately onto physical processing elements, the overall communication time does not grow by more than a factor of	N/p	P/n	N+p	N*p	If virtual processing elements are mapped appropriately onto physical processing elements, the overall communication time does not grow by more than a factor of n/p
112	3	Parallel execution time can be expressed as a function of problem size, overhead function, and the number of processing elements.The Formed eqn is:	A	B	C	D	A
113	3	In 2-D partioning, the first alignment takes time=?	Ts + twn/âˆšp.\n	Ts - twn/âˆšp.\n	Ts*twn/âˆšp.\n	Ts/ twn*âˆšp.\n	Ts + twn/âˆšp.\n
114	3	Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called_____?	Scaling Down	Scaling up	Scaling	Stimulation	Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called scaling down.
115	3	Which of the following is a drawback of matrix matrix multiplication?	Memory Optimal	Efficient	Time-bound	Complex	This is an explaination
116	3	Consider the problem of sorting 1024 numbers (n = 1024, log n = 10) on 32 processing elements. The speedup expected is	P/log n	P*log n	P+logn	N*log p	Consider the problem of sorting 1024 numbers (n = 1024, log n = 10) on 32 processing elements. The speedup expected is p/logn
117	3	Consider the problem of adding n numbers on p processing elements such that p < n and both n and p are powers of 2. The overall parallel execution time of the problem is:	ê™¨((n/p) log p).	ê™¨((n*p) log p).	ê™¨((p/n) log p).	ê™¨((n) log p).	Ans-(a)-ê™¨((n/p) log p).
118	3	DNS algorithm has____ runtime?	â„¦(n)	â„¦(n^2)	â„¦(n^3)	â„¦(logn)	DNS has â„¦(n) runtime

	marks	question	A	B	C	D	ans
119	3	The serial algorithm requires_____ multiplications and additions in matrix-vector multiplication.\n	N^2	N^3	Log n	Nlog(n)	Ans-(b)-n^2. The serial algorithm requires n^2 multiplications and additions.\n\n
120	1	The time required to merge two sorted blocks of n/p elements is_____?\n\n	Î,(n/p)	Î,(n)	Î,(p/n)	Î,(nlogp)	The time required to merge two sorted blocks of n/p elements is Î,(n/p).\n\n
121	1	In Parallel DFS,the stack is split into two equal pieces such that the size of the search space represented by each stack is the same. Such a split is called?.	Half-Split	Half-Split	Parallel-Split	None	The stack is split into two equal pieces such that the size of the search space represented by each stack is the same. Such a split is called a half-split.
122	1	To avoid sending very small amounts of work, nodes beyond a specified stack depth are not given away. This depth is called the_____depth.	Cut-Off	Breakdown	Full	Series	To avoid sending very small amounts of work, nodes beyond a specified stack depth are not given away. This depth is called the cutoff depth.
123	1	In sequential sorting algorithms, the input and the sorted sequences are stored in which memory?	Process Memory	Secondary Memory	Main Memory	External Memory	In sequential sorting algorithms, the input and the sorted sequences are stored in the process's memory
124	1	Each process sends its block to the other process. Now, each process merges the two sorted blocks and retains only the appropriate half of the merged block. We refer to this operation as?	Compare-Split	Split	Compare	Exchange.	Each process sends its block to the other process. Now, each process merges the two sorted blocks and retains only the appropriate half of the merged block. We refer to this operation as compare-split.

	marks	question	A	B	C	D	ans
125	1	Each process compares the received element with its own and retains the appropriate element.We refer this operation as_____?	Compare Exchange	Exchange	Process-Exchange	All	Each process compares the received element with its own and retains the appropriate element. We refer this as compare exchange.
126	1	Which algorithm maintains the unexpanded nodes in the search graph, ordered according to their l-value?	Parallel BFS	Parallel DFS	Both a and b	None	Parallel BFS maintains the unexpanded nodes in the search graph, ordered according to their l-value.
127	1	The critical issue in parallel depth-first search algorithms is the distribution of the search space among the_____?	Processor	Space	Memory	Blocks	The critical issue in parallel depth-first search algorithms is the distribution of the search space among the processors
128	2	Enumeration Sort uses how many processes to sort n elements?	N^2	Logn	N^3	N	This is an explaination.
129	2	Which sequence is a sequence of elements <a0, a1, ..., an-1> with the property that either (1) there exists an index i, 0 â‰¤ i â‰¤n - 1, such that <a0, ..., ai > is monotonically increasing and <ai +1, ..., an-1> is monotonically decreasing, or (2) there exists a cyclic shift of indices so that (1) is satisfied.	Bitonic Sequence	Acyclic Sequence	Asymptotic Sequence	Cyclic Sequence.	A bitonic sequence is a sequence of elements <a0, a1, ..., an-1> with the property that either (1) there exists an index i, 0 i n - 1, such that <a0, ..., ai > is monotonically increasing and <ai +1, ..., an-1> is monotonically decreasing, or (2) there exists a cyclic shift of indices so that (1) is satisfied

	marks	question	A	B	C	D	ans
130	2	To make a substantial improvement over odd-even transposition sort, we need an algorithm that moves elements long distances. Which one of these is such serial sorting algorithm?	Shell Sort	Linear Sort	Quick-Sort	Bubble Sort	To make a substantial improvement over odd-even transposition sort, we need an algorithm that moves elements long distances. Shellsort is one such serial sorting algorithm.
131	2	Quick-Sort is a_____ algorithm?	Divide and Conquer	Greedy Approach	Both a and b	None	Quicksort is a Divide and Conquer algorithm.
132	2	The_____ transposition algorithm sorts n elements in n phases (n is even), each of which requires n/2 compare-exchange operations.	Odd-Even	Odd	Even	None	This is an explaination.
133	2	The average time complexity for Bucket Sort is?	O(n+k)	O(nlog(n+k))	O(n^3)	Î,(n^2)	The average time complexity for Bucket Sort is O(n + k).
134	2	A popular serial algorithm for sorting an array of n elements whose values are uniformly distributed over an interval [a, b] is which algorithm?	Bucket Sort	Quick-Sort Algo.	Linear Sort	Bubble-Sort	A popular serial algorithm for sorting an array of n elements whose values are uniformly distributed over an interval [a, b] is the bucket sort algorithm
135	2	Best Case time complexity of Bubble Sort is:	O(n)	O(n^3)	O(nlogn)	O(n^2)	Best case complexity of bubblesort is O(n).

	marks	question	A	B	C	D	ans
136	2	When more than one process tries to write to the same memory location, only one arbitrarily chosen process is allowed to write, and the remaining writes are ignored. This process is called_____ in quick sort.	CRCW-PRAM	PRAM	Partitioning	CRCW	When more than one process tries to write to the same memory location, only one arbitrarily chosen process is allowed to write, and the remaining writes are ignored.It is called CRCW PRAM quick sort algo.
137	2	Average Time Complexity in a quicksort algorithm is:	O(nlogn)	O(n)	O(n^3)	Î¸(n^2)	This is an explainatoin.
138	2	The isoefficiency function of Global Round Robin (GRR) is:	O (p^2 log p)	O (p log p)	O (log p)	O (p^2)	The isoefficiency function of GRR is O (p^2 log p)
139	2	A_____ is a device with two inputs x and y and two outputs x' and y' in a Sorting Network.	Comparator	Router	Separator	Switch.	A comparator is a device with two inputs x and y and two outputs x' and y'
140	2	If T is a DFS tree in G then the parallel implementation of the algorithm runs in _____time complexity.	O(t)	O(tlogn)	O(logt)	O(1)	If T is a DFS tree in G then the parallel implementation of the algorithm outputs a proof that can be verified in O(t) time complexity.
141	2	In the quest for fast sorting methods, a number of networks have been designed that sort n elements in time significantly smaller than___?	Î¸(nlogn)	Î¸(n)	Î¸(1)	Î¸(n^2)	In the quest for fast sorting methods, a number of networks have been designed that sort n elements in time significantly smaller than Î¸(nlogn).
142	2	The average value of the search overhead factor in parallel DFS is less than_____?	One	Two	Three	Four	The average value of the search overhead factor in parallel DFS is less than one
143	3	Parallel runtime for Ring architecture in a bitonic sort is:	Î¸(n)	Î¸(nlogn)	Î¸(n^2)	Î¸(n^3)	Parallel runtime for Ring architecture in a bitonic sort is Î¸(n)

	marks	question	A	B	C	D	ans
144	3	The Sequential Complexity of Odd-Even Transposition Algorithm is:	Î¸(n^2)	Î¸(nlogn)	Î¸(n^3)	Î¸(n)	This is an explaination.
145	3	The Algorithm represents which bubble sort:	Sequential Bubble Sort	Circular Bubble Sort	Simple Bubble Sort	Linear Bubble Sort	This is an explaination.
146	3	Enumeration Sort uses how much time to sort n elements?	Î¸(1)	Î¸(nlogn)	Î¸(n^2)	Î¸(n)	This is an explaination.
147	3	The_____algorithm relies on the binary representation of the elements to be sorted.	Radix-sort	Bubble Sort	Quick-Sort	Bucket-Sort	The radix sort algorithm relies on the binary representation of the elements to be sorted.
148	3	Parallel runtime for Mesh architecture in a bitonic sort is:	Î¸(n/logn)	Î¸(n)	Î¸(n^2)	Î¸(n^3)	This is an explaination.
149	1	The number of threads in a thread block is limited by the architecture to a total of how many threads per block?	512	502	510	412	The number of threads in a thread block is also limited by the architecture to a total of 512 threads per block
150	1	CUDA Architecture is mainly provided by which company?	NVIDIA	Intel	Apple	IBM	NVIDIA provides CUDA services.
151	1	In CUDA Architecture, what are subprograms called?	Kernel	Grid	Element	Blocks	Subprograms are called kernels.
152	1	What is the fullform of CUDA?	Compute Unified Device Architecture	Computer Unified Device Architecture	Common USB Device Architecture	Common Unified Disk Architecture	CUDA Stands for Compute Unified Device Architecture.
153	2	Which of these is not an application of CUDA Arhitecture?	Thermo Dynamics	Neural Networks	VLSI Stimulation	Fluid Dynamics	CUDA architecture has no use on Thermo Dynamics.
154	2	CUDA programming is especially well-suited to address problems that can be expressed as_____ computations.	Data parallel	Task Parallel	Both a and b	None	CUDA programming is especially well-suited to address problems that can be expressed as dataparallel computations.
155	2	CUDA C/C++ uses which keyword in programming:	global	kernel	Cuda_void	nvcc	This is an explaination.
156	2	CUDA programs are saved with_____ extension.	.cd	.cx	.cc	.cu	This is an explaination

	marks	question	A	B	C	D	ans
157	2	The Kepler K20-X chip block, contains____ streaming multiprocessors\n(SMs).	15	8	16	7	The Kepler K20X chip block diagram, containing 15 streaming multiprocessors (SMs)
158	2	The Kepler K20X architecture increases the register file size to:	64K	32K	128K	256K	The K20X architecture increases the register fi le size to 64K
159	2	The register file in a GPU is of what size?	2 MB	1 MB	3MB	1024B	Register size in a GPU is 2MB.
160	2	NVIDIAâ€™s GPU computing platform is not enabled on which of the following product families:	AMD	Tegra	Quadro	Tesla	This is an explaination.
161	2	Tesla K-40 has compute capability of:	3.5	3.2	3.4	3.1	This is an explaination.
162	2	The SIMD unit creates, manages, schedules and executes_____ threads simultaneously to create a warp.	32	16	24	8	The SIMD unit creates, manages, schedules and executes 32 threads simultaneously to create a warp
163	2	Which hardware is used by the host interface to fasten the transfer of bulk data to and fro the graphics pipeline?	Direct Memory Access	Switch	Hub	Memory Hardware	This is an Explaination
164	2	A ____ is a collection of thread blocks of the same thread dimensionality which all execute the same kernel.	Grid	Core	Element	Blcoks	A â€˜gridâ€™ is a collection of thread blocks of the same thread dimensionality which all execute the same kernel
165	2	Active Warps can be classified into how many types?	3	2	4	5	This is an explaination.
166	2	All threads in a grid share the same_____space.	Global memory	Local Memory	Synchronized Memory	All	All threads in a grid\nshare the same global memory space
167	2	CUDA was introduced in which year?	2007	2006	2008	2010	This is an explaination.

	marks	question	A	B	C	D	ans
168	3	Unlike a C function call, all CUDA kernel launches are:	Asynchronous	Synchronous	Both a and b	None	Unlike a C function call, all CUDA kernel launches are asynchronous
169	3	A warp consists of____consecutive threads and all threads in a warp are executed in Single Instruction Multiple Thread (SIMT) fashion.	32	16	64	128	A warp consists of 32 consecutive threads and all\nthreads in a warp are executed in Single Instruction Multiple Thread (SIMT) fashion
170	3	There are how many streaming multiprocessors in CUDA architecture?	16	8	12	4	This is an explaination.
171	3	In CUDA programming, if CPU is the host then device will be:	GPU	Compiler	HDD	GPGPU	This is an explaination.
172	3	Both grids and blocks use the_____ type with three unsigned integer fields.	Dim3	Dim2	Dim1	Dim4	Both grids and blocks use the dim3 type with three unsigned integer fi elds
173	3	Tesla P100 GPU based on the Pascal GPU Architecture has 56 Streaming Multiprocessors (SMs), each capable of supporting up to____active threads.	2048	512	1024	256	Tesla P100 GPU based on the Pascal GPU Architecture has 56 Streaming Multiprocessors (SMs), each capable of supporting up to 2048 active threads.
174	3	The maximum size at each level of the thread hierarchy is_____dependent.	Device	Host	Compiler	Memory	The maximum size at each level of the thread hierarchy is device dependent.
175	3	Intel I7 has the memory bus of width:	19B	180B	152B	102B	This is an explaination.
176	3	The_____ is the heart of the GPU architecture:	Streaming Multiprocessor	Multiprocessor	CUDA	Compiler	The Streaming Multiprocessor (SM) is the heart of the GPU architecture.

	marks	question	A	B	C	D	ans
177	3	A kernel is defined using the_____ declaration specification	_global	_host	_device	_void	A kernel is defi ned using the\n__global declaration specifi cation
178	3	The function printThreadInfo() is not used to print out which of the following information about each thread:	Memory Allocations	Block Index	Matrix Coordinates	Control-Index	Ans-(d)- Memory Allocations.

Which is alternative options for latency hiding?

A. Increase CPU frequency

B. Multithreading

C. Increase Bandwidth

D. Increase Memory

ANSWER: B

_____ Communication model is generally seen in tightly coupled system.

A. Message Passing

B. Shared-address space

C. Client-Server

D. Distributed Network

ANSWER: B

The principal parameters that determine the communication latency are as follows:

A. Startup time (ts) Per-hop time (th) Per-word transfer time (tw)

B. Startup time (ts) Per-word transfer time (tw)

C. Startup time (ts) Per-hop time (th)

D. Startup time (ts) Message-Packet-Size(W)

ANSWER: A

The number and size of tasks into which a problem is decomposed determines the __

A. Granularity

B. Task

C. Dependency Graph

D. Decomposition

ANSWER: A

Average Degree of Concurrency is...

A. The average number of tasks that can run concurrently over the entire duration of execution of the process.

B. The average time that can run concurrently over the entire duration of execution of the process.

C. The average in degree of task dependency graph.

D. The average out degree of task dependency graph.

ANSWER: A

Which task decomposition technique is suitable for the 15-puzzle problem?

A. Data decomposition

B. Exploratory decomposition

C. Speculative decomposition

D. Recursive decomposition

ANSWER: B

Which of the following method is used to avoid Interaction Overheads?

A. Maximizing data locality

B. Minimizing data locality

C. Increase memory size

D. None of the above.

ANSWER: A

Which of the following is not parallel algorithm model

A. The Data Parallel Model

B. The work pool model

C. The task graph model

D. The Speculative Model

ANSWER: D

Nvidia GPU based on following architecture

A. MIMD

B. SIMD

C. SISD

D. MISD

ANSWER: B

What is Critical Path?

A. The length of the longest path in a task dependency graph is called the critical path length.

B. The length of the smallest path in a task dependency graph is called the critical path length.

C. Path with loop

D. None of the mentioned.

ANSWER: A

Which decompositioin technique uses divide-andconquer strategy?

A. recursive decomposition

B. Sdata decomposition

C. exploratory decomposition

D. speculative decomposition

ANSWER: A

If there are 6 nodes in a ring topology how many message passing cycles will be required to complete broadcast process in one to all?

A. 1

B. 6

C. 3

D. 4

ANSWER: 3

If there is 4 X 4 Mesh topology network then how many ring operation will perform to complete one to all broadcast?

A. 4

B. 8

C. 16

D. 32

ANSWER: 8

Consider all to all broadcast in ring topology with 8 nodes. How many messages will be present with each node after 3rd step/cycle of communication?

A. 3

B. 4

C. 6

D. 7

ANSWER: 4

Consider Hypercube topology with 8 nodes then how many message passing cycles will require in all to all broadcast operation?

A. The longest path between any pair of finish nodes.

B. The longest directed path between any pair of start & finish node.

C. The shortest path between any pair of finish nodes.

D. The number of maximum nodes level in graph.

ANSWER: D

Scatter is _____.

A. One to all broadcast communication

B. All to all broadcast communication

C. One to all personalised communication

D. Node of the above.

ANSWER: C

If there is 4X4 Mesh Topology _____ message passing cycles will require complete all to all reduction.

A. 4

B. 6

C. 8

D. 16

ANSWER: C

Following issue(s) is/are the true about sorting techniques with parallel computing.

A. Large sequence is the issue

B. Where to store output sequence is the issue

C. Small sequence is the issue

D. None of the above

ANSWER: B

Partitioning on series done after _____

A. Local arrangement

B. Processess assignments

C. Global arrangement

D. None of the above

ANSWER: C

In Parallel DFS processes has following roles.(Select multiple choices if applicable)

A. Donor

B. Active

C. Idle

D. Passive

ANSWER: A

Suppose there are 16 elements in a series then how many phases will be required to sort the series using parallel odd-even bubble sort?

A. 8

B. 4

C. 5

D. 15

ANSWER: D

Which are different sources of Overheads in Parallel Programs?

A. Interprocess interactions

B. Process Idling

C. All mentioned options

D. Excess Computation

ANSWER: C

The ratio of the time taken to solve a problem on a parallel processors to the time required to solve the same problem on a single processor with p identical processing elements.

A. The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements.

B. The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements

C. The ratio of number of multiple processors to size of data

D. None of the above

ANSWER: B

Efficiency is a measure of the fraction of time for which a processing element is usefully employed.

A. TRUE

B. FALSE

ANSWER: A

CUDA helps do execute code in parallel mode using _____

A. CPU

B. GPU

C. ROM

D. Cash memory

ANSWER: B

In thread-function execution scenario thread is a _____

A. Work

B. Worker

C. Task

D. None of the above

ANSWER: B

In GPU Following statements are true

A. Grid contains Block

B. Block contains Threads

C. All the mentioned options.

D. SM stands for Streaming MultiProcessor

ANSWER: C

Computer system of a parallel computer is capable of_____

A. Decentralized computing

B. Parallel computing

C. Centralized computing

D. All of these

ANSWER: A

In which application system Distributed systems can run well?

A. HPC

B. Distrubuted Framework

C. HRC

D. None of the above

ANSWER: A

A pipeline is like ..... ?

A. an automobile assembly line

B. house pipeline

C. both a and b

D. a gas line

ANSWER: A

Pipeline implements ?

A. fetch instruction

B. decode instruction

C. fetch operand

D. all of above

ANSWER: D

A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ ?

A. Super-scaling

B. Pipe-lining

C. Parallel Computation

D. None of these

ANSWER: B

In a parallel execution, the performance will always improve as the number of processors will increase?

A. True

B. False

ANSWER: B

VLIW stands for ?

A. Very Long Instruction Word

B. Very Long Instruction Width

C. Very Large Instruction Word

D. Very Long Instruction Width

ANSWER: A

In VLIW the decision for the order of execution of the instructions depends on the program itself?

A. True

B. False

ANSWER: A

Which one is not a limitation of a distributed memory parallel system?

A. Higher communication time

B. Cache coherency

C. Synchronization overheads

D. None of the above

ANSWER: B

Which of these steps can create conflict among the processors?

A. Synchronized computation of local variables

B. Concurrent write

C. Concurrent read

D. None of the above

ANSWER: B

Which one is not a characteristic of NUMA multiprocessors?

A. It allows shared memory computing

B. Memory units are placed in physically different location

C. All memory units are mapped to one common virtual global memory

D. Processors access their independent local memories

ANSWER: D

Which of these is not a source of overhead in parallel computing?

A. Non-uniform load distribution

B. Less local memory requirement in distributed computing

C. Synchronization among threads in shared memory computing

D. None of the above

ANSWER: B

Systems that do not have parallel processing capabilities are?

A. SISD

B. SIMD

C. MIMD

D. All of the above

ANSWER: A

How does the number of transistors per chip increase according to Moore ´s law?

A. Quadratically

B. Linearly

C. Cubicly

D. Exponentially

ANSWER: D

Parallel processing may occur?

A. in the instruction stream

B. in the data stream

C. both[A] and [B]

D. none of the above

ANSWER: C

To which class of systems does the von Neumann computer belong?

A. SIMD (Single Instruction Multiple Data)

B. MIMD (Multiple Instruction Multiple Data)

C. MISD (Multiple Instruction Single Data)

D. SISD (Single Instruction Single Data)

ANSWER: D

Fine-grain threading is considered as a _____ threading?

A. Instruction-level

B. Loop level

C. Task-level

D. Function-level

ANSWER: A

Multiprocessor is systems with multiple CPUs, which are capable of independently executing different tasks in parallel. In this category every processor and memory module has similar access time?

A. UMA

B. Microprocessor

C. Multiprocessor

D. NUMA

ANSWER: A

For inter processor communication the miss arises are called?

A. hit rate

B. coherence misses

C. comitt misses

D. parallel processing

ANSWER: B

NUMA architecture uses _____in design?

A. cache

B. shared memory

C. message passing

D. distributed memory

ANSWER: D

A multiprocessor machine which is capable of executing multiple instructions on multiple data sets?

A. SISD

B. SIMD

C. MIMD

D. MISD

ANSWER: C

In message passing, send and receive message between?

A. Task or processes

B. Task and Execution

C. Processor and Instruction

D. Instruction and decode

ANSWER: A

The First step in developing a parallel algorithm is_____?

A. To Decompose the problem into tasks that can be executed concurrently

B. Execute directly

C. Execute indirectly

D. None of Above

ANSWER: A

The number of tasks into which a problem is decomposed determines its?

A. Granularity

B. Priority

C. Modernity

D. None of above

ANSWER: A

The length of the longest path in a task dependency graph is called?

A. the critical path length

B. the critical data length

C. the critical bit length

D. None of above

ANSWER: A

The graph of tasks (nodes) and their interactions/data exchange (edges)?

A. Is referred to as a task interaction graph

B. Is referred to as a task Communication graph

C. Is referred to as a task interface graph

D. None of Above

ANSWER: A

Mappings are determined by?

A. task dependency

B. task interaction graphs

C. Both A and B

D. None of Above

ANSWER: C

Decomposition Techniques are?

A. recursive decomposition

B. data decomposition

C. exploratory decomposition

D. All of Above

ANSWER: D

The Owner Computes Rule generally states that the process assigned a particular data item is responsible for?

A. All computation associated with it

B. Only one computation

C. Only two computation

D. Only occasionally computation

ANSWER: A

A simple application of exploratory decomposition is_?

A. The solution to a 15 puzzle

B. The solution to 20 puzzle

C. The solution to any puzzle

D. None of Above

ANSWER: A

Speculative Decomposition consist of _?

A. conservative approaches

B. optimistic approaches

C. Both A and B

D. Only B

ANSWER: C

task characteristics include?

A. Task generation.

B. Task sizes.

C. Size of data associated with tasks.

D. All of Above

ANSWER: D

Writing parallel programs is referred to as?

A. Parallel computation

B. Parallel processes

C. Parallel development

D. Parallel programming

ANSWER: D

Parallel Algorithm Models?

A. Data parallel model

B. Bit model

C. Data model

D. network model

ANSWER: A

The number and size of tasks into which a problem is decomposed determines the?

A. fine-granularity

B. coarse-granularity

C. sub Task

D. granularity

ANSWER: A

A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is its _____ path?

A. critical

B. easy

C. difficult

D. ambiguous

ANSWER: A

The pattern of_____ among tasks is captured by what is known as a task-interaction graph?

A. Interaction

B. communication

C. optmization

D. flow

ANSWER: A

Interaction overheads can be minimized by____?

A. Maximize Data Locality

B. Maximize Volume of data exchange

C. Increase Bandwidth

D. Minimize social media contents

ANSWER: A

Type of parallelism that is naturally expressed by independent tasks in a task-dependency graph is called _____ parallelism?

A. Task

B. Instruction

C. Data

D. Program

ANSWER: A

Speed up is defined as a ratio of?

A. s=Ts/Tp

B. S= Tp/Ts

C. Ts=S/Tp

D. Tp=S /Ts

ANSWER: A

Parallel computing means to divide the job into several _____?

A. Bit

B. Data

C. Instruction

D. Task

ANSWER: D

_____ is a method for inducing concurrency in problems that can be solved using the divide-and-conquer strategy?

A. exploratory decomposition

B. speculative decomposition

C. data-decomposition

D. Recursive decomposition

ANSWER: C

The___ time collectively spent by all the processing elements Tall = p TP?

A. total

B. Average

C. mean

D. sum

ANSWER: A

Group communication operations are built using point-to-point messaging primitives?

A. True

B. False

ANSWER: A

Communicating a message of size m over an uncongested network takes time ts + tmw?

A. True

B. False

ANSWER: A

The dual of one-to-all broadcast is ?

A. All-to-one reduction

B. All-to-one receiver

C. All-to-one Sum

D. None of Above

ANSWER: A

A hypercube has?

A. 2d nodes

B. 2d nodes

C. 2n Nodes

D. N Nodes

ANSWER: A

A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes?

A. True

B. False

ANSWER: A

In All-to-All Broadcast each processor is thesource as well as destination?

A. True

B. False

ANSWER: A

The Prefix Sum Operation can be implemented using the ?

A. All-to-all broadcast kernel.

B. All-to-one broadcast kernel.

C. One-to-all broadcast Kernel

D. Scatter Kernel

ANSWER: A

In the scatter operation ?

A. Single node send a unique message of size m to every other node

B. Single node send a same message of size m to every other node

C. Single node send a unique message of size m to next node

D. None of Above

ANSWER: A

The gather operation is exactly the inverse of the ?

A. Scatter operation

B. Broadcast operation

C. Prefix Sum

D. Reduction operation

ANSWER: A

In All-to-All Personalized Communication Each node has a distinct message of size m for every other node ?

A. True

B. False

ANSWER: A

Parallel algorithms often require a single process to send identical data to all other processes or to a subset of them. This operation is known as _____?

A. one-to-all broadcast

B. All to one broadcast

C. one-to-all reduction

D. all to one reduction

ANSWER: A

In which of the following operation, a single node sends a unique message of size m to every other node?

A. Gather

B. Scatter

C. One to all personalized communication

D. Both A and C

ANSWER: D

Gather operation is also known as _____?

A. One to all personalized communication

B. One to all broadcast

C. All to one reduction

D. All to All broadcast

ANSWER: A

one-to-all personalized communication does not involve any duplication of data?

A. True

B. False

ANSWER: A

Gather operation, or concatenation, in which a single node collects a unique message from each node?

A. True

B. False

ANSWER: A

Conventional architectures coarsely comprise of a?

A. A processor

B. Memory system

C. Data path.

D. All of Above

ANSWER: D

Data intensive applications utilize?

A. High aggregate throughput

B. High aggregate network bandwidth

C. High processing and memory system performance.

D. None of above

ANSWER: A

A pipeline is like?

A. Overlaps various stages of instruction execution to achieve performance.

B. House pipeline

C. Both a and b

D. A gas line

ANSWER: A

Scheduling of instructions is determined?

A. True Data Dependency

B. Resource Dependency

C. Branch Dependency

D. All of above

ANSWER: D

VLIW processors rely on?

A. Compile time analysis

B. Initial time analysis

C. Final time analysis

D. Mid time analysis

ANSWER: A

Memory system performance is largely captured by?

A. Latency

B. Bandwidth

C. Both a and b

D. none of above

ANSWER: C

The fraction of data references satisfied by the cache is called?

A. Cache hit ratio

B. Cache fit ratio

C. Cache best ratio

D. none of above

ANSWER: A

A single control unit that dispatches the same Instruction to various processors is?

A. SIMD

B. SPMD

C. MIMD

D. None of above

ANSWER: A

The primary forms of data exchange between parallel tasks are?

A. Accessing a shared data space

B. Exchanging messages.

C. Both A and B

D. None of Above

ANSWER: C

Switches map a fixed number of inputs to outputs?

A. True

B. False

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A. Decentralized computing

B. Parallel computing

C. Centralized computing

D. Decentralized computing

E. Distributed computing

ANSWER: A

Writing parallel programs is referred to as?

A. Parallel computation

B. Parallel processes

C. Parallel development

D. Parallel programming

ANSWER: D

Simplifies applications of three-tier architecture is _____?

A. Maintenance

B. Initiation

C. Implementation

D. Deployment

ANSWER: D

Dynamic networks of networks, is a dynamic connection that grows is called?

A. Multithreading

B. Cyber cycle

C. Internet of things

D. Cyber-physical system

ANSWER: C

In which application system Distributed systems can run well?

A. HPC

D. HTC

C. HRC

D. Both A and B

ANSWER: D

In which systems desire HPC and HTC?

A. Adaptivity

B. Transparency

C. Dependency

D. Secretive

ANSWER: B

No special machines manage the network of architecture in which resources are known as?

A. Peer-to-Peer

B. Space based

C. Tightly coupled

D. Loosely coupled

ANSWER: A

Significant characteristics of Distributed systems have of ?

A. 5 types

B. 2 types

C. 3 types

D. 4 types

ANSWER: C

Built of Peer machines are over?

A. Many Server machines

B. 1 Server machine

C. 1 Client machine

D. Many Client machines

ANSWER: D

Type HTC applications are?

A. Business

B. Engineering

C. Science

D. Media mass

ANSWER: A

Virtualization that creates one single address space architecture that of, is called?

A. Loosely coupled

B. Peer-to-Peer

C. Space-based

D. Tightly coupled

ANSWER: C

We have an internet cloud of resources In cloud computing to form?

A. Centralized computing

B. Decentralized computing

C. Parallel computing

D. All of these

ANSWER: D

Data access and storage are elements of Job throughput, of _____?

A. Flexibility

B. Adaptation

C. Efficiency

D. Dependability

ANSWER: C

Billions of job requests is over massive data sets, ability to support known as?

A. Efficiency

B. Dependability

C. Adaptation

D. Flexibility

ANSWER: C

Broader concept offers Cloud computing .to select which of the following?

A. Parallel computing

B. Centralized computing

C. Utility computing

D. Decentralized computing

ANSWER: C

Resources and clients transparency that allows movement within a system is called?

A. Mobility transparency

B. Concurrency transparency

C. Performance transparency

D. Replication transparency

ANSWER: A

Distributed program in a distributed computer running a is known as?

A. Distributed process

B. Distributed program

C. Distributed application

D. Distributed computing

ANSWER: B

Uniprocessor computing devices is called_____?

A. Grid computing

B. Centralized computing

C. Parallel computing

D. Distributed computing

ANSWER: B

Utility computing focuses on a_____ model?

A. Data

B. Cloud

C. Scalable

D. Business

ANSWER: D

What is a CPS merges technologies?

A. 5C

B. 2C

C. 3C

D. 4C

ANSWER: C

Aberration of HPC?

A. High-peak computing

B. High-peripheral computing

C. High-performance computing

D. Highly-parallel computing

ANSWER: C

Peer-to-Peer leads to the development of technologies like?

A. Norming grids

B. Data grids

C. Computational grids

D. Both A and B

ANSWER: D

Type of HPC applications of?

A. Management

B. Media mass

C. Business

D. Science

ANSWER: D

The development generations of Computer technology has gone through?

A. 6

B. 3

C. 4

D. 5

ANSWER: D

Utilization rate of resources in an execution model is known to be its?

A. Adaptation

B. Efficiency

C. Dependability

D. Flexibility

ANSWER: B

Even under failure conditions Providing Quality of Service (QoS) assurance is the responsibility of?

A. Dependability

B. Adaptation

C. Flexibility

D. Efficiency

ANSWER: A

Interprocessor communication that takes place?

A. Centralized memory

B. Shared memory

C. Message passing

D. Both A and B

ANSWER: D

Data centers and centralized computing covers many and?

A. Microcomputers

B. Minicomputers

C. Mainframe computers

D. Supercomputers

ANSWER: D

Which of the following is an primary goal of HTC paradigm_____?

A. High ratio Identification

B. Low-flux computing

C. High-flux computing

D. Computer utilities

ANSWER: C

The high-throughput service provided is measures taken by

A. Flexibility

B. Efficiency

C. Dependability

D. Adaptation

ANSWER: D

What are the sources of overhead?

A. Essential /Excess Computation

B. Inter-process Communication

C. Idling

D. All above

ANSWER: D

Which are the performance metrics for parallel systems?

A. Execution Time

B. Total Parallel Overhead

C. Speedup

D. All above

ANSWER: D

The efficiency of a parallel program can be written as: E = Ts / pTp. True or False?

A. True

B. False

ANSWER: A

The important feature of the VLIW is _____?

A. ILP

B. Performance

C. Cost effectiveness

D. delay

ANSWER: A

SUB : 410241 HPC

Which of the following statements are true with regard to compute capability in CUDA

A. Code compiled for hardware of one compute capability will not need to be re-compiled to run on hardware of another

B. Different compute capabilities may imply a different amount of local memory per thread

C. Compute capability is measured by the number of FLOPS a GPU accelerator can compute.

Answer : B

True or False: The threads in a thread block are distributed across SM units so that each thread is executed by one SM unit.

A. True

B. False

Answer : B

The style of parallelism supported on GPUs is best described as

A. SISD - Single Instruction Single Data

B. MISD - Multiple Instruction Single Data

C. SIMT - Single Instruction Multiple Thread

Answer : C

True or false: Functions annotated with the __global__ qualifier may be executed on the host or the device

A. True

B. Flase

Answer : A

SUB : 410241 HPC

Which of the following correctly describes a GPU kernel

A. A kernel may contain a mix of host and GPU code

B. All thread blocks involved in the same computation use the same kernel

C. A kernel is part of the GPU's internal micro-operating system, allowing it to act as in independent host

Answer : B

Which of the following is *not* a form of parallelism supported by CUDA

A. Vector parallelism - Floating point computations are executed in parallel on wide vector units

B. Thread level task parallelism - Different threads execute a different tasks

C. Block and grid level parallelism - Different blocks or grids execute different tasks

D. Data parallelism - Different threads and blocks process different parts of data in memory

Answer :A

What strategy does the GPU employ if the threads within a warp diverge in their execution?

A. Threads are moved to different warps so that divergence does not occur within a single warp

B. Threads are allowed to diverge

C. All possible execution paths are run by all threads in a warp serially so that thread instructions do not diverge

Answer : C

Which of the following does *not* result in uncoalesced (i.e. serialized) memory access on the K20 GPUs installed on Stampede

A. Aligned, but non-sequential access

B. Misaligned data access

C. Sparse memory access

Answer : A

SUB : 410241 HPC

Which of the following correctly describes the relationship between Warps, thread blocks, and CUDA cores?

A. A warp is divided into a number of thread blocks, and each thread block executes on a single CUDA core

B. A thread block may be divided into a number of warps, and each warp may execute on a single CUDA core

C. A thread block is assigned to a warp, and each thread in the warp is executed on a separate CUDA core

Answer : B

Shared memory in CUDA is accessible to:

A. All threads in a single block

B. Both the host and GPU

C. All threads associated with a single kernel

Answer : A

CUDA Architecture CPU consist of

A. CUDA Libraries

B. CUDA Runtime

C. CUDA Driver

D. All Above

Answer : D

CUDA platform works on

A. C

B. C++

C. Forton

D. All Above

Answer : D

SUB : 410241 HPC

Threads support Shared memory and Synchronization

A. True

B. False

Answer : A

Application of CUDA are

A. Fast Video Transcoding

B. Medical Imaging

C. Computational Science

D. Oil and Natural Resources exploration

E. All Above

Answer : E

GPU execute device code

A. True

B. False

Answer : A

SUB : 410241 HPC

What are the issues in sorting?

A. Where the Input and Output Sequences are Stored

B. How Comparisons are Performed

C. All above

Answer : C

The parallel run time of the formulation for Bubble sort is

A. Tp = O(n/plogn/p) + O(n) + O(n)

B. Tp = O(n/plogn/p) + O (n/plogp) + O(ln/p)

C. Non of the above

Answer : A

What are the variants of Bubble sort?

A. Shell sort

B. Quick sort

C. Odd-Even transposition

D. Option A & C

Answer : D

What is the overall complexity of parallel algorithm for quick sort?

A. Tp = O(n/p logn/p) + O(n/p logp) + O($\log^2$p)

B. Tp = O(n/p logn/p) + O(n/p logp)

C. Tp = O(n/p logn/p) + O($\log^2$p)

Answer : A

SUB : 410241 HPC

Formally, given a weighted graph $G(V, E, w)$, the ***all-pairs shortest paths*** problem is to find the shortest paths between all pairs of vertices. True or False?

A. True
B. False

Answer : A

What is true for parallel formulation of Dijkstra's Algorithm?

A. One approach partitions the vertices among different processes and has each process compute the single-source shortest paths for all vertices assigned to it. We refer to this approach as the ***source-partitioned formulation.***
B. Another approach assigns each vertex to a set of processes and uses the parallel formulation of the single-source algorithm to solve the problem on each set of processes. We refer to this approach as the ***source-parallel formulation***.
C. Both are true
D. Non of these is true

Answer : C

Search algorithms can be used to solve discrete optimization problems. True or False ?

A. True
B. False

Answer : A

Examples of Discrete optimization problems are ;

A. planning and scheduling,
B. The optimal layout of VLSI chips,
C. Robot motion planning,
D. Test-pattern generation for digital circuits, and logistics and control.
E. All of above

Answer : E

List the important parameters of Parallel DFS

A. Work- Splitting Strategies

B. Load balancing Schemes

C. All of above

Answer : C

SUB : 410241 HPC

List the communication strategies for parallel BFS.

A. Random communication strategy

B. Ring communication strategy

C. Blackboard communication strategy

D. All of above

Answer : D

The lower bound on any comparison-based sort of *n* numbers is $\Theta(n \log n)$

A. True
B. False

Answer : A

In a compare-split operation

A. Each process sends its block of size n/p to the other process
B. Each process merges the received block with its own block and retains only the appropriate half of the merged block
C. Both A & B

Answer : C

In a typical sorting network

A. Every sorting network is made up of a series of columns
B. Each column contains a number of comparators connected in parallel
C. Both A & B

Answer : C

Bubble sort is difficult to parallelize since the algorithm has no concurrency

A. True
B. False

Answer : A

SUB : 410241 HPC

What are the sources of overhead?

A. Essential /Excess Computation
B. Inter-process Communication
C. Idling
D. All above

Answer : D

Which are the performance metrics for parallel systems?

A. Execution Time
B. Total Parallel Overhead
C. Speedup
D. Efficiency
E. Cost
F. All above

Answer : F

The efficiency of a parallel program can be written as: ***E = Ts / pTp.*** True or False?

A. True
B. False

Answer : A

Overhead function or ***total overhead*** of a parallel system as the total time collectively spent by all the processing elements over and above that required by the fastest known sequential algorithm for solving the same problem on a single processing element. True or False?

A. True
B. False

Answer : A

What is Speedup?

A. A measure that captures the relative benefit of solving a problem in parallel. It is defined as the ratio of the time taken to solve a problem on a single processing element to the time required to solve the same problem on a parallel computer with *p* identical processing elements.
B. A measure of the fraction of time for which a processing element is usefully employed.
C. None of the above

Answer : A

In an ideal parallel system, speedup is equal to *p* and efficiency is equal to one. True or False?

A. True
B. False

Answer : A

SUB : 410241 HPC

A parallel system is said to be _____ if the cost of solving a problem on a parallel computer has the same asymptotic growth (in Θ terms) as a function of the input size as the fastest-known sequential algorithm on a single processing element.

A. Cost optimal
B. Non Cost optimal

Answer : A

Using fewer than the maximum possible number of processing elements to execute a parallel algorithm is called _____ a parallel system in terms of the number of processing elements.

A. Scaling down
B. Scaling up

Answer : B

The _____ function determines the ease with which a parallel system can maintain a constant efficiency and hence achieve speedups increasing in proportion to the number of processing elements.

A. Isoefficiency
B. Efficiency
C. Scalability
D. Total overhead

Answer : A

Minimum execution time for adding n numbers is *Tp = n/p + 2 logp* True or False ?

A. True
B. False

Answer : A

The overhead function To = pTP – TS.

A. True
B. False

Answer : A

Performance Metrics for Parallel Systems: Speedup(S) =TS/TP

A. True
B. False

Answer : A

Matrix Vector multiplication 2D Partitions requires some basic communication operations

A. one-to-one communication to align the vector along the main diagonal
B. one-to-all broadcast of each vector element among the n processes of each column
C. all-to-one reduction in each row
D. All Above

Answer : D

Which is alternative options for latency hiding?
A. Increase CPU frequency
B. Multithreading
C. Increase Bandwidth
D. Increase Memory
ANSWER: B

_____ Communication model is generally seen in tightly coupled system.
A. Message Passing
B. Shared-address space
C. Client-Server
D. Distributed Network
ANSWER: B

The principal parameters that determine the communication latency are as follows:
A. Startup time (ts) Per-hop time (th) Per-word transfer time (tw)
B. Startup time (ts) Per-word transfer time (tw)
C. Startup time (ts) Per-hop time (th)
D. Startup time (ts) Message-Packet-Size(W)
ANSWER: A

The number and size of tasks into which a problem is decomposed determines the __
A. Granularity
B. Task
C. Dependency Graph
D. Decomposition
ANSWER: A

Average Degree of Concurrency is...
A. The average number of tasks that can run concurrently over the entire duration of execution of the process.
B. The average time that can run concurrently over the entire duration of execution of the process.
C. The average in degree of task dependency graph.
D. The average out degree of task dependency graph.
ANSWER: A

Which task decomposition technique is suitable for the 15-puzzle problem?
A. Data decomposition
B. Exploratory decomposition
C. Speculative decomposition
D. Recursive decomposition
ANSWER: B

Which of the following method is used to avoid Interaction Overheads?
A. Maximizing data locality
B. Minimizing data locality
C. Increase memory size
D. None of the above.

ANSWER: A

Which of the following is not parallel algorithm model
A. The Data Parallel Model
B. The work pool model
C. The task graph model
D. The Speculative Model
ANSWER: D

Nvidia GPU based on following architecture
A. MIMD
B. SIMD
C. SISD
D. MISD
ANSWER: B

What is Critical Path?

A. The length of the longest path in a task dependency graph is called the critical path length.
B. The length of the smallest path in a task dependency graph is called the critical path length.
C. Path with loop
D. None of the mentioned.
ANSWER: A

Which decompositioin technique uses divide-andconquer strategy?
A. recursive decomposition
B. Sdata decomposition
C. exploratory decomposition
D. speculative decomposition
ANSWER: A

If there are 6 nodes in a ring topology how many message passing cycles will be required to complete broadcast process in one to all?

A. 1
B. 6
C. 3
D. 4
ANSWER: 3

If there is 4 X 4 Mesh topology network then how many ring operation will perform to complete one to all broadcast?

A. 4
B. 8
C. 16
D. 32
ANSWER: 8

Consider all to all broadcast in ring topology with 8 nodes. How many messages will be present with each node after 3rd step/cycle of communication?

A. 3
B. 4
C. 6
D. 7
ANSWER: 4

Consider Hypercube topology with 8 nodes then how many message passing cycles will require in all to all broadcast operation?

A. The longest path between any pair of finish nodes.
B. The longest directed path between any pair of start & finish node.
C. The shortest path between any pair of finish nodes.
D. The number of maximum nodes level in graph.
ANSWER: D

Scatter is _____.

A. One to all broadcast communication
B. All to all broadcast communication
C. One to all personalised communication
D. Node of the above.
ANSWER: C

If there is 4X4 Mesh Topology _____ message passing cycles will require complete all to all reduction.
A. 4
B. 6
C. 8
D. 16
ANSWER: C

Following issue(s) is/are the true about sorting techniques with parallel computing.
A. Large sequence is the issue
B. Where to store output sequence is the issue
C. Small sequence is the issue
D. None of the above
ANSWER: B

Partitioning on series done after _____
A. Local arrangement
B. Processess assignments
C. Global arrangement
D. None of the above
ANSWER: C

In Parallel DFS processes has following roles.(Select multiple choices if applicable)
A. Donor
B. Active
C. Idle
D. Passive
ANSWER: A

Suppose there are 16 elements in a series then how many phases will be required to sort the series using parallel odd-even bubble sort?
A. 8
B. 4
C. 5
D. 15
ANSWER: D

Which are different sources of Overheads in Parallel Programs?
A. Interprocess interactions
B. Process Idling
C. All mentioned options
D. Excess Computation
ANSWER: C

The ratio of the time taken to solve a problem on a parallel processors to the time required to solve the same problem on a single processor with p identical processing elements.
A. The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements.
B. The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements
C. The ratio of number of multiple processors to size of data
D. None of the above
ANSWER: B

Efficiency is a measure of the fraction of time for which a processing element is usefully employed.
A. TRUE
B. FALSE
ANSWER: A

CUDA helps do execute code in parallel mode using _____
A. CPU
B. GPU
C. ROM
D. Cash memory
ANSWER: B

In thread-function execution scenario thread is a _____
A. Work
B. Worker
C. Task
D. None of the above
ANSWER: B

In GPU Following statements are true
A. Grid contains Block
B. Block contains Threads
C. All the mentioned options.
D. SM stands for Streaming MultiProcessor

ANSWER: C

Computer system of a parallel computer is capable of_____
A. Decentralized computing
B. Parallel computing
C. Centralized computing
D. All of these
ANSWER: A

In which application system Distributed systems can run well?
A. HPC
B. Distrubuted Framework
C. HRC
D. None of the above
ANSWER: A

A pipeline is like ..... ?
A. an automobile assembly line
B. house pipeline
C. both a and b
D. a gas line
ANSWER: A

Pipeline implements ?
A. fetch instruction
B. decode instruction
C. fetch operand
D. all of above
ANSWER: D

A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ ?
A. Super-scaling
B. Pipe-lining
C. Parallel Computation
D. None of these
ANSWER: B

In a parallel execution, the performance will always improve as the number of processors will increase?
A. True
B. False
ANSWER: B

VLIW stands for ?
A. Very Long Instruction Word
B. Very Long Instruction Width
C. Very Large Instruction Word
D. Very Long Instruction Width
ANSWER: A

In VLIW the decision for the order of execution of the instructions depends on the program itself?
A. True

B. False
ANSWER: A

Which one is not a limitation of a distributed memory parallel system?
A. Higher communication time
B. Cache coherency
C. Synchronization overheads
D. None of the above
ANSWER: B

Which of these steps can create conflict among the processors?
A. Synchronized computation of local variables
B. Concurrent write
C. Concurrent read
D. None of the above
ANSWER: B

Which one is not a characteristic of NUMA multiprocessors?
A. It allows shared memory computing
B. Memory units are placed in physically different location
C. All memory units are mapped to one common virtual global memory
D. Processors access their independent local memories
ANSWER: D

Which of these is not a source of overhead in parallel computing?
A. Non-uniform load distribution
B. Less local memory requirement in distributed computing
C. Synchronization among threads in shared memory computing
D. None of the above
ANSWER: B

Systems that do not have parallel processing capabilities are?
A. SISD
B. SIMD
C. MIMD
D. All of the above
ANSWER: A

How does the number of transistors per chip increase according to Moore ´s law?
A. Quadratically
B. Linearly
C. Cubicly
D. Exponentially
ANSWER: D

Parallel processing may occur?
A. in the instruction stream
B. in the data stream
C. both[A] and [B]
D. none of the above
ANSWER: C

To which class of systems does the von Neumann computer belong?
A. SIMD (Single Instruction Multiple Data)
B. MIMD (Multiple Instruction Multiple Data)
C. MISD (Multiple Instruction Single Data)
D. SISD (Single Instruction Single Data)
ANSWER: D

Fine-grain threading is considered as a _____ threading?
A. Instruction-level
B. Loop level
C. Task-level
D. Function-level
ANSWER: A

Multiprocessor is systems with multiple CPUs, which are capable of independently executing different tasks in parallel. In this category every processor and memory module has similar access time?
A. UMA
B. Microprocessor
C. Multiprocessor
D. NUMA
ANSWER: A

For inter processor communication the miss arises are called?
A. hit rate
B. coherence misses
C. comitt misses
D. parallel processing
ANSWER: B

NUMA architecture uses _____in design?
A. cache
B. shared memory
C. message passing
D. distributed memory
ANSWER: D

A multiprocessor machine which is capable of executing multiple instructions on multiple data sets?
A. SISD
B. SIMD
C. MIMD
D. MISD
ANSWER: C

In message passing, send and receive message between?
A. Task or processes
B. Task and Execution
C. Processor and Instruction
D. Instruction and decode
ANSWER: A

The First step in developing a parallel algorithm is_____?
A. To Decompose the problem into tasks that can be executed

concurrently
B. Execute directly
C. Execute indirectly
D. None of Above
ANSWER: A

The number of tasks into which a problem is decomposed determines its?
A. Granularity
B. Priority
C. Modernity
D. None of above
ANSWER: A

The length of the longest path in a task dependency graph is called?
A. the critical path length
B. the critical data length
C. the critical bit length
D. None of above
ANSWER: A

The graph of tasks (nodes) and their interactions/data exchange (edges)?
A. Is referred to as a task interaction graph
B. Is referred to as a task Communication graph
C. Is referred to as a task interface graph
D. None of Above
ANSWER: A

Mappings are determined by?
A. task dependency
B. task interaction graphs
C. Both A and B
D. None of Above
ANSWER: C

Decomposition Techniques are?
A. recursive decomposition
B. data decomposition
C. exploratory decomposition
D. All of Above
ANSWER: D

The Owner Computes Rule generally states that the process assigned a particular data item is responsible for?
A. All computation associated with it
B. Only one computation
C. Only two computation
D. Only occasionally computation
ANSWER: A

A simple application of exploratory decomposition is_?
A. The solution to a 15 puzzle
B. The solution to 20 puzzle

C. The solution to any puzzle
D. None of Above
ANSWER: A

Speculative Decomposition consist of _?
A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B
ANSWER: C

task characteristics include?
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.
D. All of Above
ANSWER: D

Writing parallel programs is referred to as?
A. Parallel computation
B. Parallel processes
C. Parallel development
D. Parallel programming
ANSWER: D

Parallel Algorithm Models?
A. Data parallel model
B. Bit model
C. Data model
D. network model
ANSWER: A

The number and size of tasks into which a problem is decomposed determines the?
A. fine-granularity
B. coarse-granularity
C. sub Task
D. granularity
ANSWER: A

A feature of a task-dependency graph that determines the average degree of concurrency for a given granularity is its _____ path?
A. critical
B. easy
C. difficult
D. ambiguous
ANSWER: A

The pattern of_____ among tasks is captured by what is known as a task-interaction graph?
A. Interaction
B. communication
C. optmization

D. flow
ANSWER: A

Interaction overheads can be minimized by____?
A. Maximize Data Locality
B. Maximize Volume of data exchange
C. Increase Bandwidth
D. Minimize social media contents
ANSWER: A

Type of parallelism that is naturally expressed by independent tasks in a task-dependency graph is called _____ parallelism?
A. Task
B. Instruction
C. Data
D. Program
ANSWER: A

Speed up is defined as a ratio of?
A. s=Ts/Tp
B. S= Tp/Ts
C. Ts=S/Tp
D. Tp=S /Ts
ANSWER: A

Parallel computing means to divide the job into several _____?
A. Bit
B. Data
C. Instruction
D. Task
ANSWER: D

_____ is a method for inducing concurrency in problems that can be solved using the divide-and-conquer strategy?
A. exploratory decomposition
B. speculative decomposition
C. data-decomposition
D. Recursive decomposition
ANSWER: C

The___ time collectively spent by all the processing elements Tall = p TP?
A. total
B. Average
C. mean
D. sum
ANSWER: A

Group communication operations are built using point-to-point messaging primitives?
A. True
B. False
ANSWER: A

Communicating a message of size m over an uncongested network takes time ts + tmw?
A. True
B. False
ANSWER: A

The dual of one-to-all broadcast is ?
A. All-to-one reduction
B. All-to-one receiver
C. All-to-one Sum
D. None of Above
ANSWER: A

A hypercube has?
A. 2d nodes
B. 2d nodes
C. 2n Nodes
D. N Nodes
ANSWER: A

A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes?
A. True
B. False
ANSWER: A

In All-to-All Broadcast each processor is thesource as well as destination?
A. True
B. False
ANSWER: A

The Prefix Sum Operation can be implemented using the ?
A. All-to-all broadcast kernel.
B. All-to-one broadcast kernel.
C. One-to-all broadcast Kernel
D. Scatter Kernel
ANSWER: A

In the scatter operation ?
A. Single node send a unique message of size m to every other node
B. Single node send a same message of size m to every other node
C. Single node send a unique message of size m to next node
D. None of Above
ANSWER: A

The gather operation is exactly the inverse of the ?
A. Scatter operation
B. Broadcast operation
C. Prefix Sum
D. Reduction operation
ANSWER: A

In All-to-All Personalized Communication Each node has a distinct

message of size m for every other node ?
A. True
B. False
ANSWER: A

Parallel algorithms often require a single process to send identical data to all other processes or to a subset of them. This operation is known as _____?
A. one-to-all broadcast
B. All to one broadcast
C. one-to-all reduction
D. all to one reduction
ANSWER: A

In which of the following operation, a single node sends a unique message of size m to every other node?
A. Gather
B. Scatter
C. One to all personalized communication
D. Both A and C
ANSWER: D

Gather operation is also known as _____?
A. One to all personalized communication
B. One to all broadcast
C. All to one reduction
D. All to All broadcast
ANSWER: A

one-to-all personalized communication does not involve any duplication of data?
A. True
B. False
ANSWER: A

Gather operation, or concatenation, in which a single node collects a unique message from each node?
A. True
B. False
ANSWER: A

Conventional architectures coarsely comprise of a?
A. A processor
B. Memory system
C. Data path.
D. All of Above
ANSWER: D

Data intensive applications utilize?
A. High aggregate throughput
B. High aggregate network bandwidth
C. High processing and memory system performance.
D. None of above
ANSWER: A

A pipeline is like?
A. Overlaps various stages of instruction execution to achieve performance.
B. House pipeline
C. Both a and b
D. A gas line
ANSWER: A

Scheduling of instructions is determined?
A. True Data Dependency
B. Resource Dependency
C. Branch Dependency
D. All of above
ANSWER: D

VLIW processors rely on?
A. Compile time analysis
B. Initial time analysis
C. Final time analysis
D. Mid time analysis
ANSWER: A

Memory system performance is largely captured by?
A. Latency
B. Bandwidth
C. Both a and b
D. none of above
ANSWER: C

The fraction of data references satisfied by the cache is called?
A. Cache hit ratio
B. Cache fit ratio
C. Cache best ratio
D. none of above
ANSWER: A

A single control unit that dispatches the same Instruction to various processors is?
A. SIMD
B. SPMD
C. MIMD
D. None of above
ANSWER: A

The primary forms of data exchange between parallel tasks are?
A. Accessing a shared data space
B. Exchanging messages.
C. Both A and B
D. None of Above
ANSWER: C

Switches map a fixed number of inputs to outputs?
A. True

B. False
ANSWER: A

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C. Execute indirectly
D. None of Above
ANSWER: A

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C. Only two computation
D. Only occasionally computation

ANSWER: A

A simple application of exploratory decomposition is?
A. The solution to a 15 puzzle
B. The solution to 20 puzzle
C. The solution to any puzzle
D. None of Above
ANSWER: A

Speculative Decomposition consist of ?
A. conservative approaches
B. optimistic approaches
C. Both A and B
D. Only B
ANSWER: C

Task characteristics include?
A. Task generation.
B. Task sizes.
C. Size of data associated with tasks.
D. All of Above.
ANSWER: D

Group communication operations are built using point-to-point messaging primitives?
A. True
B. False
ANSWER: A

Communicating a message of size m over an uncongested network takes time ts + tmw?
A. True
B. False
ANSWER: A

The dual of one-to-all broadcast is?
A. All-to-one reduction
B. All-to-one receiver
C. All-to-one Sum
D. None of Above
ANSWER: A

A hypercube has?
A. 2d nodes
B. 3d nodes
C. 2n Nodes
D. N Nodes
ANSWER: A

A binary tree in which processors are (logically) at the leaves and internal nodes are routing nodes?
A. True
B. False
ANSWER: A

In All-to-All Broadcast each processor is the source as well as destination?
A. True
B. False
ANSWER: A

The Prefix Sum Operation can be implemented using the?
A. All-to-all broadcast kernel.
B. All-to-one broadcast kernel.
C. One-to-all broadcast Kernel
D. Scatter Kernel
ANSWER: A

In the scatter operation?
A. Single node send a unique message of size m to every other node
B. Single node send a same message of size m to every other node
C. Single node send a unique message of size m to next node
D. None of Above
ANSWER: A

The gather operation is exactly the inverse of the?
A. Scatter operation
B. Broadcast operation
C. Prefix Sum
D. Reduction operation
ANSWER: A

In All-to-All Personalized Communication Each node has a distinct message of size m for every other node?
A. True
B. False
ANSWER: A

Computer system of a parallel computer is capable of?
A. Decentralized computing
B. Parallel computing
C. Centralized computing
D. Decentralized computing
E. Distributed computing
ANSWER: A

Writing parallel programs is referred to as?
A. Parallel computation
B. Parallel processes
C. Parallel development
D. Parallel programming
ANSWER: D

Simplifies applications of three-tier architecture is _____?
A. Maintenance
B. Initiation
C. Implementation
D. Deployment

ANSWER: D

Dynamic networks of networks, is a dynamic connection that grows is called?
A. Multithreading
B. Cyber cycle
C. Internet of things
D. Cyber-physical system
ANSWER: C

In which application system Distributed systems can run well?
A. HPC
D. HTC
C. HRC
D. Both A and B
ANSWER: D

In which systems desire HPC and HTC?
A. Adaptivity
B. Transparency
C. Dependency
D. Secretive
ANSWER: B

No special machines manage the network of architecture in which resources are known as?
A. Peer-to-Peer
B. Space based
C. Tightly coupled
D. Loosely coupled
ANSWER: A

Significant characteristics of Distributed systems have of ?
A. 5 types
B. 2 types
C. 3 types
D. 4 types
ANSWER: C

Built of Peer machines are over?
A. Many Server machines
B. 1 Server machine
C. 1 Client machine
D. Many Client machines
ANSWER: D

Type HTC applications are?
A. Business
B. Engineering
C. Science
D. Media mass
ANSWER: A

Virtualization that creates one single address space architecture

that of, is called?
A. Loosely coupled
B. Peer-to-Peer
C. Space-based
D. Tightly coupled
ANSWER: C

We have an internet cloud of resources In cloud computing to form?
A. Centralized computing
B. Decentralized computing
C. Parallel computing
D. All of these
ANSWER: D

Data access and storage are elements of Job throughput, of _____?
A. Flexibility
B. Adaptation
C. Efficiency
D. Dependability
ANSWER: C

Billions of job requests is over massive data sets, ability to support known as?
A. Efficiency
B. Dependability
C. Adaptation
D. Flexibility
ANSWER: C

Broader concept offers Cloud computing .to select which of the following?
A. Parallel computing
B. Centralized computing
C. Utility computing
D. Decentralized computing
ANSWER: C

Resources and clients transparency that allows movement within a system is called?
A. Mobility transparency
B. Concurrency transparency
C. Performance transparency
D. Replication transparency
ANSWER: A

Distributed program in a distributed computer running a is known as?
A. Distributed process
B. Distributed program
C. Distributed application
D. Distributed computing
ANSWER: B

Uniprocessor computing devices is called_____?

A. Grid computing
B. Centralized computing
C. Parallel computing
D. Distributed computing
ANSWER: B

Utility computing focuses on a_____ model?
A. Data
B. Cloud
C. Scalable
D. Business
ANSWER: D

What is a CPS merges technologies?
A. 5C
B. 2C
C. 3C
D. 4C
ANSWER: C

Aberration of HPC?
A. High-peak computing
B. High-peripheral computing
C. High-performance computing
D. Highly-parallel computing
ANSWER: C

Peer-to-Peer leads to the development of technologies like?
A. Norming grids
B. Data grids
C. Computational grids
D. Both A and B
ANSWER: D

Type of HPC applications of?
A. Management
B. Media mass
C. Business
D. Science
ANSWER: D

The development generations of Computer technology has gone through?
A. 6
B. 3
C. 4
D. 5
ANSWER: D

Utilization rate of resources in an execution model is known to be its?
A. Adaptation
B. Efficiency
C. Dependability
D. Flexibility

ANSWER: B

Even under failure conditions Providing Quality of Service (QoS) assurance is the responsibility of?
A. Dependability
B. Adaptation
C. Flexibility
D. Efficiency
ANSWER: A

Interprocessor communication that takes place?
A. Centralized memory
B. Shared memory
C. Message passing
D. Both A and B
ANSWER: D

Data centers and centralized computing covers many and?
A. Microcomputers
B. Minicomputers
C. Mainframe computers
D. Supercomputers
ANSWER: D

Which of the following is an primary goal of HTC paradigm_____?
A. High ratio Identification
B. Low-flux computing
C. High-flux computing
D. Computer utilities
ANSWER: C

The high-throughput service provided is measures taken by
A. Flexibility
B. Efficiency
C. Dependability
D. Adaptation
ANSWER: D

What are the sources of overhead?
A. Essential /Excess Computation
B. Inter-process Communication
C. Idling
D. All above
ANSWER: D

Which are the performance metrics for parallel systems?
A. Execution Time
B. Total Parallel Overhead
C. Speedup
D. All above
ANSWER: D

The efficiency of a parallel program can be written as: E = Ts /

pTp. True or False?
A. True
B. False
ANSWER: A

The important feature of the VLIW is _____?
A. ILP
B. Performance
C. Cost effectiveness
D. delay
ANSWER: A

1.Following is true about one to all broadcast

A.In one to all broadcast initially there will be P(Number of processors) copies of messages and after broadcast finally there will be simgle copy

B.In one to all broadcast initially there will be single copy of message and after broadcast finally there will P(Number of processors) copies.

Submit

Answer

“In one to all broadcast initially there will be single copy of message and after broadcast finally there will P(Number of processors) copies.”

2.If total 8 nodes are in ring topology after one to all message broadcasting how many source nodes will be present?

2

4

8

1

Submit

Answer

8

3.Current source node selects _____ node as next source node in linear/ring one to all message broadcast

A.nearest node

B.longest node

Submit

Answer

longest node

4.In All-to-one reduction after reduction the final copy of massage is avilible on which node?

A.Source Node

B.Destination Node

C.Both of the above

D.None of these

Answer

Destination Node

5.If there is 4 by 4 mesh topology network present(as per shown in the video) then in how many broadcast cycles will be required to reach message to all 16 nodes?

2

8

4

16

Submit

Answer

4

6.If there are 8 nodes in a ring topology how many message passing cycles will be required to complete reduction process

1

2

3

4

Submit

Answer

3

7.In One to all broadcast using Hypercube topology how source node selects next destination node?

Node which is having lowest binary code (label)

Node which is having highet binary code (label)

To all connected node at a time

None of the above

Submit

Answer

Node which is having highet binary code (label)

8.If there are 8 nodes connected in ring topology then ___ number of message passing cycles will be required to complete all to all broadcast in parallel mode.

3

4

8

7

Submit

Answer

7

9.Consider all to all broadcast in ring topology with 8 nodes.How many messages will be present with each node after 3rd step/cycle of communication?

3

4

7

None of the above

Submit

Answer

4

10.If there are 16 messages in 4x4 mesh then total how many message passsing cycles will be required to complete all to all broadcast operation?

4

5

6

8

Submit

Answer

6

11.If there are P messages in mxm mesh then total how many message passsing cycles will be required to complete all to all broadcast operation?

2 √P - 2

2 √P - 1

2 √P

None of the above

Submit

Answer

2 √P - 2

12.How many massage passing cycles required for all-to-all broadcasting in 8 nodes hypercube?

4

3

2

8

Submit

Answer

3

13.In scatter opreation after massage broadcasting every node avail with same massage copy.

True

False

Submit

Answer

False

14.CUDA helps do execute code in parallel mode using __

CPU

GPU

ROM

Cash memory

Submit

Answer

GPU

15.In thread-function execution scenario thread is a ___

Work

Worker

Task

None of the above

Submit

Answer

Worker

16.In GPU Following statements are true

Block contains Grid

Grid contains Block

Block contains Threads

SM stands for Streaming MultiMedia

SM stands for Streaming MultiProcessor

Submit

Answer

“Grid contains Block”, “Block contains Threads”, “SM stands for Streaming MultiProcessor

17.Following issue(s) is/are the true about sorting techniques with parallel computing.

Large sequence is the issue

Where to store output sequence is the issue

Where to store input sequence is the issue

None of the above

Submit

Answer

“Where to store output sequence is the issue”, “Where to store input sequence is the issue”

18.Partitioning on series done after __

Local arrangement

Processess assignments

Global arrangement

None of the above

Submit

Answer

Global arrangement

19.In Parallel DFS processes has following roles.(Select multiple choices if applicable)

Donor

Active

Idle

Recipient

Submit

Answer

“Donor”, “Recipient”

20.Suppose there are 16 elements in a series then how many phases will be required to sort the series using parallel odd-even bubble sort?

8

4

5

15

Submit

Answer

15

21.Which are different sources of Overheads in Parallel Programs?

Interprocess interactions

Process Idling

Large amount of DATA

Excess Computation

Submit

Answer

“Interprocess interactions”, “Process Idling”, “Excess Computation”

1 / 1 points
1 / 1 attempts

22,Speedup (S) is….

The ratio of the time taken to solve a problem on a parallel processors to the time required to solve the same problem on a single processor with p identical processing elements

The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements

The ratio of number of multiple processors to size of data

None of the above

Submit

Answer

The ratio of the time taken to solve a problem on a single processor to the time required to solve the same problem on a parallel computer with p identical processing elements

1 / 1 points
1 / 1 attempts

23.Efficiency is a measure of the fraction of time for which a processing element is usefully employed.

TRUE

FALSE

Submit

Answer

TRUE

SUB : 410241 HPC

1. What is Cuda Architecture?

a.CUDA Architecture included a unified shader pipeline, allowing each and every chip to be marshaled by a program.

b.CUDA Architecture included a unified shader pipeline, allowing each and every unit on the chip to be marshaled by a program intending to perform general-purpose computations

c.CUDA Architecture included a unified shader pipeline, allowing each and every logic unit on the chip to be marshaled by a program intending to perform general-purpose computations

d.CUDA Architecture included a unified shader pipeline, allowing each and every arithmetic logic unit (ALU) on the chip to be marshaled by a program intending to perform general-purpose computations

Ans.D

2. For the following code write a kernel

```
__global__ void kernel( void ) { }
int main( void ) {
// Write a kernel here

 printf( "Hello, World!\n" ); return 0; }

a.kernel<1, 1>(1,1);
b.kernel<<<1, 1>>>(1,1);
c.kernel<<<1, 1>>>();
d.kernel<<1, 1>>();
```

Ans. c

3. Find out which is the kernel from following code:

```
#include <iostream>
__global__ void add( int a, int b, int *c ) {
 *c = a + b;
}

int main( void ) {
int c; int *dev_c;

HANDLE_ERROR( cudaMalloc( (void**)&dev_c, sizeof(int) ) );
```

```
add<<<1,1>>>( 2, 7, dev_c );

HANDLE_ERROR( cudaMemcpy( &c, dev_c, sizeof(int), cudaMemcpyDeviceToHost ) );
printf( "2 + 7 = %d\n", c );
cudaFree( dev_c );
return 0;

}
```

a.cudaMalloc((void**)&dev_c, sizeof(int))
b.add<<<1,1>>>(2, 7, dev_c)
c.add<<1,1>>(2, 7, dev_c);
d.add<<<1,1>>>()

Ans.b

4. From following code which particular line is responsible for copying between device to host

```
#include <iostream>
__global__ void add( int a, int b, int *c ) {
 *c = a + b;
}

int main( void ) {
int c; int *dev_c;

HANDLE_ERROR( cudaMalloc( (void**)&dev_c, sizeof(int) ) );

add<<<1,1>>>( 2, 7, dev_c );

HANDLE_ERROR( cudaMemcpy( &c, dev_c, sizeof(int), cudaMemcpyDeviceToHost ) );
printf( "2 + 7 = %d\n", c );
cudaFree( dev_c );
return 0;

}
```

a. c, dev_c, sizeof(int);
b. HANDLE_ERROR(&c, dev_c, sizeof(int), cudaMemcpyDeviceToHost);

c. HANDLE_ERROR(cudaMemcpy(&c, dev_c, sizeof(int), cudaMemcpyDeviceToHost));
d. cudaMemcpy(&c, dev_c, sizeof(int), cudaMemcpyDeviceToHost) ;

Ans.c

5. What is output of the following code:

```
#include <iostream>
__global__ void add( int a, int b, int *c ) {
 *c = a + b;
}

int main( void ) {
int c; int *dev_c;

HANDLE_ERROR( cudaMalloc( (void**)&dev_c, sizeof(int) ) );

add<<<1,1>>>( 2, 7, dev_c );

HANDLE_ERROR( cudaMemcpy( &c, dev_c, sizeof(int), cudaMemcpyDeviceToHost ) );
printf( "2 + 7 = %d\n", c );
cudaFree( dev_c );
return 0;

}
```

a.2
b.9
c.7
d.0

Ans. b

6.what is function of e __global__ qualifier in cuda program

a. alerts the compiler that a function should be compiled to run on a device instead of the host
b. alerts the interpreter that a function should be compiled to run on a device instead of the host

c. alerts the interpreter that a function should be interpreted to run on a device instead of the host
d. alerts the interpreter that a function should be compiled to run on a host instead of the device

ans.a

7.The on-chip memory which is local to every multithreaded Single Instruction Multiple Data (SIMD) Processor is called

a.Local Memory
b.Global Memory
c.Flash memory
d.Stack

Ans. a

8. The machine object created by the hardware, managing, scheduling, and executing is a thread of

a.DIMS instructions
b.DMM instructions
c.SIMD instructions
d.SIM instructions

Ans. c

9. The primary and essential mechanism to support the sparse matrices is

a.Gather-scatter operations
b.Gather operations
c.Scatter operations
d.Gather-scatter technique

Ans. a

10. Which of the following architectures is/are not suitable for realizing SIMD ?

a.Vector Processor
b.Array Processor
c.Von Neumann
d.All of the above
Ans . c

11. Multithreading allowing multiple-threads for sharing the functional units of a
a.Multiple processor
b.Single processor
c.Dual core
d. Corei5

Ans . b

12. Which compiler is used to compile the cude source code:

a.gcc
b.nvc++
c.nc++
d.nvcc

Ans.d

13. which command line is used to execute a cuda program :

a.nvcc hello.cu -o hello
b.nvg++ heloo.cpp -o hello
c.ncc hello.c -o hello
D.g++ hello.cu -o hello

Ans.a

14.The syntax of kernel execution configuration is as follows

a.<<< M , T >>> with a grid of M thread blocks. Each thread block has T parallel blocks
b.<<< M , T >>> with a grid of M blocks. Each thread block has T parallel threads
c.<<< M , T >>> with a grid of M thread blocks. Each thread block has T parallel threads
d.<<< M , T >>> with a grid of M thread blocks. Each thread block has T threads

Ans. c

15.what it contains threadIdx.x

A.contains the index of the thread within the block
b.contains the index of the block within the thread
c.contains the index of the thread size within the block
d.contains the index of the block size within the thread

Ans. A

16.what it contains blockDim.x

a.contains the size of block
b.contains the size of block thread
c.contains the size of thread block (number of threads in the thread block).
d.the size of thread block

Ans. c

17.memory allocation of of variable x and y in cuda:

A.float *b, *a;
cudaMallocManaged(&, N*sizeof(float));
cudaMallocManaged(&, N*sizeof(float));
B.float *x, *y;
cudaMallocManaged(&a, N*sizeof(float));
cudaMallocManaged(&b, N*sizeof(float));
c.float *a, *b;
cudaMallocManaged(&x, N*sizeof(float));
cudaMallocManaged(&y, N*sizeof(float));
d.float *x, *y;
cudaMallocManaged(&x, N*sizeof(float));
cudaMallocManaged(&y, N*sizeof(float));

Ans. d

18.which function is used for free the memory in cuda

a.cudaFree()

b.Free()
c.Cudafree()
d.CudaFree()

Ans. a

19. Which of the following is *not* a form of parallelism supported by CUDA

a.Vector parallelism - Floating point computations are executed in parallel on wide vector units
b.Thread level task parallelism - Different threads execute a different tasks
c.Block and grid level parallelism - Different blocks or grids execute different tasks
d.Data parallelism - Different threads and blocks process different parts of data in memory

Ans . a

20.The style of parallelism supported on GPUs is best described as
a.SISD - Single Instruction Single Data
b.MISD - Multiple Instruction Single Data
c.SIMT - Single Instruction Multiple Thread
d.MIMD - Multiple Instruction Multiple Data

Ans. c

21. Which of the following correctly describes a GPU kernel

a.A kernel may contain a mix of host and GPU code
b.All thread blocks involved in the same computation use the same kernel
c.A kernel is part of the GPU's internal micro-operating system, allowing it to act as in independent host
d.All thread blocks involved in the same computation use the different kernel

Ans .b

22.Shared memory in CUDA is accessible to:

a.All threads in a single block
b.Both the host and GPU
c.All threads associated with a single kernel
d.one thread in a single block

Ans.a

23.Which of the following correctly describes the relationship between Warps, thread blocks, and CUDA cores?

a.A warp is divided into a number of thread blocks, and each thread block executes on a single CUDA core

b.A thread block may be divided into a number of warps, and each warp may execute on a single CUDA core

c.A thread block is assigned to a warp, and each thread in the warp is executed on a separate CUDA core

d. A block index is same as thread index

Ans .b

24. A processor assigned with a thread block, that executes a code ,which we usually call a

A. multithreaded MIMD processor

b. multithreaded SIMD processor

c. multithreaded

D. multicore

Ans. c

25. Thread blocked altogether and being executed in the sets of 32 thread called as

a.block of thread

b.thread block

c.thread

d.block

Ans. b

26.Who developed CUDA :

a. ARM

b. INTEL

c. AMD

d. NVIDIA

Ans. d

Seat No -

Total number of questions : 60

11342_High Performance Computing

Time : 1hr

Max Marks : 50

N.B

1) All questions are Multiple Choice Questions having single correct option.

2) Attempt any 50 questions out of 60.

3) Use of calculator is allowed.

4) Each question carries 1 Mark.

5) Specially abled students are allowed 20 minutes extra for examination.

6) Do not use pencils to darken answer.

7) Use only black/blue ball point pen to darken the appropriate circle.

8) No change will be allowed once the answer is marked on OMR Sheet.

9) Rough work shall not be done on OMR sheet or on question paper.

10) Darken ONLY ONE CIRCLE for each answer.

Q.no 1. MIPS stands for?

A : Mandatory Instructions/sec

B : Millions of Instructions/sec

C : Most of Instructions/sec

D : Many Instructions / sec

Q.no 2. Depth First Search is equivalent to which of the traversal in the Binary Trees?

A : Pre-order Traversal

B : Post-order Traversal

C : Level-order Traversal

D : In-order Traversal

Q.no 3. Regarding implementation of Breadth First Search using queues, what is the maximum distance between two nodes present in the queue? (considering each edge length 1)

A : Can be anything

B : 0

C : At most 1

D : Insufficient Information

Q.no 4. Calling a kernel is typically referred to as _____.

A : kernel thread

B : kernel initialization

C : kernel termination

D : kernel invocation

Q.no 5. The decomposition technique in which the function is used several number of times is called as_____

A : Data Decomposition

B : Recursive Decomposition

C : Speculative Decomposition

D : Exploratory Decomposition

Q.no 6. The decomposition technique in which the input is divided is called as_____

A : Data Decomposition

B : Recursive Decomposition

C : Speculative Decomposition

D : Exploratory Decomposition

Q.no 7. Several instructions execution simultaneously in _____

A : processing

B : parallel processing

C : serial processing

D : multitasking

Q.no 8. Following is not decomposition technique

A : Data Decomposition

B : Recursive Decomposition

C : Serial Decomposition

D : Exploratory Decomposition

Q.no 9. How many Attibutes required to characterize messsage passing paragdigm

A : 2

B : 4

C : 6

D : 8

Q.no 10. Which of the following is not an in-place sorting algorithm?

A : Selection sort

B : Heap sort

C : Quick Sort

D : Merge sort

Q.no 11. The time complexity of heap sort in worst case is

A : O(log n)

B : O(n)

C : O(nlogn)

D : O(n^2)

Q.no 12. Most message-passing programs are written using

A : the single program multiple data (SPMD) model.

B : the multiple program and single data(MPSD) model

C : the single program single data (SPSD) model

D : the Multiple program multiple data (SPMD) model

Q.no 13. Decomposition stands for

A : Dividing Problem statement

B : Dividing no of processors

C : Dividing number of tasks

D : Dividing number of operation

Q.no 14. Message-passing programs are often written using

A : symetric Paradigm

B : asymetric Paradigm

C : asynchronous paradigm

D : synchronous paradigm

Q.no 15. Following is not mapping technique

A : Static Mapping

B : Dynamic Mapping

C : Hybrid Mapping

D : All of Above

Q.no 16. Which of the following is not a stable sorting algorithm?

A : Insertion sort

B : Selection sort

C : Bubble sort

D : Merge sort

Q.no 17. Type of HPC applications of

A : Management

B : Media mass

C : Business

D : Science

Q.no 18. The kernel code is dentified by the _____qualifier with void return type

A : _host_

B : __global__

C : _device_

D : void

Q.no 19. The time complexity of a quick sort algorithm which makes use of median, found by an O(n) algorithm, as pivot element is

A : O(n^2)

B : O(nlogn)

C : O(nlog(log(n))

D : O(n)

Q.no 20. When the Breadth First Search of a graph is unique?

A : When the graph is a Binary Tree

B : When the graph is a Linked List

C : When the graph is a n-ary Tree

D : When the graph is a Ternary Tree

Q.no 21. Which of the following is not an application of Depth First Search?

A : For generating topological sort of a graph

B : For generating Strongly Connected Components of a directed graph

C : Detecting cycles in the graph

D : Peer to Peer Networks

Q.no 22. The logical view of a machine supporting the message-passing paradigm consists of p processes, each with its own _____

A : Partitioned Address space

B : Exclusive address space

C : Logical Adress Space

D : Non shared Adress Space

Q.no 23. Which one of the following is not shared by threads?

A : program counter

B : stack

C : both program counter and stack

D : none of the mentioned

Q.no 24. Which of the following is a stable sorting algorithm?

A : Merge sort

B : Typical in-place quick sort

C : Heap sort

D : Selection sort

Q.no 25. In ..... only one process at a time is allowed into its critical section, among all processes that have critical sections for the same resource.

A : Mutual Exclusion

B : Synchronization

C : Deadlock

D : Starvation

Q.no 26. We have an internet cloud of resources In cloud computing to form

A : Centralized computing

B : Decentralized computing

C : Parallel computing

D : All of Above

Q.no 27. Broader concept offers Cloud computing .to select which of the following.

A : Parallel computing

B : Centralized computing

C : Utility computing

D : Decentralized computing

Q.no 28. Writing parallel programs is referred to as

A : Parallel computation

B : Parallel processes

C : Parallel development

D : Parallel programming

Q.no 29. Network interfaces allow the transfer of messages from buffer memory to desired location without ____ intervention

A : DMA

B : CPU

C : I/O

D : Memory

Q.no 30. Consider the situation in which assignment operation is very costly. Which of the following sorting algorithm should be performed so that the number of assignment operations is minimized in general?

A : Insertion sort

B : Selection sort

C : Bubble sort

D : Merge sort

Q.no 31. A process can be _____

A : single threaded

B : multithreaded

C : both single threaded and multithreaded

D : none of the mentioned

Q.no 32. High performance computing of the computer system tasks are done by

A : node clusters

B : network clusters

C : both a and b

D : Beowulf clusters

Q.no 33. Interprocessor communication that takes place

A : Centralized memory

B : Shared memory

C : Message passing

D : Both A and B

Q.no 34. Which of the following is not a noncomparison sort?

A : Counting sort

B : Bucket sort

C : Radix sort

D : Shell sort

Q.no 35. Parallel computing uses _____ execution

A : sequential

B : unique

C : simultaneous

D : none of the answers is correct

Q.no 36. When the event for which a thread is blocked occurs?

A : thread moves to the ready queue

B : thread remains blocked

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Q.no 37. Which of the following is NOT a characteristic of parallel computing?

A : Breaks a task into pieces

B : Uses a single processor or computer

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Q.no 38. _____ are major issues with non-buffered blocking sends

A : concurrent and mutual exclsion

B : Idling and deadlocks

C : synchronization

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Q.no 39. If the given input array is sorted or nearly sorted, which of the following algorithm gives the best performance?

A : Insertion sort

B : Selection sort

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Q.no 40. Message passing system allows processes to _____

A : communicate with one another without resorting to shared data

B : communicate with one another by resorting to shared data

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Q.no 41. _____ leads to concurrency.

A : Serialization

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Q.no 42. The time required to create a new thread in an existing process is _____

A : greater than the time required to create a new process

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Q.no 43. RMI stands for?

A : Remote Mail InvocationRemote Message Invocation

B : Remaining Method Invention

C : Remaining Method Invocation

D : Remote Method Invocation

Q.no 44. Dynamic networks of networks, is a dynamic connection that grows is called

A : Multithreading

B : Cyber cycle

C : Internet of things

D : None of these

Q.no 45. If one thread opens a file with read privileges then _____

A : other threads in the another process can also read from that file

B : other threads in the same process can also read from that file

C : any other thread can not read from that file

D : all of the mentioned

Q.no 46. the basic operations in the message-passing programming paradigm are ___

A : initiate and listen

B : wait and acknoweldge

C : request and reply

D : send and receive

Q.no 47. What is Inter process communication?

A : allows processes to communicate and synchronize their actions when using the same address space

B : allows processes to communicate and synchronize their actions without using the same address space

C : allows the processes to only synchronize their actions without communication

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Q.no 48. Which of the ceramic components are easier through nano structuring?

A : Lubrication

B : Coating

C : Fabrication

D : Wear

Q.no 49. Execution of several activities at the same time.

A : multi processing

B : parallel processing

C : serial processing

D : multitasking

Q.no 50. It is _____ speed and _____ latency.

A : High, high

B : Low, low

C : High, low

D : Low, high

Q.no 51. Process synchronization of programs is done by

A : input

B : output

C : operating system

D : memory

Q.no 52. The management of data flow between computers or devices or between nodes in a network is called

A : Flow control

B : Data Control

C : Data Management

D : Flow Management

Q.no 53. Which of the following are TRUE for direct communication?

A : A communication link can be associated with N number of process(N = max. number of processes supported by system)

B : A communication link can be associated with exactly two processes

C : Exactly N/2 links exist between each pair of processes(N = max. number of processes supported by system)

D : Exactly two link exists between each pair of processes

Q.no 54. Thread synchronization is required because _____

A : all threads of a process share the same address space

B : all threads of a process share the same global variables

C : all threads of a process can share the same files

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Q.no 55. Which of the following two operations are provided by the IPC facility?

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Q.no 57. Which of the following algorithms has lowest worst case time complexity?

A : Insertion sort

B : Selection sort

C : Quick Sort

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Q.no 58. A thread shares its resources(like data section, code section, open files, signals) with _____

A : other process similar to the one that the thread belongs to

B : other threads that belong to similar processes

C : other threads that belong to the same process

D : all of the mentioned

Q.no 59. The parallelism achieved on the basis of conditions is called as

A : Instruction level

B : Thread level

C : Transaction level

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Q.no 60. The register context and stacks of a thread are deallocated when the thread?

A : terminates

B : blocks

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Answer for Question No 25. is a

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Answer for Question No 27. is c

Answer for Question No 28. is d

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Answer for Question No 31. is c

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11342_High Performance Computing

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A : Management

B : Media mass

C : Business

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C : serial processing

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C : share data

D : name the recipient or sender of the message

Q.no 29. Network interfaces allow the transfer of messages from buffer memory to desired location without ____ intervention

A : DMA

B : CPU

C : I/O

D : Memory

Q.no 30. Interprocessor communication that takes place

A : Centralized memory

B : Shared memory

C : Message passing

D : Both A and B

Q.no 31. Nanoscience can be studied with the help of _____

A : Quantum mechanics

B : Newtonian mechanics

C : Macro-dynamic

D : Geophysics

Q.no 32. The network topology used for interconnection network.

A : Bus based

B : Mesh

C : Linear Array

D : All of above

Q.no 33. The time required to create a new thread in an existing process is _____

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B : Parallelism

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Q.no 36. Dynamic networks of networks, is a dynamic connection that grows is called

A : Multithreading

B : Cyber cycle

C : Internet of things

D : None of these

Q.no 37. Running merge sort on an array of size n which is already sorted is

A : O(n)

B : O(nlogn)

C : O(n^2)

D : O(log n)

Q.no 38. Broader concept offers Cloud computing .to select which of the following.

A : Parallel computing

B : Centralized computing

C : Utility computing

D : Decentralized computing

Q.no 39. Which of the ceramic components are easier through nano structuring?

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B : Coating

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Q.no 44. Writing parallel programs is referred to as

A : Parallel computation

B : Parallel processes

C : Parallel development

D : Parallel programming

Q.no 45. High performance computing of the computer system tasks are done by

A : node clusters

B : network clusters

C : both a and b

D : Beowulf clusters

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Q.no 47. Consider the situation in which assignment operation is very costly. Which of the following sorting algorithm should be performed so that the number of assignment operations is minimized in general?

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B : Idling and deadlocks

C : synchronization

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B : Decentralized computing

C : Parallel computing

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A : Insertion sort

B : Selection sort

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Q.no 51. The link between two processes P and Q to send and receive messages is called _____

A : communication link

B : message-passing link

C : synchronization link

D : all of the mentioned

Q.no 52. Dynamic networks is a dynamic connection that grows is called

A : Multithreading

B : Cyber cycle

C : Internet of things

D : Cyber-physical system

Q.no 53. The amount of data that can be carried from one point to another in a given time period is called

A : Scope

B : Capacity

C : Bandwidth

D : Limitation

Q.no 54. Octa-core processor are the processors of the computer system that contains

A : 2 processors

B : 4 processors

C : 6 processors

D : 8 processors

Q.no 55. Given a number of elements in the range [0….n^3]. which of the following sorting algorithms can sort them in O(n) time?

A : Counting sort

B : Bucket sort

C : Radix sort

D : Quick sort

Q.no 56. Termination of the process terminates _____

A : first thread of the process

B : first two threads of the process

C : all threads within the process

D : no thread within the process

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11342_High Performance Computing

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A : High, high

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Q.no 51. Which of the following is not the possible ways of data exchange?

A : Simplex

B : Multiplex

C : Half-duplex

D : Full-duplex

Q.no 52. A thread shares its resources(like data section, code section, open files, signals) with _____

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B : other threads that belong to similar processes

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A : cost

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A : input

B : output

C : operating system

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A : Light Weight Process(LWP)

B : Heavy Weight Process(HWP)

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11342_High Performance Computing

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A : A communication link can be associated with N number of process(N = max. number of processes supported by system)

B : A communication link can be associated with exactly two processes

C : Exactly N/2 links exist between each pair of processes(N = max. number of processes supported by system)

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Q.no 60. In indirect communication between processes P and Q _____

A : a) there is another process R to handle and pass on the messages between P and Q

B : there is another machine between the two processes to help communication

C : there is a mailbox to help communication between P and Q

D : none of the mentioned

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Q.no 49. The time required to create a new thread in an existing process is _____

A : greater than the time required to create a new process

B : less than the time required to create a new process

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Q.no 50. Network interfaces allow the transfer of messages from buffer memory to desired location without ____ intervention

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Q.no 51. Thread synchronization is required because _____

A : all threads of a process share the same address space

B : all threads of a process share the same global variables

C : all threads of a process can share the same files

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Q.no 52. Which of the following are TRUE for direct communication?

A : A communication link can be associated with N number of process(N = max. number of processes supported by system)

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Q.no 53. Resources and clients transparency that allows movement within a system is called

A : Mobility transparency

B : Concurrency transparency

C : Performance transparency

D : Replication transparency

Q.no 54. In indirect communication between processes P and Q _____

A : a) there is another process R to handle and pass on the messages between P and Q

B : there is another machine between the two processes to help communication

C : there is a mailbox to help communication between P and Q

D : none of the mentioned

Q.no 55. The architecture which can compute several tasks simultaneously at processor level itself is called as:

A : Multi core architecture

B : Multi processor architecture

C : Multi threaded architecture

D : All of above

Q.no 56. The amount of data that can be carried from one point to another in a given time period is called

A : Scope

B : Capacity

C : Bandwidth

D : Limitation

Q.no 57. Process synchronization of programs is done by

A : input

B : output

C : operating system

D : memory

Q.no 58. NVIDIA thought that 'unifying theme' of every forms of parallelism is the

A : CDA thread

B : PTA thread

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Q.no 59. The transparency that enables accessing local and remote resources using identical operations is called _____

A : Access transparency

B : Concurrency transparency

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D : Scaling transparency

Q.no 60. Termination of the process terminates _____

A : first thread of the process

B : first two threads of the process

C : all threads within the process

D : no thread within the process

Answer for Question No 1. is a

Answer for Question No 2. is d

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Answer for Question No 38. is c

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Answer for Question No 41. is b

Answer for Question No 42. is a

Answer for Question No 43. is a

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11342_High Performance Computing

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Q.no 6. When the Breadth First Search of a graph is unique?

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B : When the graph is a Linked List

C : When the graph is a n-ary Tree

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Q.no 7. The decomposition technique in which the function is used several number of times is called as_____

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C : both program counter and stack

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B : Media mass

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B : Newtonian mechanics

C : Macro-dynamic

D : Geophysics

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B : Coating

C : Fabrication

D : Wear

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B : other threads that belong to similar processes

C : other threads that belong to the same process

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A : input

B : output

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D : memory

Q.no 58. The management of data flow between computers or devices or between nodes in a network is called

A : Flow control

B : Data Control

C : Data Management

D : Flow Management

Q.no 59. A thread is also called _____

A : Light Weight Process(LWP)

B : Heavy Weight Process(HWP)

C : Process

D : None of the mentioned

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B : Thread level

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B : Mesh

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Q.no 54. A thread shares its resources(like data section, code section, open files, signals) with _____

A : other process similar to the one that the thread belongs to

B : other threads that belong to similar processes

C : other threads that belong to the same process

D : all of the mentioned

Q.no 55. NVIDIA thought that 'unifying theme' of every forms of parallelism is the

A : CDA thread

B : PTA thread

C : CUDA thread

D : CUD thread

Q.no 56. Termination of the process terminates _____

A : first thread of the process

B : first two threads of the process

C : all threads within the process

D : no thread within the process

Q.no 57. Given a number of elements in the range [0….n^3]. which of the following sorting algorithms can sort them in O(n) time?

A : Counting sort

B : Bucket sort

C : Radix sort

D : Quick sort

Q.no 58. Which of the following two operations are provided by the IPC facility?

A : write & delete message

B : delete & receive message

C : send & delete message

D : receive & send message

Q.no 59. In indirect communication between processes P and Q _____

A : a) there is another process R to handle and pass on the messages between P and Q

B : there is another machine between the two processes to help communication

C : there is a mailbox to help communication between P and Q

D : none of the mentioned

Q.no 60. Octa-core processor are the processors of the computer system that contains

A : 2 processors

B : 4 processors

C : 6 processors

D : 8 processors

Answer for Question No 1. is a

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Answer for Question No 27. is c

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Answer for Question No 47. is c

Answer for Question No 48. is b

Answer for Question No 49. is d

Answer for Question No 50. is d

Answer for Question No 51. is a

Answer for Question No 52. is c

Answer for Question No 53. is d

Answer for Question No 54. is c

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11342_High Performance Computing

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B : Media mass

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D : Science

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B : Recursive Decomposition

C : Serial Decomposition

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B : Remaining Method Invention

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B : Newtonian mechanics

C : Macro-dynamic

D : Geophysics

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B : Low, low

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B : multithreaded

C : both single threaded and multithreaded

D : none of the mentioned

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D : Wear

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A : Centralized computing

B : Decentralized computing

C : Parallel computing

D : All of Above

Q.no 33. What is Inter process communication?

A : allows processes to communicate and synchronize their actions when using the same address space

B : allows processes to communicate and synchronize their actions without using the same address space

C : allows the processes to only synchronize their actions without communication

D : none of the mentioned

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B : θ (nlogn)

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A : communicate with one another without resorting to shared data

B : communicate with one another by resorting to shared data

C : share data

D : name the recipient or sender of the message

Q.no 37. _____ leads to concurrency.

A : Serialization

B : Parallelism

C : Serial processing

D : Distribution

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A : node clusters

B : network clusters

C : both a and b

D : Beowulf clusters

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B : Idling and deadlocks

C : synchronization

D : scheduling

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A : sequential

B : unique

C : simultaneous

D : none of the answers is correct

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A : Parallel computation

B : Parallel processes

C : Parallel development

D : Parallel programming

Q.no 46. Which of the following is NOT a characteristic of parallel computing?

A : Breaks a task into pieces

B : Uses a single processor or computer

C : Simultaneous execution

D : May use networking

Q.no 47. Interprocessor communication that takes place

A : Centralized memory

B : Shared memory

C : Message passing

D : Both A and B

Q.no 48. Running merge sort on an array of size n which is already sorted is

A : O(n)

B : O(nlogn)

C : O(n^2)

D : O(log n)

Q.no 49. Which of the following is not a noncomparison sort?

A : Counting sort

B : Bucket sort

C : Radix sort

D : Shell sort

Q.no 50. The time required to create a new thread in an existing process is _____

A : greater than the time required to create a new process

B : less than the time required to create a new process

C : equal to the time required to create a new process

D : none of the mentioned

Q.no 51. Multi-processor systems of the computer system has advantage of

A : cost

B : reliability

C : uncertainty

D : scalability

Q.no 52. The parallelism achieved on the basis of operations is called as

A : Instruction level

B : Thread level

C : Transaction level

D : None of Above

Q.no 53. Process synchronization of programs is done by

A : input

B : output

C : operating system

D : memory

Q.no 54. Octa-core processor are the processors of the computer system that contains

A : 2 processors

B : 4 processors

C : 6 processors

D : 8 processors

Q.no 55. Thread synchronization is required because _____

A : all threads of a process share the same address space

B : all threads of a process share the same global variables

C : all threads of a process can share the same files

D : all of the mentioned

Q.no 56. Data access and storage are elements of Job throughput, of _____.

A : Flexibility

B : Adaptation

C : Efficiency

D : Dependability

Q.no 57. Messages sent by a process _____

A : have to be of a fixed size

B : have to be a variable size

C : can be fixed or variable sized

D : None of the mentioned

Q.no 58. The link between two processes P and Q to send and receive messages is called _____

A : communication link

B : message-passing link

C : synchronization link

D : all of the mentioned

Q.no 59. Which of the following algorithms has lowest worst case time complexity?

A : Insertion sort

B : Selection sort

C : Quick Sort

D : Heap sort

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A : terminates

B : blocks

C : unblocks

D : spawns

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11342_High Performance Computing

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B : Typical in-place quick sort

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C : Utility computing

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B : Parallelism

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A : initiate and listen

B : wait and acknoweldge

C : request and reply

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B : Heavy Weight Process(HWP)

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C : uncertainty

D : scalability

Answer for Question No 1. is c

Answer for Question No 2. is c

Answer for Question No 3. is c

Answer for Question No 4. is b

Answer for Question No 5. is b

Answer for Question No 6. is a

Answer for Question No 7. is c

Answer for Question No 8. is d

Answer for Question No 9. is a

Answer for Question No 10. is b

Answer for Question No 11. is a

Answer for Question No 12. is c

Answer for Question No 13. is b

Answer for Question No 14. is b

Answer for Question No 15. is a

Answer for Question No 16. is a

Answer for Question No 17. is a

Answer for Question No 18. is d

Answer for Question No 19. is b

Answer for Question No 20. is b

Answer for Question No 21. is d

Answer for Question No 22. is d

Answer for Question No 23. is d

Answer for Question No 24. is b

Answer for Question No 25. is d

Answer for Question No 26. is a

Answer for Question No 27. is c

Answer for Question No 28. is c

Answer for Question No 29. is b

Answer for Question No 30. is d

Answer for Question No 31. is c

Answer for Question No 32. is b

Answer for Question No 33. is d

Answer for Question No 34. is a

Answer for Question No 35. is d

Answer for Question No 36. is b

Answer for Question No 37. is b

Answer for Question No 38. is c

Answer for Question No 39. is d

Answer for Question No 40. is b

Answer for Question No 41. is a

Answer for Question No 42. is a

Answer for Question No 43. is b

Answer for Question No 44. is d

Answer for Question No 45. is a

Answer for Question No 46. is d

Answer for Question No 47. is b

Answer for Question No 48. is c

Answer for Question No 49. is b

Answer for Question No 50. is b

Answer for Question No 51. is a

Answer for Question No 52. is c

Answer for Question No 53. is c

Answer for Question No 54. is a

Answer for Question No 55. is d

Answer for Question No 56. is c

Answer for Question No 57. is b

Answer for Question No 58. is a

Answer for Question No 59. is c

Answer for Question No 60. is b

Seat No -

Total number of questions : 60

11342_High Performance Computing

Time : 1hr

Max Marks : 50

N.B

1) All questions are Multiple Choice Questions having single correct option.

2) Attempt any 50 questions out of 60.

3) Use of calculator is allowed.

4) Each question carries 1 Mark.

5) Specially abled students are allowed 20 minutes extra for examination.

6) Do not use pencils to darken answer.

7) Use only black/blue ball point pen to darken the appropriate circle.

8) No change will be allowed once the answer is marked on OMR Sheet.

9) Rough work shall not be done on OMR sheet or on question paper.

10) Darken ONLY ONE CIRCLE for each answer.

Q.no 1. MIPS stands for?

A : Mandatory Instructions/sec

B : Millions of Instructions/sec

C : Most of Instructions/sec

D : Many Instructions / sec

Q.no 2. In ..... only one process at a time is allowed into its critical section, among all processes that have critical sections for the same resource.

A : Mutual Exclusion

B : Synchronization

C : Deadlock

D : Starvation

Q.no 3. Which of the following is not an application of Breadth First Search?

A : Finding shortest path between two nodes

B : Finding bipartiteness of a graph

C : GPS navigation system

D : Path Finding

Q.no 4. Regarding implementation of Breadth First Search using queues, what is the maximum distance between two nodes present in the queue? (considering each edge length 1)

A : Can be anything

B : 0

C : At most 1

D : Insufficient Information

Q.no 5. The decomposition technique in which the input is divided is called as_____

A : Data Decomposition

B : Recursive Decomposition

C : Speculative Decomposition

D : Exploratory Decomposition

Q.no 6. Which of the following is a stable sorting algorithm?

A : Merge sort

B : Typical in-place quick sort

C : Heap sort

D : Selection sort

Q.no 7. Which one of the following is not shared by threads?

A : program counter

B : stack

C : both program counter and stack

D : none of the mentioned

Q.no 8. Several instructions execution simultaneously in _____

A : processing

B : parallel processing

C : serial processing

D : multitasking

Q.no 9. When the Breadth First Search of a graph is unique?

A : When the graph is a Binary Tree

B : When the graph is a Linked List

C : When the graph is a n-ary Tree

D : When the graph is a Ternary Tree

Q.no 10. Message-passing programs are often written using

A : symetric Paradigm

B : asymetric Paradigm

C : asynchronous paradigm

D : synchronous paradigm

Q.no 11. How many Attibutes required to characterize messsage passing paragdigm

A : 2

B : 4

C : 6

D : 8

Q.no 12. Following is not mapping technique

A : Static Mapping

B : Dynamic Mapping

C : Hybrid Mapping

D : All of Above

Q.no 13. The time complexity of a quick sort algorithm which makes use of median, found by an O(n) algorithm, as pivot element is

A : O(n^2)

B : O(nlogn)

C : O(nlog(log(n))

D : O(n)

Q.no 14. Following is not decomposition technique

A : Data Decomposition

B : Recursive Decomposition

C : Serial Decomposition

D : Exploratory Decomposition

Q.no 15. Most message-passing programs are written using

A : the single program multiple data (SPMD) model.

B : the multiple program and single data(MPSD) model

C : the single program single data (SPSD) model

D : the Multiple program multiple data (SPMD) model

Q.no 16. The logical view of a machine supporting the message-passing paradigm consists of p processes, each with its own _____

A : Partitioned Address space

B : Exclusive address space

C : Logical Adress Space

D : Non shared Adress Space

Q.no 17. The time complexity of heap sort in worst case is

A : O(log n)

B : O(n)

C : O(nlogn)

D : O(n^2)

Q.no 18. Decomposition stands for

A : Dividing Problem statement

B : Dividing no of processors

C : Dividing number of tasks

D : Dividing number of operation

Q.no 19. Type of HPC applications of

A : Management

B : Media mass

C : Business

D : Science

Q.no 20. The kernel code is dentified by the _____qualifier with void return type

A : _host_

B : __global__

C : _device_

D : void

Q.no 21. Which of the following is not a stable sorting algorithm?

A : Insertion sort

B : Selection sort

C : Bubble sort

D : Merge sort

Q.no 22. Which of the following is not an application of Depth First Search?

A : For generating topological sort of a graph

B : For generating Strongly Connected Components of a directed graph

C : Detecting cycles in the graph

D : Peer to Peer Networks

Q.no 23. Calling a kernel is typically referred to as _____.

A : kernel thread

B : kernel initialization

C : kernel termination

D : kernel invocation

Q.no 24. Which of the following is not an in-place sorting algorithm?

A : Selection sort

B : Heap sort

C : Quick Sort

D : Merge sort

Q.no 25. Depth First Search is equivalent to which of the traversal in the Binary Trees?

A : Pre-order Traversal

B : Post-order Traversal

C : Level-order Traversal

D : In-order Traversal

Q.no 26. Broader concept offers Cloud computing .to select which of the following.

A : Parallel computing

B : Centralized computing

C : Utility computing

D : Decentralized computing

Q.no 27. RMI stands for?

A : Remote Mail InvocationRemote Message Invocation

B : Remaining Method Invention

C : Remaining Method Invocation

D : Remote Method Invocation

Q.no 28. Dynamic networks of networks, is a dynamic connection that grows is called

A : Multithreading

B : Cyber cycle

C : Internet of things

D : None of these

Q.no 29. the basic operations in the message-passing programming paradigm are ___

A : initiate and listen

B : wait and acknoweldge

C : request and reply

D : send and receive

Q.no 30. Which of the following is NOT a characteristic of parallel computing?

A : Breaks a task into pieces

B : Uses a single processor or computer

C : Simultaneous execution

D : May use networking

Q.no 31. Parallel computing uses _____ execution

A : sequential

B : unique

C : simultaneous

D : none of the answers is correct

Q.no 32. A process can be _____

A : single threaded

B : multithreaded

C : both single threaded and multithreaded

D : none of the mentioned

Q.no 33. Network interfaces allow the transfer of messages from buffer memory to desired location without ____ intervention

A : DMA

B : CPU

C : I/O

D : Memory

Q.no 34. High performance computing of the computer system tasks are done by

A : node clusters

B : network clusters

C : both a and b

D : Beowulf clusters

Q.no 35. Message passing system allows processes to _____

A : communicate with one another without resorting to shared data

B : communicate with one another by resorting to shared data

C : share data

D : name the recipient or sender of the message

Q.no 36. The time required to create a new thread in an existing process is _____

A : greater than the time required to create a new process

B : less than the time required to create a new process

C : equal to the time required to create a new process

D : none of the mentioned

Q.no 37. It is _____ speed and _____ latency.

A : High, high

B : Low, low

C : High, low

D : Low, high

Q.no 38. Which of the ceramic components are easier through nano structuring?

A : Lubrication

B : Coating

C : Fabrication

D : Wear

Q.no 39. _____ are major issues with non-buffered blocking sends

A : concurrent and mutual exclsion

B : Idling and deadlocks

C : synchronization

D : scheduling

Q.no 40. Time complexity of bubble sort in best case is

A : θ (n)

B : θ (nlogn)

C : θ (n^2)

D : θ (n(logn)^2)

Q.no 41. When the event for which a thread is blocked occurs?

A : thread moves to the ready queue

B : thread remains blocked

C : thread completes

D : a new thread is provided

Q.no 42. If the given input array is sorted or nearly sorted, which of the following algorithm gives the best performance?

A : Insertion sort

B : Selection sort

C : Bubble sort

D : Merge sort

Q.no 43. If one thread opens a file with read privileges then _____

A : other threads in the another process can also read from that file

B : other threads in the same process can also read from that file

C : any other thread can not read from that file

D : all of the mentioned

Q.no 44. The network topology used for interconnection network.

A : Bus based

B : Mesh

C : Linear Array

D : All of above

Q.no 45. Execution of several activities at the same time.

A : multi processing

B : parallel processing

C : serial processing

D : multitasking

Q.no 46. What is Inter process communication?

A : allows processes to communicate and synchronize their actions when using the same address space

B : allows processes to communicate and synchronize their actions without using the same address space

C : allows the processes to only synchronize their actions without communication

D : none of the mentioned

Q.no 47. Which of the following is not a noncomparison sort?

A : Counting sort

B : Bucket sort

C : Radix sort

D : Shell sort

Q.no 48. Running merge sort on an array of size n which is already sorted is

A : O(n)

B : O(nlogn)

C : O(n^2)

D : O(log n)

Q.no 49. Writing parallel programs is referred to as

A : Parallel computation

B : Parallel processes

C : Parallel development

D : Parallel programming

Q.no 50. Nanoscience can be studied with the help of _____

A : Quantum mechanics

B : Newtonian mechanics

C : Macro-dynamic

D : Geophysics

Q.no 51. Given a number of elements in the range [0….n^3]. which of the following sorting algorithms can sort them in O(n) time?

A : Counting sort

B : Bucket sort

C : Radix sort

D : Quick sort

Q.no 52. Thread synchronization is required because _____

A : all threads of a process share the same address space

B : all threads of a process share the same global variables

C : all threads of a process can share the same files

D : all of the mentioned

Q.no 53. In indirect communication between processes P and Q _____

A : a) there is another process R to handle and pass on the messages between P and Q

B : there is another machine between the two processes to help communication

C : there is a mailbox to help communication between P and Q

D : none of the mentioned

Q.no 54. Which of the following is not the possible ways of data exchange?

A : Simplex

B : Multiplex

C : Half-duplex

D : Full-duplex

Q.no 55. The link between two processes P and Q to send and receive messages is called _____

A : communication link

B : message-passing link

C : synchronization link

D : all of the mentioned

Q.no 56. Octa-core processor are the processors of the computer system that contains

A : 2 processors

B : 4 processors

C : 6 processors

D : 8 processors

Q.no 57. Multi-processor systems of the computer system has advantage of

A : cost

B : reliability

C : uncertainty

D : scalability

Q.no 58. Termination of the process terminates _____

A : first thread of the process

B : first two threads of the process

C : all threads within the process

D : no thread within the process

Q.no 59. The transparency that enables accessing local and remote resources using identical operations is called _____

A : Access transparency

B : Concurrency transparency

C : Performance transparency

D : Scaling transparency

Q.no 60. NVIDIA thought that 'unifying theme' of every forms of parallelism is the

A : CDA thread

B : PTA thread

C : CUDA thread

D : CUD thread

Answer for Question No 1. is b

Answer for Question No 2. is a

Answer for Question No 3. is d

Answer for Question No 4. is c

Answer for Question No 5. is a

Answer for Question No 6. is a

Answer for Question No 7. is c

Answer for Question No 8. is b

Answer for Question No 9. is b

Answer for Question No 10. is c

Answer for Question No 11. is a

Answer for Question No 12. is d

Answer for Question No 13. is b

Answer for Question No 14. is c

Answer for Question No 15. is c

Answer for Question No 16. is b

Answer for Question No 17. is c

Answer for Question No 18. is a

Answer for Question No 19. is d

Answer for Question No 20. is b

Answer for Question No 21. is b

Answer for Question No 22. is d

Answer for Question No 23. is d

Answer for Question No 24. is d

Answer for Question No 25. is a

Answer for Question No 26. is c

Answer for Question No 27. is d

Answer for Question No 28. is c

Answer for Question No 29. is d

Answer for Question No 30. is a

Answer for Question No 31. is c

Answer for Question No 32. is c

Answer for Question No 33. is b

Answer for Question No 34. is d

Answer for Question No 35. is a

Answer for Question No 36. is b

Answer for Question No 37. is c

Answer for Question No 38. is c

Answer for Question No 39. is b

Answer for Question No 40. is a

Answer for Question No 41. is a

Answer for Question No 42. is b

Answer for Question No 43. is b

Answer for Question No 44. is d

Answer for Question No 45. is b

Answer for Question No 46. is b

Answer for Question No 47. is d

Answer for Question No 48. is b

Answer for Question No 49. is d

Answer for Question No 50. is a

Answer for Question No 51. is c

Answer for Question No 52. is d

Answer for Question No 53. is c

Answer for Question No 54. is b

Answer for Question No 55. is a

Answer for Question No 56. is d

Answer for Question No 57. is b

Answer for Question No 58. is c

Answer for Question No 59. is a

Answer for Question No 60. is c