

LAB4

VIRTUOSO

Outline

1. Virtuoso setup
2. Create Library
3. Schematic
4. Run Spectre simulation

1. Virtuoso setup

Step 1: Create and change directory to "*layout_env*" folder. In this Lab 4, we will work at this place:

```
%> cd /home/cc??group??/vlsi/${Student_ID}/work/layout_env
```

Step 2: Copy Sample Environment Kit from Cadence to each of your synthesis working folder

```
%> cp -rf /home/share_file/cadence/pdk/ pdk
```

1. Virtuoso setup

Step 3: Get license and start virtuoso with a executable file:

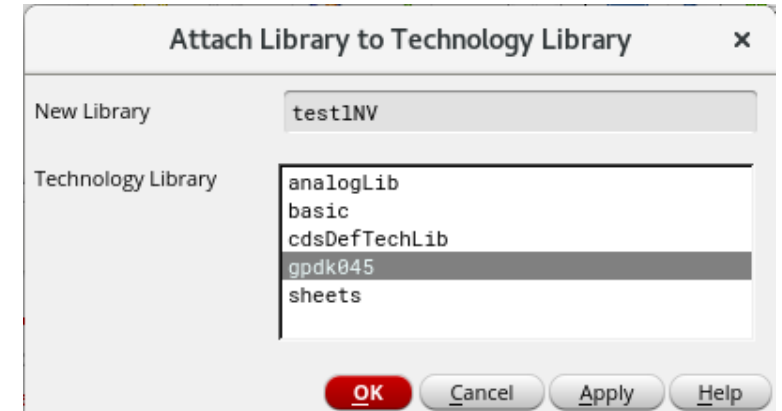
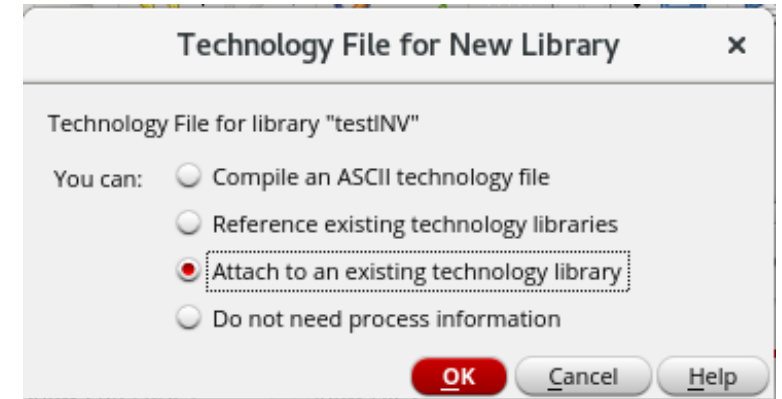
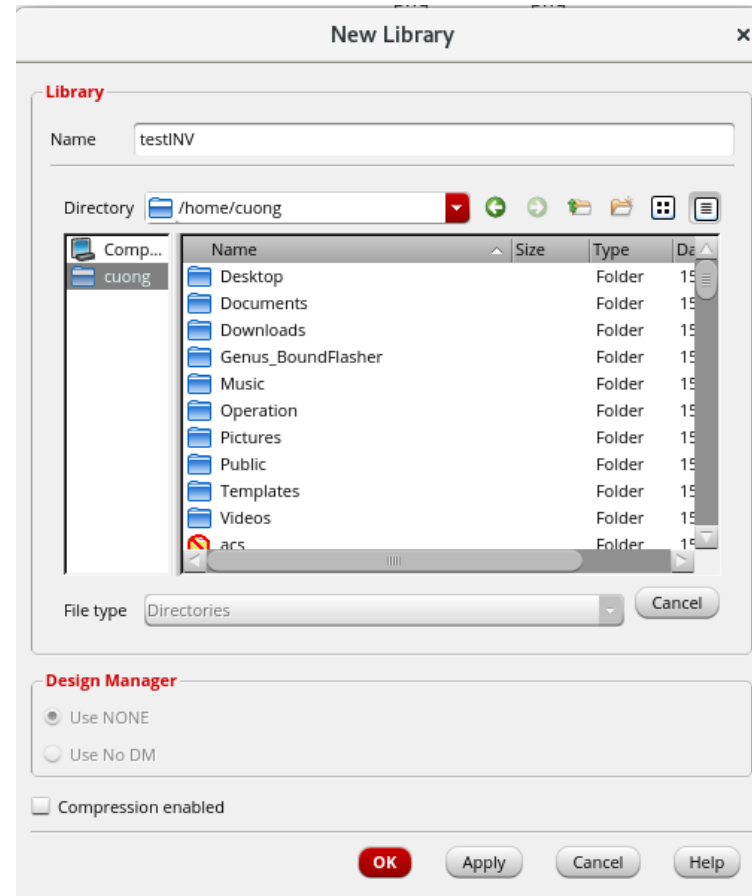
Create a file called "go_vir" with the content as follows:

```
#!/bin/bash -f  
  
cd pdk/gpdk045_v_6_0/  
cd /home/share_file/cadence/  
source add_path  
source add_license  
cd -  
  
virtuoso &
```

2. Create Library

Step 1: Open **Tools** → **Library Manager**

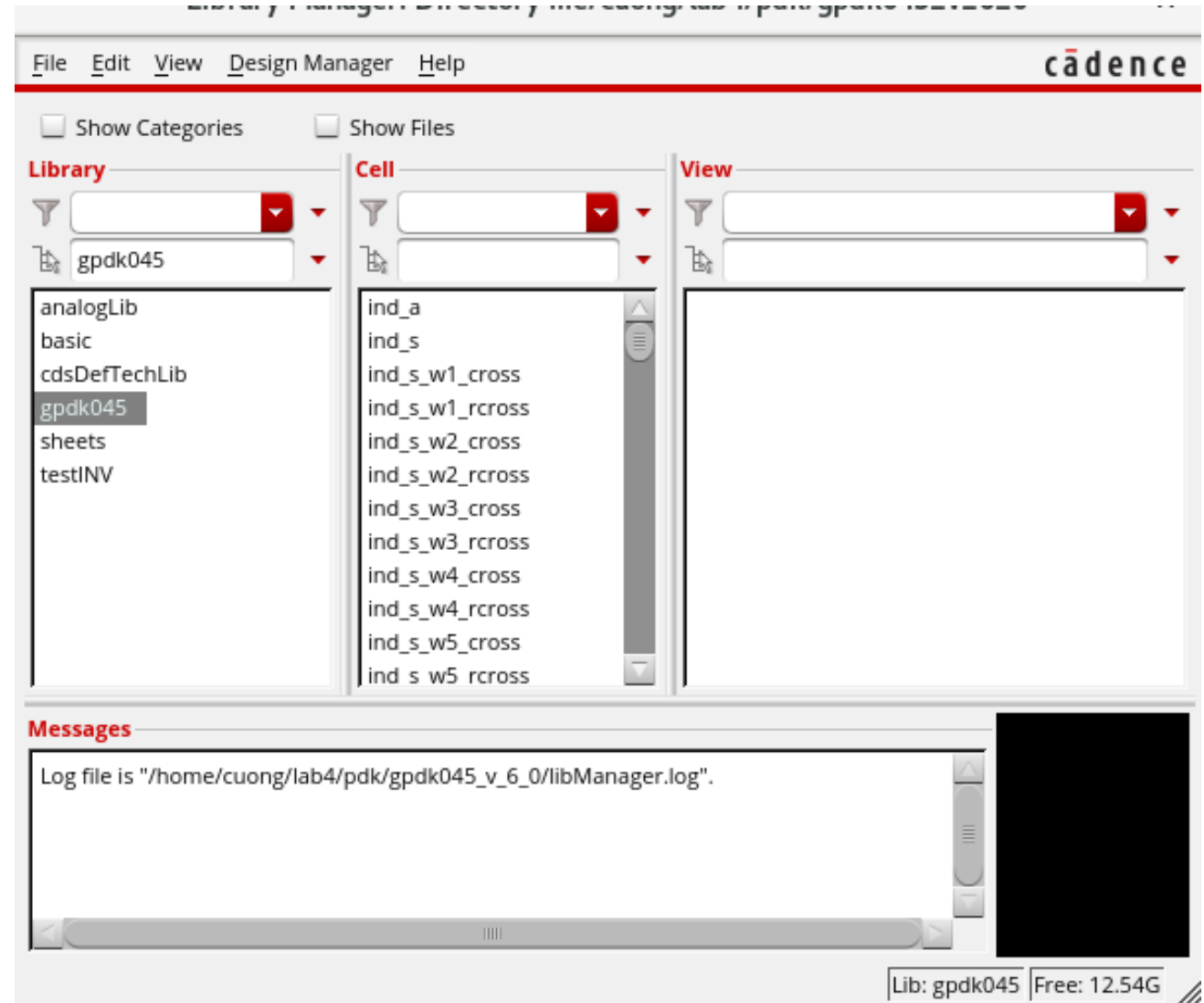
Step 2: Select **File** → **New** → **Library** and enter a name for the library



2. Create Library

Step 3: Tools → Library Manager...

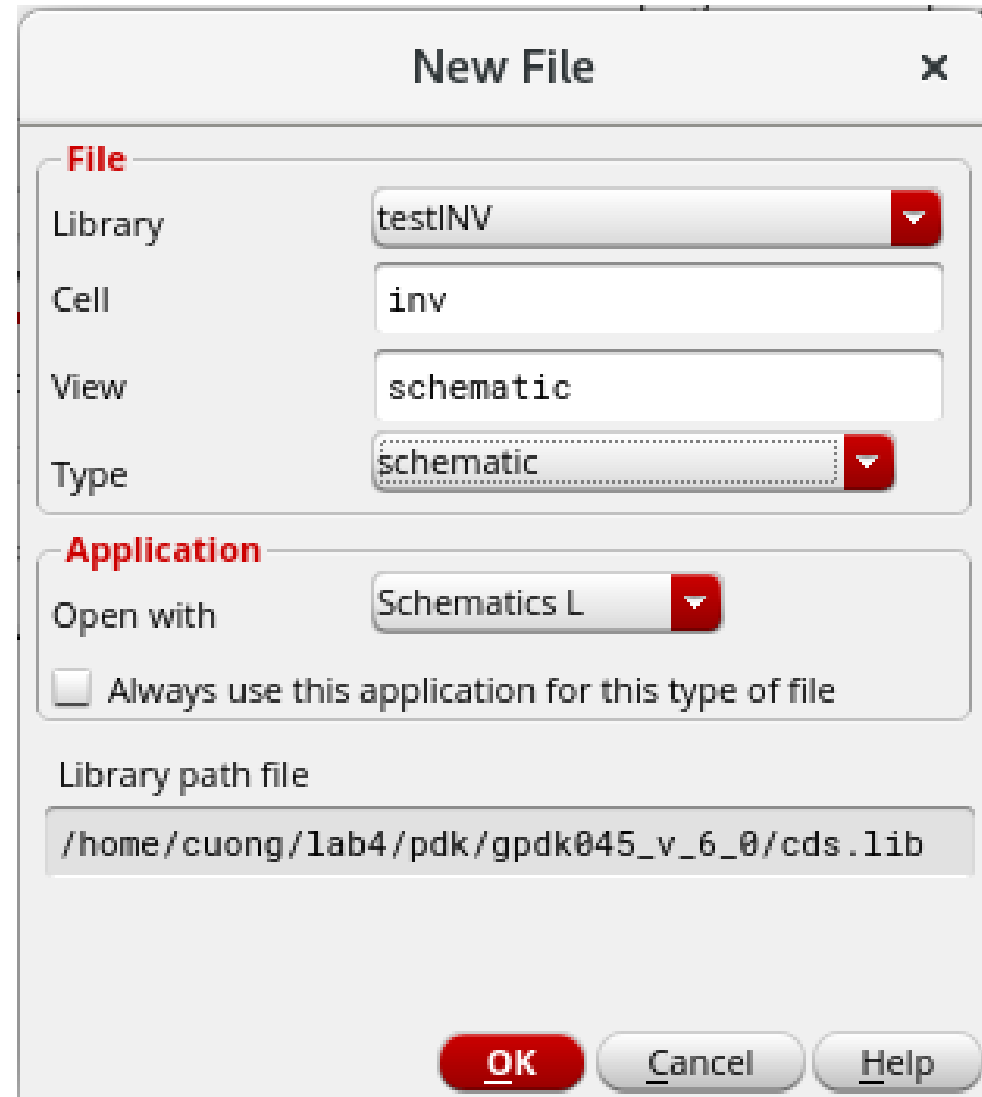
Here you can find all your libraries as well as the built-in libraries and their contents.



3. Schematic

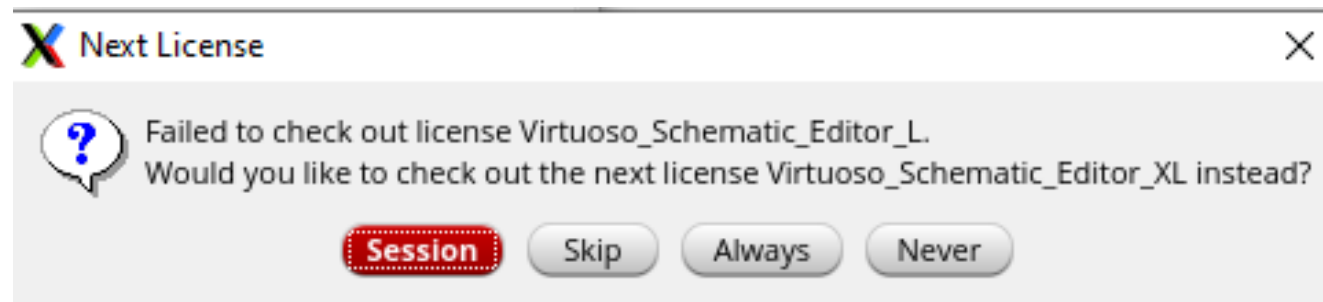
Step 1: Create a cell view:
Select **File** → **New** → **Cell View**

Name the cell “inv” and click OK.



3. Schematic

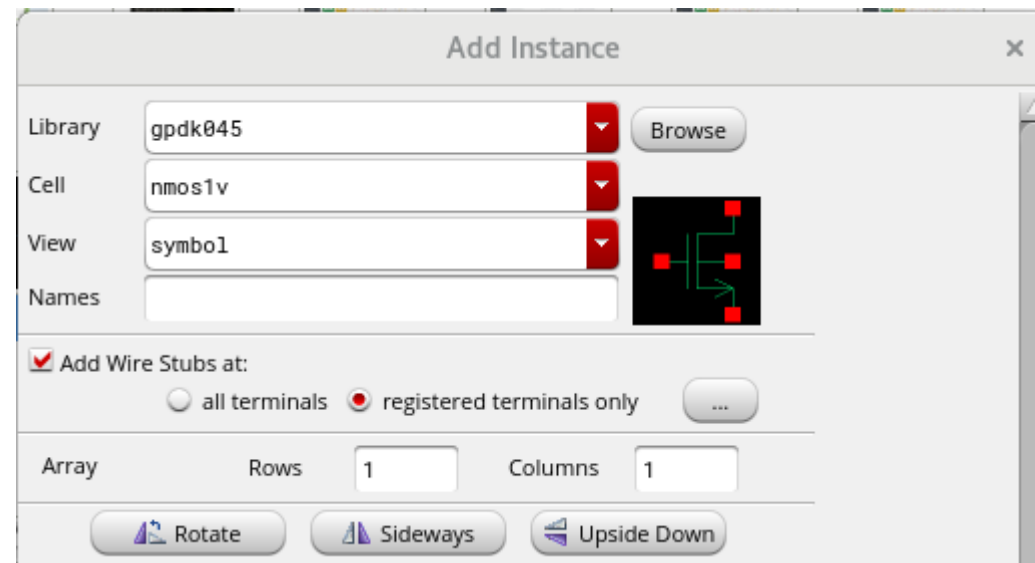
Step 1: If this pop up appears, choose **Always**



3. Schematic

Step 2: Draw a schematic:

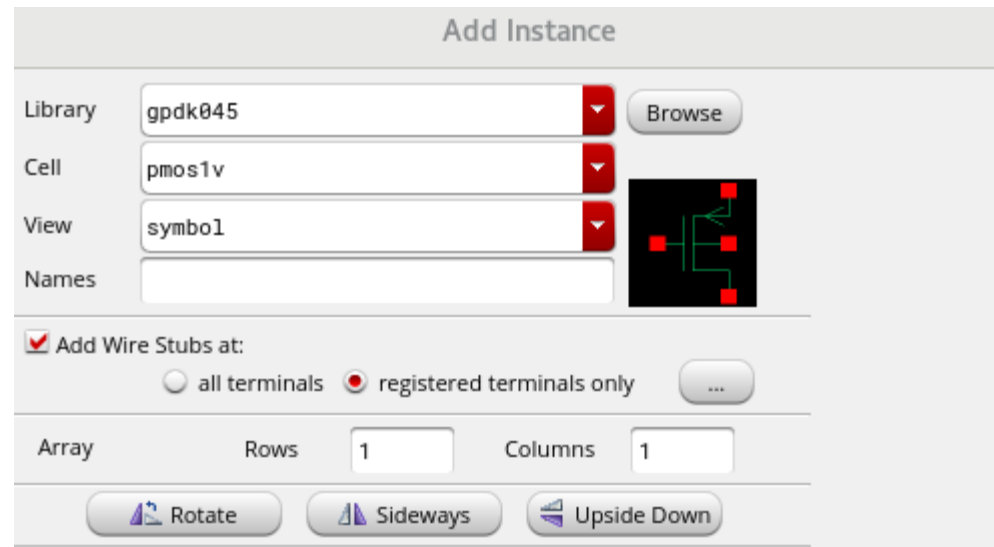
1. select **Create** → **Instance (I)** and choose the NMOS transistor



3. Schematic

Step 2: Draw a schematic:

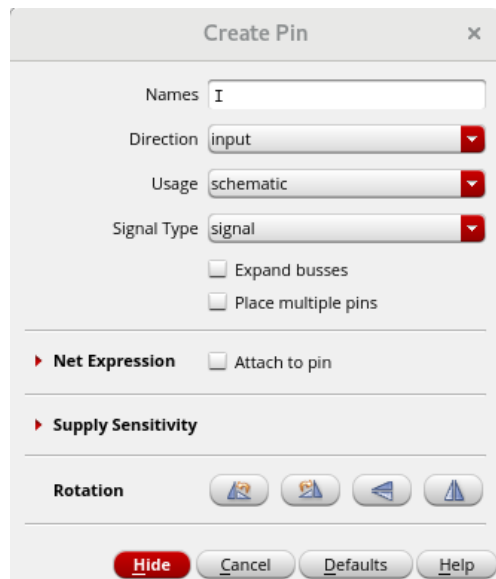
2. select **Create → Instance (I)** and choose the PMOS transistor



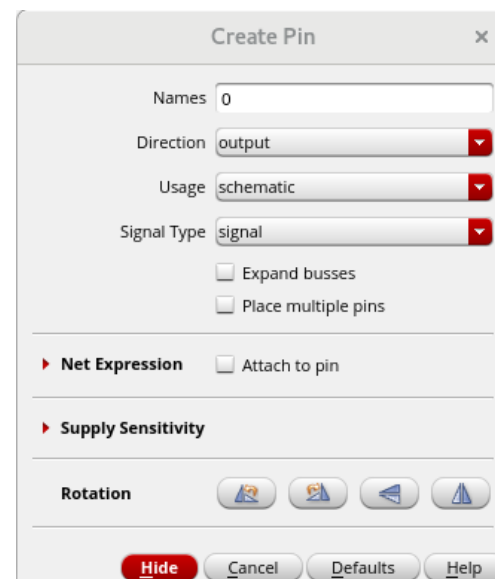
3. Schematic

Step 2: Draw a schematic:

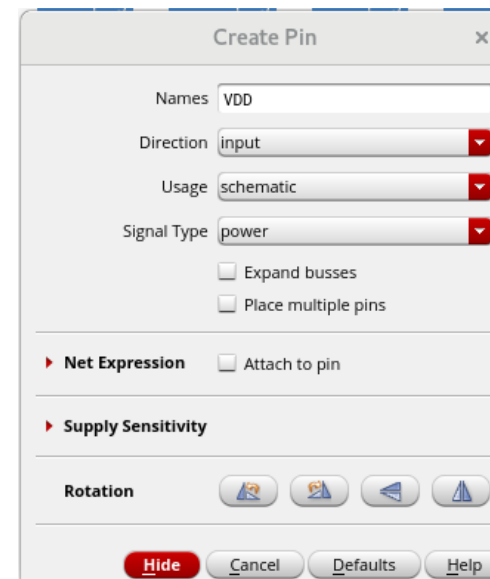
3. To add pin, Select **Create → Pin. (P)**, then add **input, output, vdd** and **gnd**



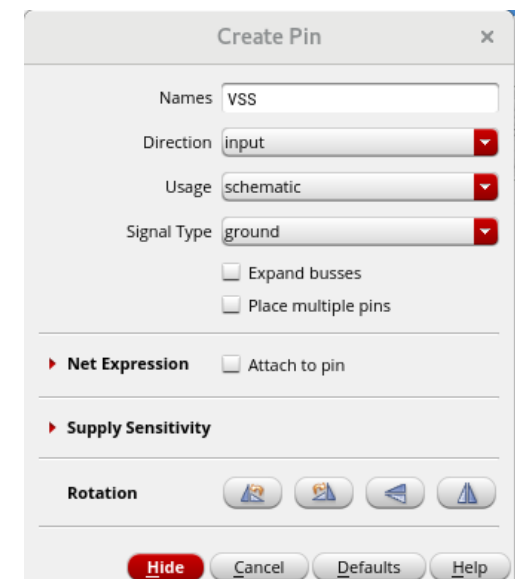
Create Pin dialog box for pin I. The Name is 'I', Direction is 'input', Usage is 'schematic', and Signal Type is 'signal'. There are checkboxes for 'Expand busses' and 'Place multiple pins'. The 'Net Expression' section has an 'Attach to pin' checkbox. The 'Supply Sensitivity' section is collapsed. The 'Rotation' section has four icons. At the bottom are buttons for 'Hide', 'Cancel', 'Defaults', and 'Help'.



Create Pin dialog box for pin 0. The Name is '0', Direction is 'output', Usage is 'schematic', and Signal Type is 'signal'. There are checkboxes for 'Expand busses' and 'Place multiple pins'. The 'Net Expression' section has an 'Attach to pin' checkbox. The 'Supply Sensitivity' section is collapsed. The 'Rotation' section has four icons. At the bottom are buttons for 'Hide', 'Cancel', 'Defaults', and 'Help'.



Create Pin dialog box for pin VDD. The Name is 'VDD', Direction is 'input', Usage is 'schematic', and Signal Type is 'power'. There are checkboxes for 'Expand busses' and 'Place multiple pins'. The 'Net Expression' section has an 'Attach to pin' checkbox. The 'Supply Sensitivity' section is collapsed. The 'Rotation' section has four icons. At the bottom are buttons for 'Hide', 'Cancel', 'Defaults', and 'Help'.



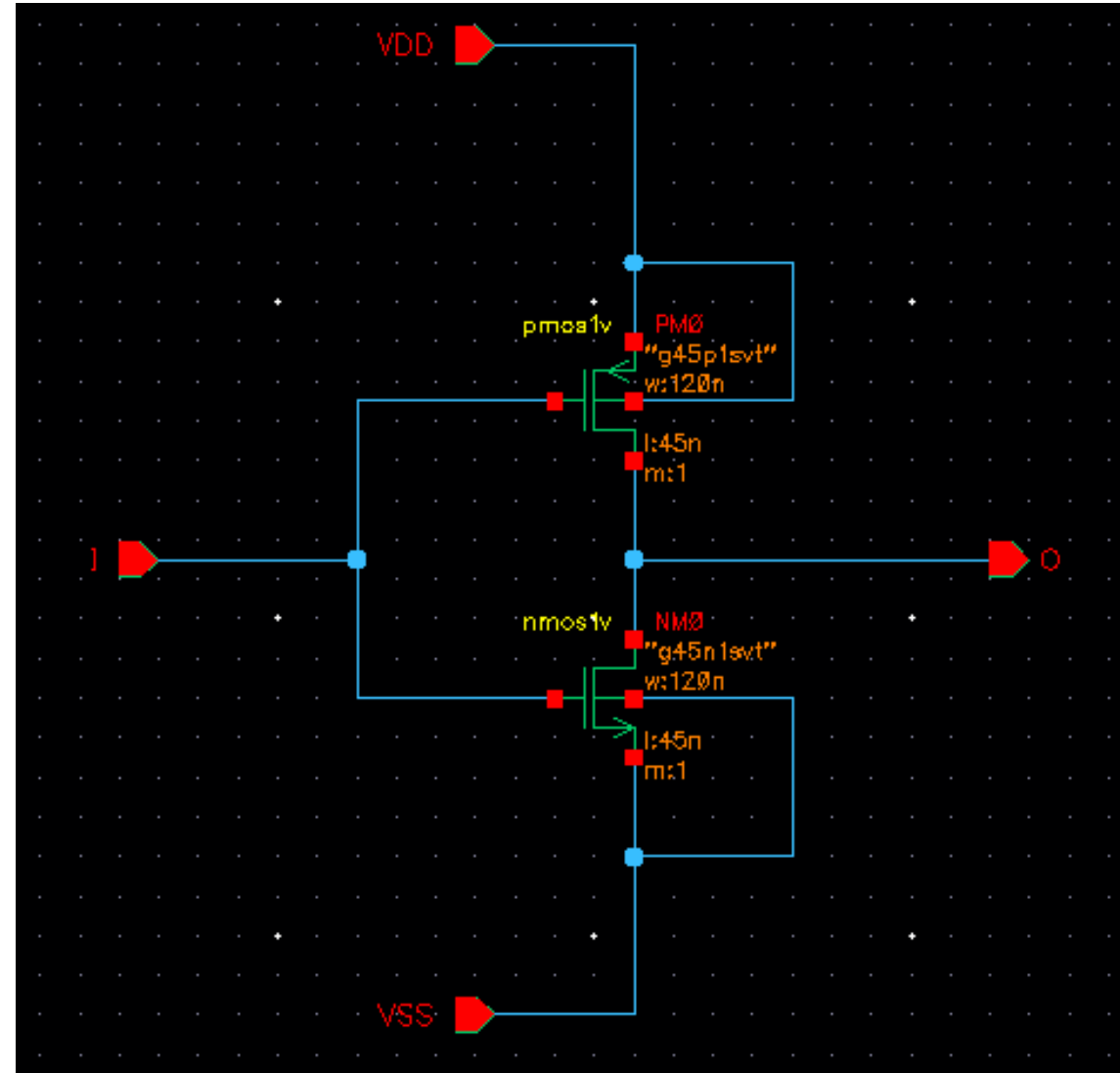
Create Pin dialog box for pin VSS. The Name is 'VSS', Direction is 'input', Usage is 'schematic', and Signal Type is 'ground'. There are checkboxes for 'Expand busses' and 'Place multiple pins'. The 'Net Expression' section has an 'Attach to pin' checkbox. The 'Supply Sensitivity' section is collapsed. The 'Rotation' section has four icons. At the bottom are buttons for 'Hide', 'Cancel', 'Defaults', and 'Help'.

3. Schematic

Step 2: Draw a schematic:

4. Connect the components: Select **Create** → **Wire. (W)**

Complete the circuit



3. Schematic

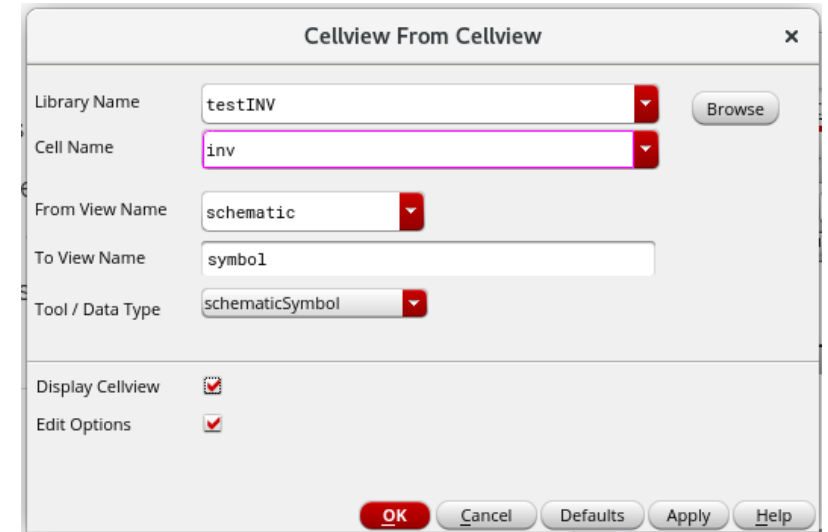
Step 2: Draw a schematic:

5. Check and save: Select ***File*** → ***Check and Save***.

3. Schematic

Step 3: In order to use your cell in a test bench, you first need to create a symbol that represents it.

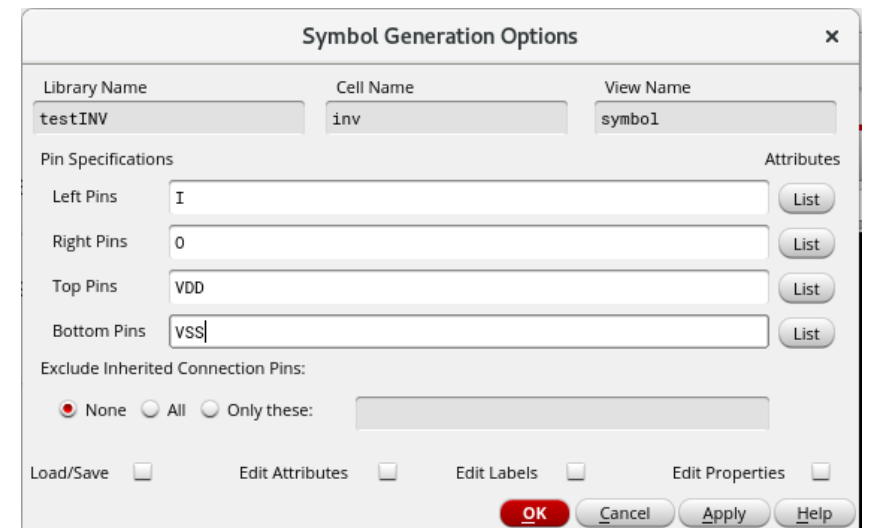
In order to do that, select **Create → Cellview → From Cellview**.



The 'Cellview From Cellview' dialog box is used to create a symbol for a cell. It contains the following fields and options:

- Library Name: testINV
- Cell Name: inv
- From View Name: schematic
- To View Name: symbol
- Tool / Data Type: schematicSymbol
- Display Cellview: ☒
- Edit Options: ☒

Buttons at the bottom: OK, Cancel, Defaults, Apply, Help.



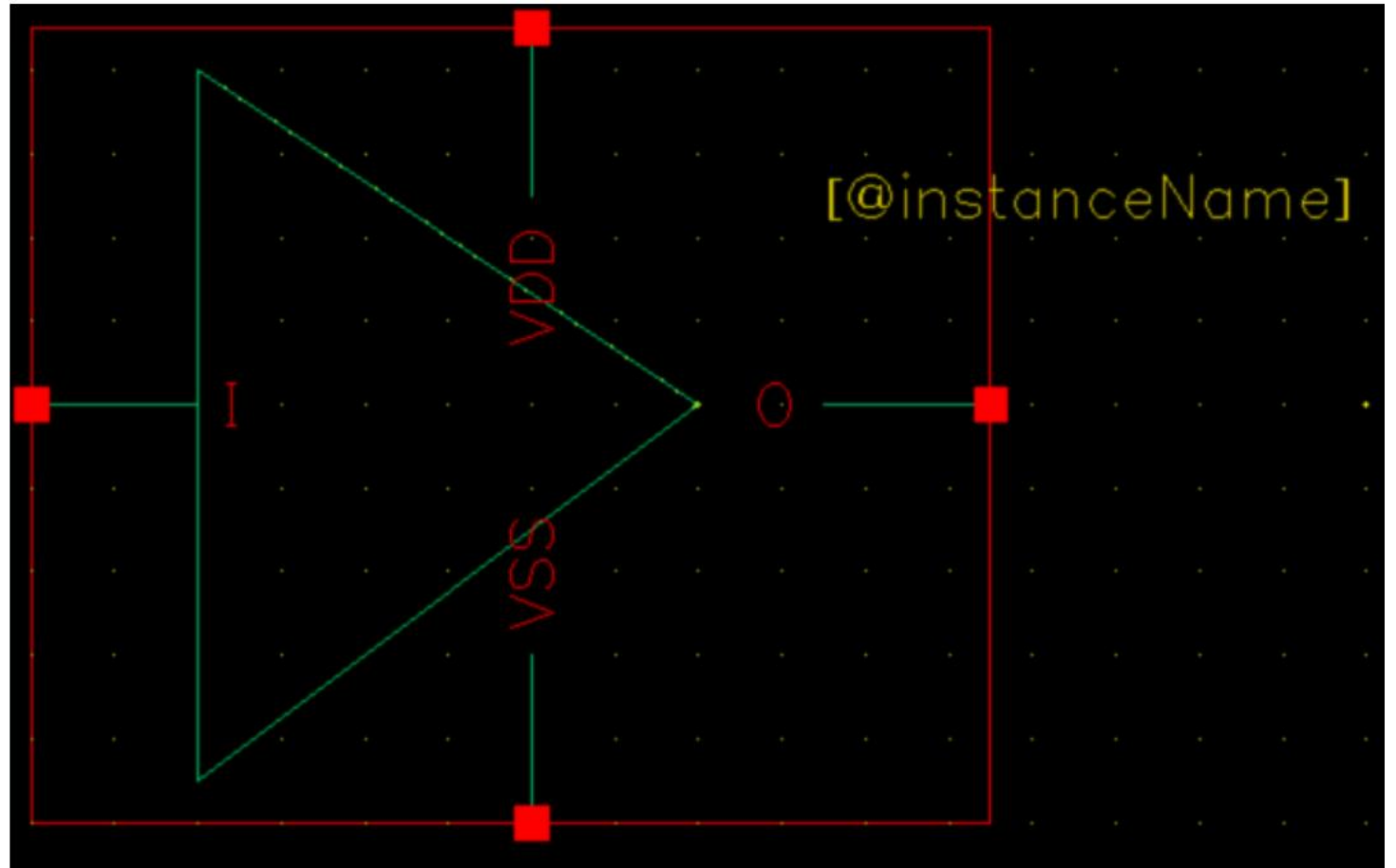
The 'Symbol Generation Options' dialog box is used to configure the symbol generation process. It contains the following fields and options:

- Library Name: testINV
- Cell Name: inv
- View Name: symbol
- Pin Specifications:
 - Left Pins: I
 - Right Pins: 0
 - Top Pins: VDD
 - Bottom Pins: VSS
- Attributes: List buttons for each pin specification.
- Exclude Inherited Connection Pins:
 - None (selected)
 - All
 - Only these:
- Load/Save: ☐
- Edit Attributes: ☐
- Edit Labels: ☐
- Edit Properties: ☐

Buttons at the bottom: OK, Cancel, Apply, Help.

3. Schematic

Step 4: You can modify the symbol by simply delete things that you don't want, and add the shape by: (from the Symbol Editor) Create → Shape → Line/Rectangle/Polygon/Circle/...

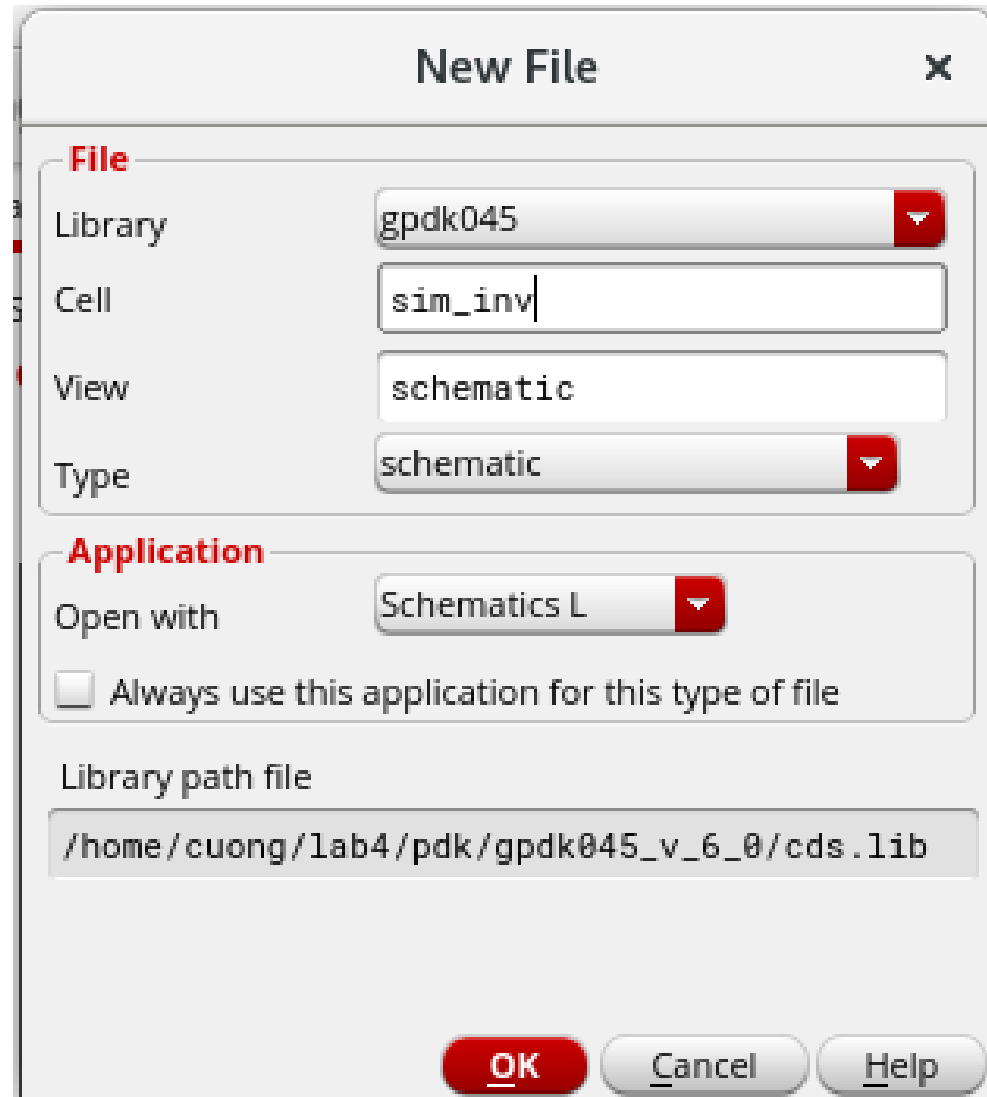


4. Run Spectre simulation

Step 1: To simulate the circuit, we create a new schematic: (from the Library Manager)

File → **New** → **Cellview**.

This time, we name it something like sim_inv:



4. Run Spectre simulation

To add the cell inv: press **I**

Add Instance

Library

testINV

Browse

Cell

inv

View

symbol

Names

☒ Add Wire Stubs at:

☐ all terminals

☒ registered terminals only

...


Array


Rows


1

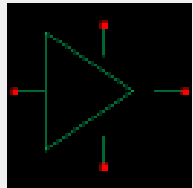
Columns

1

 Rotate

 Sideways

 Upside Down



4. Run Spectre simulation

To add **VDD** and **In** voltages: press **I** then browse to **vdc** in the **analogLib** library, set **DC** voltage as **1.8**:

Add Instance [X]

Library: analogLib [v] [Browse]

Cell: vdc [v]

View: symbol1 [v]

Names: []

☒ Add Wire Stubs at:
☐ all terminals ☒ registered terminals only [...]

Array: Rows: 1 Columns: 1

[Rotate] [Sideways] [Upside Down]

Noise file name: []

Number of noise/freq pairs: 0

DC voltage: 1.8 V

AC magnitude: []

AC phase: []

XF magnitude: []

PAC magnitude: []

PAC phase: []

Temperature coefficient 1: []

Temperature coefficient 2: []

Nominal temperature: []

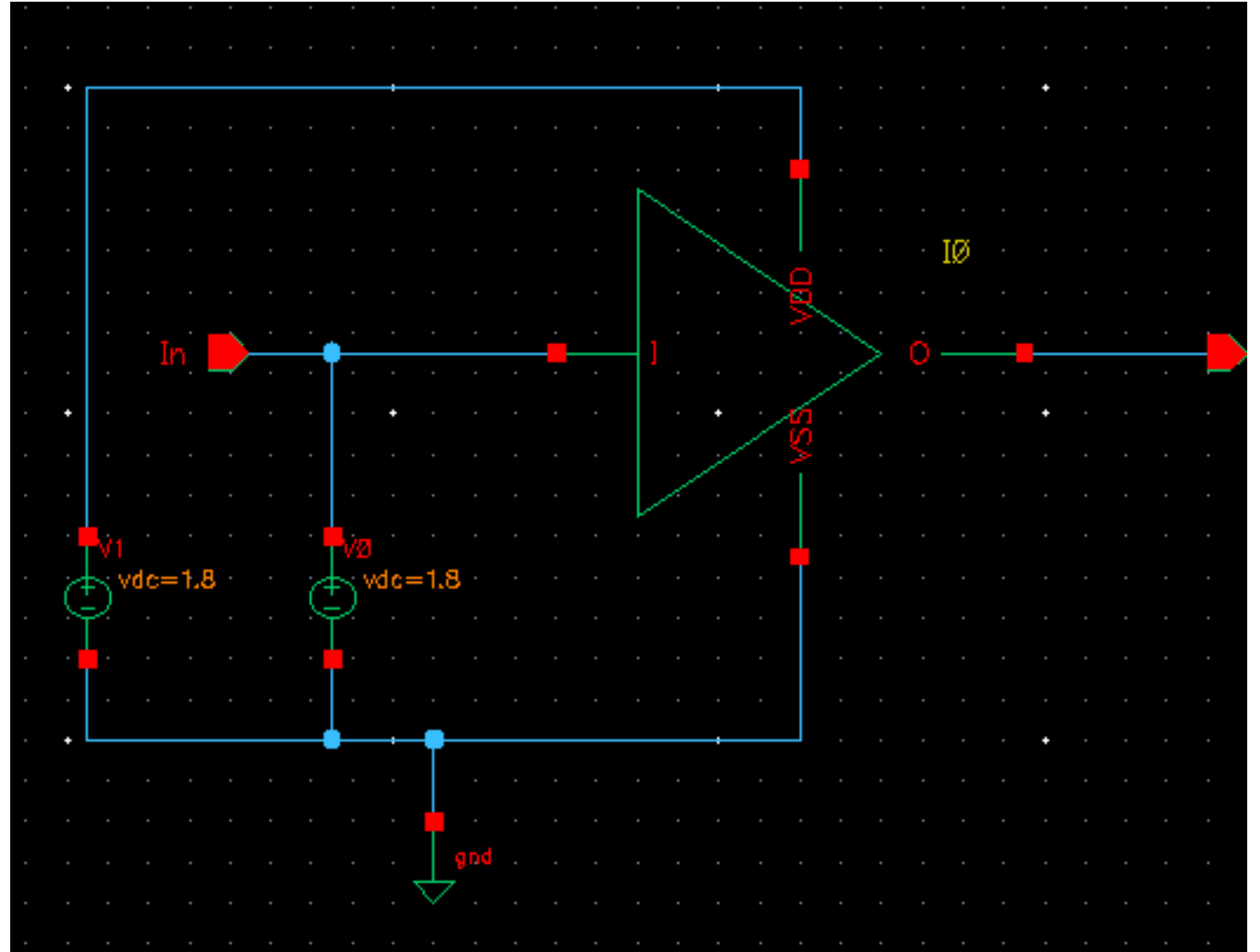
4. Run Spectre simulation

To add **VSS**: press **I** then browse to **gnd** in the **analogLib** library:



4. Run Spectre simulation

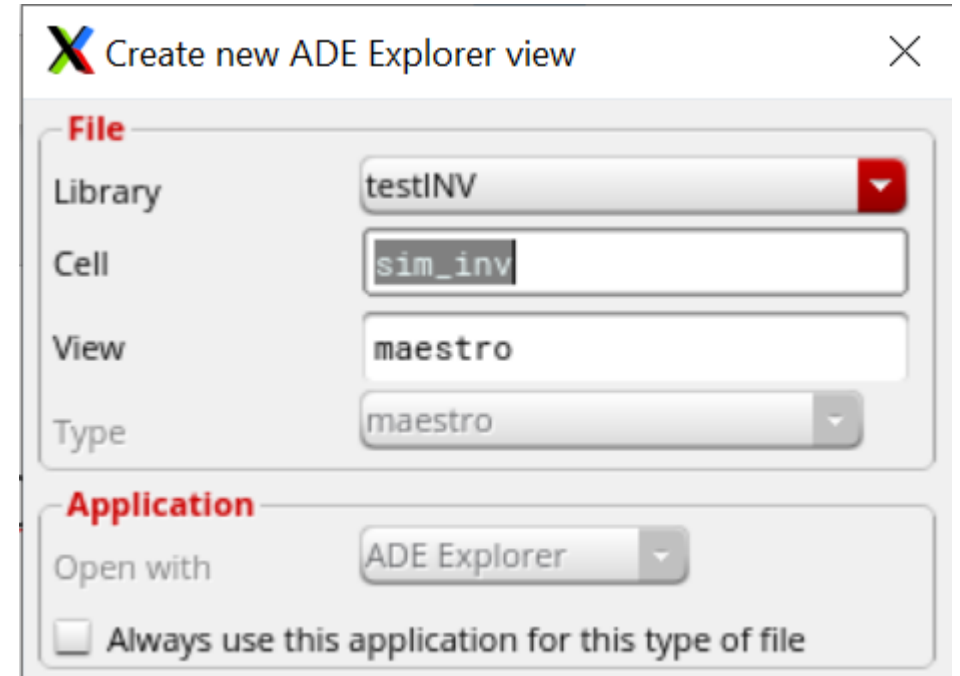
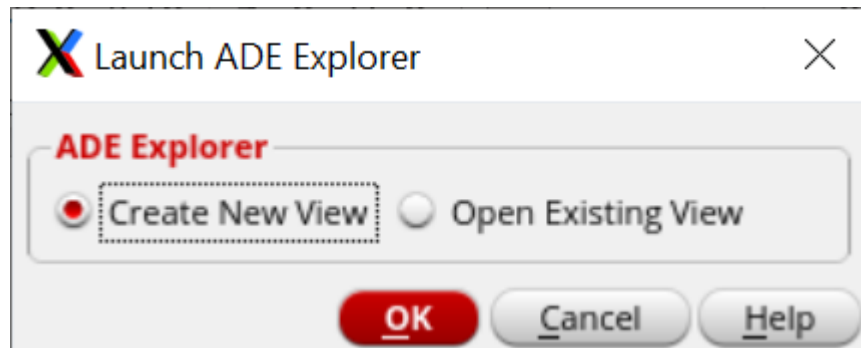
Complete the test circuit.



4. Run Spectre simulation

Step 2: Now we will use the tool **ADE Explorer** to run the analyses.

1. In Schematic Editor, select **Launch** → **ADE Explorer**.

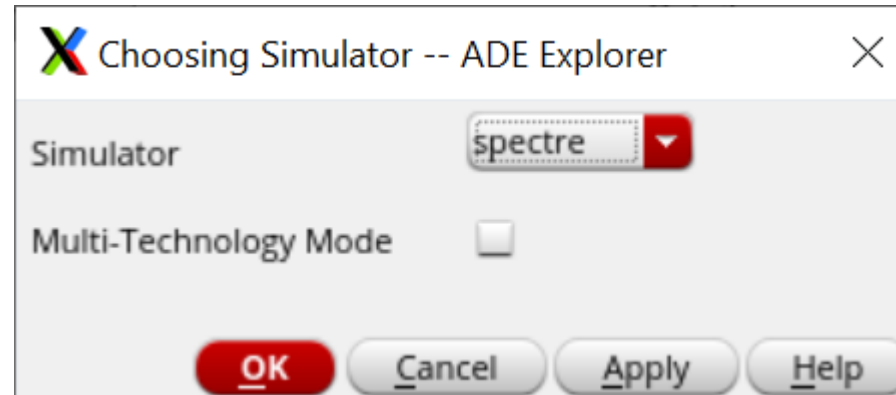


4. Run Spectre simulation

2. From the ADE Explorer,

Setup → **Simulator**,

then select *spectre*



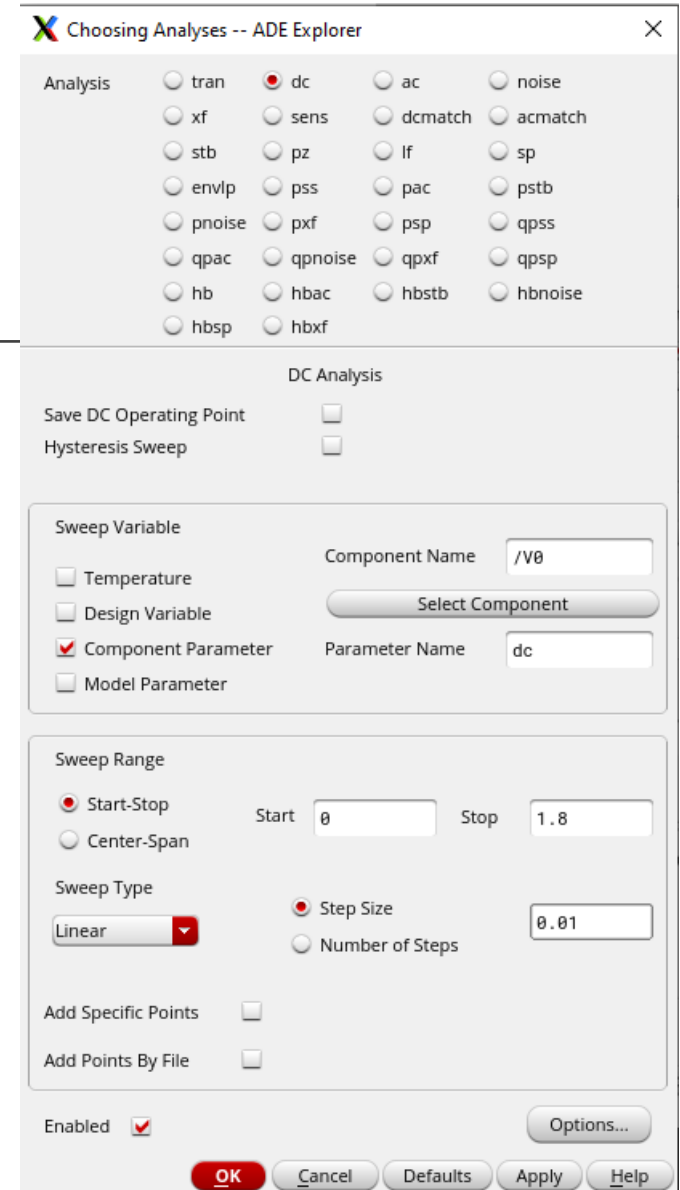
4. Run Spectre simulation

4. To run a simulation, we need to choose the type of analysis. Select **Analyses** → **Choose...**

Select as below

Select **Select Component** and click on V0 vdc on schematic.

The **Start** point should be 0, the **Stop** should be 1.8, the **Step Size** should be **0.01**

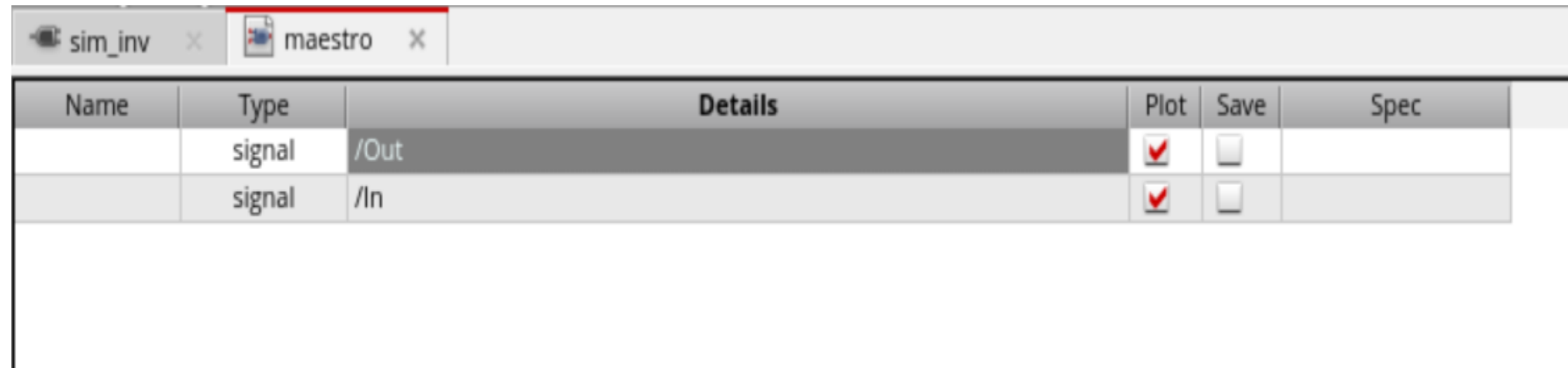


4. Run Spectre simulation

5. Return back to **maestro** view

Select **Outputs → To Be Plotted → Select on Design**.

Point to the **In** and **Out** pins on schematic



Name	Type	Details	Plot	Save	Spec
	signal	/Out	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
	signal	/In	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

4. Run Spectre simulation

6. To run the simulation, select **Simulation → Netlist and Run**

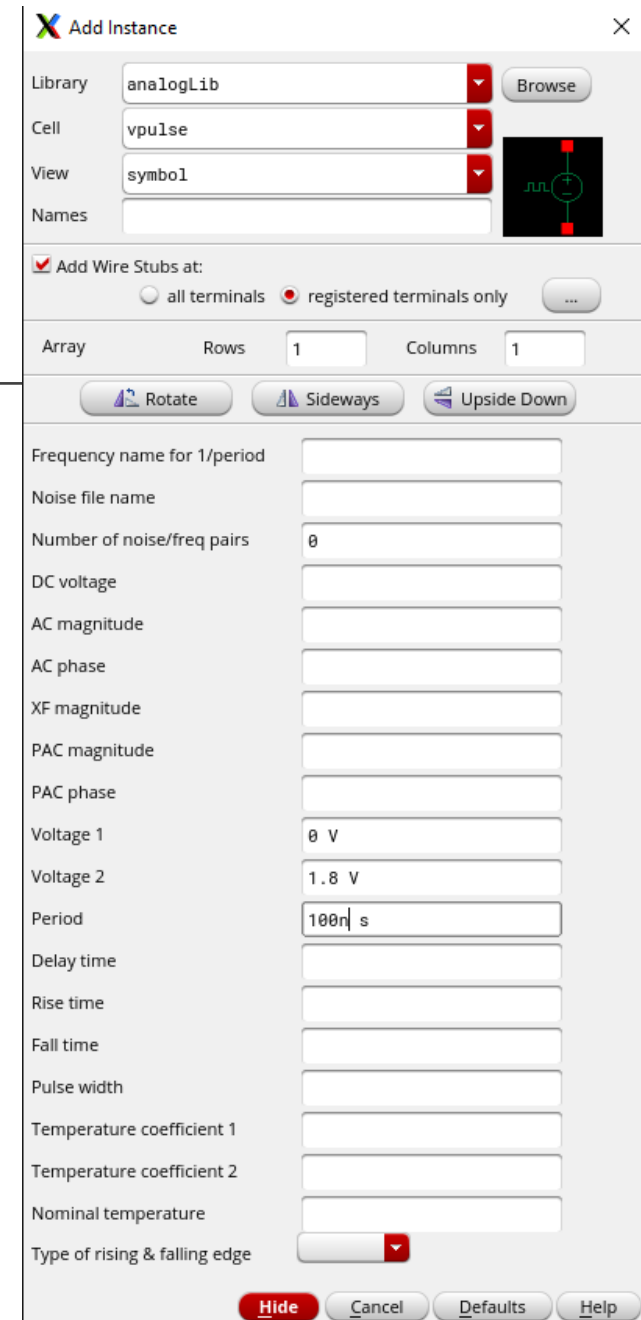
4. Run Spectre simulation

In case you want to simulate multiple inputs:

Step 1: Change the simulation schematic's **vdc** components connecting to the inputs into **vpulse**

Step 2: Set up the **vpulse** component

Example: The image is showing a **vpulse** component moving from 0-1.8V with period 100ns



Add Instance

Library: analogLib Browse

Cell: vpulse

View: symbol +

Names:

☒ Add Wire Stubs at:
☐ all terminals ☒ registered terminals only ...

Array: Rows: 1 Columns: 1

Rotate Sideways Upside Down

Frequency name for 1/period:

Noise file name:

Number of noise/freq pairs: 0

DC voltage:

AC magnitude:

AC phase:

XF magnitude:

PAC magnitude:

PAC phase:

Voltage 1: 0 V

Voltage 2: 1.8 V

Period: 100n s

Delay time:

Rise time:

Fall time:

Pulse width:

Temperature coefficient 1:

Temperature coefficient 2:

Nominal temperature:

Type of rising & falling edge: ▼

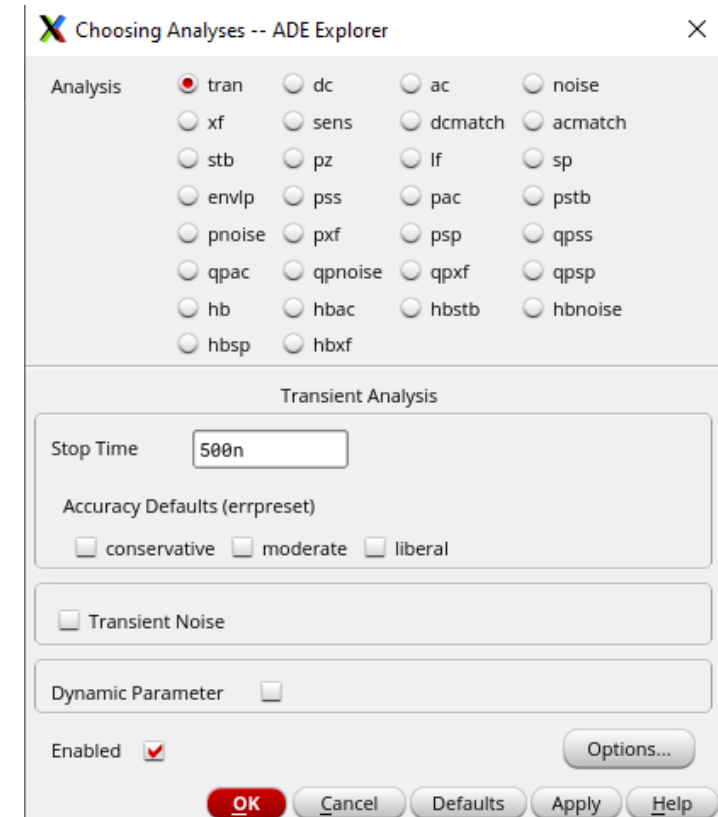
Hide Cancel Defaults Help

4. Run Spectre simulation

In case you want to simulate multiple inputs:

Step 3: Instead of using the **dc** analysis mode, use **tran** for multiple inputs

Example: the image is showing a **tran** analysis mode running in 500ns



5. Submission

This slide just showed an example of an Inverter

Your exercise is to do the same with And gate and Or gate

Each individual submit a report with schematics and simulation of those gates.

There must be your comments showing your own understanding of the schematics and simulation result you submitted in your report