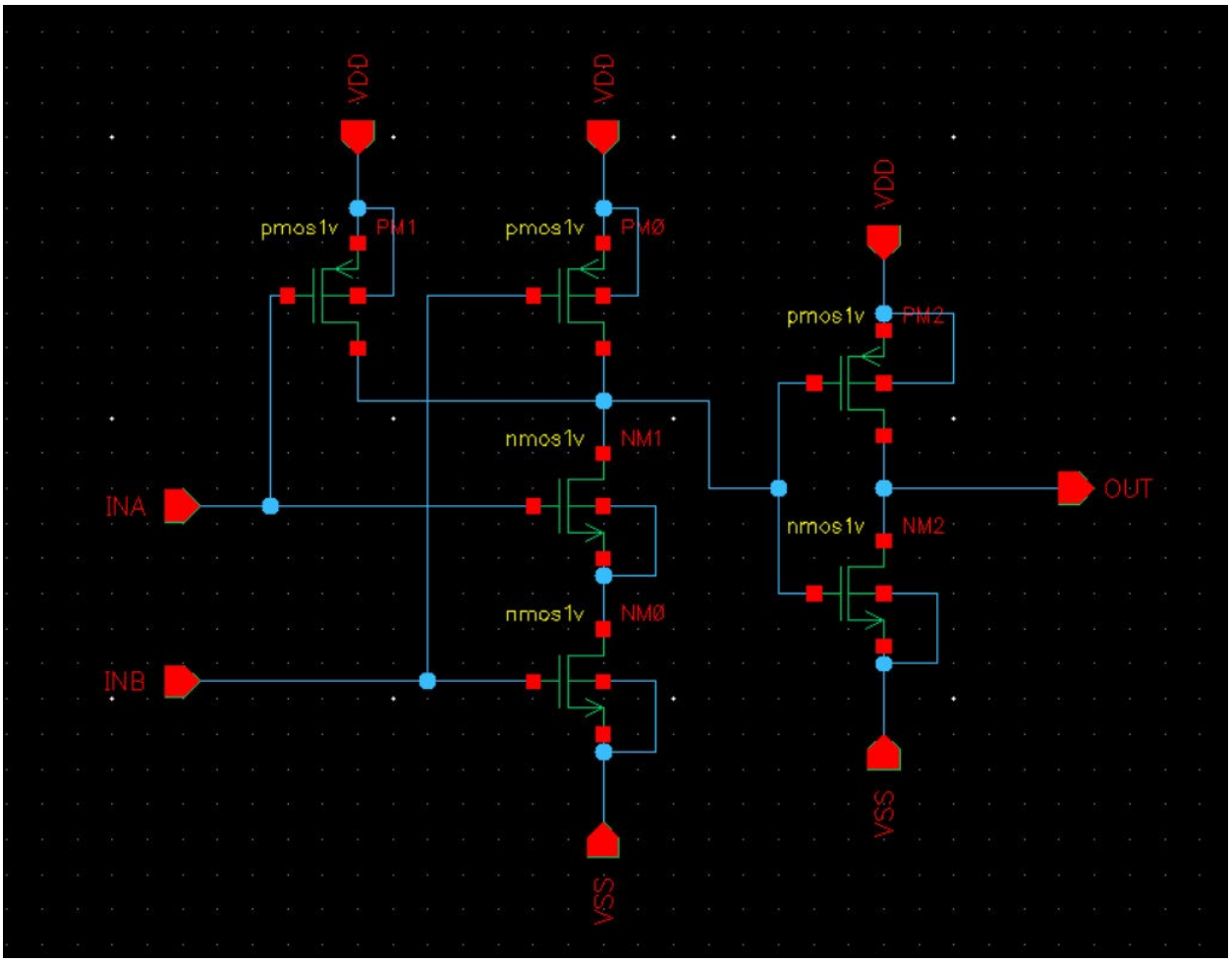
Author: Le Tuan Hung (2052508)

LSI LOGIC DESIGN (LAB) (CO3098)_CC02

LAB 4: VIRTUOSO

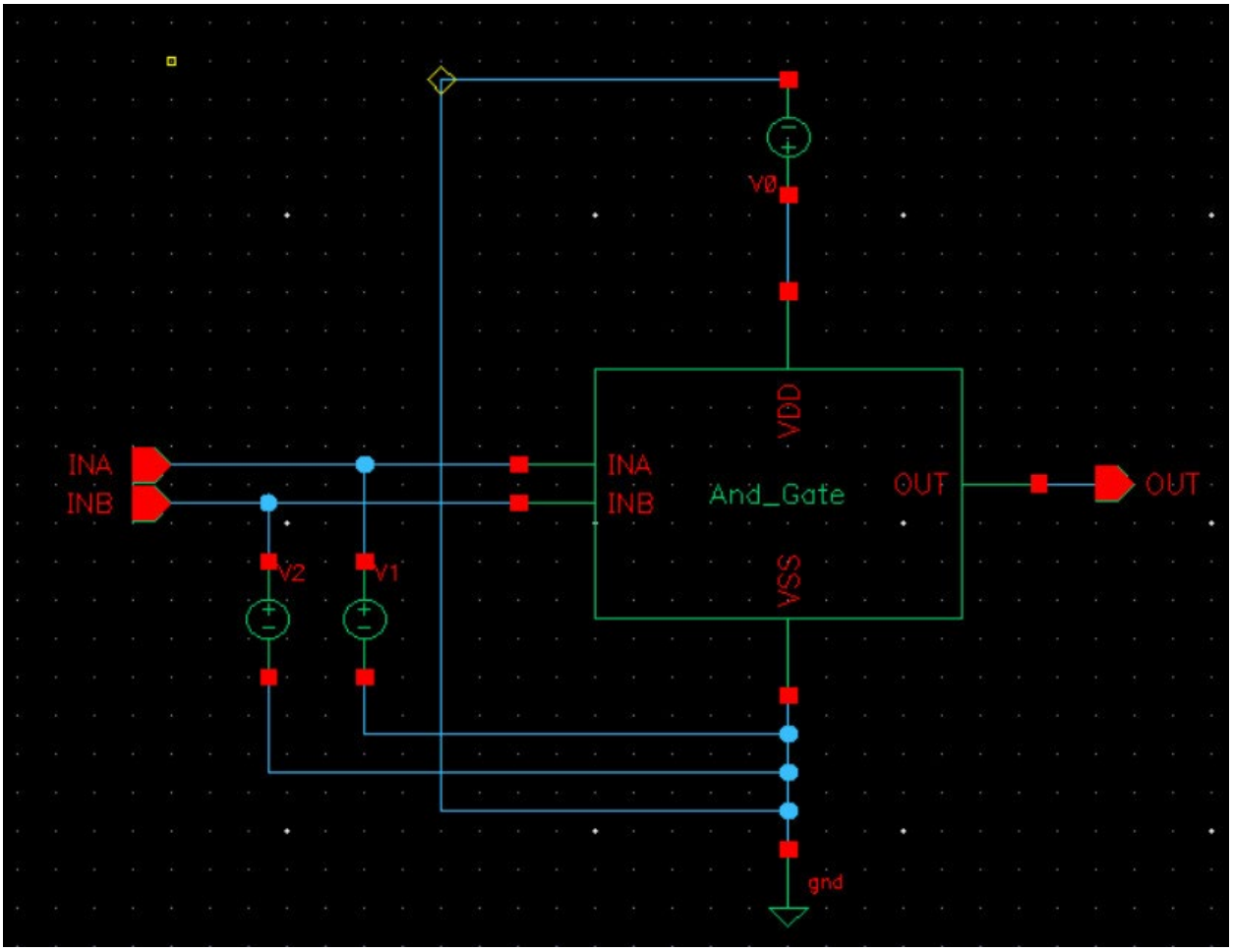
4.1. AND Gate

The schematic for AND Gate.



2 Parallel PMOS followed with and 2 serial NMOS will give us NAND gate then the result go into the NOT gate in the example lab.

The symbol for AND_Gate



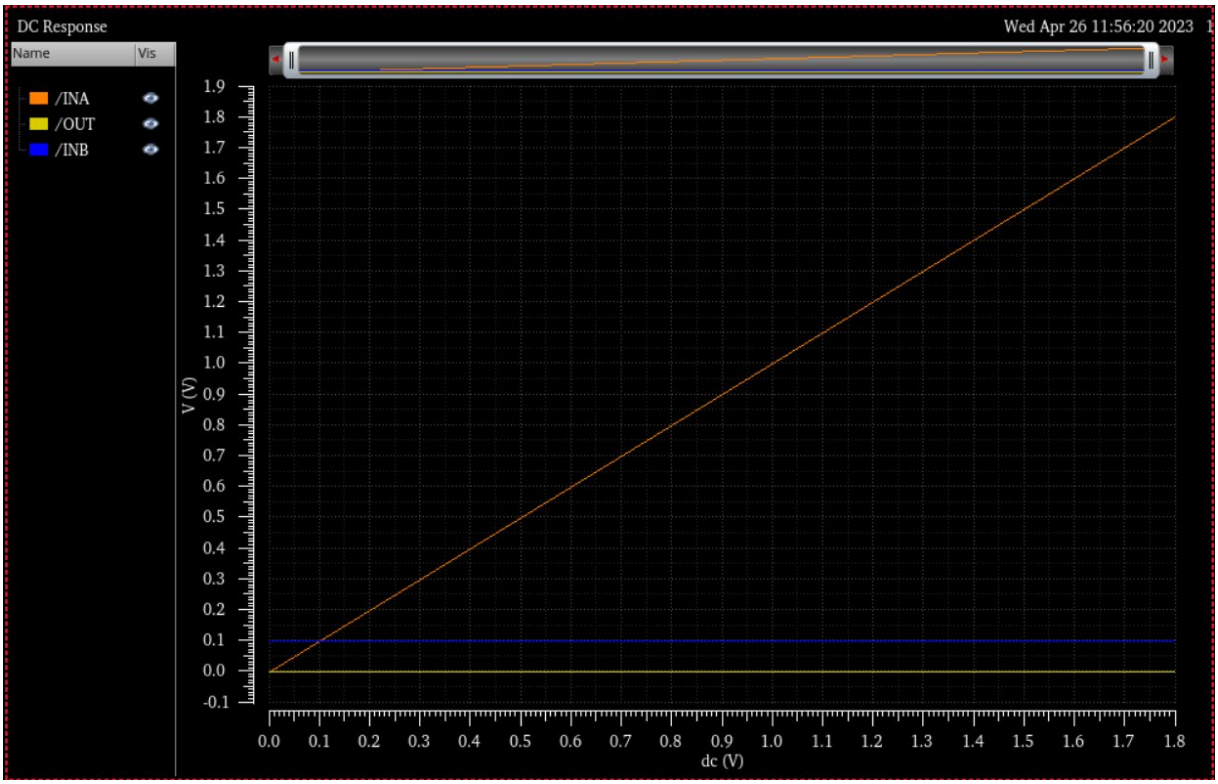
Simulation:

Because AND gate have 2 inputs, so I will do 2 simulations. Then, here is the simulation result:

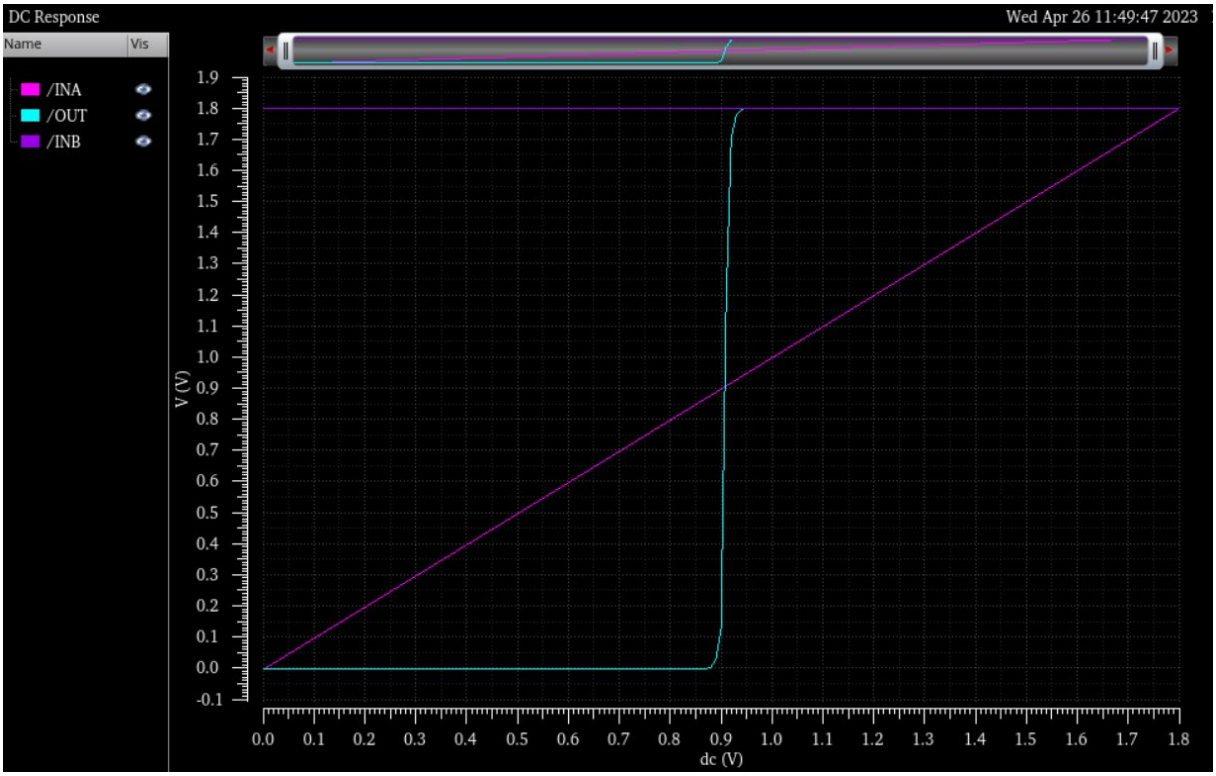
The Truth Table of AND:

INA	INB	OUT
0	0	0
0	1	0
1	0	0
1	1	1

When INB = 0 (0.1V for line not overlap), the voltage of INA sweeps from 0 -> 1.8V

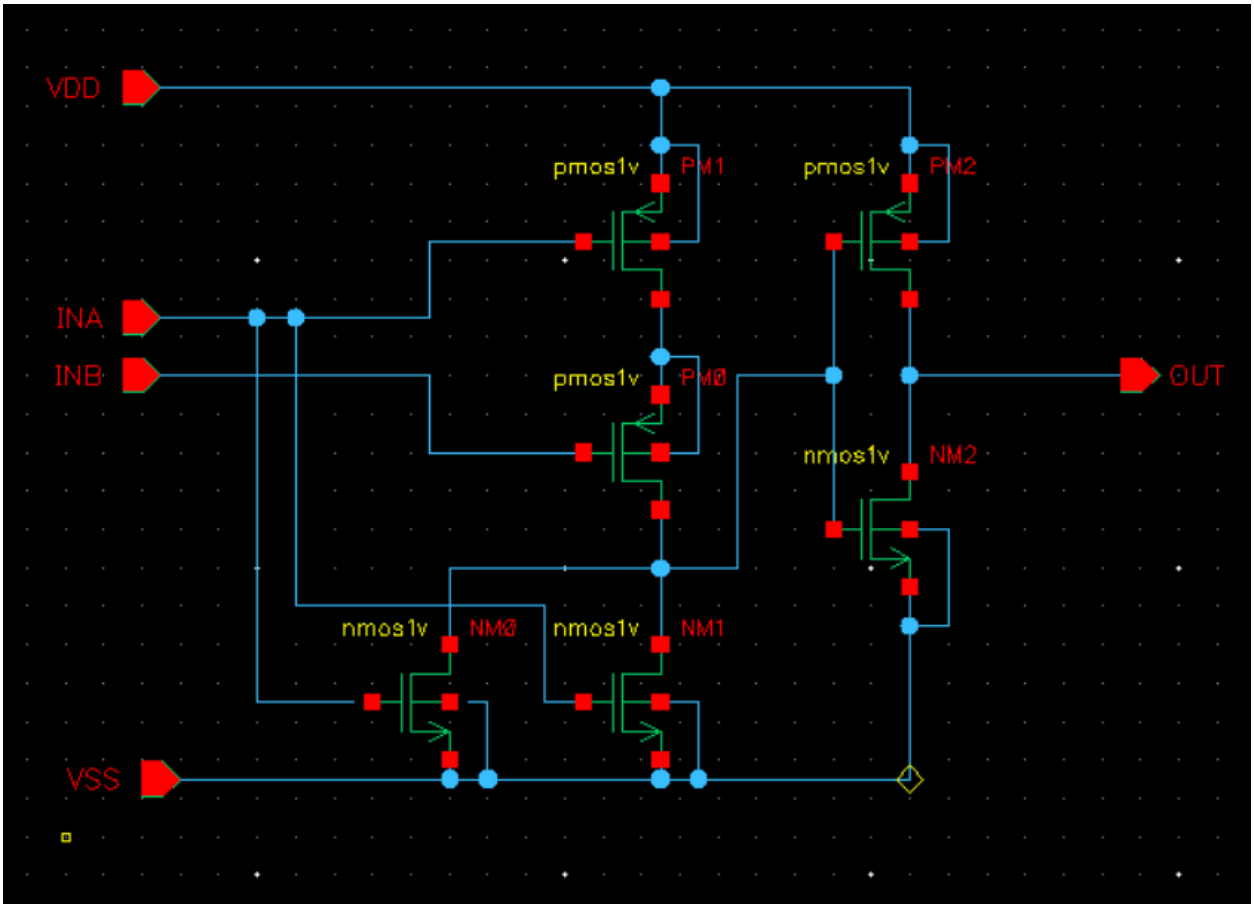


When INB = 1, the voltage of INA sweeps from 0 -> 1.8V



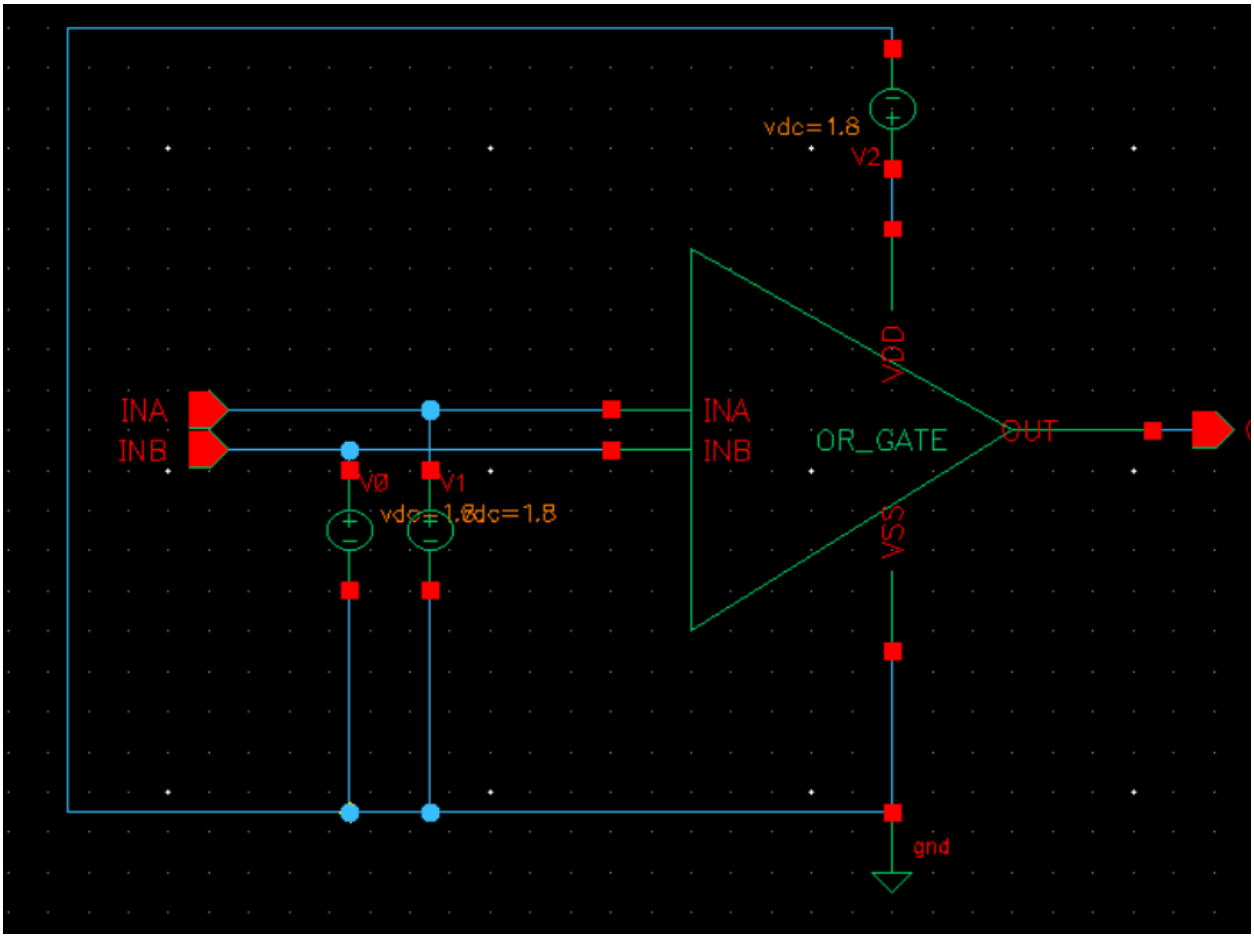
4.2. OR Gate

The schematic for OR Gate.



2 Parallel NMOS followed with and 2 serial PMOS will give us NOR gate then the result go into the NOT gate in the example lab.

The symbol for OR_Gate



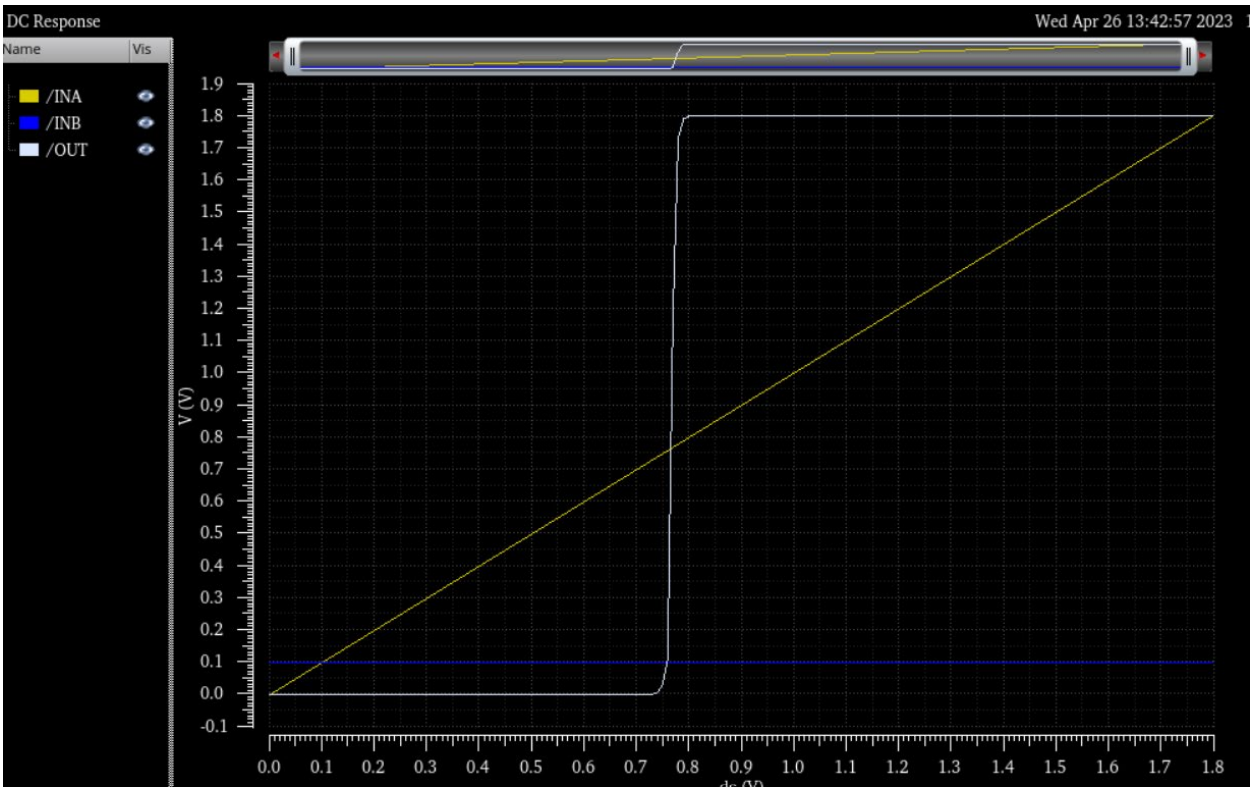
Simulation:

Because OR gate have 2 inputs, so I will do 2 simulations. Then, here is the simulation result:

The Truth Table of OR:

INA	INB	OUT
0	0	0
0	1	1
1	0	1
1	1	1

When INB = 0 (0.1v for line not overlap), the voltage of INA sweeps from 0 -> 1.8V



When INB = 1, the voltage of INA sweeps from 0 -> 1.8V