EE618(Zele) : CMOS Analog IC Design

Course Project - I.
Deadline : 15^{th} October 2018 11:55 PM
Total Marks : 50

Specifications

Design an Operational Transconductance Amplifier in SCL 180nm technology (fully differential input, single ended output) to meet the following specifications:
[**Note:** For two stage OTA designs, R_Z tracking must be implemented for pole-zero cancellation.]

- DC gain $\geq$ 100dB.
- Unity gain frequency $\geq$ 90 MHz.
- Output voltage swing $\geq 1V_{p-p}$.
- Slew rate $\geq 200V/\mu s$.
- Phase Margin $\geq 60^{\circ}$.
- Input referred spot noise (Thermal only) = $20\,nV/\sqrt{Hz}$.
- Input Common mode voltage = 0.9V.
- Output load capacitance = 1pF (From analogLib).
- VDD = 1.8V
- Power consumption $\leq$ 2mW.

Note: Students will get the initial hand calculation reviewed from TA before 3^{rd} October 2018. A Viva voce will be held after the submission deadline. Students must explain the design flow and the results that they obtain and show the simulations on laptops.

Simulations to be performed

Tabulate the Opamp Specifications in typical corner as shown below: [Typical corner: TT, 27°C]

DC gain	
Unity Gain frequency	
Phase Margin	
Slew Rate	
Output Swing (V_{p-p})	
Settling Time (1% accuracy)	
RMS Thermal Noise Voltage	
CMRR	
PSRR	
ICR (Input Common Mode Range)	
Power	

Tabulate the following specifications in the corners specified in the table below.

Corner	**SS**		**TT**	**FF**	
Temperature (°C)	**0**	**100**	**27**	**0**	**100**
DC Gain					
Unity Gain Frequency					
Phase Margin					

Grading

- Initial design/Hand Calculation : 10 Marks.
- Simulation Results : 20 Marks.
- Quality of the report : 10 Marks.
- Viva voce : 10 Marks.
- Bonus points (Based on architecture) : 12.5 Marks.

Architectures: Folded cascode, Gain boosting, Slew rate enhancement, Rail-to-rail OTA or any other architecture with prior approval from your TA.