OTA Design

Specifications:

- DC gain ≥ 100 dB
- Output voltage swing ≥ 1 V_{p-p}
- Phase margin ≥ 60°
- Output load capacitance = 1 pF
- Unity gain frequency ≥ 90 MHz
- Slew rate ≥ 200 V /µs
- Input referred thermal noise ≤ 20 nV $/\sqrt{Hz}$

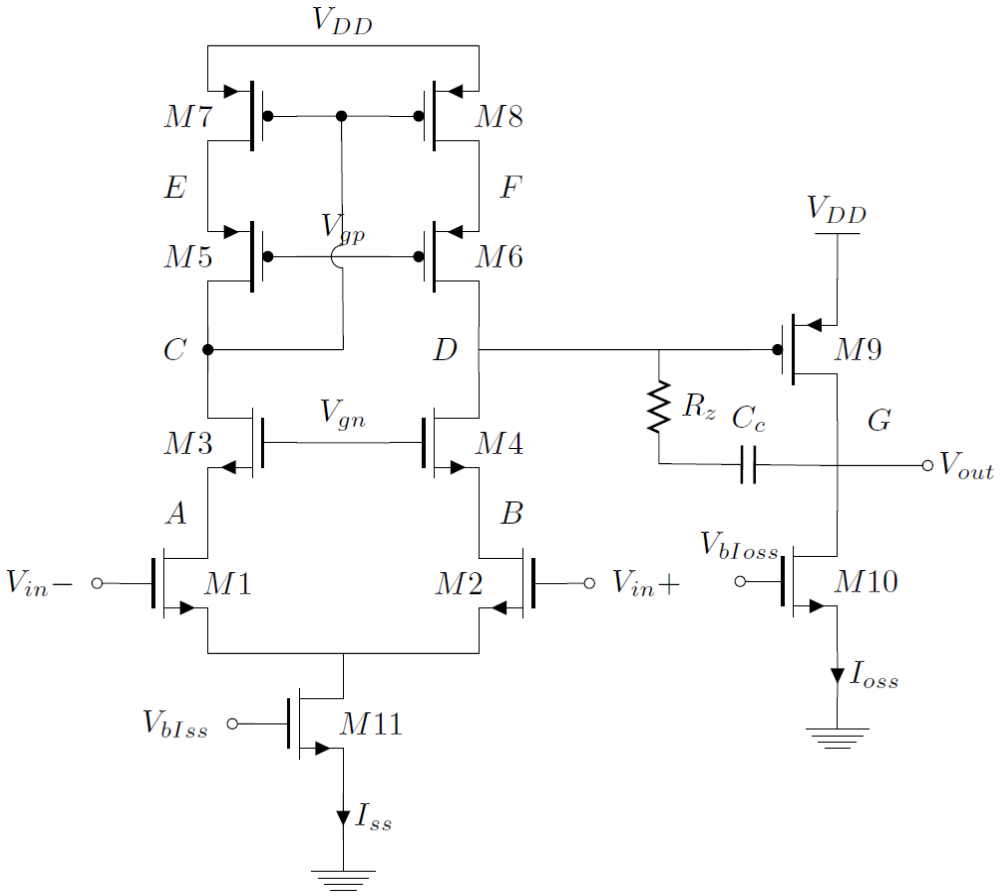


Figure 1: Two Stage Cascode (Telescopic) OTA with high swing

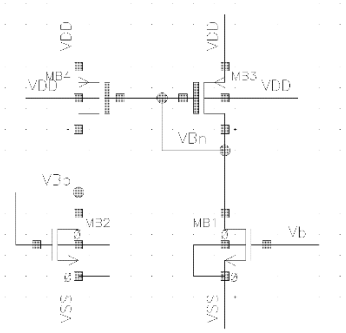


Figure 2: Biasing Circuit

Part I: Layout

Final Design

Table 1: Transistor parameters

	W/L	Fingers	Multipliers	W (in µm)	L(in µm)
M1	6	3	2	3.3	0.55
M2	6	3	2	3.3	0.55
M3	16	4	4	8.8	0.55
M4	16	4	4	8.8	0.55
M5	20	2	10	7	0.35
M6	20	2	10	7	0.35
M7	4	2	2	1.4	0.35
M8	4	2	2	1.4	0.35
M9	150	15	10	52.5	0.35
M10	112	14	8	61.6	0.55
M11	6	2	3	3.3	0.55
M12	2	2	1	1.1	0.55
M13	8	2	4	4.4	0.55
Mx	8	8	1	2.8	0.35
My	20	10	2	7	0.35
Mz	34	17	2	11.9	0.35
MB1	2	2	1	1.1	0.55
MB2	2	2	1	1.1	0.55
MB3	6	3	2	2.1	0.35
MB4	6	3	2	2.1	0.35

C_C = 0.17 pF

Simulated Results

Table 2: Comparision of Simulation Results of Layout vs Schematic

	Schematic	Layout
DC Gain	100.287 dB	98.5745 dB
Unity Gain Frequency	152.99 MHz	106.2 MHz
Phase Margin	62.926°	60.036°
Slew Rate	140 V/µs	124 V/µs
Input Referred Thermal Noise	18.0282 nV/$\sqrt{Hz}$	18.7849 nV/$\sqrt{Hz}$
Settling Time	7.22088 ns	10.8387 ns
Common Mode Gain	-12.093 dB	-35.7374 dB
Output Swing	1.06 V	1 V
$PSRR_{VDD}$	100.19 dB	102.042 dB
$PSRR_{VSS}$	106.094 dB	108.202 dB
CMRR	112.38 dB	134.311 dB
Input Common Mode Range	[709 mV, 1.225 V]	[689 mV, 1.024 V]
Power	1.188 mW	1.191 mW
Area	--	6375 μm^2

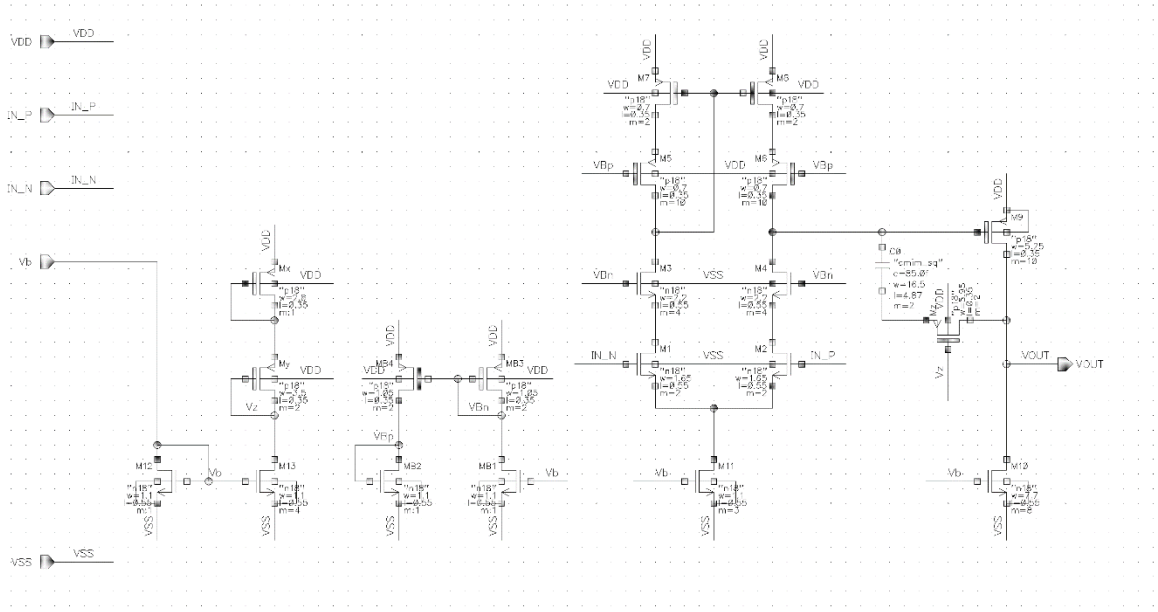


Figure 3: Schematic

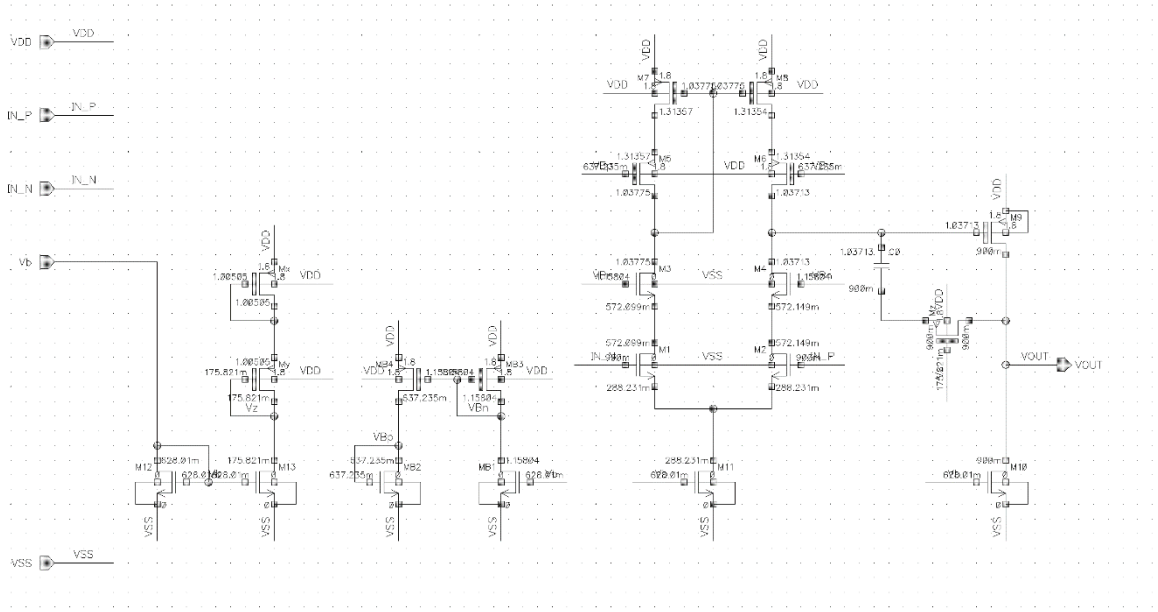


Figure 4: DC Analysis (Layout)

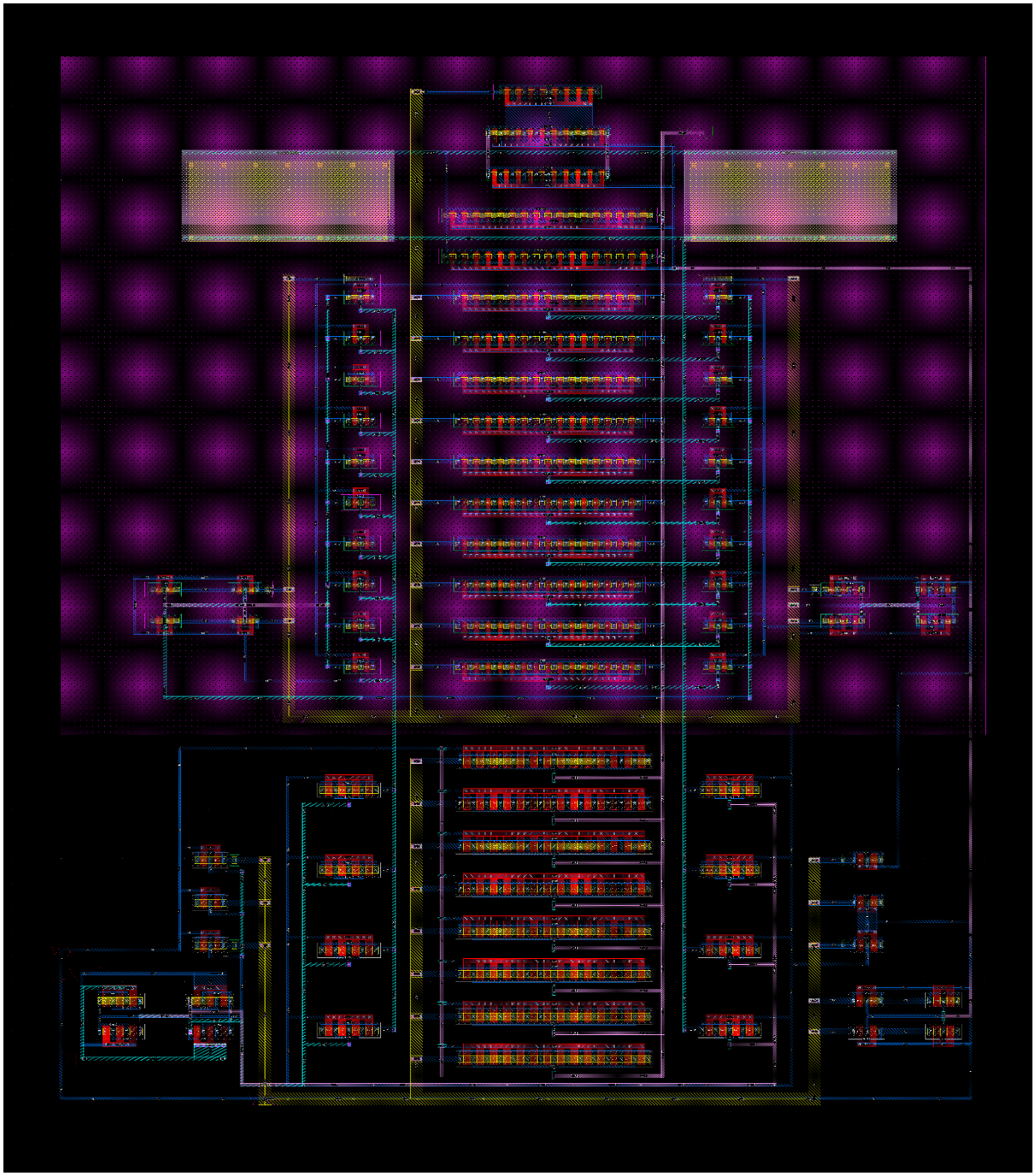


Figure 5: Layout

Area = 75 µm × 85 µm

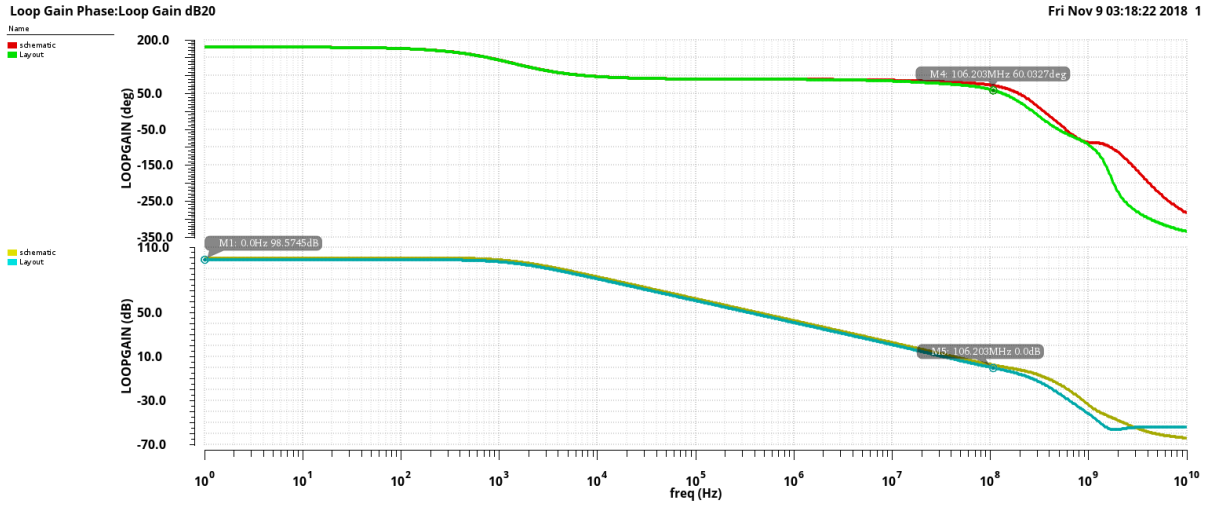


Figure 6: STB Analysis

Dc gain = 98.574 dB, Unity gain Frequency = 106.203 MHz , Phase Margin = 60.0327°

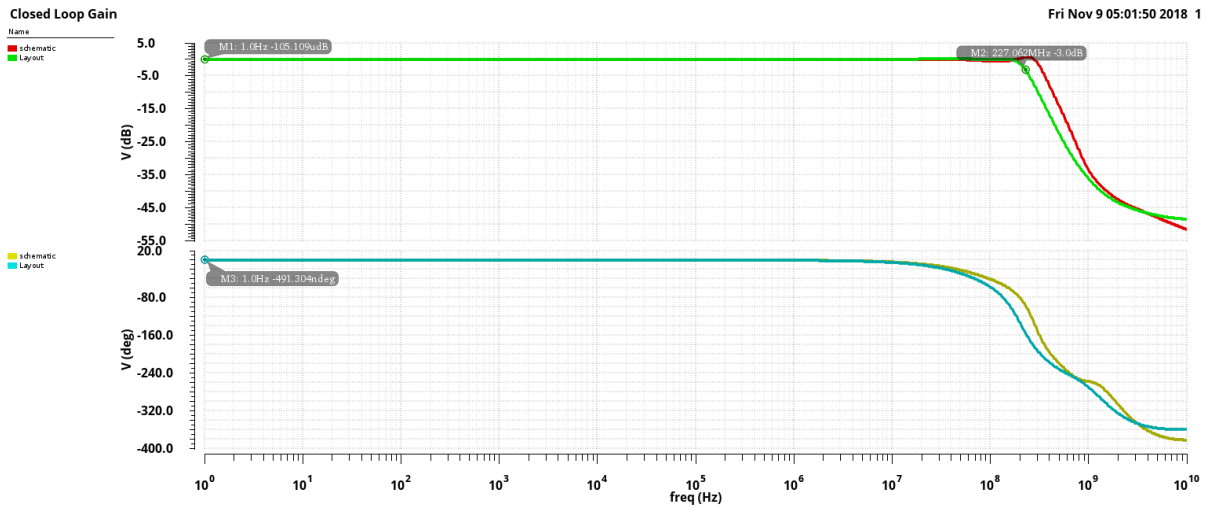


Figure 7: Closed-Loop Gain

V_{out} ≈ 0 dB, Phase = 0°. 3 dB Frequency = 227.062 MHz

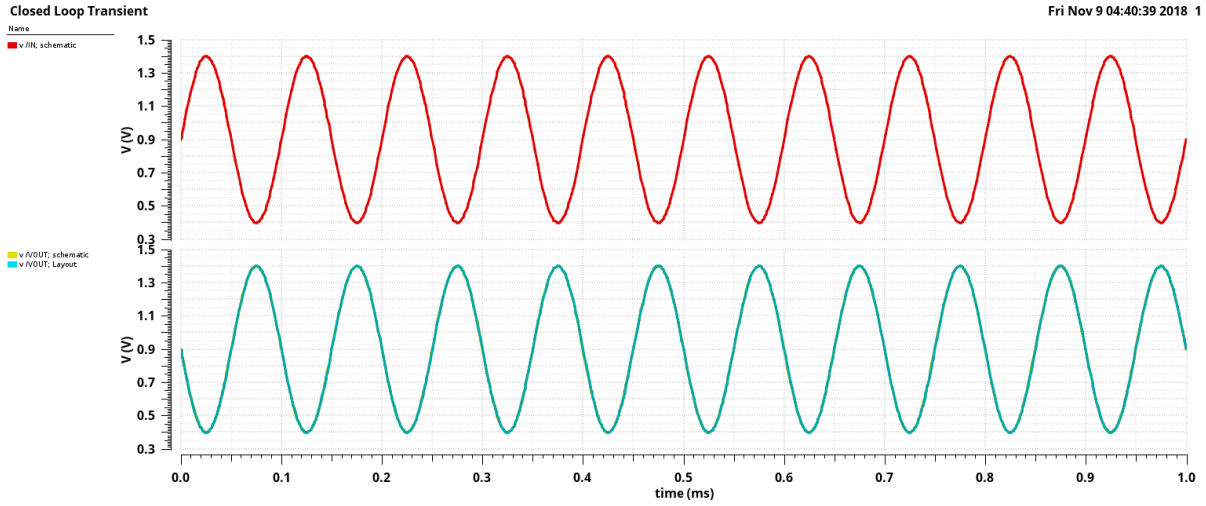


Figure 8: Closed-Loop Transient Response

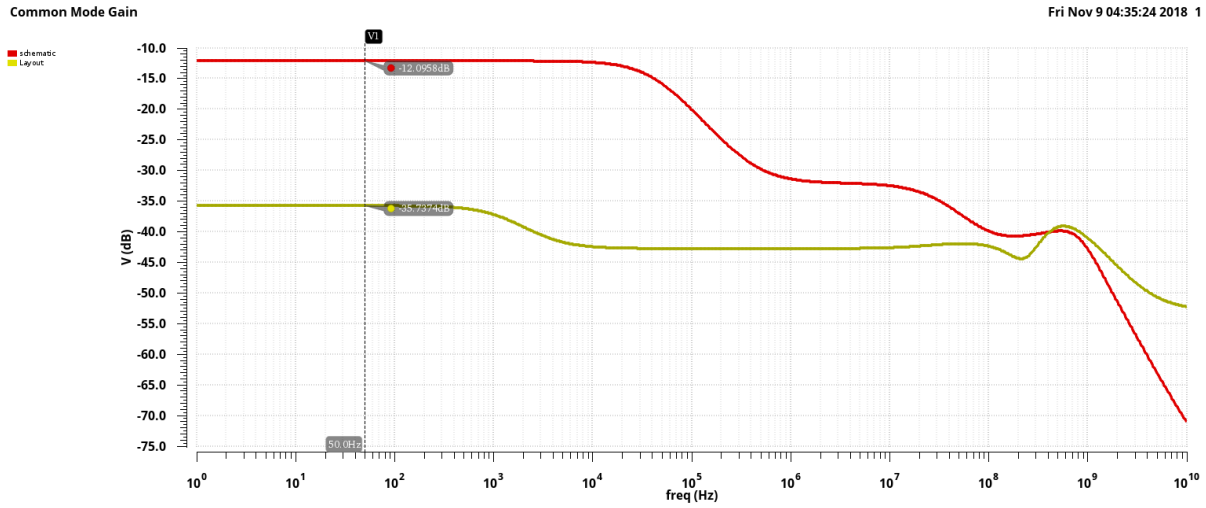


Figure 9: Common Mode Gain

A_{CM} = -35.7374 dB, So CMRR = 20×(ln A_{dm} – ln A_{cm}) = 134.311 dB

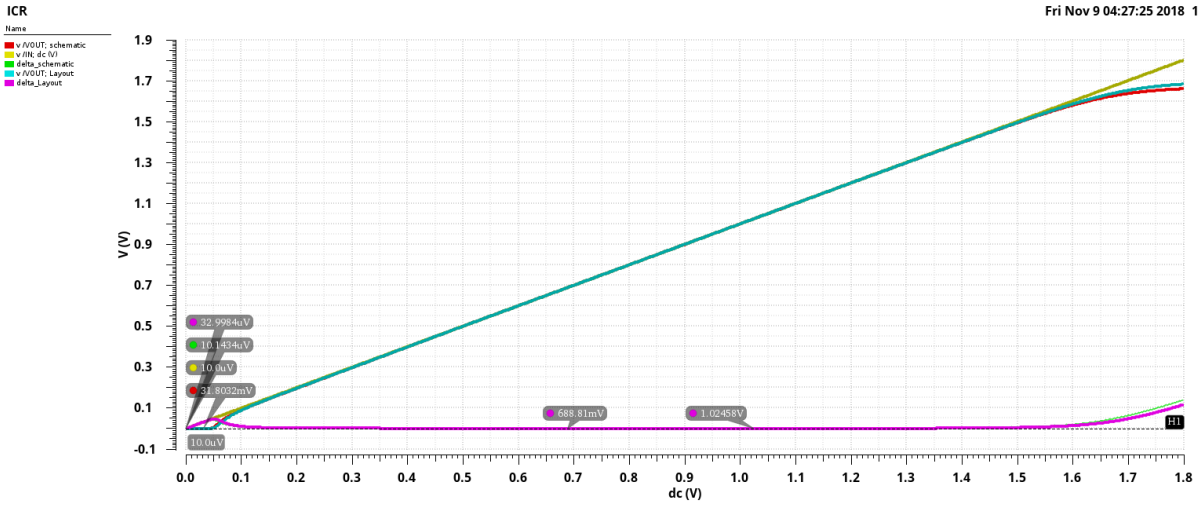
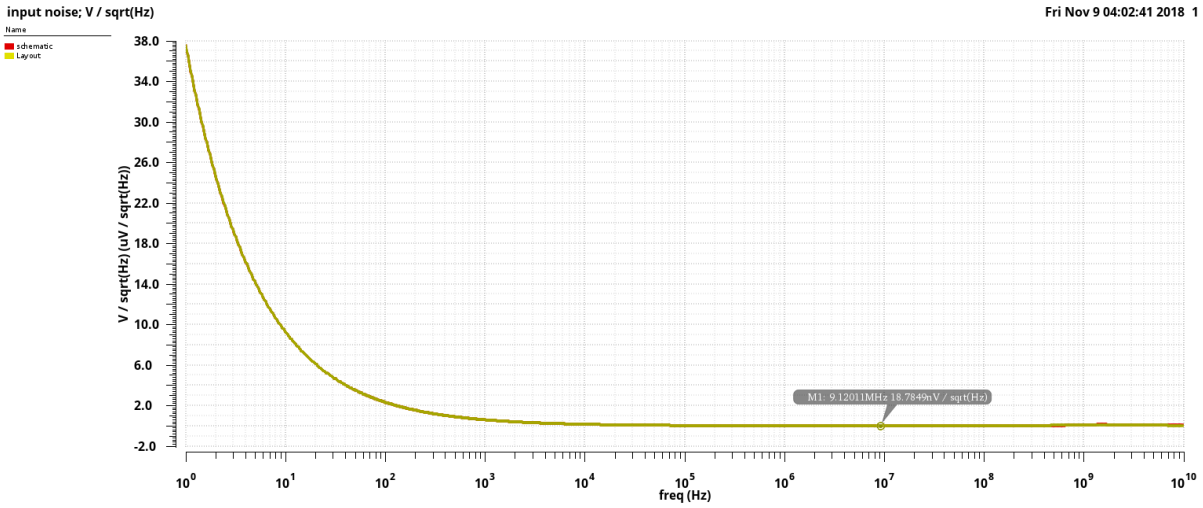


Figure 10: Input Common Mode Range

ICR = 689 mV to 1.024 V

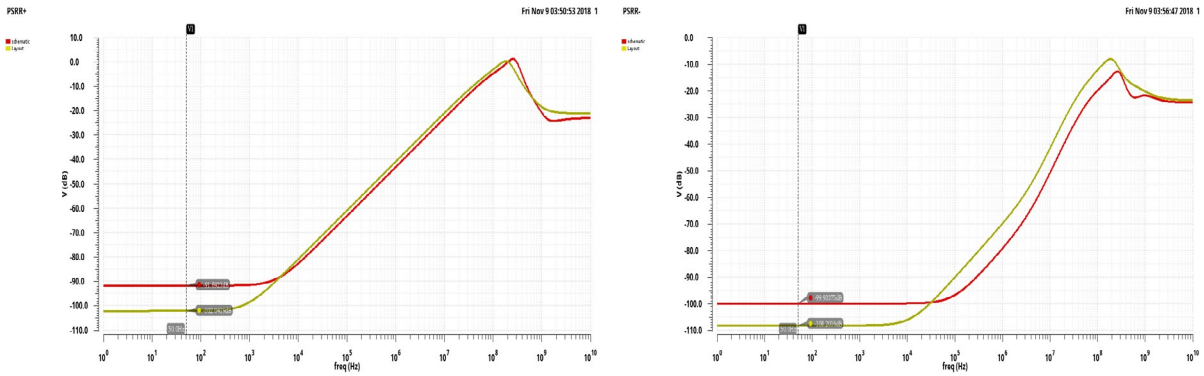


(a) Input referred noise PSD from 1Hz to 1GHz

```
Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000230136
Total Input Referred Noise = 0.000228047
The above noise summary info is for noise data
```

(b) Observed integrated noise voltage over the unity gain bandwidth

Figure 11: Input Referred Noise



(a) $PSRR^+$ (b) $PSRR^-$

Figure 12: Power Supply Rejection Ratio

$PSRR^+$ = 102.042 dB

$PSRR^-$ = 108.202 dB

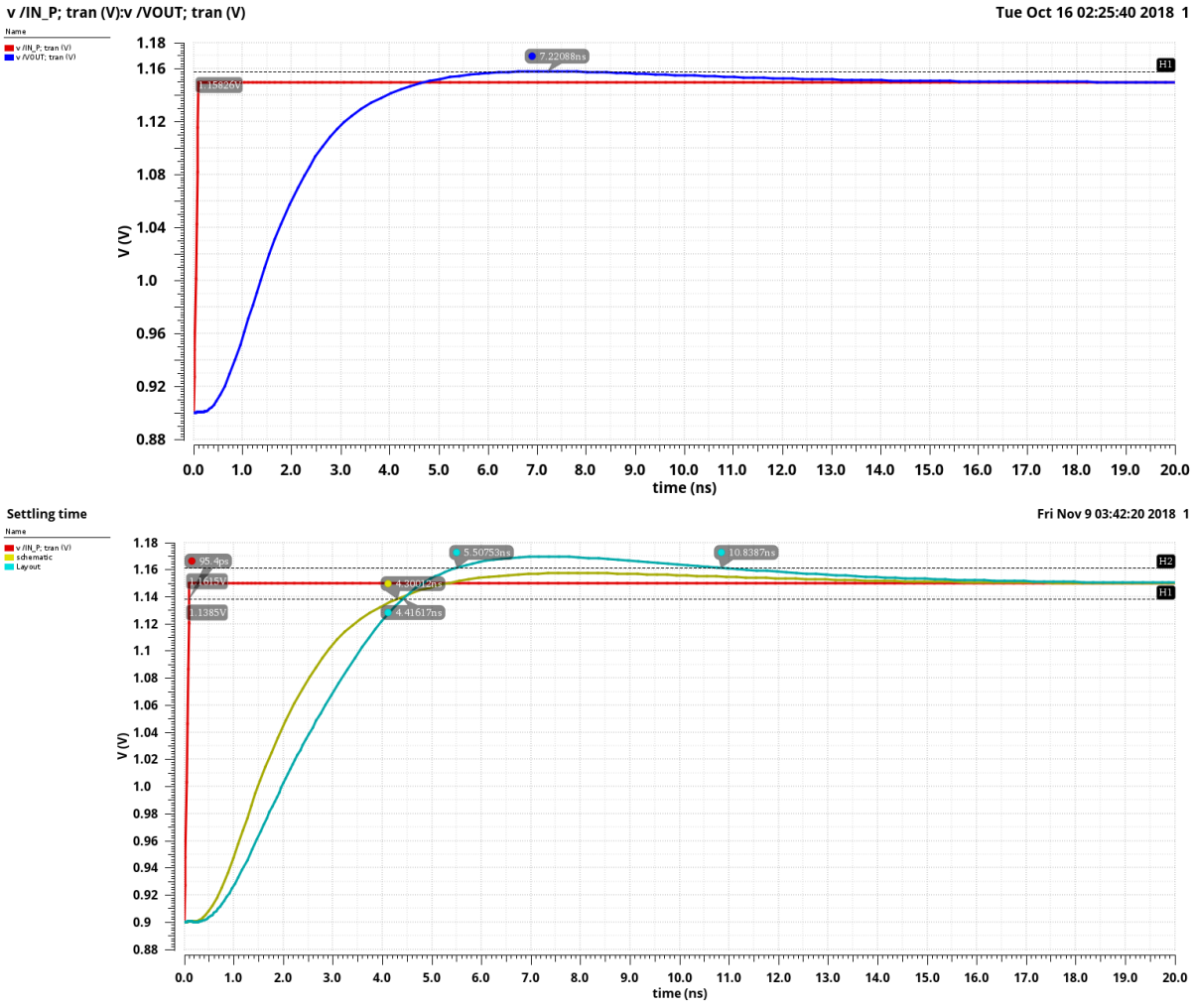
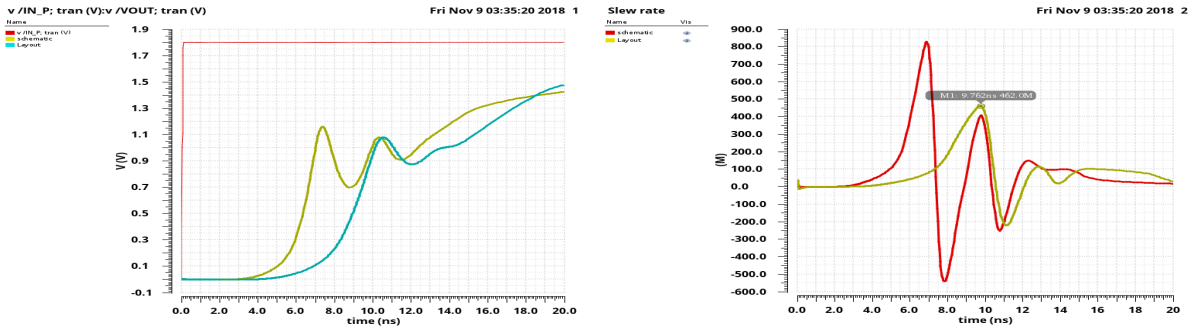


Figure 13: Settling Time

1% Settling Voltage = 1.1615 V, Settling time = 10.8387 ns



(a) Step Response (b) Derivative of Step Response

Figure 14: Slew Rate

$$\text{Slew Rate } = \max\left(\frac{dV_{out}}{dt}\right) = 462\ V/\mu s$$

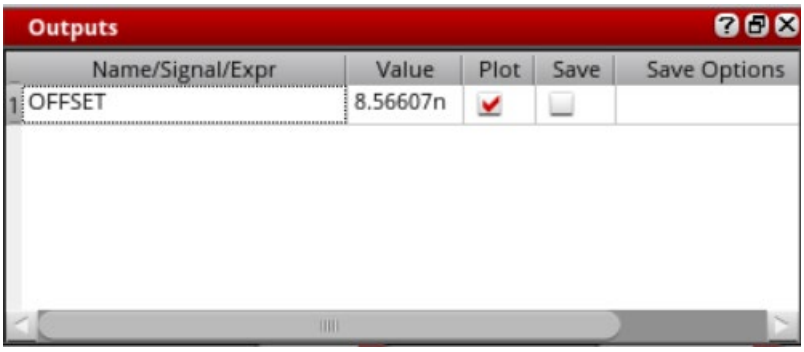


Figure 15: Systematic Offset

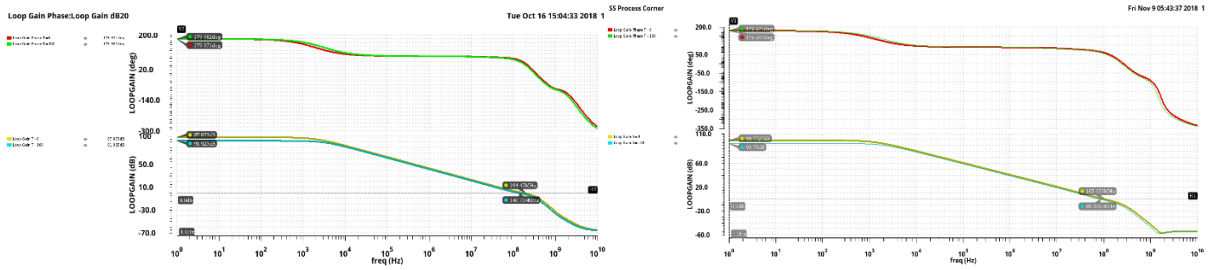
Offset by 8.566 nV.

Power Consumption

Total power consumed = Total Current × Operating Voltage

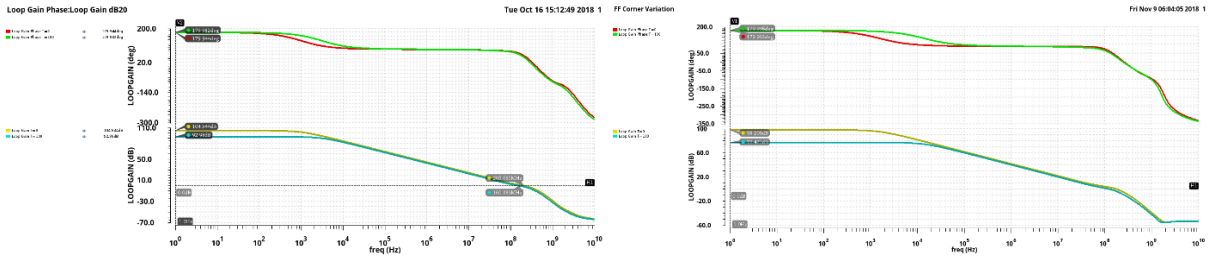
= 662 µA × 1.8 V = 1.191 mW ≤ 2 mW

Part II: Process Corners



(a) Schematic (b) Layout

Figure 16: Stability Analysis for SS process variation



(a) Schematic (b) Layout

Figure 17: Stability Analysis for FF process variation

Table 3: Variation in OTA with Process (Layout)

Corner	**SS**		**TT**	**FF**	
Temperature (°C)	**0**	**100**	**27**	**0**	**100**
DC Gain	98.7727 dB	93.76 dB	98.5745 dB	98.206 dB	77.471 dB
Unity Gain Frequency	105.95 MHz	85.303 MHz	106.2 MHz	179.47 MHz	125.32 MHz
Phase Margin	59.982°	61.889°	60.036°	35.276°	54.623 °