OTA Design

Specifications:

- DC gain ≥ 100 dB
- Output voltage swing ≥ 1 V_{p-p}
- Phase margin ≥ 60°
- Output load capacitance = 1 pF
- Unity gain frequency ≥ 90 MHz
- Slew rate ≥ 200 V /µs
- Input referred thermal noise ≤ 20 nV $/\sqrt{Hz}$

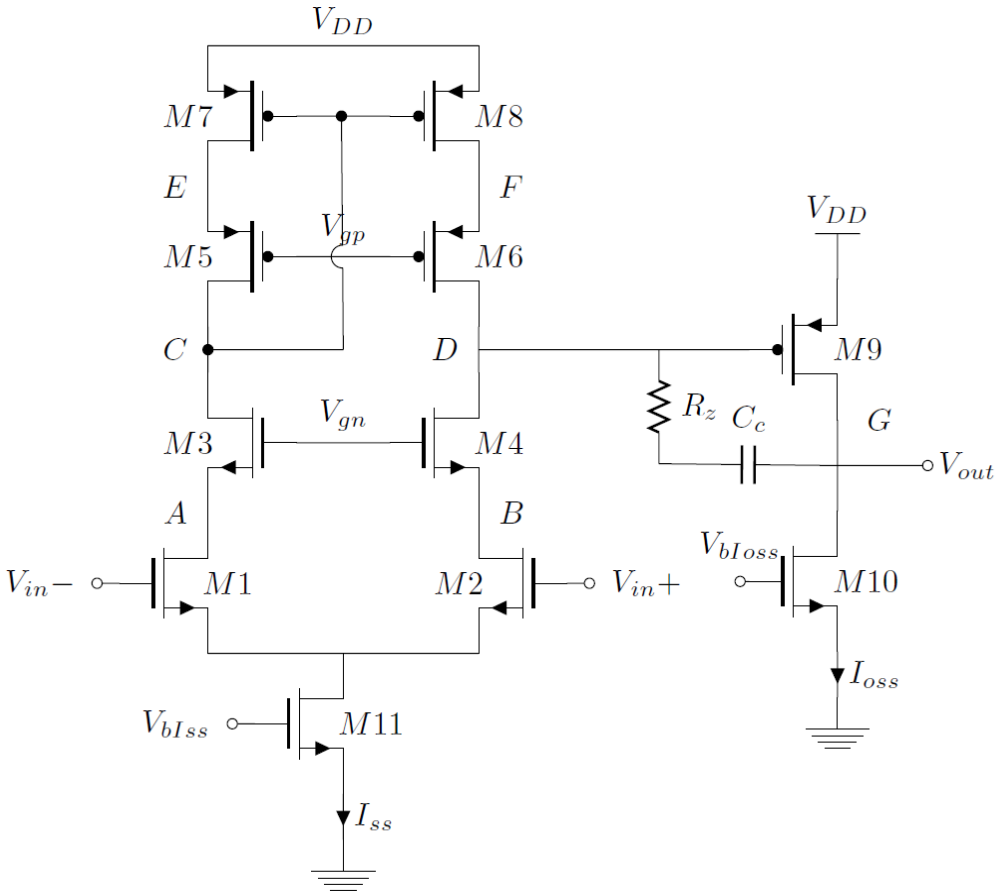


Figure 1: Two Stage Cascode (Telescopic) OTA with high swing

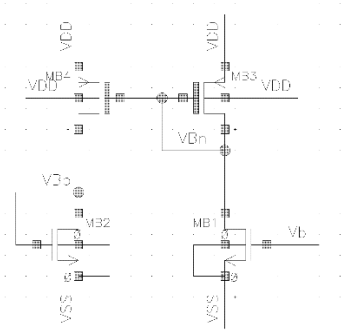


Figure 2: Biasing Circuit

Part I: Hand Calculations

SCL Process Parameters (180 nm)

K_n 263 µA/V^2

V_{Tn} 0.48 V

K_p 63 µA/V^2

V_{Tp} 0.4 V

Input Referred Thermal Noise

Input referred thermal noise for cascode amplifier shown in figure 1, is given by:

$$\overline{V_{n,eq}^2} = 2\left(\overline{V_{n,eq}^2} + \frac{g_{m7}^2}{g_{m1}^2}\right)$$

$$= \frac{8kT\gamma}{g_{m1}}\left[1 + \frac{g_{m7}}{g_{m1}}\right]$$

Assuming that $g_{m7} << g_{m1}$ for simplification (although not true), the above equation becomes

$$\overline{V_{n,eq}^2} = \frac{16kT}{3}\frac{1}{(10 \times 10^{-9})^2}$$

$g_{m1} \geq 53.33$ µS

Let's assume g_{m1} = 60 µS.

$$\left(W/L\right)_1 = \frac{g_{m1}^2}{I_{ss} \times K_n}$$

$$= \frac{60^2}{20 \times 263} = 0.57$$

Since we can work with $\left(W/L\right)$ values not smaller than 1, we use $\left(W/L\right)_1 = 1$

Unity Gain Frequency

$$2\pi f_{ug} = \text{DC Gain} \times P_D$$

$$= \frac{g_{m1}}{C_C}$$

According to specification,

$$C_C = \frac{g_{m1}}{2\pi \times 90 \times 10^6}$$

$$C_C \leq 0.094\ pF$$

Slew Rate

$$\frac{dV_{out}}{dt} = \frac{I_{ss}}{C_C} \; and$$

$$I_{oss} \geq I_{ss}\left(1 + \frac{C_L}{C_C}\right)$$

According to specification,

$$\frac{I_{ss}}{C_C} \geq 200\, V/\mu s$$

$$I_{ss} \geq C_C \times 200 \times 10^6 = 18.8\, \mu A$$

Let's assume I_{ss} = 20 µA. Therefore

$$I_{oss} \geq 20\left(1 + \frac{1}{0.09}\right)\, \mu A = 242\, \mu A$$

Let's assume I_{oss} = 250 µA.

Output Swing

$$V_{\mathrm{Dsat9}} = \sqrt{\frac{2 \times I_{oss}}{K_p \times \left(W/L\right)_9}}$$

$$= \sqrt{\frac{2 \times 250}{62 \times 75}} = 227\, mV\; (which\; is\; good\; enough)$$

Similiarly for a V_{Dsat10} of 250 mV, we have

$$\left(W/L\right)_{10} = \frac{2 \times I_{oss}}{{V_{\mathrm{Dsat10}}}^2 \times K_n}$$

$$= \frac{2 \times 250}{0.25^2 \times 263} = 30$$

Phase Margin

$$\emptyset = 90° - tan^{-1}\left(\frac{f_{ug}}{f_{ND}}\right)$$

$$= 90° - tan^{-1}\left(\frac{g_{m1}/C_C}{g_{m9}/C_L}\right)$$

For a phase margin of 60°,

$$g_{m9} \geq 2\pi \times C_L \times f_{ND}$$

$f_{ND} = 155.88\ MHz; C_L = 0.09\ pF$

$$\Rightarrow \quad g_{m9} \geq 1.5\ mS$$

$$\left(W/L\right)_9 = \frac{g_{m9}^2}{2 \times I_{oss} \times K_p}$$

$$= \frac{1500^2}{2 \times 250 \times 62} = 73.4$$

Let's assume $\left(W/L\right)_9 = 75$ (It will only result in better PM).

Zero Systematic Offset

Zero systematic offset requires $|V_{gs7}| = |V_{gs9}|$. Therefore

$$\left(W/L\right)_7 = \frac{I_{ss}}{2 \times I_{oss}} \times \left(W/L\right)_9 = 2.88$$

We use $\left(W/L\right)_7 = 3$.

DC Gain

$$A_v = \frac{2g_{m1}(g_{m4} + g_{m6})g_{m9}}{\lambda^3 \times I_{ss}^2 \times I_{oss}}$$

For L_N = 0.55 µm, λ = 0.747. That gives $L_P \approx$ 0.35 µm.

Plugging the value of λ in the gain equation, we get $g_{m4} + g_{m6} = 215.37\ \mu S$.

This can be satisfied by taking $\left(W/L\right)_{3,4}$ and $\left(W/L\right)_{5,6}$ = 8.

Table 1: Calculated Transistor Parameters [Figures 1 and 2]

	W/L	W(in µm)	L(in µm)
M1	1	0.35	0.55
M2	1	0.35	0.55
M3	8	4.4	0.55
M4	8	4.4	0.55
M5	8	2.8	0.35
M6	8	2.8	0.35
M7	3	1.05	0.35
M8	3	1.05	0.35
M9	75	18	0.35
M10	30	16.5	0.55
M11	2	1.1	0.55
M12	1	0.55	0.55

Table 2: Other Components

R_Z	4.54338K
C_C	0.09 pF

Part II

Meeting Specifications

It can be immediately observed that the specifications are not met, when simulations are run with the above parameters are plugged into Cadence. As mentioned earlier, the contribution of $M_{7,8}$ to noise is not negligible and needs to be accounted for. To ensure that the input referred noise stays below the limit, the ratio $\left(W/L\right)_1$ is increased. More remarkably, gain and phase margin are off by a huge margin. Also, $\left(W/L\right)_9$ is doubled to double the gain of M_9. However, I_{oss} is also doubled by doubling $\left(W/L\right)_{10}$ to maintain V_{dsat} of M_9. To further increase gain, ratio $\left(W/L\right)_3$ and ratio $\left(W/L\right)_5$ are increased. Phase margin is also improved when the gain of M_9 is doubled. To further increase PM, the value of C_C is increased. However, I_{SS} also has to be increased to meet the slew rate condition.

Final Design

Table 3: Transistor parameters

	W/L	W (in µm)	L(in µm)
M1	6	3.3	0.55
M2	6	3.3	0.55
M3	16	8.8	0.55
M4	16	8.8	0.55
M5	20	7	0.35
M6	20	7	0.35
M7	4	1.4	0.35
M8	4	1.4	0.35
M9	150	52.5	0.35
M10	112	61.6	0.55
M11	6	3.3	0.55
M12	2	1.1	0.55
M13	2	1.1	0.55
Mx	8	2.8	0.35
My	20	7	0.35
Mz	30	10.5	0.35
MB1	2	1.1	0.55
MB2	2	1.1	0.55
MB3	6	2.1	0.35
MB4	6	2.1	0.35

C_C = 0.17 pF

Simulated Results

Table 4: Simulation Results

DC Gain	100.245 dB
Unity Gain Frequency	166.69 MHz
Phase Margin	60.216°
Slew Rate	223.57 V/µs
Input Referred Thermal Noise	18.0282 nV
Settling Time	7.22088 ns
Common Mode Gain	7.714 dB
Output Swing	1.06 V
$PSRR_{VDD}$	100.19 dB
$PSRR_{VSS}$	106.094 dB
CMRR	92.531 dB
Input Common Mode Range	[709 mV, 1.225 V]
Power	1.188 mW

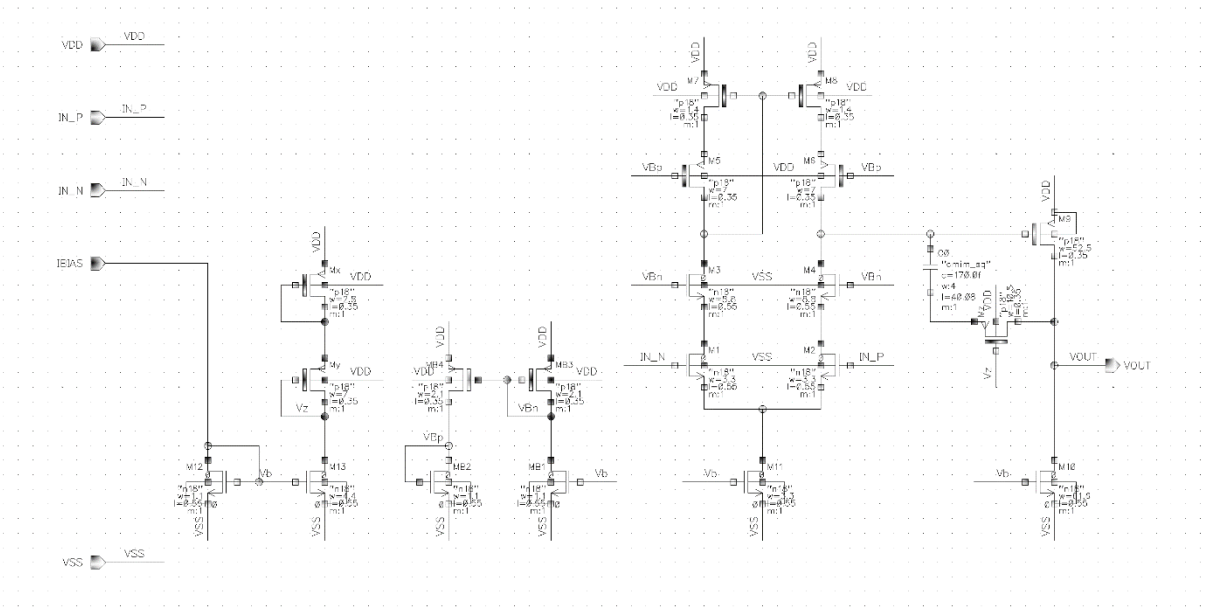


Figure 4: Schematic

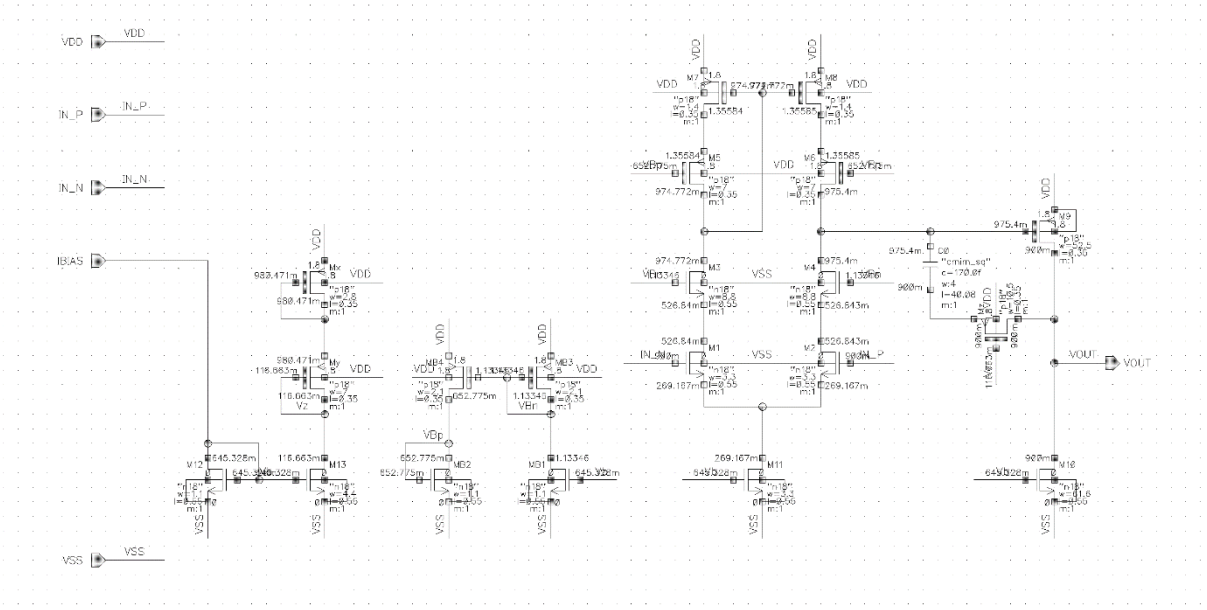


Figure 5: DC Analysis

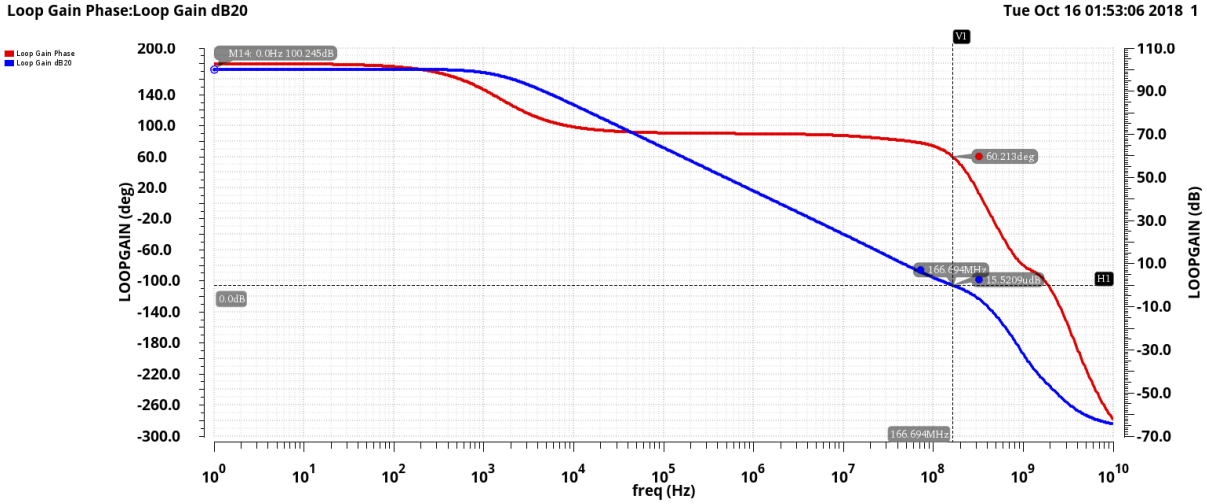


Figure 6: STB Analysis

Dc gain = 100.254 dB, Unity gain Frequency = 166.69 MHz , Phase Margin = 60.216°

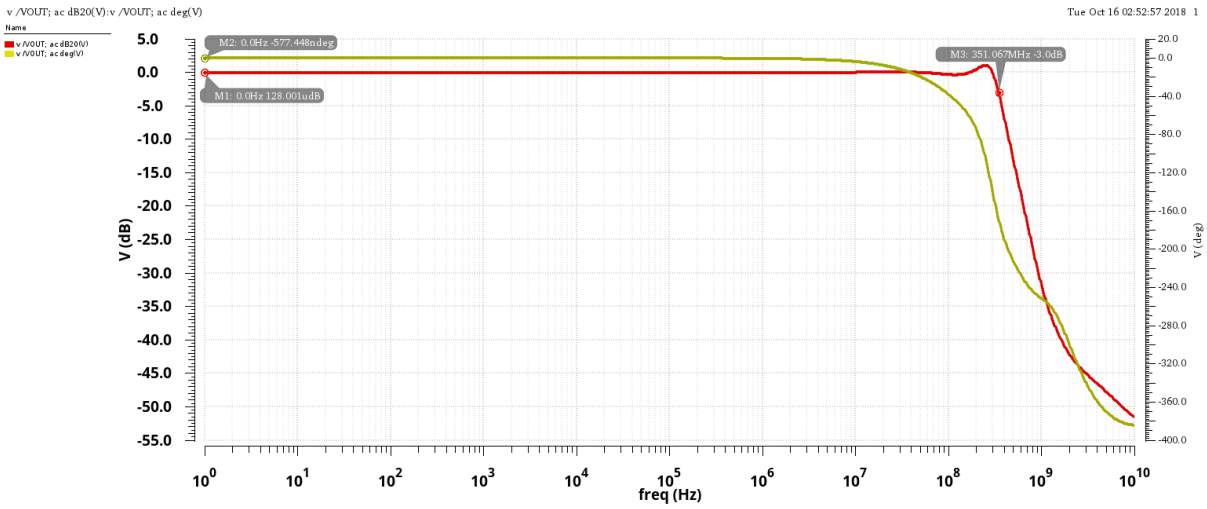


Figure 7: Closed-Loop Gain

V_{out} = 0 dB, Phase = 0°. 3 dB Frequency = 351.067 MHz

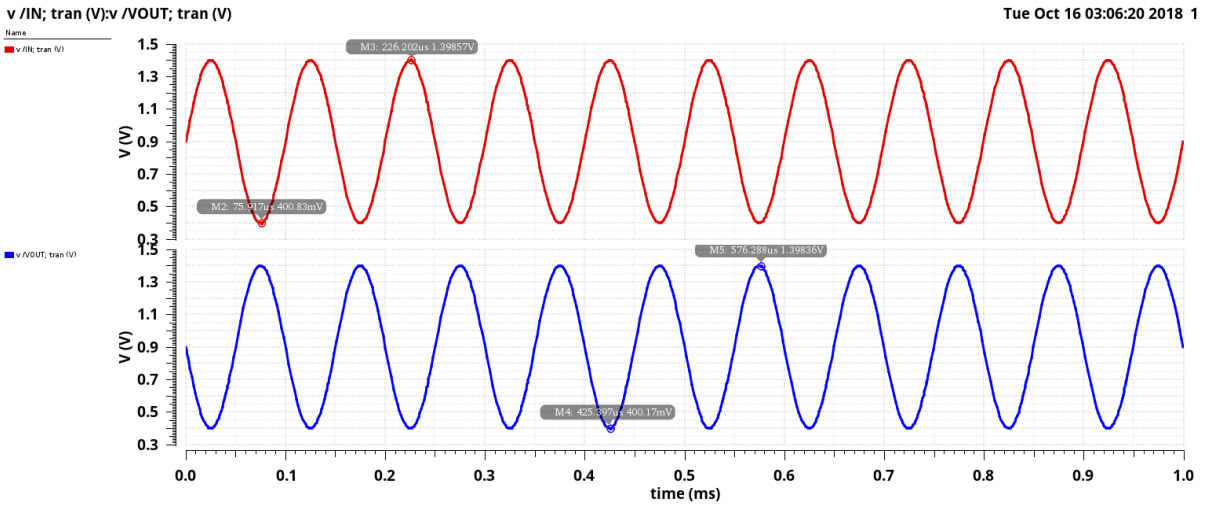


Figure 8: Closed-Loop Transient Response

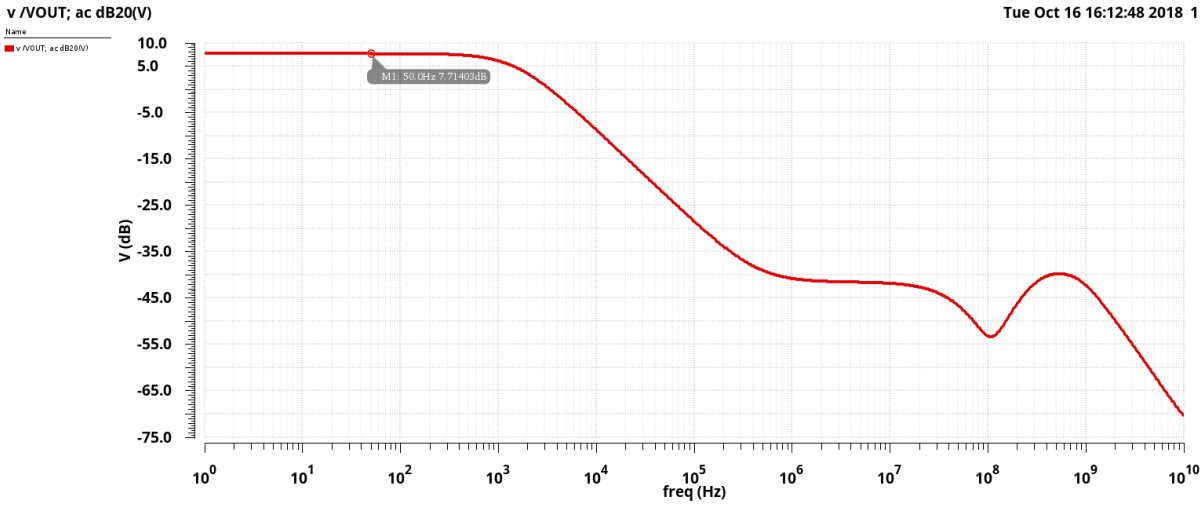


Figure 9: Common Mode Gain

A_{CM} = 7.714 dB, So CMRR = 20×(ln A_{dm} – ln A_{cm}) = 92.531 dB

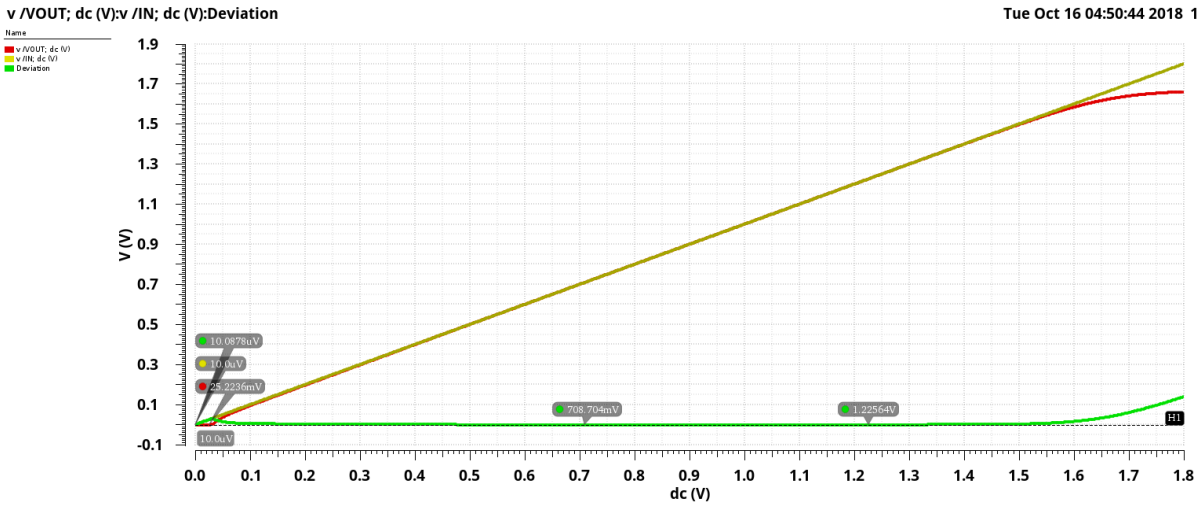
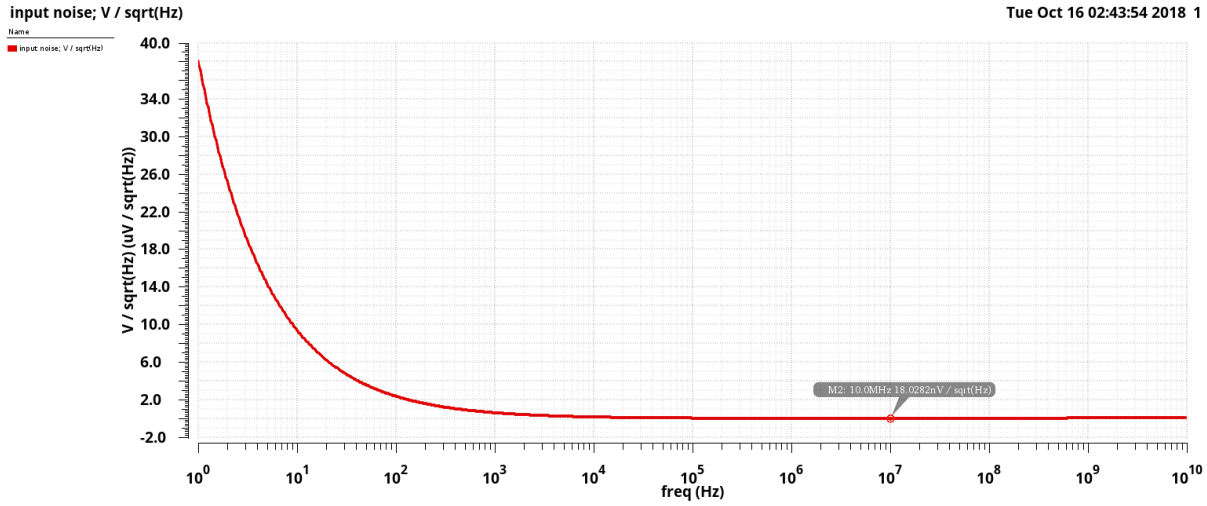


Figure 10: Input Common Mode Range

ICR = 708 mV to 1.225 V



(a) Input referred noise PSD from 1Hz to 1GHz

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Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000285944
Total Input Referred Noise = 0.000291275
The above noise summary info is for noise data
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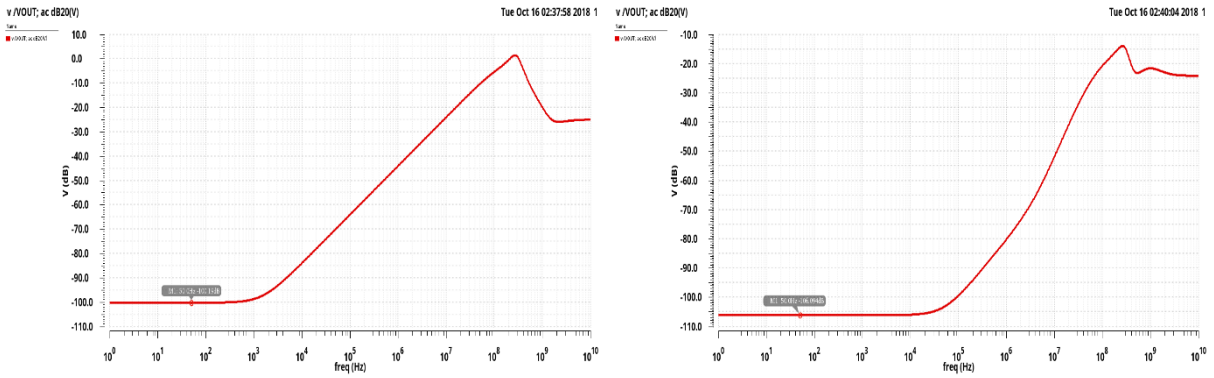
(b) Observed integrated noise voltage over the unity gain bandwidth

Figure 11: Input Referred Noise



(a) $PSRR^+$ (b) $PSRR^-$

Figure 12: Power Supply Rejection Ratio

$PSRR^-$ = 106.094 dB

$PSRR^+$ = 100.19 dB

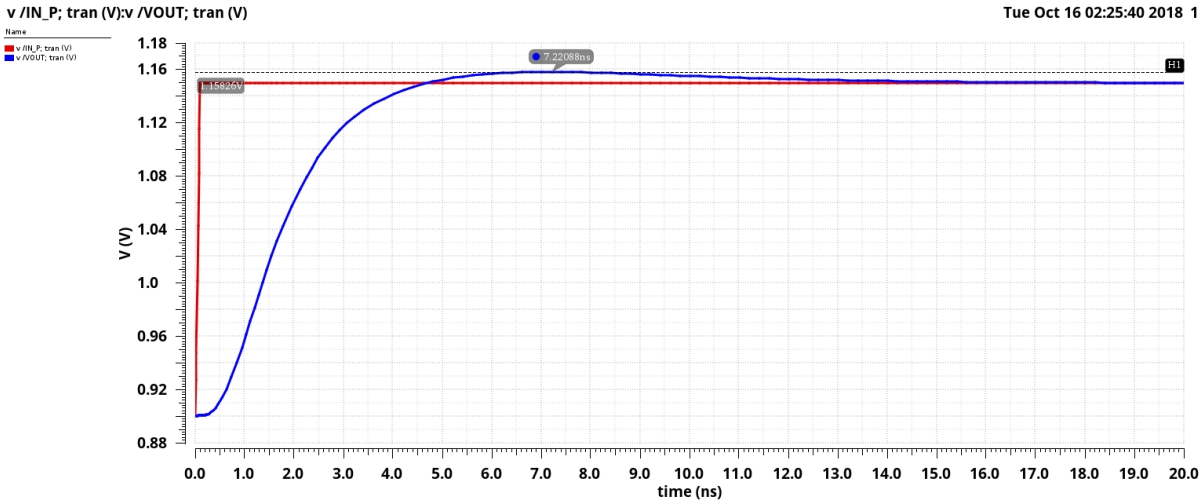
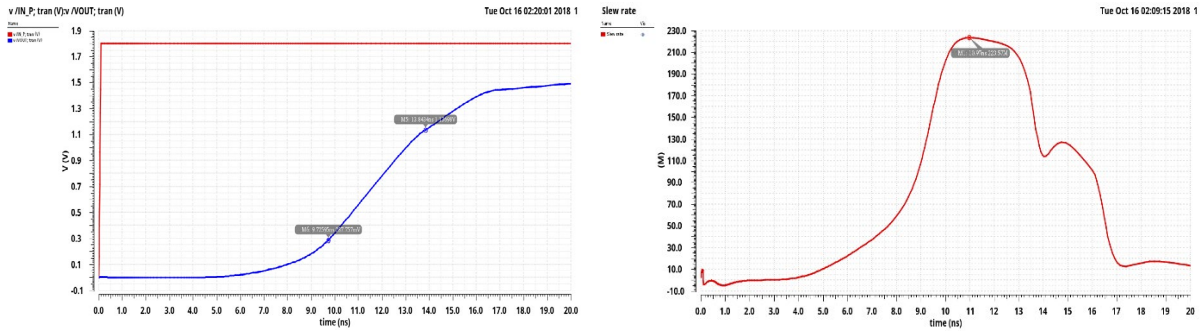


Figure 13: Settling Time

1% Settling Voltage = 1.1615 V, Settling time = 7.22088 ns



(a) Step Response (b) Derivative of Step Response

Figure 14: Slew Rate

$$\text{Slew Rate } = \max\left(\frac{dV_{out}}{dt}\right) = 223.57\ V/\mu s$$

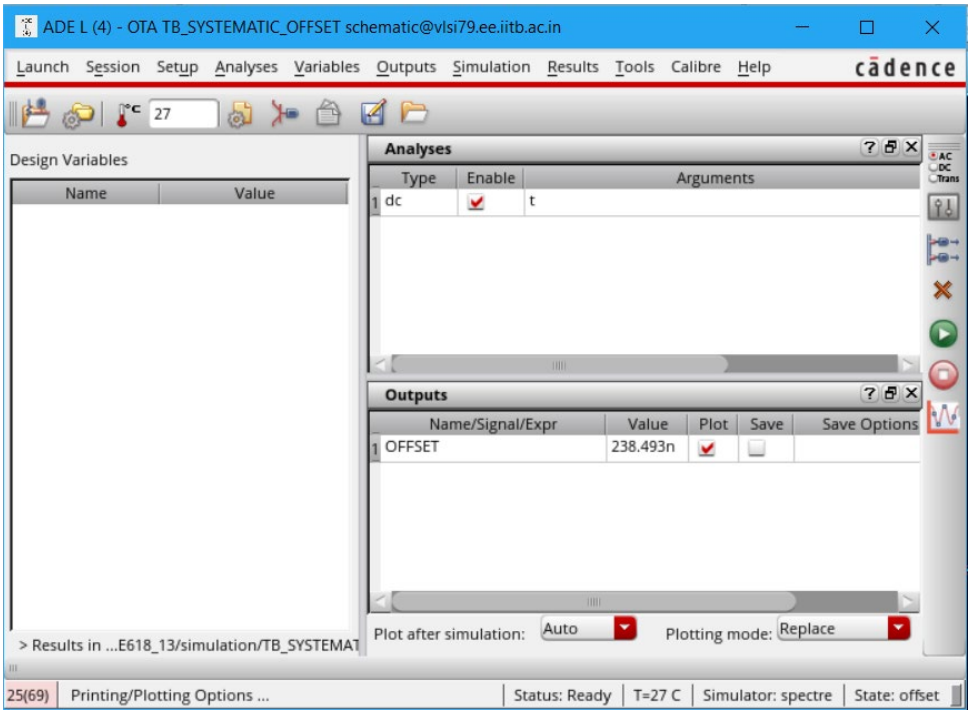


Figure 15: Systematic Offset

Offset by 0.24 µV.

Power Consumption

Table 6: Current Drawn from Source

M11	30 µA
M12	10 µA
M13	40 µA
M10	560 µA
MB1	10 µA
MB2	10 µA

Total power consumed = Total Current × Operating Voltage

= 660 µA × 1.8 V = 1.188 mW ≤ 2 mW

Output Swing

From DC Analysis,

$VD_{sat9} = |V_{gs9}| - |V_{th9}| = 975.4\ mV - 431.782\ mV = 543.618\ mV$

$VD_{sat10} = V_{gs10} - V_{th10} = 645.328\ mV - 444.323\ mV = 201.005mV$

$\therefore$ Output Swing = $V_{DD} - V_{Dsat9} - V_{Dsat10}$ =

$1.8\ V - 543.618\ mV - 201.005\ mV = 1055.377\ mV \approx 1.06\ V$

Part III: Process Corners

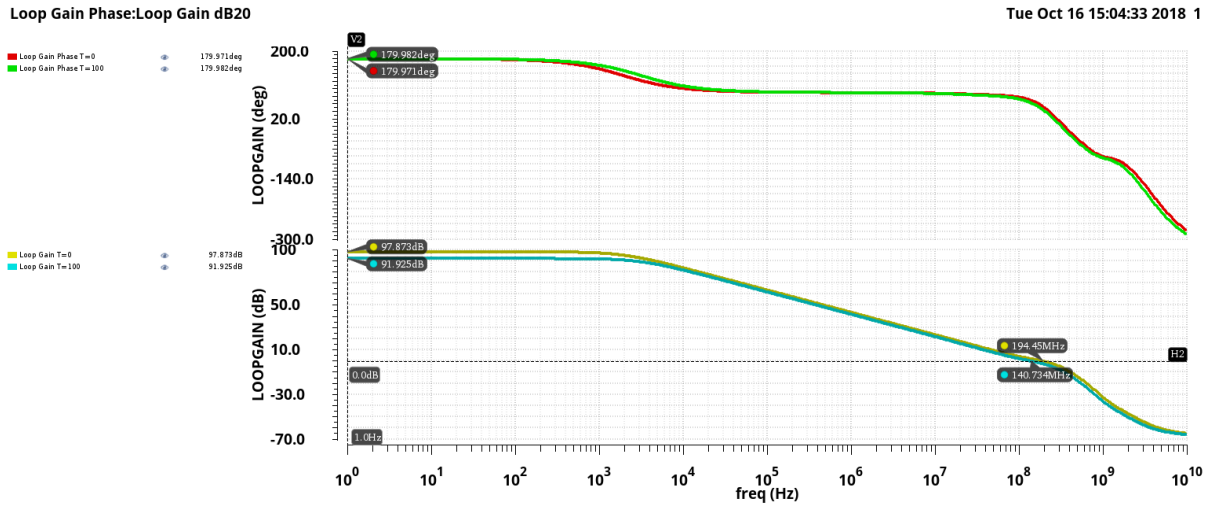


Figure 16: Stability Analysis for SS process variation

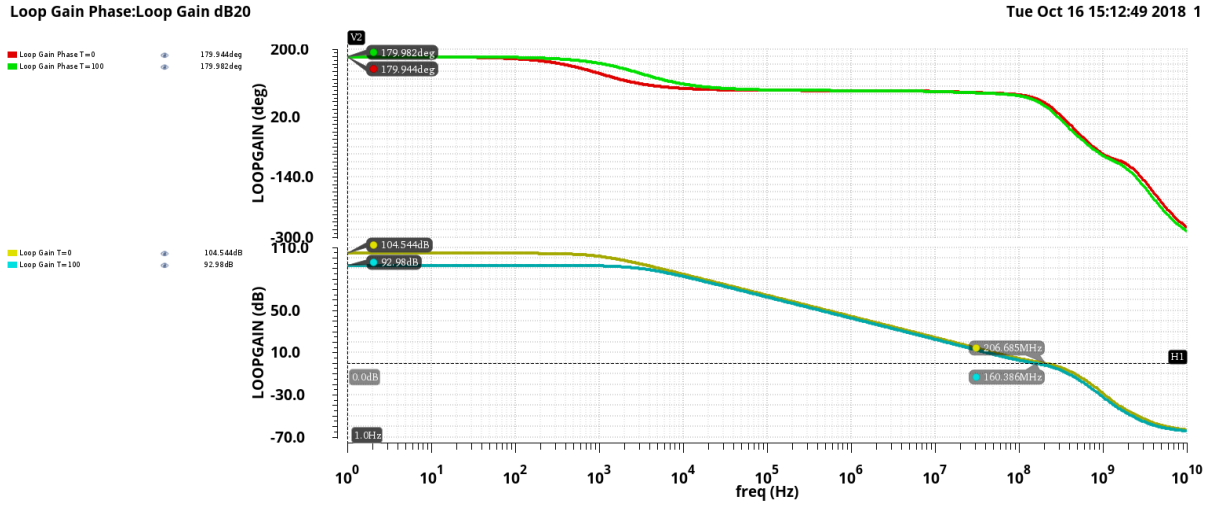


Figure 17: Stability Analysis for FF process variation

Table 6: Variation in OTA with Process

Corner	SS		TT	FF	
Temperature (°C)	**0**	**100**	**27**	**0**	**100**
DC Gain	97.873 dB	91.925 dB	100.254 dB	104.544 dB	92.98 dB
Unity Gain Frequency	194.45 MHz	140.734 MHz	166.69 MHz	206.685 MHz	160.386 MHz
Phase Margin	53.44°	62.852°	60.216°	57.35°	63.371°