EE618(Zele)
CMOS Analog IC Design

Course Project - II.
Deadline : 5^{th} November 2018 11:55 PM
Total Marks : 50

Part-I: Layout

For the OTA (fully differential input single ended output) designed in course project -I,

- Layout the OTA designed in course project - I (except for load cap and current source) in SCL 180nm process technology. Use common centroid and other layout matching techniques wherever needed.
- Layout the design with minimum area.
- All the input pins (IN_P, IN_N, IBIAS) must be routed to the left side of the layout boundary and the output (VOUT) to the right side of layout boundary.
- Run the DRC and LVS checks and attach the DRC and LVS log file for submission.
- Once DRC and LVS is cleaned run the RC (coupled) extraction and generate the calibre view.

Part-II: Characterization

Perform all the characterization on the calibre view (post layout view) as done in course project-I. Use the testbench library provided for course project - I. Tabulate the Opamp Specifications as shown below. Compare the schematic and layout results in the table.

Parameter	Schematic	Layout
DC gain		
Unity Gain frequency		
Phase Margin		
Slew Rate		
Output Swing (V_{p-p})		
Settling Time (1% accuracy)		
RMS Thermal Noise Voltage		
CMRR		
PSRR		
ICR (Input Common Mode Range)		
Power		
Area	-	

NOTE: Mention area as a $\times$ b, where a and b are length and height in μm respectively. Eg: 25μm $\times$ 35μm.

Part-III: Report and Poster Presentation

Students will report the layout and the results. The report will have three slides. The content of the slides are as below

- Slide 1: Schematic of the OTA with Width, Length, R and C values annotated (Use Xcircuit or any other tool to draw the schematic).
- Slide 2: High resolution screenshot of the layout clearly indicating all the ports. Mention the area in the same slide.
- Slide 3: Table comparing the schematic and the post layout simulation results (The table in part - I)

This report needs to be uploaded on moodle. The slides will be used to create a poster for the poster presentation competition.

Grading

- Layout : 20 Marks.
- Simulation Results/comparing result with schematic : 20 Marks.
- Report + Poster presentation participation : 10 Marks.
- Bonus points (Based on parameters below) : 10 Marks.

Bonus Parameters: Optimal area, symmetry of the layout and correlating RC extraction (post-layout) results with schematic results.

Place, Route, Run and have fun !!! ☺