DDL, Измерение сигналов, TDC

TDC

- time-to-digital converter
- Определение временного интервала между событиями
- У счетчиков низкая скорость
- Например, лидары

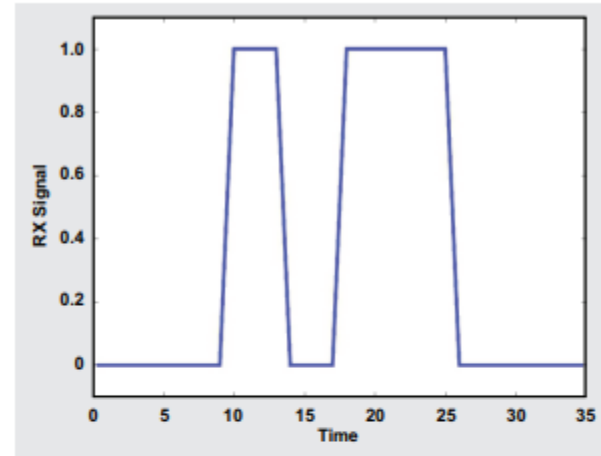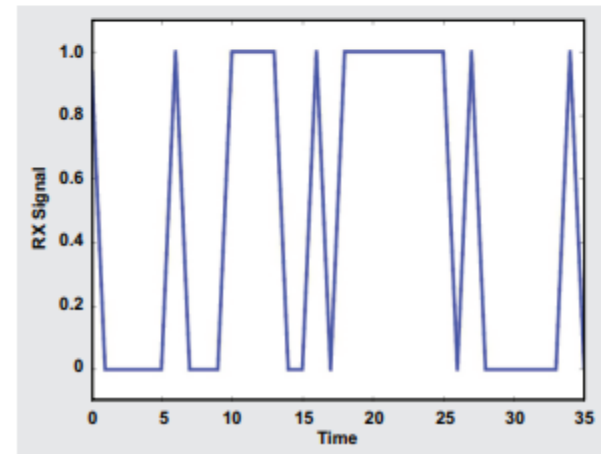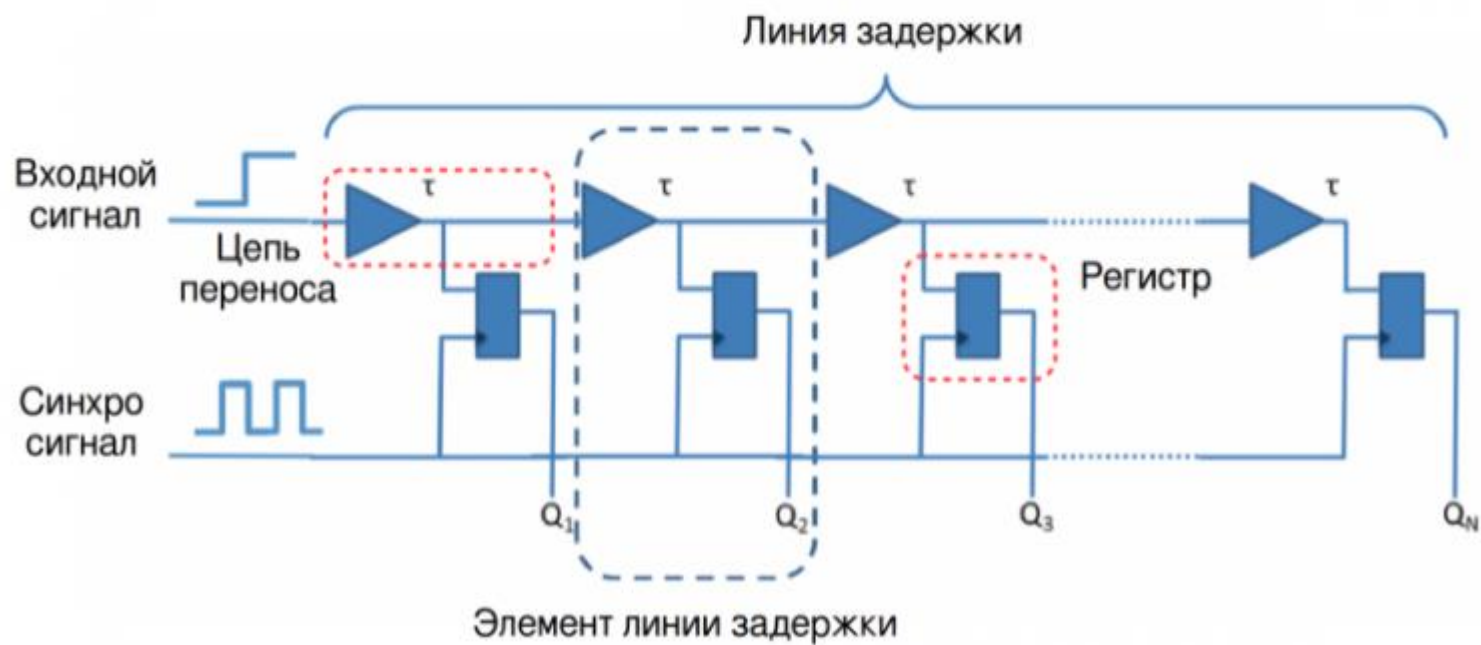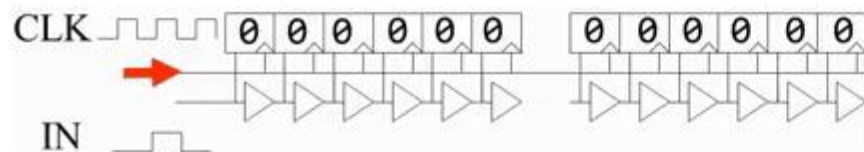Figure 4. The output of the comparator in the absence of noise*
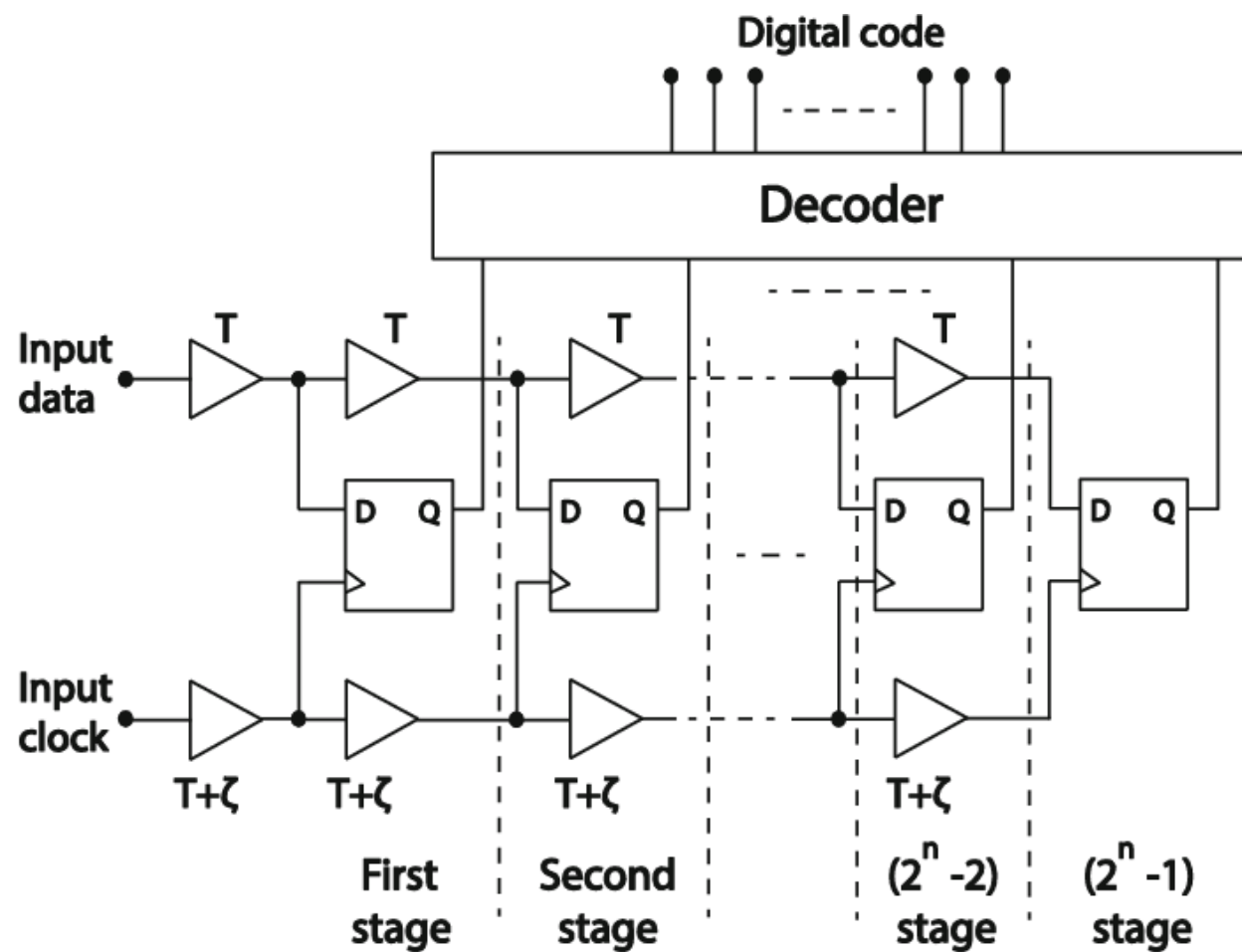

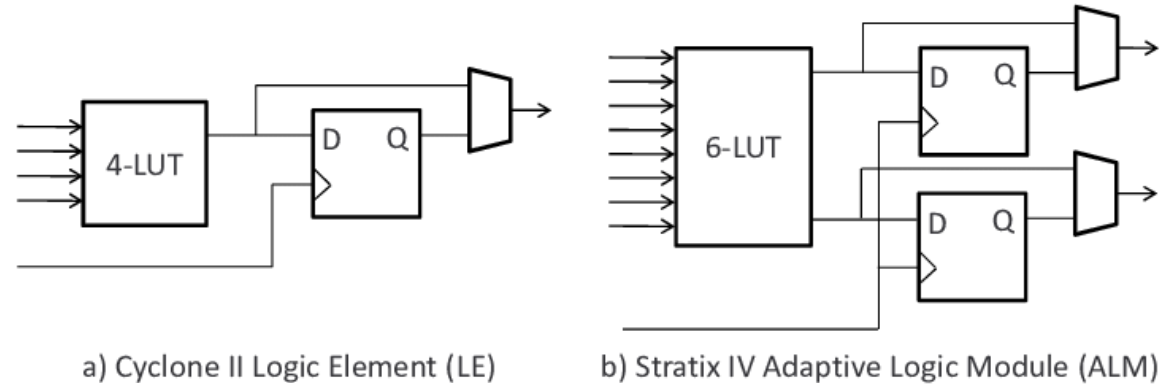Figure 5. Output of the comparator feeding the TDC in the presence of noise

TDC субтактовая линия

TDC линия Вернье

TDC реализация

a) Cyclone II Logic Element (LE)   b) Stratix IV Adaptive Logic Module (ALM)

Example 2–18. LCELL Primitive Instantiation, Verilog HDL

```
lcell <instance_name> (.in(<input_wire>), .out(<output_wire>);
```

Syntax	`set_location_assignment` [-h | -help] [-long_help] [-comment <comment>] [-disable] [-remove] -to <destination> [<value>]

Arguments		
`-h` | `-help`	Short help
`-long_help`	Long help with examples and possible return values
`-comment` <comment>	Comment
`-disable`	Option to disable assignment
`-remove`	Option to remove assignment
`-to` <destination>	Destination of assignment
<value>	Assignment value