

PC - 5000

SHARP SERVICE MANUAL

CODE: 00ZPC5000S / ME



MODEL **PC-5000**

(CE-510P OPTION)
(CE-100M OPTION)

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SHARP CORPORATION

CHAPTER 1 GENERAL DESCRIPTION

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[1] GENERAL DESCRIPTION

1-1. Products outline

The last few years have seen marked improvements in the pocket and personal computer field. This has greatly advanced the dawn of the office and personal automation age.

To satisfy this growing market, sharp has designed a portable computer that incorporates the features that are necessary for personal information processing. The new sharp PC-5000 is making the dream of personal information processing a reality. In addition to the large, highly accurate, liquid crystal display unit, full advantage of the latest in solid state technologies have been used, such as a battery powered thermal printer, low power consumption, CMOS CPU and bubble memory. The thermal printer is incorporated in the model PC-5001.

1-2. Specifications of main unit

1-2-1. Basic functions

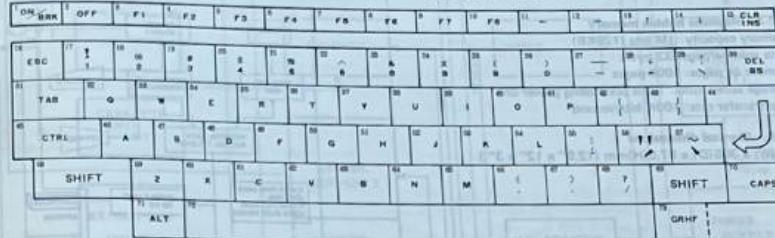
- The main unit is extremely portable, and is powered by a rechargeable lead battery source. The unit can also be powered via an AC adapter which doubles as a battery charger.
- The LCD display, full size keyboard, bubble memory, and printer (PC-5001 only) are in one self-contained unit. The bubble memory cassette and printer are optional equipment.
- A compact floppy disk and expansion RAM are also available as options.

1-2-2. Keyboard

Key contact type: Mechanical switch contact.

Keypad markings are in two colors.

Key travel: 4 ± 0.5 mm



1-2-3. Liquid crystal display

Effective display area: $228.95 \times 81.95\text{mm}$ ($9.09'' \times 3.25''$),
 640×80 dot matrix.

Contrast adjustment: By means of a VR.

Display characters (column x row)	Display pattern (dots)	Character size (mm/in)
AN 80 x 8	5 x 7	1.75 x 2.8 mm 0.07" x 0.11"
Printing character type	Maximum printing positions	Character pitch (mm/in)
Character pitch (mm/in)	Dot size (mm/in)	Dot pitch (mm/in)
2.8 mm 0.1"	0.3 x 0.35 mm 0.011" x 0.013"	0.35 mm 0.013"

AN = Alphanumeric

1-2-4. Thermal printer (CE-510)

Printing sequence: character by character

Printing speed: 37 c/s (elite), 30 c/s (pica)

Paper feed: Friction feed

Linefeed speed: 19mm/sec

Print form width: 220mm, max. (8.6")

Ink ribbon: Replaceable ink cartridge, approx. 100m long (571.3")

Ink color: Black

Printing dot heads: 24
Expected service life: 1 million lines ($\times 60\text{kM}$)

Printing character type	Maximum printing positions	Character pitch (mm/in)	Character size (mm/in)
AN	80 chars	2.1 mm 0.082"	1.7 x 2.4 mm 0.068 x 0.091"
Printing character type	Printing pattern (dots)	Dot pitch (mm/in)	Linefeed pitch
AN	12 x 17 (Elite) 15 x 19 (Pica)	0.4 mm 0.015 in	1/6", 1/4"

1-2-5. Power supply

Power source: 6V DC rechargeable lead battery

Recharge time: About 8 hours

Operating time: About 6 hours

AC adaptor: EA-56

1-26. LS

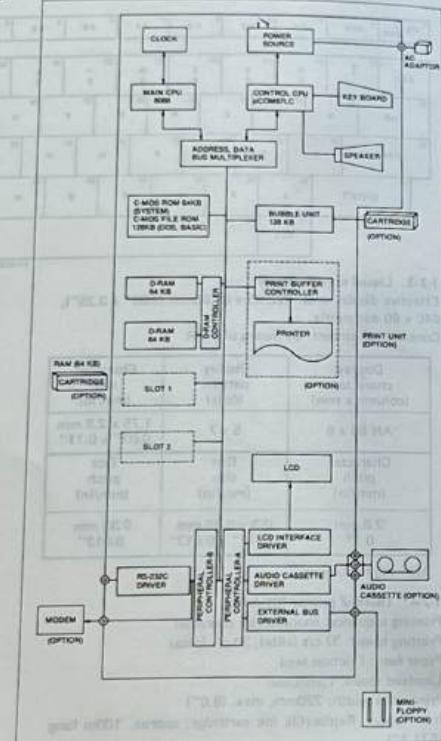
Item	Type	No. of Pins
Main CPU	μ PD8088	40
Local CPU	SC78026G	64
Peripheral control A	SC65010G24	44
Peripheral control B	SC65010G29	44
DRAM control	LH5703	48
Control multiplexer	LH5704	60
Address multiplexer	LH5705	96
Real time clock	146818P	24
D-RAM	μ PD4164G	16
256K (Low-speed) ROM	61256FC	44
256K (Hi-speed) ROM	613256FPC	54
LCD backplate driver	LH5030	96
LCD segment driver	LH5035	96

1.2.7. Magnetic bubble memory

1-2-7. Magnetic bubble memory
Memory capacity: 1 MB (128KB)
Data volume/page: 32 bytes
Number of pages: 4096 pages
Average access time: 13 ms (excluding power on)
Data transfer rate: 100 Kbit/second

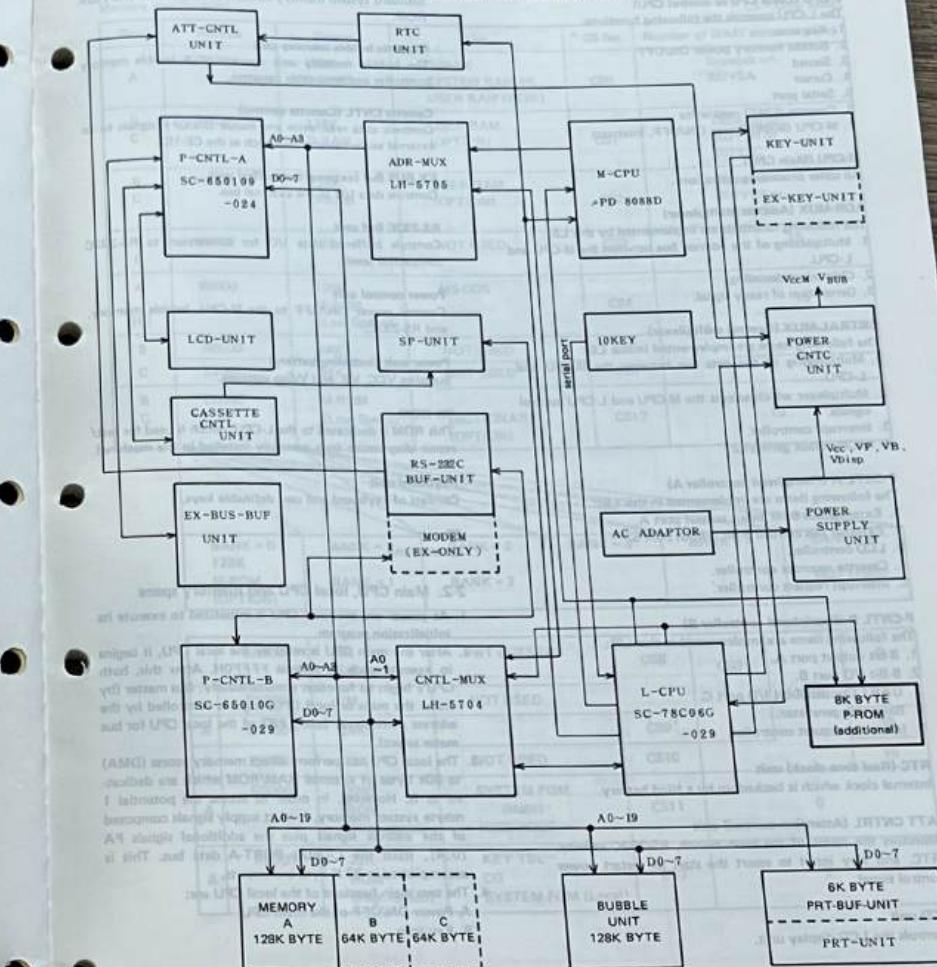
1-2-8 Physical dimensions

326(W) x 305(D) x 87.5(H)mm (12.9" x 12" x 3").



- Computer on!

[2] BLOCK DIAGRAM OF MAIN UNIT



2-1. Block diagram description**L-CPU (Local CPU or control CPU)**

The L-CPU controls the following functions:

1. Key scan
2. Bubble memory power ON/OFF
3. Sound
4. Cursor
5. Serial port
6. Cassette (CMT) read/write
7. M-CPU (B088) Power ON/OFF, interrupt

M-CPU (Main CPU)

All other processing operations.

ADR-MUX (Address multiplexer)

The following functions are implemented by this LSI:

1. Multiplexing of the address bus between the M-CPU and L-CPU.
2. Chip select decoding.
3. Generation of ready signal.

CNTRAL-MUX (Control multiplexer)

The following items are implemented in this LSI:

1. Multiplexing of the data bus between the M-CPU and L-CPU.
2. Multiplexer which selects the M-CPU and L-CPU control signals.
3. Interrupt controller.
4. M-CPU clock generator.

P-CNTL A (Peripheral controller A)

The following items are implemented in this LSI:

1. External bus 8-bit input output port A.
2. External bus control 8-bit output port S.
3. LCD controller.
4. Cassette recorder controller.
5. Interrupt request controller.

P-CNTL B (Peripheral controller B)

The following items are implemented in this LSI:

1. 8-bit output port A.
2. 8-Bit I/O port B.
3. UART Control 4-bit I/O port C.
4. Baud rate generator.
5. Interrupt request controller.

RTC (Real time clock) unit

Internal clock which is backed up by a NiCd battery.

ATT CNTRL (Attention control) unit

Monitors the states of the main switch, RS-232C activity, RTC, and Key input to assert the start or restart power control signal.

LCD unit

Controls the LCD display unit.

PRT (Printer) unit

Consists of the thermal printer and printer buffer (SRAM).

Memory unit

Standard system memory consists of 128K RAM and 182K ROM.

Magnetic bubble memory unit

The bubble memory unit consists of a bubble memory controller and removable cassettes.

Cassette CNTL (Cassette control)

Controls data read/write and motor ON/OFF signals to an external audio cassette unit such as the CE-152.

EX-BUS Buf (external bus buffer) unit

Controls data I/O to the external bus.

RS-232C Buf unit

Controls buffered data I/O for conversion to RS-232C compatible levels.

Power control unit

Controls power ON/OFF to the M-CPU, bubble memory, and RS-232C.

Power unit (including battery)

Supplies VCC, VB, and Vdisp voltages.

8K-ROM

This ROM is dedicated to the L-CPU, which is used for test/repair diagnostics (not normally installed in the machine).

Keyboard unit

Consists of keyboard and user definable keys.

SP unit

Speaker unit.

2-2. Main CPU, local CPU and memory space

1. At power on, the local CPU is initialized to execute its initialization program.
2. After the main CPU is reset by the local CPU, it begins to execute code at address FFFF0H. After this, both CPU's begin to function simultaneously. Bus master (by either the main or local CPU) logic is controlled by the address multiplexer (using PB3 of the local CPU for bus master select).
3. The local CPU can perform direct memory access (DMA) to 60k bytes of external RAM/ROM which are dedicated to it. However, in order to access the potential 1 mbbyte system memory, it must supply signals composed of the address signals plus the additional signals PA [0:4], from the L-CPU's PORT-A data bus. This is accomplished in 32 K byte increments.
4. The two main functions of the local CPU are:
 - A. Power ON/OFF of the main CPU
 - B. Key scan

2-3. Memory I/O map**Memory map (system)**

Slot	Address	Device	Use	* CS No.	Number of WAIT states required
A	00000	128K D-RAM	CUP 1K SYSTEM RAM 4K USER RAM (123K)	CS0	Depends on RDYSA
B	20000	128K D-RAM	USER RAM (OPTION)	CS1	Depends on RDYSB or RDYSC
C	40000	128K D-RAM	USER RAM (OPTION)	CS2	Depends on RDYSB or RDYSC
B	60000	128K	NOT USED	CS3	15
C	80000	128K M-ROM (Low-Speed)	MS-DOS BASIC	CS4	15
(C)	A0000	64K	NOT USED	CS5	15
B	B0000	64K	NOT USED	CS6	15
B	C0000	M-ROM (Low-Speed)	DICTIONARY (OPTION)	CS12	15

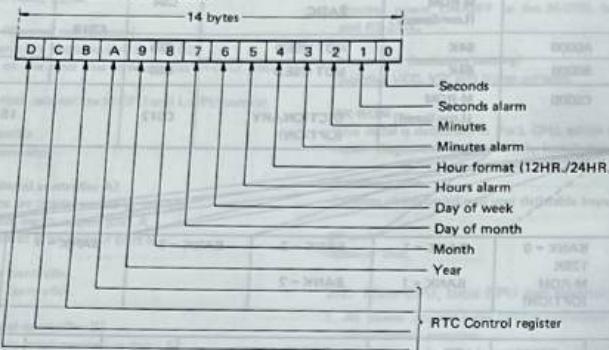
* CS = Chip Select

BANK = 0 128K M-ROM (OPTION)	BANK = 1 BANK = 1	BANK = 2 BANK = 2	BANK = 3	BANK = 4	BANK = 5 ~ 7 NOT USED
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E0000	6K SRAM	PRT BUFFER	CS8	CS9	0
E1800	2M	NOT USED			CS19
A E2000	24K		CS9'		15
A E8000	32K	NOT USED	CS10	0001	15
A F0000	32K ROM (High-speed)	SYSTEM PGM (Main) IOCS BOOT	CS11	0000 0	0000
A F8000	32K ROM (High-Speed)	KEY TBL CG SYSTEM PGM (Local)	CS7		0

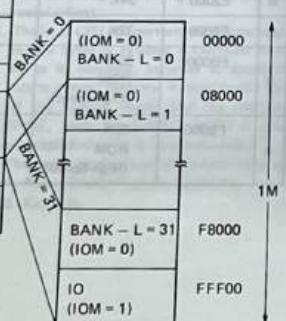
Address	# of bytes	Device	CS No.	Number of WAIT states required
0000	14	Real Time Clock (see below) (*)	CS13	0
003F	50			
0040	16	P-CNTL A	CS14	0
0050	16			3
0060	16	P-CNTL B	CS15	0
0070	16			
0080	8	CNTL MUX	CS16	0
	8			
0090	8	BUBBLE	CS17	1
	8			

(*) Real time clock I/o definition

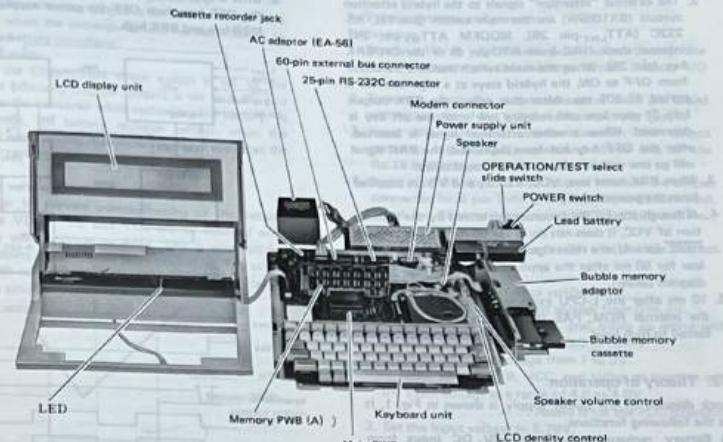


Memory (I/O map (L-CPU))

Address	# of bytes	Device	Use
0000	4K	Internal ROM	SYSTEM PRG
1000	8K	External PROM	(TEST) ROM
3000			NOT USED
4000			PACES 32 x 32KB BLOCKS
0000			NOT USED
FF80	128	Internal RAM	



2.4. Actual chart



[3] POWER SUPPLY

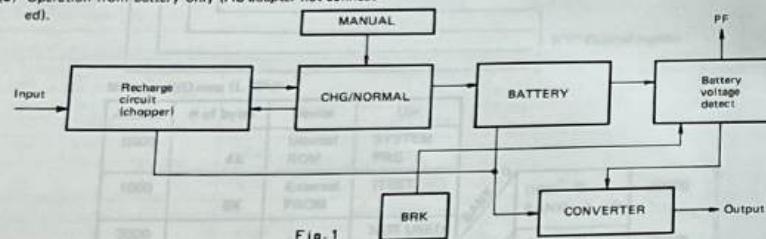
3-1. Start up sequence

- When the main switch is turned ON, V_{CHPP} , V_p is applied to the attention circuit hybrid IC BX7059.
- The external "attention" signals to the hybrid attention circuit (BX1059W) are the main switch (pin 12), RS-232C (ATT_{LN1} pin 26), MODEM ATT_{M1} pin 24), internal clock (IRQ from RTC-pin 9) or the ON/BRK key (pin 28). When the main switch makes a transition from OFF to ON, the hybrid stays at a high level for a period of 105 ms. After this delay, the BRK output (pin 2) goes low and remains low until the off key is depressed. When another attention signal is asserted, after the OFF key has been depressed, the BRK signal will go low without the aforementioned delay.
- When BRK turns low, VCC, VDISP, and VB are supplied from the power supply.
- Although the L-CPU becomes initialized by the application of VCC, it does not do so for 50 ms. This is because RESL (pin 4), the reset signal to the local CPU, is forced low for 50 ms after the application of VCC (see timing diagram below).
- 10 ms after the L-CPU executes the program stored in the internal ROM, PA5 (MCBR) and PA6 (MBR) are forced to high level.

3-2. Theory of operation

Block diagram of the power supply is shown in Fig. 1. It has the following functions:

- Battery recharge only from 18V DC Input from adapter. (Charge mode)
- System operation plus battery recharging (18V DC adapter connected). (Normal mode)
- Operation from battery only (AC adapter not connected).

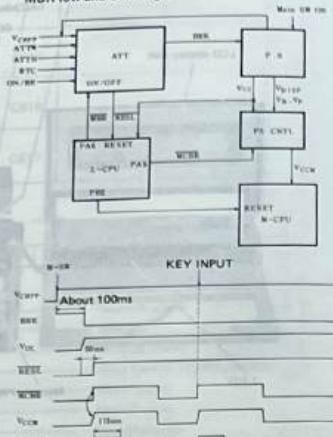


3-2-1. Operational description

Recharge circuit (chopper)

The recharge circuit is controlled by hybrid switching regulator IC 494 and an operational amplifier. Recharge voltage is controlled in the chopper mode. Input of 18V DC $\pm 15\%$ is controlled to obtain the outputs shown in Fig. 2.

- when MCBR goes high, the M-CPU power supply VCCM is applied and PB2 (RESET) of the L-CPU goes high for a period of 115 ms. The M-CPU is reset by this signal.
- The M-CPU now waits for a command. Unless a command is received, it halts with VCCM low.
- BRK is at low level while MBR is high, but depression of the OFF-key shuts OFF the power supply by turning MBR low and BRK high.



(1) Charge mode

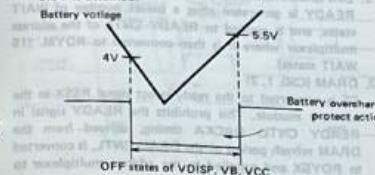
When operated in the Charge mode (by means of the CHG/NORM select switch), 7.6V appears on the chopper output to recharge the battery only. The current limiter allows no more than 1.3A when recharging a completely discharged battery. In addition, chopper output is set to the normal state (6.9V) when the recharge current reaches 100mA, to prevent battery overcharge.

(2) Normal mode

When the CHG/NORM select switch is set to the Normal position, chopper output is set to 6.9V and supplies the converter while recharging the battery. In this mode, the battery recharge voltage, when the battery is connected, is as shown in Fig. 2 such that the battery recharge current is limited to 0.4A.

3-2-2. Low voltage detect

- In order to prevent overdischarging of the battery, outputs VDISP, VB and VCC are all disabled when battery voltage drops to 4.0V. This is accomplished by stopping the converter from oscillating. The oscillator will not start again, until a minimum voltage of 5.5V is attained.



(2) Low battery signal

When the battery voltage drops below 5.8V, the power fall alert signal (PF) is sent to the main unit. This signal, however, does not affect the output voltages.

(3) Output break signal (BRK)

When BRK is received from the main unit, converter oscillation stops and all outputs (VDISP, VB, VCC) are turned OFF.

3-2-3. Converter

Chopper and battery outputs are controlled by a switching regulator to supply proper output voltages.

VP: Battery or chopper output is supplied without converter intervention.

VCC: 5.0V, 600mA

VB: 12.9V, 300mA

VDISP: With VCC at more than 50mA, it is possible to control the VDISP output voltage within a range of 12.2V to 17.9V by adjusting the VR from its maximum to minimum setting. The 30kOhm VR is connected between the VDISP output and the VDISP output.

VCCR: Output approximately equal to VCC is supplied from the NiCd battery inside the power supply.

3-3. Power supply adjustment (and performance verification) procedure

The power supply unit consists of three blocks of recharge circuit, voltage detector circuit, and converter circuit.

1. Voltage detector and converter

- Initial setup
- Supply a 10V/0~5A variable power source through the input connector of the recharge circuit (battery I/O connector).
 - Externally short the output connector No.9 pin (blue) with either one of No.1, 2, 3, or 4 output pin (gray).
 - Insert the 10kOhms resistor between the output connector No.5 pin (purple) and either one of the No.15 or 16 output pin (brown).
 - Insert the 30kOhms variable resistor between the output connector No.8 pin (white) and No.12 pin (black). And, insert the 6kOhms resistor between No.8 pin and No.11 pin.
 - Set the ON/OFF switch to the ON side and the S switch to the yellow side.

Adjustments and performance verification

- Gradually increase the input voltage from 0 to 7V.
→ Make sure that VB, VCC, and Vdisp go active with the input voltage at a range of 5.2 to 5.65V.
- Decrease the input voltage from 7 to 0V.
→ Make sure the VB, VCC, and Vdisp go inactive with the input voltage at a range of 4.6 to 4.0V.
..... Above is for the POD operation.
- Set the input voltage to 5.70V.
→ Adjust the VR so that the voltage between either one of output connector pin No.1, 2, 3, or 4 (gray) or No.5 pin (purple) becomes the voltage ON/OFF breakpoint.
..... Above is for the PF operation.
- Set the input voltage to 6V.
Remove short pin between output connector pin No.1, 2, 3, 4 (gray) and No.9 (blue) to see that:
1. VCC, VB, and Vdisp go active, when the short pin is removed.
2. VCC, VB, and Vdisp go inactive, when the short pin is connected.
..... Above is for the BRK operation.
- Set the input voltage to 6V.
 - Adjust the VR so that the VB output (No.10 pin orange) should become 12.92V.
 - Adjust the VR so that the VCC outputs (No.11, 14 pins red) should become 5.05V.
 - Gradually turn the VR, which is externally connected between the output connector No.8 pin (white) and No.12 pin (black), to its full position to see that the output on Vdisp (white) changes from 12 to 17.9V.
 - Check to see that difference between the NiCd battery output and VCC is on VCCR.
 - Check to see that input and output are active on VP (No.15 and 16 pins brown) and VCHPP (No.7 pin green).

2. Recharge circuit

- Initial setup**

 1. Connect the AC adaptor or the power source (20V/3A) to the input connector.
 2. Insert either an electronic load (2A/20V) or a variable resistor to the recharge circuit output connector (battery I/O connector).
 3. Set the S switch to the orange side, then turn the ON/OFF switch to the ON side.

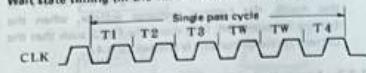
Adjustments

1. Set the input voltage to 18V.
→ Adjust the VR so that recharge output should become 6.90V.
 2. Gradually increase the recharge current and check to see that the output voltage changes from 7.4 to 8.4V while the current value changes from 60 to 140mA.
 3. Set the recharge current to 1.85A.
→ Manipulate the VR1 and set it to such a position that the limiter is activated.
* It also may be possible to set the recharge current to 1.5A first, then the VR1 be adjusted so that the output voltage should become 4.5~4.8V.
 4. Set the recharge current to 400mA.

[4] CPU, I/O AND MEMORY

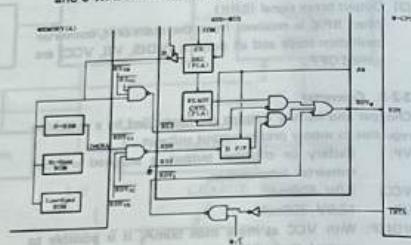
Memory configuration A is standard on the PC-5000 (128 K Byte). Memories B = C (2X CE-100M) are optional. The accessing of memory and I/O devices is performed by means of chip select signals (CS0-19), which are derived by the address signals encoded by the address multiplexor. Since this system is non-READY active, the signal READY must be returned to the CPU in order to access memory and I/O, otherwise the CPU continues to execute the TW cycle. This READY signal may occur in the following manner, depending on the type of device:

Wait state timing (in the case of two WAIT states)



REAR

1. High speed ROM (CS11, 7)
CS is supplied to RDY CNTL of the address multiplexer to make it RDMM (0 WAIT states).
 2. Low speed ROM (CS12, 18)
READY is generated after a preset number of WAIT states, and is applied to READY CNTL of the address multiplexer where it is then converted to RDYM. (15 WAIT states).
 3. DRAM (CS0, 1, 2)
CS is converted to the ready select signal RSSX in the memory module. This prohibits the READY signal in READY CNTL DACKA timing, derived from the DRAM refresh period of the DRAM CNTL, is converted to RDYSX and supplied to the address multiplexer to create RDY.
 4. I/O (CS13, 17)
RDYM is generated by a predetermined number of WAIT states which was pre set to READY CNTL of the address multiplexer. (1 WAIT state for bubble memory and 9 WAIT states for all other).



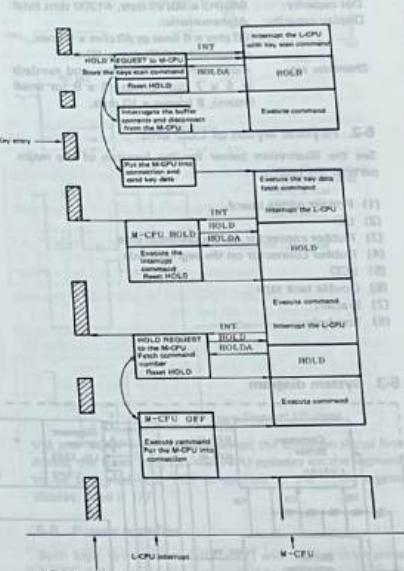
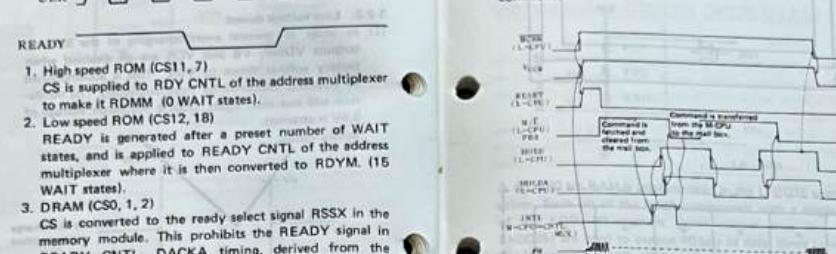
Communication between the M-CPU and L-CPU

After the system starts, the M-CPU turns OFF, leaving the L-CPU executing a continuous key scan. When a keystroke is encountered, the L-CPU forces the M-CPU on by setting MCBR high. The key code is then transferred to the M-CPU. If the key code is a command, the M-CPU will execute it.

If the M-CPU needs the L-CPU to assist in executing a command, necessary information (i.e. L-CPU command numbers) are stored in the "mail box" of the DRAM to invoke an interrupt to the L-CPU.

(M-CPU = INT CNTRL \Rightarrow L-CPU \Rightarrow INTL

Next the L-CPU issues a hold to the M-CPU. Hold acknowledge (HOLDLA) is then output from the M-CPU to the L-CPU now fetches the stored command from the DRAM "mail box", and it is interpreted. If it is a high priority command, it is immediately executed. After execution, the L-CPU removes hold from the M-CPU. For a low priority command (i.e. CMT), hold is cleared immediately after the command is fetched. If there is no call for the use of the M-CPU at this point, (i.e. No key input, etc.) it is turned OFF and the L-CPU begins executing the fetched command.



[5] LCD UNIT

5-1. Description

Dot capacity: 640(H) x 80(V) dots, 51200 dots total

Display capacity: Alphanumeric

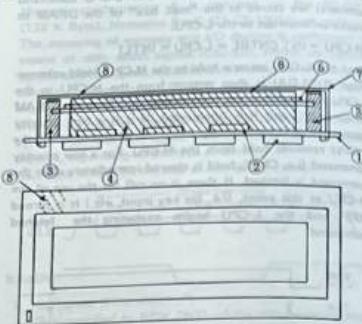
80 chars x 8 lines or 40 chars x 4 lines
comprised of 640 dots x 80 dots.

Character set: Alphanumeric characters and symbols in 5 x 7 dot format (5 x 9 for small letters), 8 frames x 10 dots.

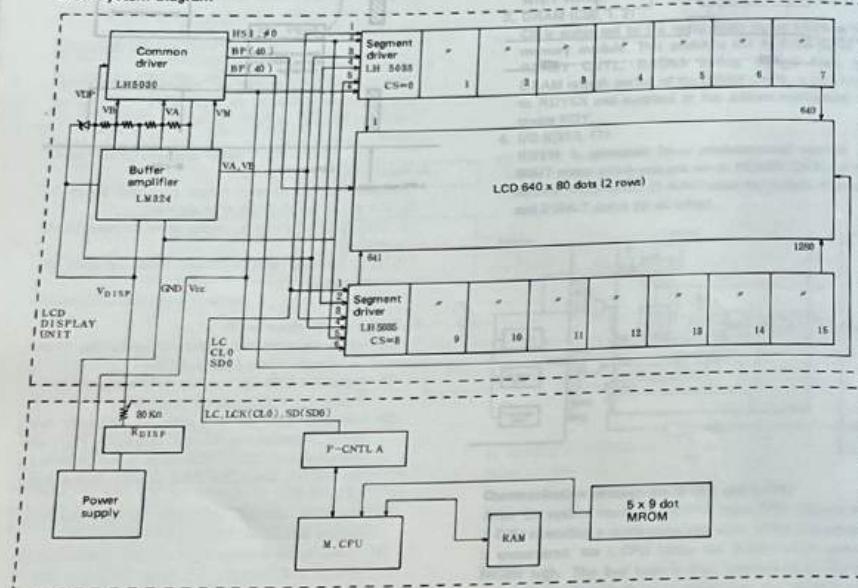
5-2. Physical layout of LCD unit

See the illustration below for the location of the major parts of the LCD unit.

- (1) Printed wiring board
 - (2) LSI
 - (3) Rubber connector on the common side
 - (4) Rubber connector on the segment side
 - (5) LCD
 - (6) Double tack tape
 - (7) Bracket
 - (8) Test hole

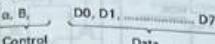


5.3. System diagram



5.4 Operations

Display data is sent in bit serial format via P-CNTLA as follows:

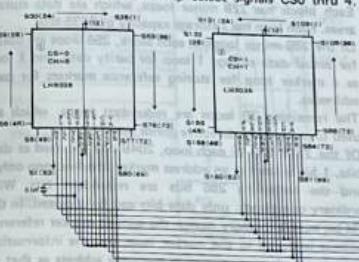


When terminal DY1 of the LH5030 common driver goes to low level (GND) and terminal DY0 goes to high level (VCC), the display duty cycle is set to 1/40. Since clock signals ϕ_0 and H_{SI} are supplied to the LH5035 segment driver from the internal clock oscillator, the common output is synchronized with the segment outputs.

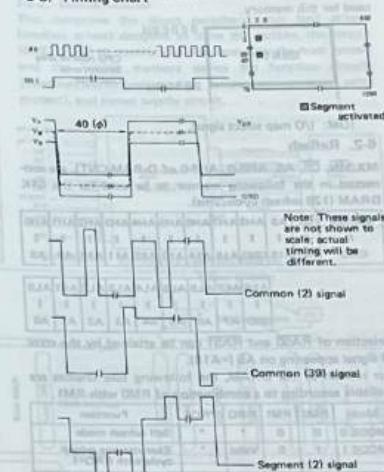
Common signal and segment signal driving power is obtained from 1/7 of the bias from the common driver internal switching transistor and external resistors, R1 and R2.



A 40 x 80 bit RAM is implemented in the LH5035 segment driver. Each bit of the RAM corresponds with a single dot of the LCD. 80 segment signal output lines (for each LH5035) are used to output 40-bits of data. Since terminal CH is connected with VCC or GND, data will be written at the location where COL address and DATA bits are inverted with respect to the serial data input. (Note the correspondence of the pin number of the LSI with the segment number in the following Figure.) Chip 0 thru 15 can be selected by means of chip select signals CS0, the word



5-5. Timing chart



VM and VDOP (or GND) appear on the common signal line during the fixed interval. VB (VA) appears on the segment to be activated and VDP is applied to the liquid crystal display. Bias is 1/7.

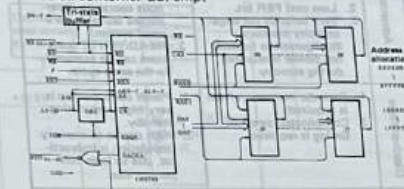
5-6. Power supplies

Both logic drive power (VCC, 5V) and display drive power (VDP', 19V maximum) are applied to the LCD unit. Buffer amplifier LM-324N drive power, LCD drive power VDP (VDO'~4V), common signal VM, and segment signals, VA, VB are derived from VDP'.

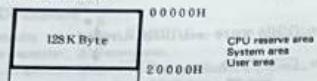
[6] MEMORY CIRUCIT

6-1. DRAM (dynamic RAM) PWB unit

The memory PWB (also called the DRAM) contains masked ROM, DRAM, and the DRAM controller LSI chips. As shown in Figure below, 16 chips (8×2) of 64KB DRAM (65,568 bits \times 1) comprise a 128KB RAM area. Read, write, and refresh of the DRAM are performed by the DRAM controller LSI chip.



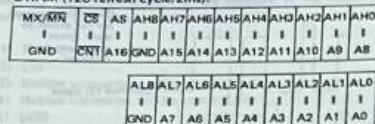
Addresses 00000H thru 20000H of the system. RAM are used for this memory.



IOM: I/O map select signal.

6-2. Refresh

MX/MN, CS, AS, AH0-AH3, AL0-AH0 of D-RAM-CNTL are connected in the following manner to be used for the 64K DRAM (128 refresh cycle/2ms).



Selection of RAS0 and RAS1 can be attained by the state of signal appearing on AS (=A16).

For refresh of the DRAM, the following four choices are available according to a combination of RMO with RM1.

Mode	RMO	RM1	RRO	PROG	Function
MODE 0	0	0	*	*	Self refresh mode
MODE 1	1	0	Valid	*	Executes one refresh cycle with RRO=1.
MODE 2	0	1	Valid	*	Executes 128 refresh cycles with RRO=1.
MODE 3	1	1	*	Valid	Executes one refresh cycle when RD, WR is executed while RRQS=1.

*: Invalid

128 refresh will be automatically executed once per ϕ x 1914 times. ϕ is used for refresh of RAS. When the DRAM is tried to access in a middle of refreshing, a wait will be issued to the CPU which is being accessed with low level of DACKA. Upon completion of refresh, it makes DACK, connected to the READY pin of the CPU, turned high level.

6-3. DRAM memory general description

The Table below show the general characteristic of dynamic RAM and static RAM.

	Dynamic	Static
Advantages	<ul style="list-style-type: none"> 1. Small component size permits higher population density on PWB. 2. Low cost PER bit. 3. Very suitable for large capacity memory configurations because less power is required during standby. 	<ul style="list-style-type: none"> 1. Memory refresh is not required. 2. As an external clock is unnecessary, a synchronous operation is permitted (suitable for a small system). 3. READ/WRITE operations can be executed in the same cycle.
Disadvantages	<ul style="list-style-type: none"> 1. Periodic memory refresh is required. 2. Complicated external timing is required. 	<ul style="list-style-type: none"> 1. Power consumption is very high even during standby. 2. High degree of memory population is impractical, due to large component size.

Type	Dynamic memory cell	Static memory cell
Typical circuit		
Practical example of memory element	N-MOS dynamic RAM	N-MOS E/E static RAM N-MOS E/D static RAM N-MOS polysilicon Static MOS-RAM

[7] MAGNETIC BUBBLE MEMORY

7-1. Outline

The magnetic bubble memory system consists of a bubble memory cassette which has a data storage capacity of 128 K bytes and a bubble memory adapter which controls the cassette.

The bubble memory adapter is interfaced with the host system via 8 bits of parallel data, and performs various types of controls and transfers of data through the register in the Bubble Memory Controller (BMC).

The magnetic bubble cassette has addresses of 4096 pages, each of which contains 32 bytes of data. Block access is performed for each page.

Data is transferred from the bubble memory adapter to the host system or vice versa via 8 bit parallel format and from the adapter to cassette or vice versa a bit at a time in serial format.

The magnetic bubble device employs a major line and minor loop system, comprising two 512-kbit blocks.

Each block has 228 minor loops, which are data storage areas. Each loop has a storage capacity of 2335 bits. Of the 285 minor loops in each block, 256 loops are usable for actual data storage 1 loop for parity data, and 1 loop as a marker loop for storing reference markers for page addresses.

The remaining 30 loops are redundant loops, which are used to replace any defective minor loop.

Of the 2335 bits in each loop, 2048 bits are used as data bits, 1 bit is used as an address marker (marker loop only), and the remaining 286 bits are redundant bits. With ordinary commands, only data bits can be accessed. In the 1M bit bubble memory device, the address marker reference address is stored in the marker loop and the information on defective loops is stored in the same address as that of the marker inside the device. Before the bubble memory is initially accessed, the address marker is searched and the address of the BMC is synchronized with that of the bubble memory device. Simultaneously the information on defective loops stored in the device is read and fetched in RAM inside the BMC. After this, defective loops are omitted automatically by the BMC by referring to the information in RAM.

7-2. Structure

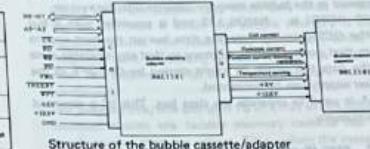
7-2-1. Bubble Memory Cassette BKL1131

This comprises the 1M bit bubble memory device, sense amplifier circuit, temperature sensing element, etc.

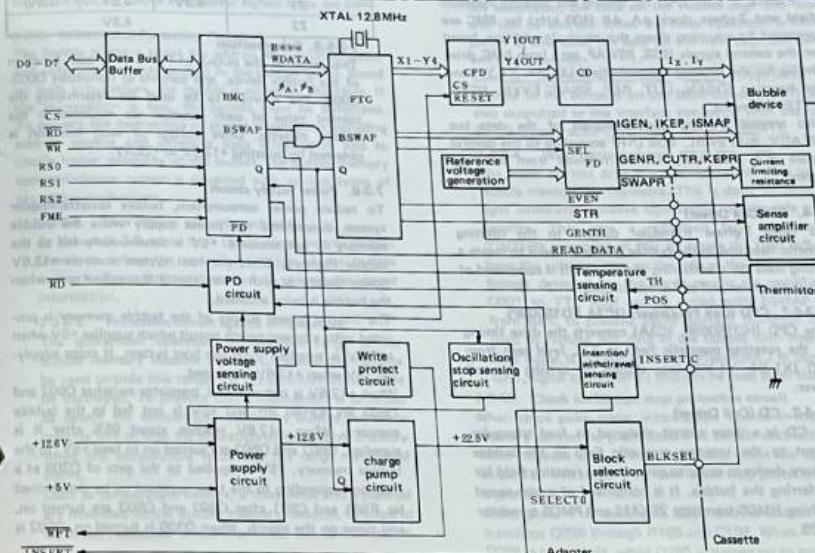
Loop Name	No. of loops per 512kbit	Meeting
Data loops	256	
Parity loops	1	Loop which stores data.
Redundant loops	30	Loop used to substitute for defective data loops.
Marker loops	1	Loop which stores the address of the page address marker.

7-2-2. Bubble Adapter

This comprises the direct peripheral unit (coil driver, function driver) designed to drive the bubble, the circuit (BMC, FTG) to control the interface with the host system and the bubble memory device the function circuits (insertion/withdrawal sensing, temperature protect, write protect), and power supply circuit.



7-2-3. Block Diagram



7-3. Circuit operation

The previous figure shows the block diagram of the bubble memory cassette/adapter. (7-2-3)

7-3-1. Data Bus Buffer (IC5A, TC40H245F)

To reduce power consumption, the power supply to the bubble memory is turned off while the memory is not accessed in the bubble memory cassette/adapter system.

BMC (IC4B) is a NMOS LSI and is provided with a bus buffer (IC5A) to separate the data bus on the host system from that on the bubble memory so that any unstable state of the data bus which might be caused by ON/OFF of the power supply can be prevented.

IC5A is used to separate the data bus. This IC is powered continuously.

7-3-2. BMC (Bubble Memory Controller) (IC4B, HD46507PA23)

BMC is a NMOS LSI and is connected to the host system in 8 bit parallel format, and is used to control the bubble memory based on the commands issued from the host system.

The BMC is provided with 6 types of registers, which are selected by 0 to 2 of CS (Chip Select) and RS (Register Select) and process READ or WRITE according to the timing signals RD and WR.

7-3-3. FTG (Function Timing Generator) (IC5B, H4803F02)

FTG is a CMOS LSI and is connected to a 12.8 MHz crystal oscillator to produce a 12.8 MHz clock.

The clock θ (100 kHz) for driving the rotating magnetic field and 2-phase clock ϕ_A , ϕ_B (400 kHz) for BMC are prepared by counting down this clock. In addition, based on the control signals (BS5, BSWAP, etc.) from BMC, drive timing for the rotating magnetic field (X1-X4, Y1-Y4) and for function (DGEN, CUT, REP, SWAP, EVEN, NSTR, WSTR) is created.

Also created are the control signals of the data bus (READY, BUS ENBL, BUS DIR) according to the control signals (CS, RD, WR, TXAK) received from the host system.

7-3-4. CD (Coil Driver)

This feeds 2-phase triangular current to the rotating magnetic field coil in the bubble memory device to create a rotating field for transferring the bubble. It is comprised of the coil pre-driver and coil driver circuits.

7-3-4-1. CPD (Coil Pre-Driver) (IC3A FD15009P)

The CPD (HD15009P, IC3A) converts the drive timing of the rotating magnetic field at TTL level sent from FIG (X1-X4, Y1-Y4) into timing for driving the coil driver.

7-3-4-2. CD (Coil Driver)

The CD is a drive circuit designed to feed triangular current to the rotating magnetic field in the bubble memory device in order to generate the rotating field for transferring the bubble. It is comprised of a high-speed switching NMOS transistor 2SK416 and PMOS transistor 2SJ120.

The coil driver consists of the X coil drive circuit (Q405, Q408) and Y coil drive circuit (Q401-Q404), and generates a 100 kHz rotating magnetic field.

7-3-5. FD (Function Driver)

The FD is a circuit designed to feed pulse current to each function in the bubble memory device, comprising IC HD29101P and associated transistors.

7-3-5-1. FD IC (IC18 HD29101P)

The FD (HD29101P mounted at IC18) converts function drive timing signals (DGEN, CUT, REP, SWAP, EVEN) at TTL level from FTG, and outputs constant current signals (GENO, GENE, CUT, REP, SWAP) to drive the drive transistors (Q002-Q006). The reference voltage used to obtain the constant current is generated by an external circuit and is fed to Z1 and Z2 terminals in the FD IC.

7-3-6. Reference voltage generating section

This consists of a Zener diode and resistors. The voltage to be supplied to Z1 is used for generator current, while the voltage to be fed to Z2 determines replicator cut and SWAP current.

Generator current must be compensated for temperature variation. This is achieved using the temperature characteristics of a thermistor (GENTH terminal) mounted in the bubble cassette.

The table below shows the supply voltage to Z1 and Z2.

Supply voltage to Z1 and Z2

Temperature Item	5°C	25°C	40°C
Z1	4.2V	3.8V	3.5V
Z2		4.5V	

7-3-7. Driver section

This amplifies the output of FD to drive each function of the bubble device, and consists of transistors Q002-Q006. The resistors to be used for determining the current value of each function are mounted in the bubble cassette. Drive voltage of each function is obtained by boosting +12.6V to +22.5V.

7-3-8. Power supply circuit

To reduce power consumption, bubble cassette/adapter system disconnects the power supply while the bubble memory is not accessed. +5V is continuously fed to the bubble memory, while the host system controls +12.6V power supply in such a way that it is supplied only when the bubble is being accessed.

The internal power supply of the bubble memory is provided with a power switch circuit which supplies +5V when +12.6V is supplied from the host system. It stops supplying +5V when +12.6V is stopped.

When +12.6V is not supplied, transistor switches Q0602 and Q0503 are turned off and +5V is not fed to the bubble memory. When +12.6V reaches about 95% after it is supplied, Q0602 and Q0503 are turned on to feed +5V to the bubble memory. +5V is applied to the gate of Q305 at a time corresponding to the time constant to be determined by R501 and C501 after Q0602 and Q0503 are turned on, and turns on the switch. When Q305 is turned on, Q502 is

also turned on to supply +12.6V to the bubble memory. To prevent malfunction of the bubble, PD signal must be kept to "L" level until the power supply voltage reaches the specified level.

When the bubble is operated with the supply voltage too low, bubble information may be destroyed. This adapter is provided with a function to detect low voltage level when +12.6V supply voltage decreases so that the bubble memory can be stopped at the correct time.

Power supply voltage level is detected by IC3B and input to PD terminal in the BMC to stop the bubble in the specified sequence. Detection level for the lowered +12.6V power supply voltage is set to 11.97V or less.

Q601 connected to +12.6V line is to remove the charge remaining inside when power supply switch Q502 is turned off.

7-3-9. Charge pump circuit

At least 20V is required for the function driving voltage of the bubble memory. Since the voltages supplied to this device are +5V and +12.6V, the 112.6V source is boosted for this purpose. This is a voltage-multiplying circuit using a clock pulse comprising Q101-Q102, Q201-Q203, C101, and D102 and D103. Thus, $V_p = 22.5V$ is obtained.

7-3-10. Block changeover circuit

The bubble device comprises 2 blocks of 512 kb. Since the first block contains pages 0-2047 and the next block contains pages 2048-4095, the corresponding block must be selected according to the page to be accessed.

This is done by the block changeover circuit which selects a block by switching the transistors Q301 and Q303 according to SELECTO (block changeover signal) from the BMC.

7-3-11. Information Protection Circuit

The bubble memory stores the address marker information and defective loop information in the bubble device. Based on such information, the bubble is accessed. Therefore, if the information is lost, the bubble must be initialized. To prevent the destruction of stored information including address marker and defective loop information and to obtain higher reliability of the bubble, the bubble memory cassette/adapter system is provided with various types of protective mechanisms.

7-3-9-1. Low voltage protection circuit

As shown in 3.6, when the +12.6V power supply voltage lowers to below the operation voltage of the bubble memory, the voltage is detected to protect the stored information.

7-3-9-2. Protective circuit against temperature

The guaranteed operation temperature range of the bubble memory cassette is 5-40°C. Should the cassette be used outside this range, the stored information might be destroyed. To prevent this, a mechanism is provided to detect the temperature inside the bubble memory cassette and to stop the operation of the bubble memory when the temperature is outside the range mentioned above.

Used as temperature sensors, a thermistor and a positistor are mounted in the bubble memory cassette. Changes in electrical resistance of the thermistor due to the temper-

ature variation is detected by IC3B. When the temperature thus detected is outside the specified range, the corresponding signal is input to PD input terminal in the BMC to stop the operation of the cassette.

7-3-9-3. Protective circuit for insertion/withdrawal of cassettes

Since the bubble cassette can be inserted in or withdrawn from the adapter any time, care must be taken not to withdraw it while the bubble memory is being accessed. Should the cassette be withdrawn while the magnetic field is rotating or each function is in operation, the information in the bubble memory would be destroyed.

To prevent this, one pin (pin 15 in CN2) in the interface connector with the bubble memory cassette has been made shorter than the others. Thus, when the cassette is inserted, all pins other than this pin touch first and the signal becomes stable before the shorter pin touches, releasing PD signal to the BMC. When the cassette is withdrawn, the pin is disconnected first of all to obtain PD signal from the BMC. The BMC enters into a sequential Power Down operation and stops the bubble in a specified sequence. Thus, the stored information disconnected by the other pins is preserved. When the cassette is withdrawn while it is being read out, the readout data at the other pins is preserved. When the cassette is withdrawn while it is being read out, the readout data at Power Down and later is not guaranteed. When the cassette is withdrawn while it is being written and the swap operation of the data on the page being accessed is not completed, the data on the related page and later will not be written. When the swap operation is completed at this time, the data on the next page and later will not be written.

Cassette insertion/withdrawal signal (INSERTC) is applied to PD terminal on the BMC through Q501 and also outputted to the interface connector with the host (pin 9 on connector CN1, signal name: INSERT).

7-3-9-4. Write protect circuit

The write protect prohibits the writing of data on the bubble memory by hardware. This is done by detecting light deflecting adhesive tape applied to the side of the cassette. This uses a reflection type photo-sensor (ON2160, mounted at PS) to detect the light reflected from the adhesive tape on the side of the cassette.

Signals detected by the photo-sensor are amplified by Q001 to TTL level and isanded with BSWAP signal from BMC to prevent SWAP current (function current used to replace old data in the bubble with new data). This signal is output to the interface (pin 7 in connector CN1, signal name: WPT) and can be read from the host.

7-3-10. Clock oscillation stop protective circuit

When clock pulse stops, information stored in the bubble memory cannot be guaranteed and circuit destruction may occur because each circuit is unstable when the oscillation stops. For this reason, the oscillation stop protective circuit is provided.

Clock pulse θ is applied to Q204 and its output turns off transistor Q205 through R105 and C104. When θ stops and Q204 is turned off, while Q205 is turned on to stop +12.6V power supply, protecting the circuit.

7-3-11. Bubble Cassette

The bubble cassette consists of a 1Mb bubble device, sense amplifier circuit, temperature detecting thermistor, positioner, and function current limiting resistor.

7-3-11-1. Bubble memory device

The bubble device comprises two 512 kbit blocks, which are identical. Each block has a generator, replicator, swap, and detector. The device incorporates X coil and Y coil for generating the rotating magnetic field and Z coil for bubble erase.

7-3-11-2. Sense Amplifier Circuit

The sense amplifier IC amplifies the analog output from the bubble to discriminate between "1" and "0". The bubble output is sampled according to the strobe pulse signals and is output to the adapter as readout data.

7-3-11-3. In-cassette temperature sensing element

As mentioned in 3-9-2, stored information is protected when the temperature in the cassette is outside the operation guaranteed temperature range. As temperature-sensing elements, thermistor R_{TH1} and positioner R_p are incorporated. R_{TH2} is a thermistor to be used for temperature compensation of the generator.

7-3-11-4. Function Current Limiting Resistors

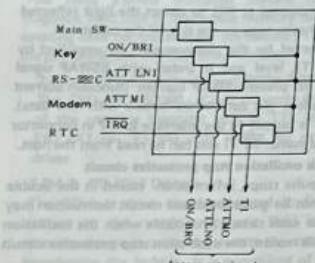
$R9-R12$ are limiting resistors to be used for determining each function current value.

7-4. Note

When the rotating magnetic field coil or each function is open, insertion of any other cassette may damage (open) the rotating magnetic field coil of the cassette or the function. Thus, connect a dummy resistor before checking the coil driver circuit or function driver circuit.

[8] MAIN P.W.B.**8-1. Description of each circuit****8-1-1. Attention control circuit**

This circuit consists of the hybrid IC BX7059W which monitors the main power switch, ON/BRK key, RS-232C interface, modem and RTC. When any of these become active, the power on initiate request signal (MBK) and interrupt are generated.

**Transmission format specification****Xregister (P-CNTLB)**

D6	D5	D4	D3	D2	D1	D0
EP	BRK	RXE	TXZ	PEN	STP	DL

DL = 0 7 BIT word

= 1 8 BIT word

STP = 0 One stop bit

= 1 Two stop bits

PEN = 0 No parity bit

= 1 Parity bit on

TXZ = 1 That particular bit is executed to completion even if turned to 0 during sending.

RXE = 1 That particular bit is executed to completion even if turned to 0 during receiving.

B-1-2. Power control circuit (PS-CNTL)

This is the switching circuit that supplies operating power to devices which generate initiate request signals. The following three power supply lines are controlled:

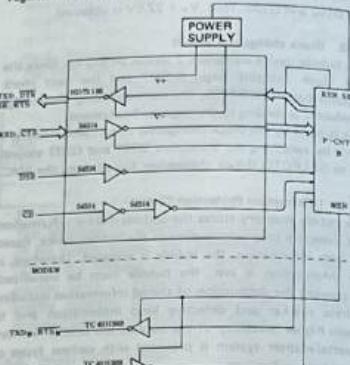
DEVICE	Initiate request signal	Input	Output
M-CPU	MCBR	VCC	VCCM (5V)
RS-232C	SEN	VP	(To oscillator transformer) (4.0~7.1V)
BUBBLE	BUBBR	VB	VBUB (12V)

Each of the initiate request signals is active high.

B-1-3. RS-232C Buffer circuit

This circuit is composed of IC-HD7518B and the hybrid IC BX7058W which convert the P.CNTLB logic output to RS-232C compatible signals.

When SEN (pin 36, P.CNTLB) goes high, the power supply converter becomes active and data transmission on the RS-232C line begins after an approximate 5 ms. delay. Transmission format is selected by the Data in the X and B registers internal to P.CNTLB.

**Transmission format specification**

BRK = 0 Output

= 1 Break

EP = 0 Odd parity

= 1 Even parity

Baud rate setup**Register (P.CNTLB)**

D3	D2	D1	D0	Baud rate
0	0	0	0	(76800)
0	0	0	1	19200
0	0	1	0	9600
0	0	1	1	4800
0	1	0	0	2400
0	1	0	1	1200
0	1	1	0	600
1	1	1	1	300
1	1	1	0	200
1	1	1	1	110

B-1-4. Cassette control circuit

This circuit consists of the motor ON/OFF relay, hybrid IC BX7061W, and speaker driving transistor. I/O data (CRX, CTX) and the key click sound (TO) are amplified by a transistor to drive the speaker. CRXE is a buffer protect signal when no data is input.

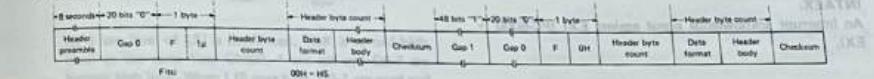
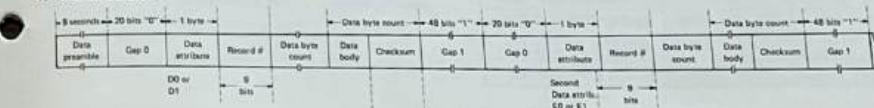
Cassette tape recording is controlled in the following manner:

Recording method: PWM (Pulse width modulation)

Baud rate: 1600bps ("1" represented by 2.4kHz and "0" by 1.2kHz)

Modes of data transfer:

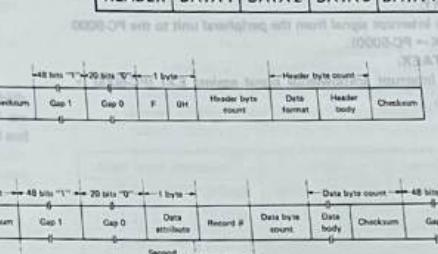
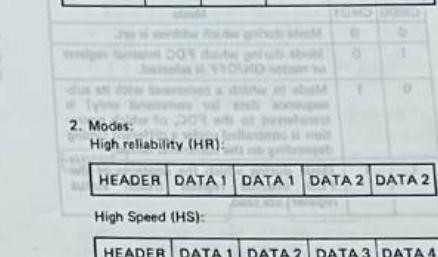
- 1 High reliability (HR)
- 2 High speed (HS)

Data Format:**1. Byte structure:****3. Header structure:****4. Data structure:****RS-232C control interface pin description****RS-232C**

Connector No.	Signal name	In/Out	Description
7	SG	-	Signal ground
2	TXD	Out	Transmit data
3	RXD	In	Receive data
4	RTS	In	Request to send
5	CTS	In	Clear to send
6	DSR	In	Data set ready
20	DTR	Out	Data terminal ready
8	CD	In	Carrier detect
11	RR	Out	Ready to receive
1	FG	-	Frame ground
24	ATTLN	In	Power initiate request from an external source

Model (U.S.A.)

Connector No.	Signal name	In/Out	Description
10	SG	-	Signal ground
5	TXDM	Out	Transmit data (modem)
3	RXDM	In	Receive data (modem)
4	RTSM	Out	Request to send (modem)
2	CTSM	In	Clear to send (modem)
11	FG	-	Frame ground
6	ATTM	In	Power initiate request from the modem



[9] PRINTER

9-1. Printer specifications

9-1-1. Print method

Thermal printing (24 dots)

9-1-2. Printing sequence

The print direction of the CE-510P Printer is Uni-directional from left to right. The carriage returns after printing each line.

9-1-3. Printing speed

1197 dots, at 25°C.
VP: Printing time Total (including return time)

5V 2.2 S/line 6.05/line

6V 2.2 S/line 5.05/line

7V 2.2 S/line 4.85/line

Ribbon life: 46,000 characters

= 600 lines

= 10 pages @ 60 lines/page

9-1-4. Printing format

Total number of dots: 1197 dots/line

Alphanumeric characters

Graphic

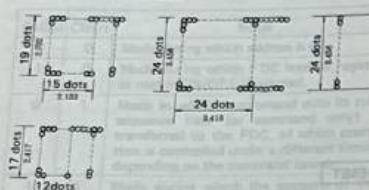
Printing positions: 80 chrs/line, 1197 dots/line

9-1-5. Character structure

Alphanumeric: 19 x 15 dots (66 chrs/line), Pica

Alphanumeric: 17 x 12 dots (80 chrs/line), Elite

Graphics: 23 x 1197 dots



9-1-6. Print control

Printing takes place after one line of data (dot pattern, control data) is sent to the printer control unit from the main CPU.

9-1-7. Thermal head

- Structure of thermal element: 1 x 24 dots

- Average resistance: 44 ohms ± 15%

- Grading

Grade	Class	Resistance mean value
A	+15% ~ +4%	50.6 Ω ≥ Ra ≥ 45.8 Ω
B	+6% ~ -6%	46.6 Ω ≥ Ra ≥ 41.4 Ω
C	-4% ~ -15%	42.2 Ω ≥ Ra ≥ 37.4 Ω

Print heads are classified into three grades:

Grade A: No cut is needed for the grade sense line.

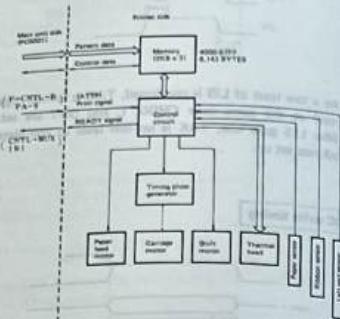
Grade B: The grade sense line on the right is cut.

Grade C: Grade sense lines on both sides are cut.

(Pulse width is adjusted by cutting grade sense line).

* No adjustment is required in the field because print heads have already been adjusted at the factory.

9-2. Printer block diagram



Printer action, READY signal, vs ATTP signal

1. Data transmission

The printer CPU can access external RAM only when READY is high.
Accessing external RAM is prohibited when READY is low.

2. Initiate

A high on the ATTP input line while READY is at high level will cause the printer to begin printing the contents of the line buffer. ATTP goes low during the print cycle.

3. Enforced stop (Power Fail-Print buffer is cleared)

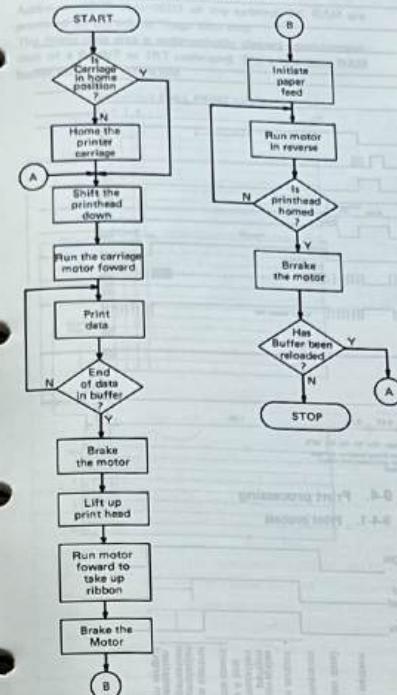
A high on the ATTP input line during printing with READY low interrupts printer operation. It then makes READY 60 high.

4. Standby state

The CPU is held in the STOP mode while in the standby mode in order to save power consumption. RAM accessing and ATTP signal reception are still enabled in the standby mode.

Digital format of DAT, determined at IC2. The total width is 12A, the T-0.0 ms has one 1.000000 serial access with 25 bits from the T-0.0 digital using 2.5V ref/V. Total digital format is 1.0 microsecond to view a total level width of DAT

9-3. PRINTER OPERATIONAL FLOW



9-3-1. Timing chart description

I. Data setting

- READY high causes the main unit to send print data to the printer buffer.

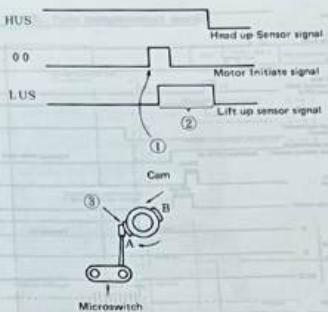
- Control data in the buffer storage are then fetched to the RAM of the printer CPU.

II. Printer operation (Initial operation)

- When the printer receives the initiate signal (ATTP), READY is forced low.
- With READY low, VCS is turned ON.
- A high on the LES line causes the printhead or return to its home position. If it is low, the control proceeds to the next step.

III. Printer operation

- With HUS high, the printhead shifts down.



(a) With signal 00 high (motor initiate signal), the motor (1) starts to run.

(b) When the cam starts to rotate, the microswitch-actuator disengages from the protrusion (3) on the cam.

(c) DLS then goes high at point (2) as the actuator disengages from the cam.

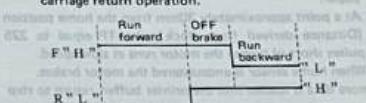
(d) The next time the actuator contacts the cam protrusion, LUS is forced low which causes the printhead to shift down and HUS is then forced low.

2. The motor starts to run forward with F high and R low.

3. Motor is braked with F and R High.

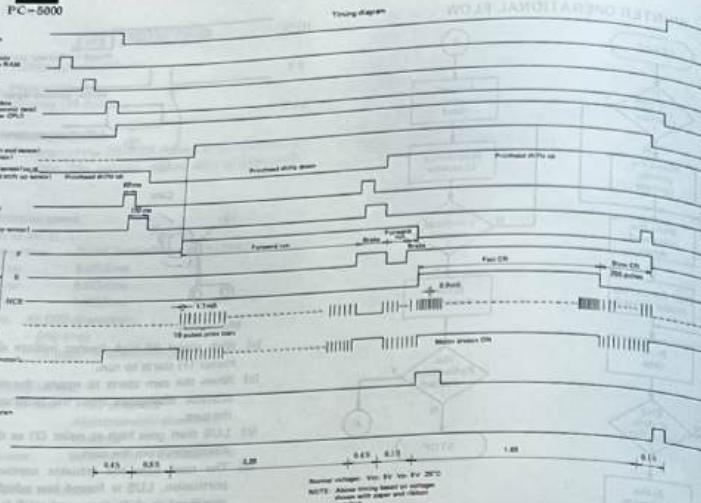
4. The printhead is shifted up in a similar manner to item 1. (above), but HUS goes from low to high.

5. The motor starts to run forward for about 45 ms. Then it runs backward, during the paper feed and carriage return operation.



When HCR is high, the carriage is returned at high speed. When the carriage reaches a position approximately 30mm (1.18") from the home position, HCR goes low causing the carriage to move at slow speed, until the home position is reached. The internal CPU frequency count informs the CPU of this speed change location. The 30mm slow cycle distance is approximately equivalent to 255 pulses of TP.

6. When the carriage returns to its home position, LES is forced low.



Single line printer sequence:

1. Print head shifts down onto the platen.
2. Forward motor rotation is initiated.
3. Data is printed.
4. Motor brakes when printer buffer data is exhausted.
5. Print head shifts up off of platen.
6. The motor runs forward to take up ribbon.
7. Motor runs in reverse to home the carriage and feed paper.
8. At a point approximately 30mm from the home position (Distance derived from clock pulse TP equal to 225 pulses short of home) the motor runs at slow speed.
9. When home sensor is encountered the motor brakes.
10. If more data is loaded into the printer buffer, return to step (1).

Printing takes place when the printer buffer data control signal is sent to the printer controller from the main CPU. A

8-5-7. Thermistor feedback

4. Sequence of events: 1 x 25 dots

High performance thermal printer (HPI) x RDP printer

For high resolution < 200 dpi resolution soft copy W. image

RDP resolution sensor and sensor TBL1,2 memory values

Printer mode to ensure no registration errors and image

QPI resolution soft. Address of memory address soft. Address

Printer mode to QPI, RDP, memory address print mode

Address of memory address soft. Address of memory address

QPI resolution soft. Address of memory address print mode

Address of memory address soft. Address of memory address

QPI resolution soft. Address of memory address print mode

Address of memory address soft. Address of memory address

QPI resolution soft. Address of memory address print mode

Address of memory address soft. Address of memory address

QPI resolution soft. Address of memory address print mode

Address of memory address soft. Address of memory address

QPI resolution soft. Address of memory address print mode

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QPI resolution soft. Address of memory address print mode

Address of memory address soft. Address of memory address

QPI resolution soft. Address of memory address print mode

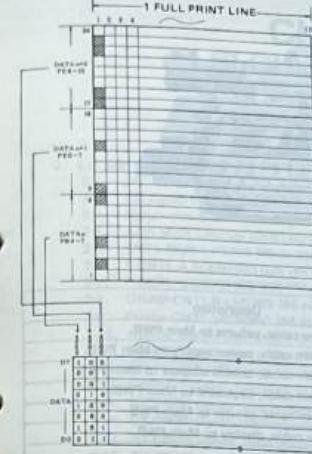
Address of memory address soft. Address of memory address

QPI resolution soft. Address of memory address print mode

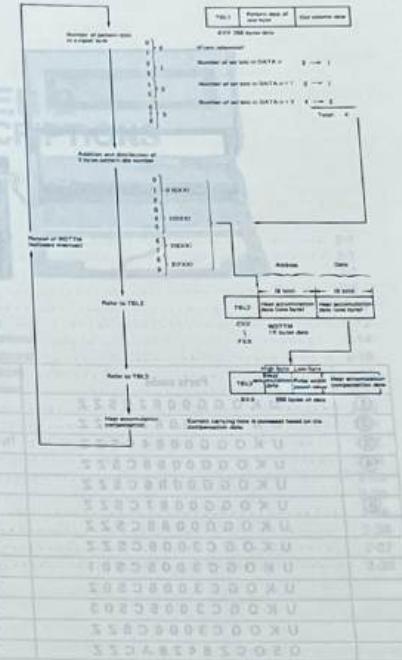
9-4-2. Image data

Addresses 0000 thru 0E07 of the external 6K RAM are provided for the printer image data area.

The image data area is automatically cleared upon completion of a PRINT or IRT command. The image data RAM buffer stores one entire line.



9-4-3. Heat compensation control



[10] SPECIAL TOOLS



No.	Parts code	Description
①	U K O G G 0 8 2 C S Z Z	4-pin extension cable, volume to Main PWB.
②	U K O G G 0 8 3 C S Z Z	16-pin extension cable, power supply to Main PWB.
③	U K O G G 0 8 4 C S Z Z	26-pin extension cable, bubble adaptor to Main PWB.
④	U K O G G 0 8 5 C S Z Z	27-pin extension cable, keyboard to Main PWB.
⑤	U K O G G 0 8 6 C S Z Z	34-pin extension cable, printer to Main PWB.
⑥	U K O G G 0 8 7 C S Z Z	6-pin extension cable, display to Main PWB.
	U K O G G 0 8 8 C S Z Z	28-pin IC socket with lever
	U K O G C 3 0 0 5 C S Z Z	Service use PROM, data bus test
	U K O G C 3 0 0 5 C S 0 1	Service use PROM, tape select test
	U K O G C 3 0 0 5 C S 0 2	Service use PROM, address bus test
	U K O G C 3 0 0 5 C S 0 3	Service use PROM, address bus test
	U K O G C 3 0 0 6 C S Z Z	Operational test program stored bubble cassette
	Q S O C Z 6 4 2 8 A C Z Z	28-pin IC socket

NOTE: For specification of the service use PROM's (A ~ D) and test program bubble cassette, refer to the publication which scheduled to be available around the end of October, 1983.

CHAPTER 2
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[2] LIS CHIP DESCRIPTIONS

2.1. μPD8088 M-CPU pin functions

Pin functions for the minimum system configuration
"Local bus" means the multiplexed bus directly interfaces to the 8088.

AD7-AD0 (Address/Data Bus) ... 3-state

These lines carry the multiplexed memory access address during T1 and data bus during T2, T3, TW, T4. These are active high and go high impedance during interrupt acknowledge and local bus hold acknowledge.

A15-A8 (Address Bus) ... 3-state output

Address bits 8 thru 15 are supplied on these lines during bus cycles T1-T4. There is no need of latching by the ALE. A15 thru A8 are active high and go high impedance during interrupt acknowledge and local bus hold acknowledge.

A19/S6, A18/S5, A17/S4, A16/S3 (Address Bus) ... 3-state output

Upper 4 bits of the memory address appear on these lines during the memory addressing clock cycle T1. During I/O operation, these lines go all low level. Status information is sent out during T1, T3, TW, and T4 of memory addressing or I/O addressing. The status of interrupt enable flag IF (S5) is renewed at the beginning of each clock cycle (T1). S6 remains at zero at all times.

A17/S4 and A16/S8 are encoded in the following manner:

A17/S4	A16/S8	
0	0	Alternate Data
0	1	Stack
1	0	Code or None
1	1	Data

This indicates what relocation register is currently used for data access.

These lines go high impedance during local bus hold acknowledge.

RD (Read Strobe) ... 3-state output

Indicates that the CPU is executing a memory or I/O read cycle. This signal is used to read the device connected to the 8088 local bus. RD goes active (low) during T2 and T3 of all read cycles and during TW. However, RD is kept high level during T2 until the 8088 local bus goes to the high impedance state.

READY ... Input

Used to indicate termination of data transfer. A high level is an acknowledge signal sent from the memory or I/O that the CPU addressed.

The signal READY from the memory and I/O becomes the signal READY which is synchronized to the clock. The signal is active high.

The 8088 READY input can not be synchronized. Unless specific setup and hold times are achieved, proper operation is not certain.

INTR (Interrupt Request) ... Input

This is a level trigger that is sampled during the last clock cycle of an instruction to determine whether the CPU

should go into the interrupt acknowledge operation. One subroutine is called by means of an interrupt vector lookup table which is assigned to the system memory. INTR can be masked internally by resetting the enable flag (IF) in software.

INTR ... Input

The TEST input is interrogated by a WAIT (Wait For Test) instruction. Execution continues if TEST input is low. However, the CPU waits in an idle state, if high. It is internally synchronized at the rising edge of CLK during each clock cycle.

NMI (Non-Maskable Interrupt) ... Input

NMI is an edge triggered input that causes a type 2 interrupt. One subroutine is called by means of an interrupt vector lookup table assigned to the system memory. It is not possible to mask it internally by means of software. At a rising edge of low to high level, an interrupt is caused to the last instruction currently in execution. The signal is internally synchronized.

RESET ... Input

The CPU is forced to immediate termination of operation by this signal. It has to be in the active (high) state for at least four clock cycles. When RESET returns to the low level, the program will start from the top address (FFFFFOH) in about 10 clocks later. The signal is internally synchronized.

CLK (Clock) ... Input

Supplies the basic timing signal to the CPU and the bus controller. CLK is a uneven waveform that has the duty cycle of 33% for obtaining optimum internal timing.

VCC

+5V ±10% supply.

GND (Ground)

Ground pin.

MN/MX (Minimum/Maximum) ... Input

Used to specify whether the CPU should operate in either the minimum or maximum mode.

The following paragraphs discuss pin functions of the 8088 in the minimum mode (MN/MX-VCC).

M/I/O (Memory) ... 3-state output

This status line is an inversion of S2 (from the maximum mode). M/I/O is valid only during clock cycle T4, immediately before the bus cycle and keeps active high (high=memory access low=I/O access) until T4 of the next cycle. It floats to high impedance during local bus hold acknowledge.

WR (Write Strobe) ... 3-state output

Indicates that the CPU is executive 4 memory or I/O write cycles. The signal is active (low) during T2, T3 of all write cycles and during TW.

This signal floats to high impedance during local bus hold acknowledge.

INTA (Interrupt Acknowledge) ... 3-state output

Used for read strobe during the interrupt acknowledge cycle. It goes active (low) during T2 and T3 of each interrupt acknowledgement clock cycle and during TW (wait cycle).

ALE (Address Latch Enable) ... Output

ALE is sent from the CPU to latch the address information on the address mux. This signal is active (high) during T1 of the bus cycle. It is not tri-state.

D/T/R (Data Transmit/Receive) ... 3-state

This signal is necessary for an 8088 configured in the minimum mode. Its assertion or deassertion determine the direction of data transmission (high = transmit data on to the bus; low = receive data from the bus) it is connected to the control mux (LHS704). It floats to a high impedance state during the assertion of local bus hold acknowledge.

DEN (Data Enable) ... 3-state output

DEN is supplied as a control mux output enable signal. The signal goes active (low) during memory and I/O access and during INTA cycle. For the read or INTA cycle, it will be active from the middle part of clock cycle T2 until the beginning of clock cycle T4. During an INTA cycle, it will be active from the middle of clock cycle T1 until the middle of clock T4 cycle (for the write cycle). It floats to high impedance during local bus hold acknowledge.

HOLD (Hold Request) ... Input & HOLDA (Hold Acknowledge) ... Output

HOLD indicates that another master has requested a local bus hold. When the CPU acknowledges the hold request, the acknowledge signal HLDA (active high) is issued in the middle of clock cycles T4 or T1. At the same time HLDA is issued, the CPU causes the local bus and control lines to a high impedance state. After sensing a low state of HOLD, the CPU forces HLDA low. If the CPU needs to execute another cycle, the CPU drives the local bus and the control lines again.

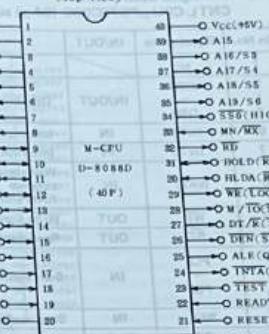
Because HOLD is not an synchronous input, it needs external synchronization since the system can not insure set up time by any other means.

S50 (Status Line) ... Output

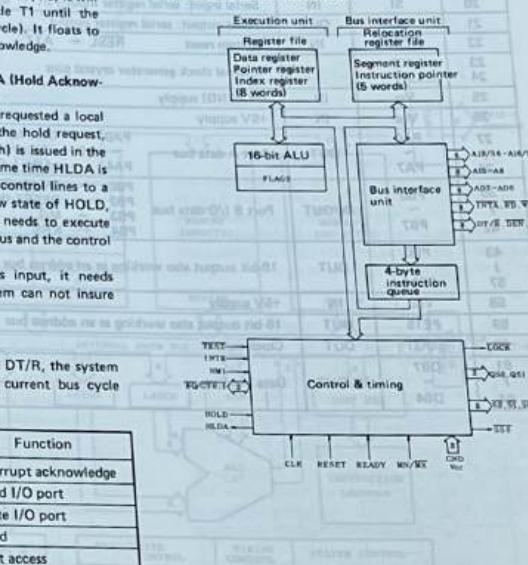
Using a combination of S50, M/I/O, and DT/R, the system can attain complete decoding of the current bus cycle status.

IO/M	DT/R	S50	Function
1	0	0	Interrupt acknowledge
1	0	1	Read I/O port
1	1	0	Write I/O port
0 (low)	1	1	Hold
0	0	1	Port access
0	1	0	Read memory
0	1	1	Write memory
			Passive

(Top View) Pinout Diagram 8088

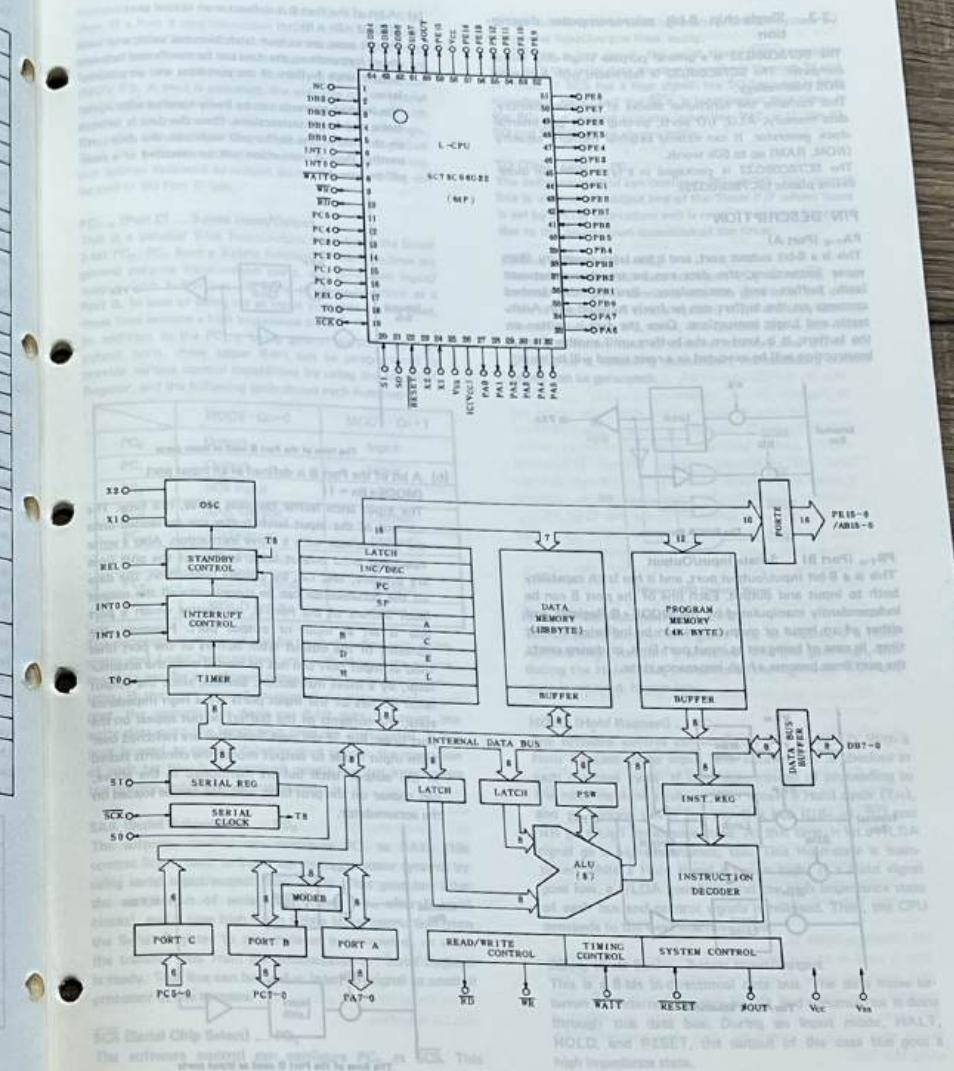


μPD8088 BLOCK DIAGRAM



2-2. LSI signal descriptions

Pin No.	Signal name	IN/OUT	
1	NC		
2	DB3 ~ DB0	IN/OUT	Data bus line
6	INT1	IN	Interrupt request INT1 ← INTL
7	INTD	IN	Interrupt request INTO ← ENBBS
8	WAIT	IN	Wait signal (to be used to extend read/write timing for a slow access device like external RAM and I/O.) WAIT ← WAITL (CNSL-MLX)
9	WR	OUT	Write signal (strobe used in writing data to an external memory)
10	RD	OUT	Read signal (strobe used in reading data from an external memory)
11	PC5 ~ PC0	IN	6-bit input port PC5 ← ON/BRD PC4 ← KR4 ~ ← ~ PC0 ← KR0
17	REL	IN	Stop mode reset input REL ← PF
18	TO	OUT	Timer out: internal timer output
19	SCK	IN/OUT	Serial clock: serial data I/O control clock
20	SI	IN	Serial input: serial register input SI ← MODEM
21	SO	OUT	Serial output: serial register output
22	RESET	IN	System reset RESL ← ATT
23	X2		Internal clock generator crystal pins
24	X1		
25	Vss	IN	0V (GND) supply
26	Vcc	IN	+5V supply
27	PA0 ~ PA7	OUT	Port A data bus PA0 → Used for address bus of the L-CPU PA5 → MCBR PA6 → MBR PA7 → BUBBR PA4 → D
35	PB0 ~ PB7	IN/OUT	Port B I/O data bus PB0 → SM (CNTL-MUX) PB2 → RESET (M-CPU) PB3 → M/L PB4 ← KR5
43	PE0 ~ PE14	OUT	16-bit output also working as an address bus
58	Vcc	IN	+5V supply
59	PE15	OUT	16-bit output also working as an address bus
60	φOUT	OUT	Clock output
61	DB7 ~ DB4	IN/OUT	Data bus line



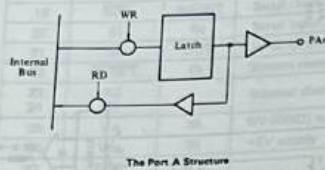
2-3. Single-chip 8-bit microcomputer description

The SC78C06G32 is a general purpose single-chip microcomputer. The SC78C06G32 is fabricated with N-channel MOS technology. This contains the functional blocks of program memory, data memory, ALU, I/O ports, on-chip timer and internal clock generator. It can extend external memory capacity (ROM, RAM) up to 60k words. The SC78C06G32 is packaged in a type of 64 pin quad-in-line plastic (SC78C06G32).

PIN DESCRIPTION

PA₇₋₀ (Port A)

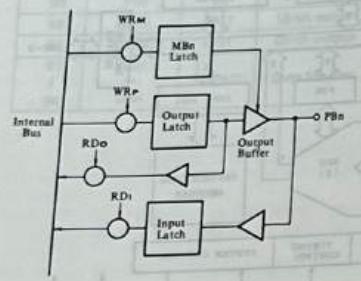
This is a 8-bit output port, and it has latch capability. With move instructions, the data can be transferred between latch buffers and accumulator. Besides, the latched contents on the buffers can be freely handled with Arithmetic and Logic instructions. Once the data is written on the buffers, it is kept on the buffers until another Port A instruction will be executed or a reset signal will be issued.



The Port A Structure

PB₇₋₀ (Port B) ... 3-state Input/Output

This is a 8-bit input/output port, and it has latch capability both to input and output. Each line of the port B can be independently manipulated by the MODE·B Register, and either of an input or output port can be indicated at that time. In case of being set as input port lines, or during reset, the port lines become a high impedance state.

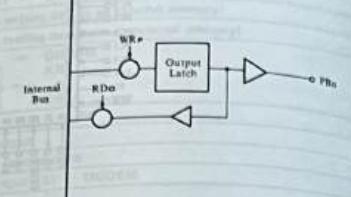


The Port B Structure

(a) A bit of the Port B is defined as an output port (MODE·Bn = 0)

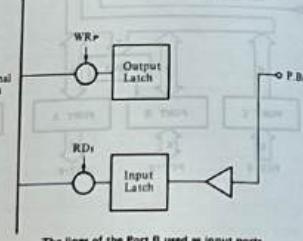
In this case, an output latch becomes valid, and with move instructions, the data can be transferred between output latch buffers of the port-lines and an accumulator.

The latched contents can be freely handled with Arithmetic and Logic instructions. Once the data is written on the buffer, the buffer will maintains the data until another Port B instruction will be executed or a reset will be issued.



(b) A bit of the Port B is defined as an input port (MODE·Bn = 1)

The input latch buffer becomes active, this time. The content of the input latch buffer can be loaded onto the accumulator with a move instruction. Also a write operation onto output latch buffers of the port lines are possible, too, i.e., by a move instruction, the data on the accumulator can be stored onto all the output latch buffers of the Port B, no matter which a port line is set as input or output port. However, the contents of the output latch buffer of the port lines used as input port can not be loaded onto the accumulator, by a move instruction. Besides, since the output latch buffers of the input ports are a high impedance state, the contents of the buffers do not appear on the port lines. But, if the port lines then are switched over from input mode to output mode, the contents stored in the output latch buffers mentioned in the above, can appear on the port lines, and also can be loaded on the accumulator.



The lines of the Port B used as input ports

However, an actual instruction execution is done per 8-bit data. If a Port B read instruction (MOV A, PB) is executed, the contents of input latch buffers indicated as input ports and the ones of output latches indicated as output ports are loaded onto the accumulator. If a Port B write instruction (MOV PB, A etc.) is executed, the contents of the output latch buffers indicated as input ports are not replaced with another data by the instruction execution, and accordingly, the write data corresponding to these bits are disregarded. Thus, the write data operation is executed only to the output latches indicated as output ports. The same thing can be said to the Port C, too.

PC₇₋₀ (Port C) ... 3-state Input/Output

This is a peculiar 8-bit input/output port. Only the lower 2-bit PC₀, PC₁ have a 3-state function. These two lines are general purpose input/output ports, and have each input/output latch buffer just the same structure/function as a Port B. In case of being set as input ports, or during reset, these lines become a high impedance state.

In addition to the PC₇₋₀ being general purpose input or output ports, these upper 6-bit can be programmed to provide various control capabilities by using the MODE·C Register, and the following table shows each function:

	MODE·Cn=0	MODE·Cn=1
PC ₀	Output	Input
PC ₁	Output	Input
PC ₂	SCS Input	Input
PC ₃	SAK Output	Output
PC ₄	TO Output	Output
PC ₅	IO/M Output	Output
PC ₆	HDLA Output	Output
PC ₇	HOLD Input	Input

The contents of this port can be freely handled with Arithmetic and Logic instructions, and with Move instructions, the data can be transferred between the port and accumulator. If the port is used as general purpose input/output port, the operation is done per 8-bit data. However, the write data onto the input port lines are disregarded. If the port is used as control input/output signals, the operation of each bit line is determined mostly by not instructions but on-chip serial or hold control circuit.

SAK (Serial Acknowledge) ... PC₃

The software control can configure PC₃ as SAK. This control line is used to build up multi-processor systems by using serial input/output lines, easily. This goes low after the completion of serial data move (i.e., after 8 serial clocks), and it goes high when a data Move instruction from the Serial Register to accumulator is completed, or when the transfer data from the accumulator to Serial Register is ready. This line can be used as interrupt signal to another processor at the systems.

SCS (Serial Chip Select) ... PC₂

The software control can configure PC₂ as SCS. This

control line is used to build up multi-processor system by using serial input/output lines, easily.

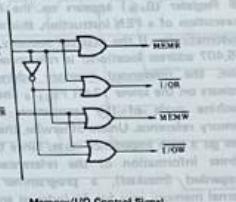
If SCS has a low signal, the serial clock (SCK) becomes valid, and the serial data transfer is available through SI and SO lines. If SCS has a high signal, the SO becomes a high impedance state, and the SCK is inhibited at that time. If the PC₂ is a general purpose input line (MC₂ = 1), the SI, SO and SCK lines are always active.

TO (Timer Out) ... PC₄

The software control can configure PC₄ as TO. This control line is used as an output line of the Timer F/F whose timer is set by a STM instruction and is reset if a borrow happens due to the count-down operation of the timer.

IO/M (IO/Memory) ... PC₅

The software control can configure PC₅ as IO/M. If an external memory is accessed, this line goes low, and otherwise, it goes high. If in the system, there are only external memories and no I/O, then this control line is not necessary. If there are both of external memory and I/O in the systems, by a following connection, the necessary control signals can be generated:



HDLA (Hold Acknowledge) ... PC₆

The software control configures PC₆ as HDLA. If a Hold Acknowledge Request is accepted, this line goes high, and during the Hold-cycle, it maintains the high level. If a Hold state is released, it goes low.

HOLD (Hold Request) ... PC₇

The software control can configure PC₇ as HOLD. With a Hold Request signal input, this control line is checked at each machine cycle. If it is high, instead of proceeding to the next machine cycle, the CPU enters a Hold cycle (TH), and an address bus (PE₁₅₋₁), data bus (DB₇₋₀), RD and WR go a high impedance state. At this time, it let a HDLA signal go a high impedance, too. This Hold-state is maintained while a Hold signal stays in high. If a Hold signal goes low, a HDLA goes low, and the high impedance state of each bus and control signals is released. Then, the CPU proceeds to the next machine cycle.

DB₇₋₀ (Data Bus) ... 3-state Input/Output

This is a 8-bit bi-directional data bus. The data move between an external memory or I/O, and accumulator is done through this data bus. During an input mode, HALT, HOLD, and RESET, the output of the data bus goes a high impedance state.

PE₁₅₋₀ (Port E) ... 3-state Output

This is a 16-bit address bus/output port. There are three ways to use these lines as follows:

(a) 16-bit Address Bus Mode

If users want to attach external memories up to 60k bytes to the μCOM-87 (SC78C6G32), they can attain their intention by using all these lines as 16-bit address bus. This mode can be set by a PER instruction or reset signal. If the external memory space (4,096 – 65,407 address locations) is referenced by an instruction, the referenced memory address information appears on the PE₁₅₋₀ only during a machine cycle of the instruction for an external memory reference. Unless otherwise, all the bit-lines (PE₁₅₋₀) go a high impedance state. At this mode (16-bit Address Bus Mode), all the bit-lines (PE₁₅₋₀) also go a high impedance state during a Halt, Hold, and Reset operation.

(b) 4-bit Output Port + 12-bit Address Bus Mode

If users want to attach external memories to up 4k bytes to the system, they can attain its intention by using the lower 12-bit lines (PE₁₁₋₀) as the address bus. By a PEN instruction, the upper 4-bit data of the B Register (B₇₋₄) appears on the PE₁₅₋₁₂. By an execution of a PEN instruction, this mode can be set automatically. If the external memory space (4,096 – 65,407 address locations) is referenced by an instruction, the referenced memory address information appears on the lower 12-bit PE₁₁₋₀ lines only during a machine cycle of the instruction of an external memory reference. Unless otherwise, the 12-bit PE₁₁₋₀ lines go a high impedance state. Since the upper 4-bit address information of the referenced memory is disregarded (masked), a programmer can set an external memory area for 4k bytes at any place in the external memory space, arbitrarily. At this mode (4-bit Output Port + 12-bit Address Bus Mode), the lower 12-bit lines of the Port E (PE₁₁₋₀) go a high impedance state during a Halt, Hold, and Reset operation. However, the rest of the upper 4-bit lines of the Port E (PE₁₅₋₁₂) are not influenced by a Halt and Hold operation.

(c) 16-bit Output Port Mode

If users do not want to extend any external memory on the system, they can use the full 16-bit lines of the Port E as general purpose output ports. By a PEX instruction, the contents of the B Register and C Register appear on PE₁₅₋₄ and PE₇₋₀, respectively. By an execution of a PEX instruction, this mode can be set automatically. At this mode (16-bit Output Port Mode), all the bit-lines of the Port E are not influenced by a Halt and Hold operation.

M1 (Machine Cycle 1)

This is used as an output signal of notifying the outside of first machine cycle of each instruction. It goes high and maintains the high level during the fetch cycle of the first OP₁ code over the T₁ to T₃. If users want to perform a single step or break operation, they can complete it by using this line.

WAIT (Wait Request)

If users use rather slow speed external memories in the systems, they can extend a READ/WRITE timing to meet this slow device, by providing a low level signal to this line. The WAIT signal is checked at the end of T₂. If it is low, it goes to a wait state (T_w), and it stays in the state until the WAIT goes high.

INT 0, INT 1, INT 2 (Interrupt Request)

These are Interrupt Request Input lines. INT 0 is level sensitive, INT 1 is a rising-edge sensitive, and INT 2 is a falling-edge sensitive, respectively. The interrupt priority among the interrupts is shown below.

INT 0 > INT 2 > INT 1 > INT 2 > INTS

Here, INTT and INTS are internal interrupts.

(a) INT 0

It is a level-sensitive interrupt input line which is high level active.

(b) It is a rising-edge sensitive interrupt line, and it becomes valid when INT 1 input goes low to high. Subsequently, if users want to perform another interrupt, they must take it into consideration that INT 1 input should be maintained at low state a little while, and then it should go high. Unless, it does not enable another interrupt.

(c) INT 2

It is a rising or falling-edge sensitive interrupt line. It depends upon a state of the ES-bit of the MASK Register which of the two, rising edge or falling edge becomes valid. If the ES-bit is high('1'), this interrupt line is rising edge sensitive. If it is low it is falling edge sensitive. The contents of the MASK Register can be set or reset with instructions.

In order to avoid a possible mis-operation due to noise signals less than 2 μs, all the above three interrupt lines are sampled with internal clocks by 2 μs rate, periodically. Subsequently, an interrupt request signal must have more than 4 μs active time.

X₀, X₁ (Xtal)

These are connected to the crystal for the internal clock generator circuit. The X₁ is used as the external clock input, instead of the crystal, too.

SCK (Serial Clock)

This is used as control clocks for serial input/output data. At the rising edge of SCK, the data on a SI line is loaded to the Serial Register (S/P), and at the falling edge of SCK, the contents of the Serial Register appear on a SO line with a bit-order from MSB to LSB.

SI (Serial Input)

This is a serial input port, and the data on the SI is loaded to the Serial Register at the rising edge of SCK. The beginning bit is a MSB.

SO (Serial Output)

This is a serial output port, and the data on the Serial Register appears on the SO. The beginning bit is a MSB.

RESET (Reset)

In order to avoid a possible mis-operation due to noise signals less than 2 μs, this line does not accept less than 2 μs level signals as valid ones. If more than 4 μs low level signal is issued to this line, μCOM87 is reset, and it becomes as follows:

- (1) Interrupt Enable Flags are reset, and Interrupts are inhibited.
- (2) Interrupt Request Flag is reset.
- (3) HALT F/F is reset, and a Halt-state is released.
- (4) The contents of the MODE - B Register are set to F_{F1(16)}, and the Port B lines become an input mode (the output latch buffers of the Port B go a high impedance state).
- (5) The contents of the MODE - C Register are set to F_{F1(16)}, and the PC₂ and PC₁ become an input mode (the output latch buffers of these port lines go a high impedance state), and the reset of the PC₂-7 becomes an input or output port mode. At this time, the output port lines go low.
- (6) The output lines of the Port A go low.
- (7) All the Flags are reset to 0.
- (8) The on-chip COUNT Register for a time operation is set to FFF₍₁₆₎, and a timer F/F is reset.
- (9) ACK F/F is set.
- (10) HLDA F/F is reset.
- (11) The contents of the PC is reset to 0000₍₁₆₎.
- (12) The address bus (PF₁₅₋₀), data bus (DB₇₋₀), RD, and WR signals go a high impedance state.

If the RESET input goes high, the program runs from 0000₍₁₆₎ address;

WR (Write Strobe) ... 3-state Output

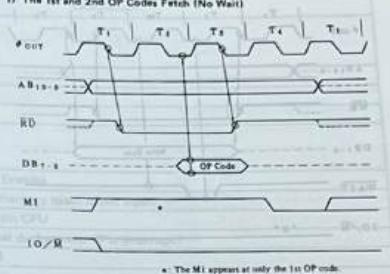
This is used as a strobe signal for a write operation for an external memory or I/O. This line goes a high impedance state except during a machine cycle for a data write by an execution of an external memory reference instruction and OUT instruction. This line also goes a high impedance state during a Halt, Hold, and Reset operation, too.

RD (Read Strobe) ... 3-state Output

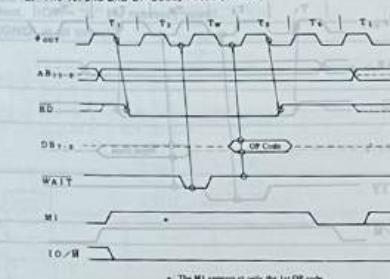
This is used as a strobe signal for a read operation for an external memory or I/O. This line goes a high impedance state except during a read machine cycle for an external program memory, and a machine cycle for a data read by an execution of an external memory reference instruction and IN instruction. This line also goes a high impedance state during a Halt, Hold, and Reset operation, too.

TIMING WAVEFORMS

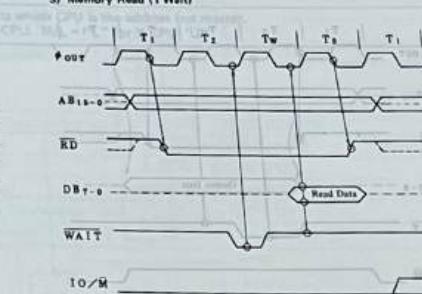
1) The 1st and 2nd OP Codes Fetch (No Wait)



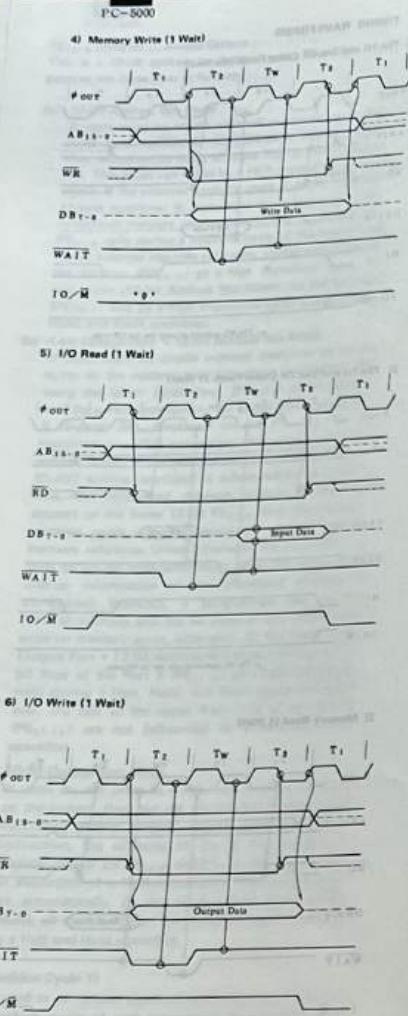
2) The 1st and 2nd OP Codes Fetch (1 Wait)



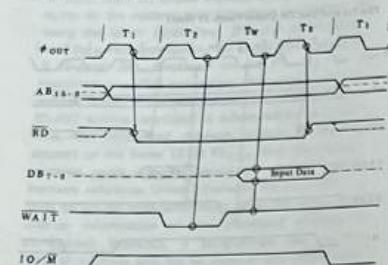
3) Memory Read (1 Wait)



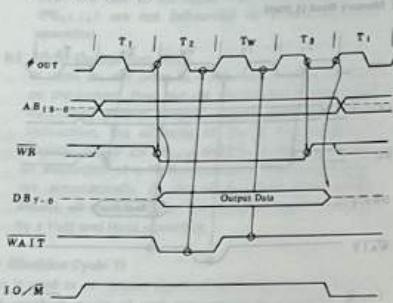
4) Memory Write (1 Wait)



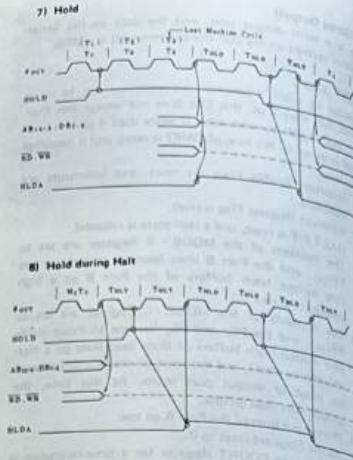
5) I/O Read (1 Wait)



6) I/O Write (1 Wait)

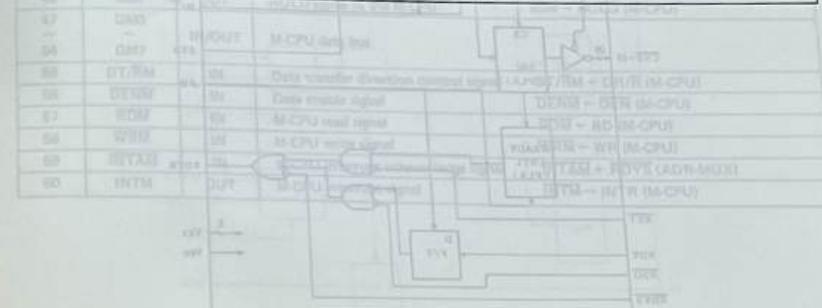


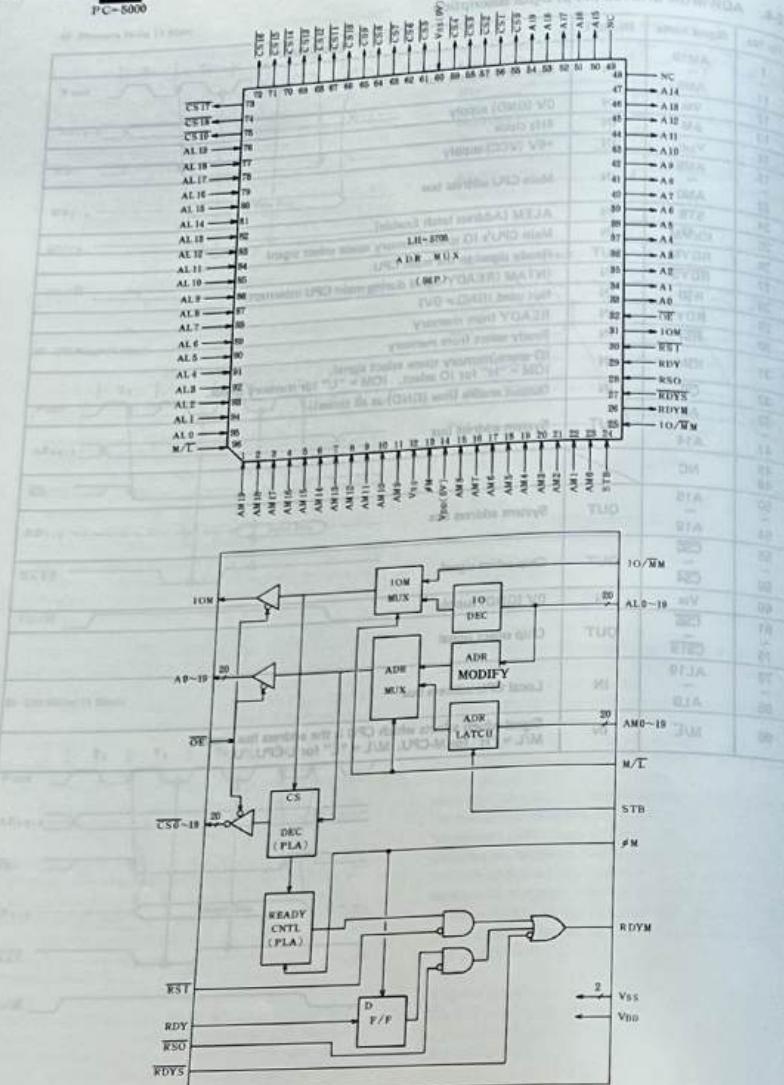
7) Hold



24. ADR-MUX LH5705 (96-p) signal description

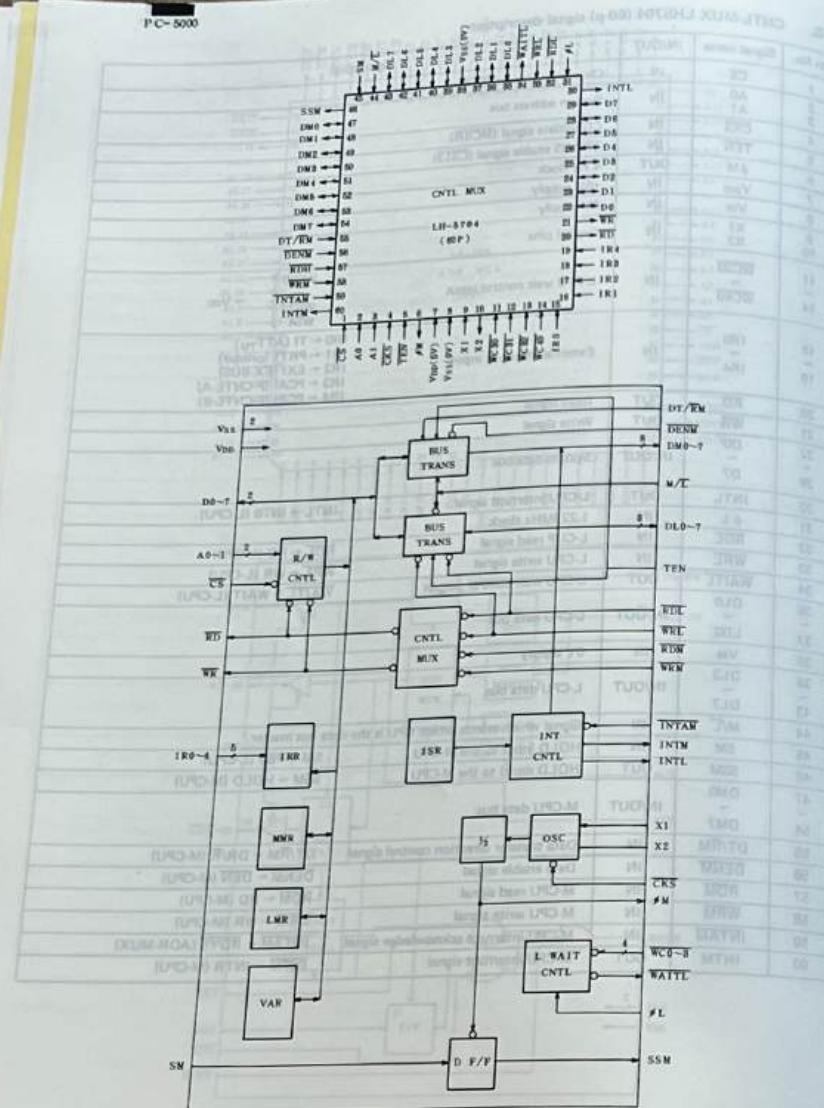
Pin No.	Signal name	IN/OUT	Description
1 ~	AM19 ~ AM9	IN	Main CPU address bus
11 ~	V _{SS}	IN	0V (GND) supply
12 ~	φ _M	IN	4Hz clock
14 ~	V _{DD}	IN	+5V (V _{CC}) supply
15 ~	AM8 ~ AM0	IN	Main CPU address bus
24 ~	STB	IN	ALEM (Address latch Enable)
25 ~	IOM/MM	IN	Main CPU's I/O space/memory space select signal
26 ~	RDYM	OUT	Ready signal to the main CPU
27 ~	RDYS	IN	INTAM (READY signal during main CPU interrupt)
28 ~	RS0	IN	Not used (GND = 0V)
29 ~	RDY	IN	READY from memory
30 ~	RSI	IN	Ready select from memory
31 ~	IOM	IN	I/O space/memory space select signal. IOM = "H" for I/O select. IOM = "L" for memory select.
32 ~	OE	IN	Output enable (low (GND) at all times)
33 ~	A0 ~ A14	OUT	System address bus
48 ~	NC		
50 ~	A15 ~ A19	OUT	System address bus
54 ~	CS0 ~ CS4	OUT	Chip select signal
55 ~	V _{SS}	IN	0V (GND) supply
61 ~	CS5 ~ CS19	OUT	Chip select signal
60 ~	AL19 ~ AL0	IN	Local CPU address bus
96 ~	M/L	IN	Signal which selects which CPU is the address bus master. M/L = "H" for M-CPU. M/L = "L" for L-CPU. "U"





2-5. CNTL-MUX LH5704 (60-p) signal description

Pin No.	Signal name	IN/OUT	Description
1	CS	IN	Chip select signal (CS16)
2	A0	IN	System address bus
3	A1	IN	
4	CRS	IN	CG initiate signal (MCBR)
5	TEN	IN	TRANS enable signal (CST3)
6	φM	OUT	4 Hz clock
7	VDD	IN	+5V supply
8	VSS	IN	0V supply
9	X1	IN	
10	X2	IN	Crystal pins
11	WC30	IN	
~	WC40	IN	
14			WS30 } WS32 } WS54 } → Vcc
15	IR0	IN	External interrupt input IR0 ← TI (ATT-to) IR1 ← PRT1 (printer)
~	IR4	IN	IR2 ← EXI (EX-BUS) IR3 ← PCA1 (P-CNTL-A) IR4 ← PCB1 (P-CNTL-B)
20	RD	OUT	Read signal
21	WR	OUT	Write signal
22	~	IN/OUT	
29	D0	IN/OUT	System data bus
30	INTL	OUT	L-CPU interrupt signal INTL → INT0 (L-CPU)
31	φL	IN	1.229MHz clock
32	RDL	IN	RDL ← RD (L-CPU)
33	WRL	IN	WRL ← WR (L-CPU)
34	WAITE	OUT	WAITL → WAIT (L-CPU)
35	DL0	IN/OUT	L-CPU data bus
~	DL2	IN/OUT	
37			
38	VSS	IN	0V supply
39	DL3	IN/OUT	L-CPU data bus
~	DL7	IN/OUT	
43			
44	M/L	IN	Signal which selects which CPU is the data bus master.
45	SM	IN	HOLD input to the M-CPU SM ← PBO (L-CPU)
46	SSM	OUT	HOLD signal to the M-CPU SSM → HOLD (M-CPU)
47	DM0	IN/OUT	
~	DM7	IN/OUT	M-CPU data bus
54			
55	DT/RM	IN	Data transfer direction control signal DT/RM ← DR/R (M-CPU)
56	DENM	IN	Data enable signal DENM ← DEN (M-CPU)
57	RDM	IN	M-CPU read signal RDM ← RD (M-CPU)
58	WRM	IN	M-CPU write signal WRM ← WR (M-CPU)
59	INTAM	IN	M-CPU interrupt acknowledge signal INTAM ← RDYS (ADR-MUX)
60	INTM	OUT	M-CPU interrupt signal INTM → INTR (M-CPU)

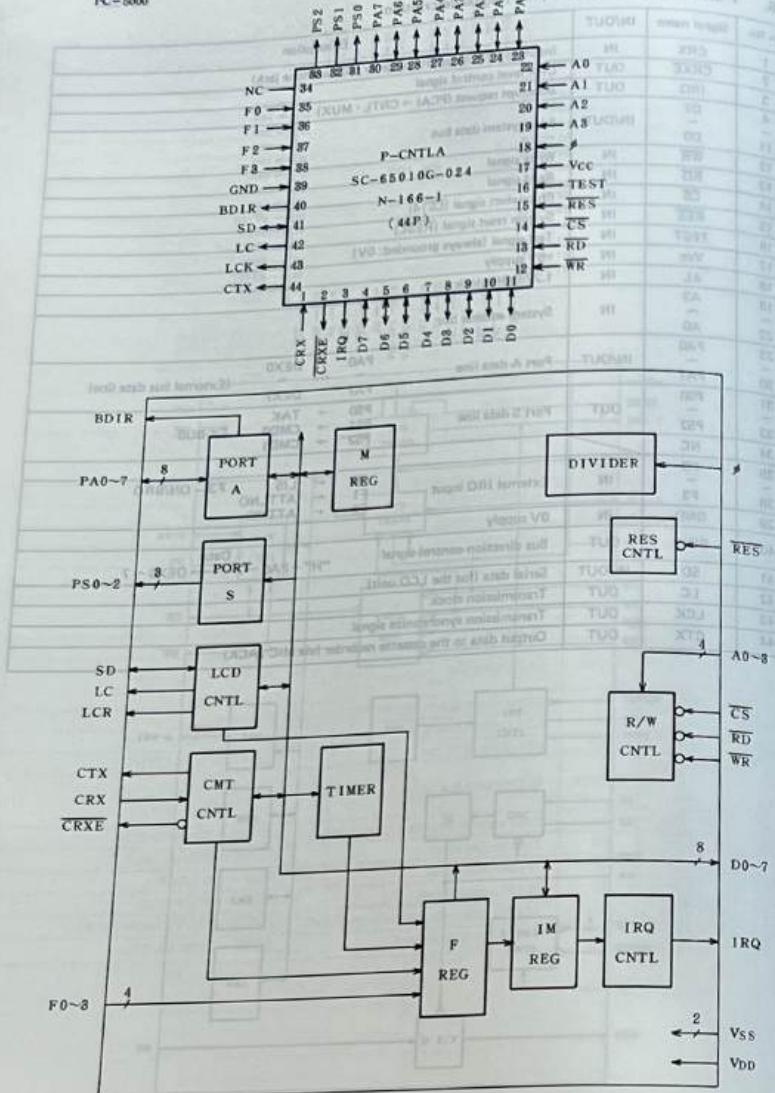


2-13

2-6. P-CNTL-A SC65010G-024 (44-P) signal description

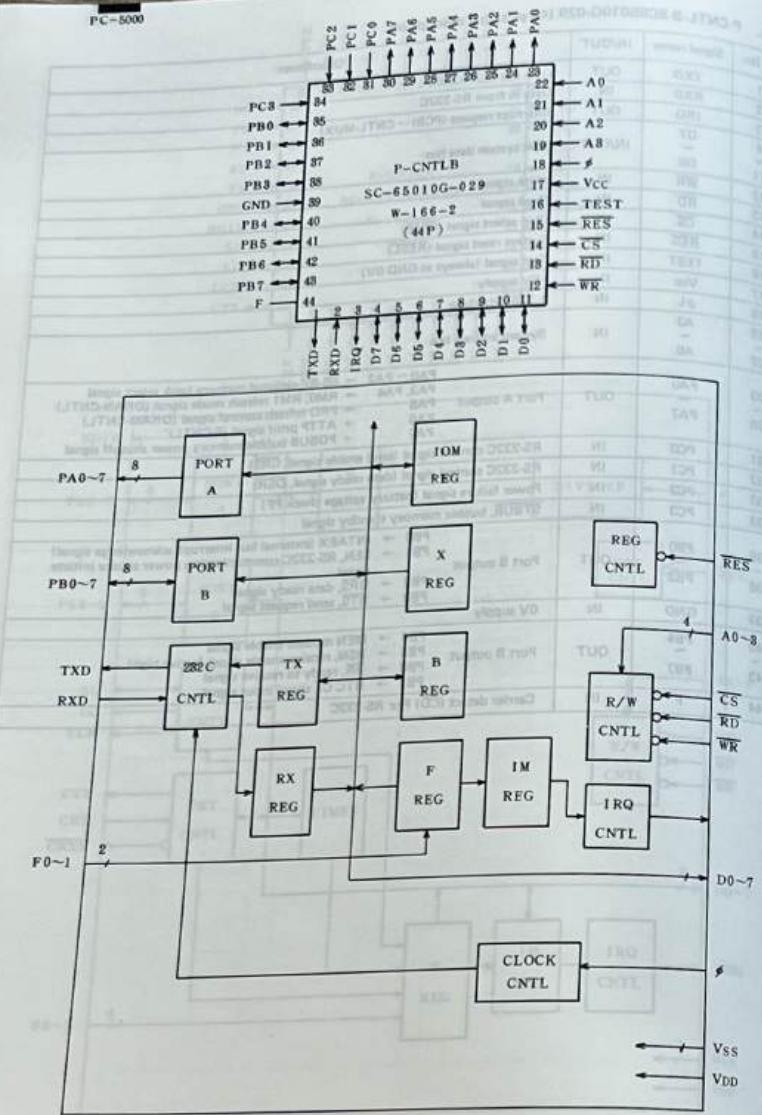
Pin No.	Signal name	IN/OUT	Description					
1	CRX	IN	Input data from cassette recorder (via earphone jack)					
2	CRXE	OUT	CRX level control signal					
3	IRO	OUT	Interrupt request (PCA1 → CNTL + MUX)					
4	D7							
~	~							
11	DO	IN/OUT	8-bit system data bus					
12	WR	IN	Write signal					
13	RD	IN	Read signal					
14	CS	IN	Chip select signal (CS14)					
15	RES	IN	System reset signal (RESL)					
16	TEST	IN	Test signal (always grounded; 0V)					
17	Vcc	IN	+5V supply					
18	φL	IN	1.229MHz clock					
19	A3							
~	~							
22	A0	IN	System address bus					
23	PA0							
~	~							
30	PA7	IN/OUT	Port A data line		PA0 ~ DEX0 PA7 ↔ DEX7	(External bus data line)		
31	PS0							
~	~							
33	PS2	OUT	Port S data line		PS0 → TAK PS1 → CMD0 PS2 → CMD1	EX-BUS		
34	NC							
35	F0							
~	~							
38	F3	IN	External IRO input		F0 ← LIS F1 ← ATTINO F2 ← ATTMO	F3 — ON/BRO		
39	GND	IN	0V supply					
40	BDIR	OUT	Bus direction control signal		Data “H” = PA0 ~ 7 → DEX0 ~ 7			
41	SD	IN/OUT	Serial data (for the LCD unit)					
42	LC	OUT	Transmission clock					
43	LCK	OUT	Transmission synchronize signal					
44	CTX	OUT	Output data to the cassette recorder (via MIC JACK)					

2 - 1



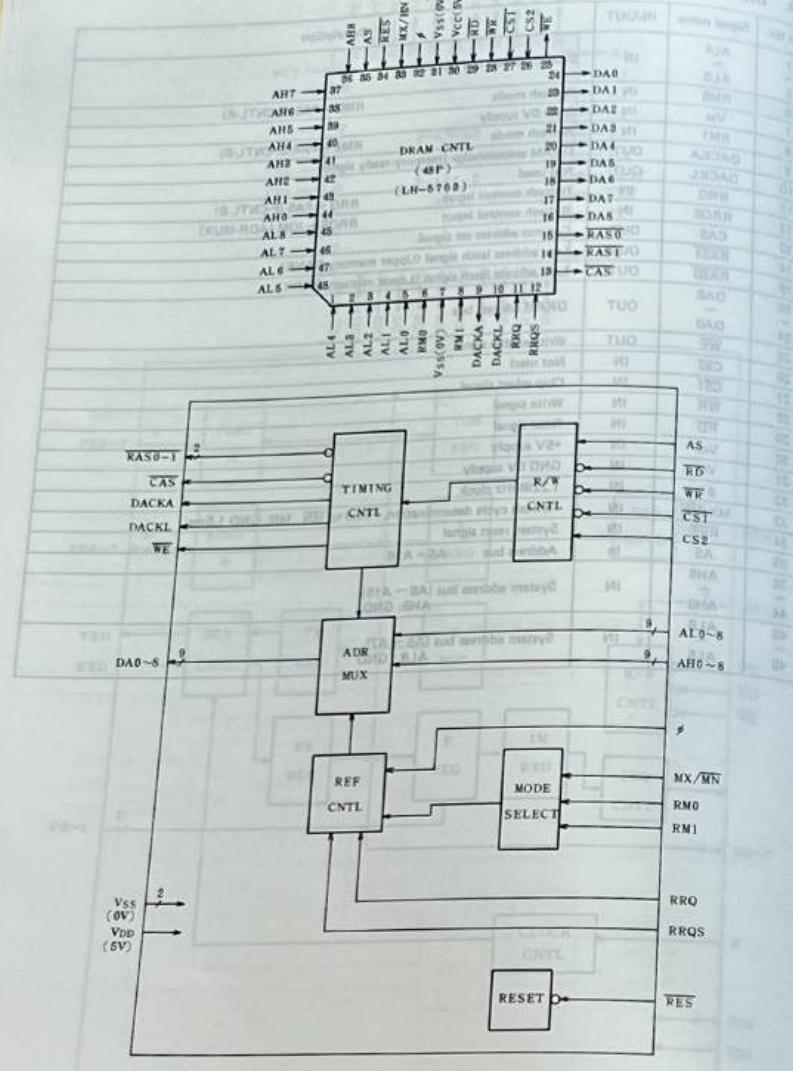
2-7. P-CNTL-B SC65010G-029 (44-p) signal description

Pin No.	Signal name	IN/OUT	Description
1	TXD	OUT	Data out to RS-232C
2	RXD	IN	Data in from RS-232C
3	IRQ	OUT	Interrupt request (PCBI → CNTL-MUX)
4	D7	IN/OUT	8-bit system data bus
~	D0	IN/OUT	
11	WR	IN	Write signal
12	RD	IN	Read signal
13	CS	IN	Chip select signal (CS15)
15	RES	IN	System reset signal (RESL)
16	TEST	IN	Test signal (always at GND 0V)
17	Vcc	IN	+5V supply
18	φL	IN	1.229MHz clock
19	A3	IN	System address bus
~	A0	IN	
23	PA0 ~ PA2	OUT	PA0 ~ PA2 → BO-B2 optional memory bank select signal PA3, PA4 → RMD, RM1 refresh mode signal (DRAM-CNTL)
~	PA7	OUT	PA5 → PRO refresh control signal (DRAM CNTL) PA6 → ATTTP print signal (P-CNTL) PA7 → PDBUB bubble memory power shutoff signal
31	PC0	IN	RS-232C control signal (send enable signal, CRS)
32	PC1	IN	RS-232C control signal (data ready signal, DSR)
33	PC2	IN	Power failure signal (battery voltage check PF)
34	PC3	IN	STBUB, bubble memory standby signal
35	PB0 ~ PB3	OUT	PB0 → INTAEX (external bus interrupt acknowledge signal) PB1 → SEN, RS-232C communication power source initiate signal PB2 → DR5, data ready signal PB3 → RTS, send request signal
38	GND	IN	0V supply
40	PB4 ~ PB7	OUT	PB4 → MEN modem enable signal PB5 → RSN, receive enable signal (active high) PB6 → RR, ready to receive signal PB7 → RTC CE signal input signal
43	F	IN	Carrier detect (CD) For RS-232C



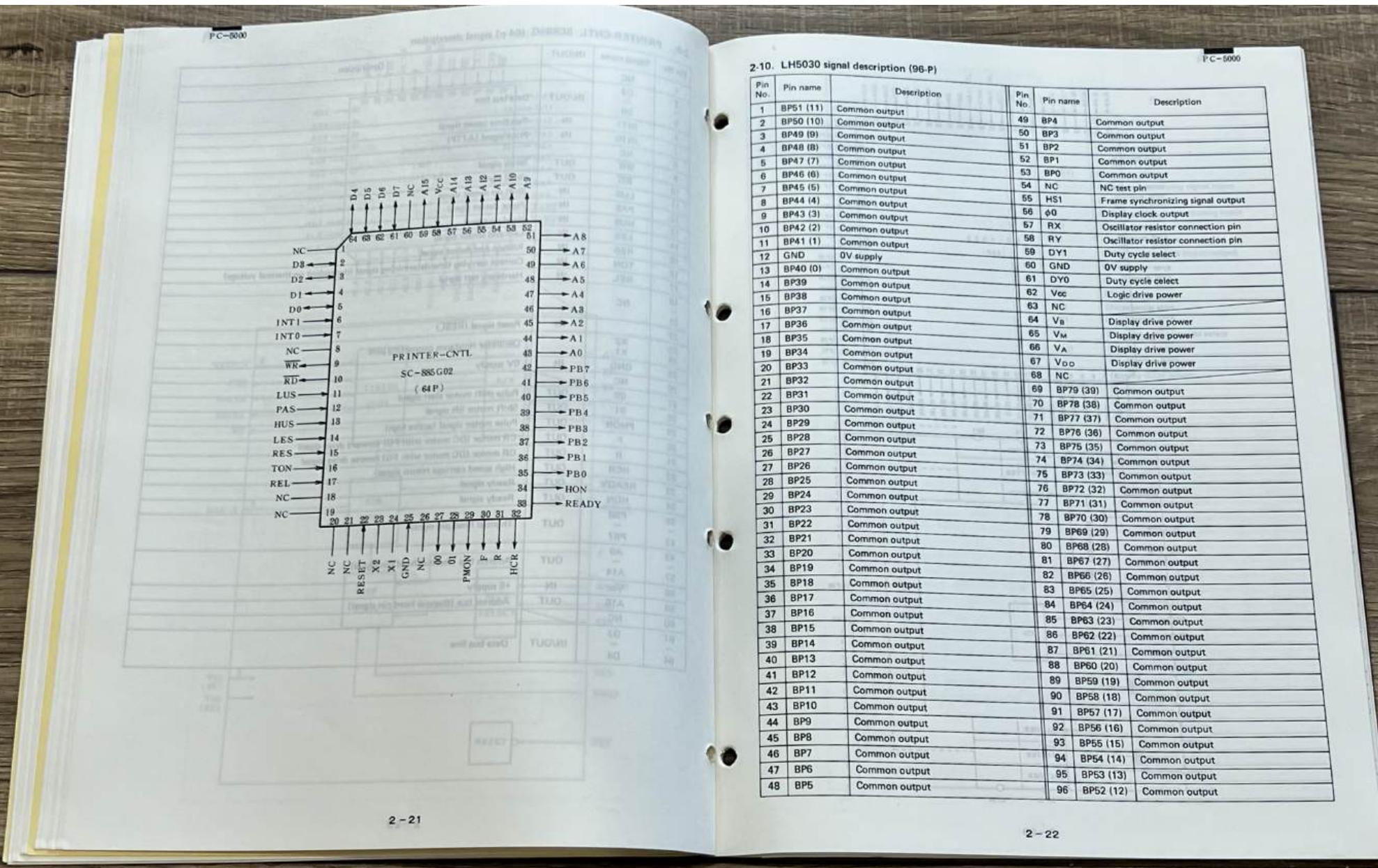
2-8. DRAM-CNTRL LH5703 (48-p) signal description

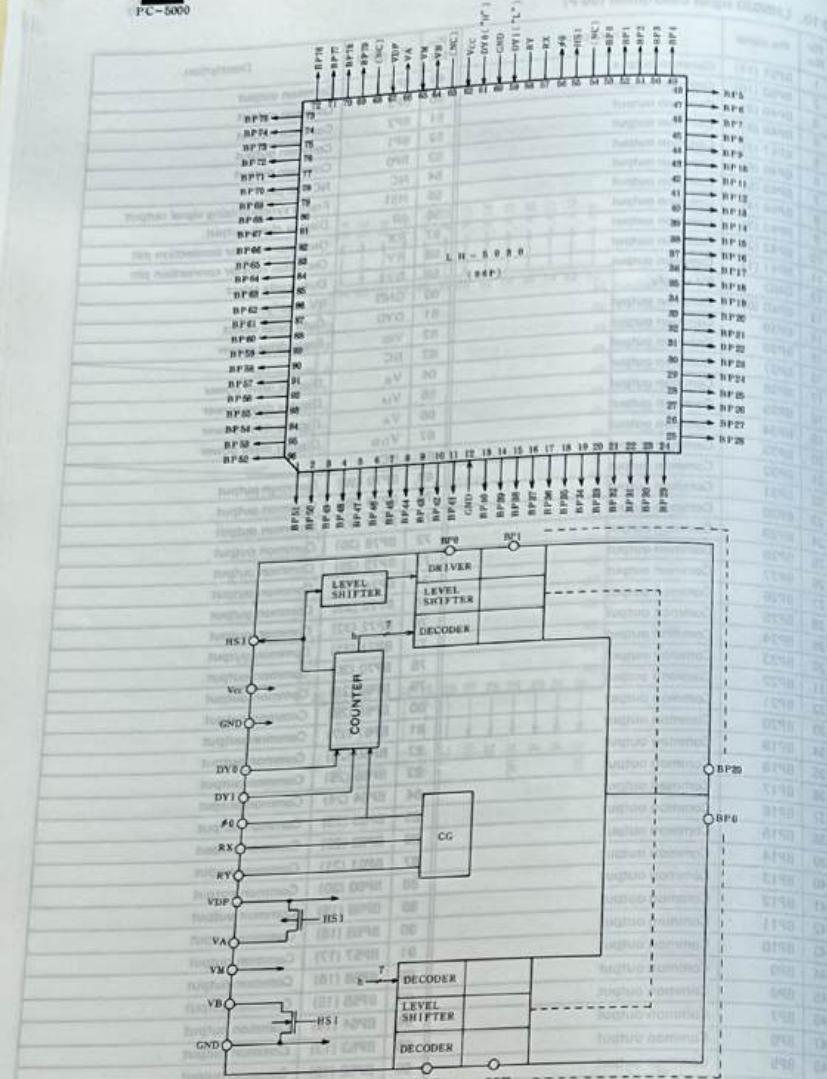
Pin No.	Signal name	IN/OUT	Description
1	AL4 ~ AL0	IN	System address bus (A4-A0)
5	RMO	IN	Refresh mode
6	RM1	IN	GND 0V supply
7	Vss	IN	Refresh mode
8	IN		RM1 ~ PA3 (P-CNTL-B)
9	DACKA	OUT	DRAM acknowledge (memory ready signal)
10	DACKL	OUT	Not used
11	RRO	IN	Refresh control input
12	RRQS	IN	Refresh control input
13	CAS	OUT	Column address set signal
14	RASI	OUT	Low address latch signal (Upper memory BANK)
15	RAS0	OUT	Low address latch signal (Lower memory BANK)
16	DAB	~	DRAM address bus
24	DAO	OUT	
25	WE	OUT	Write enable signal
26	CS2	IN	Not used
27	CSI	IN	Chip select signal
28	WR	IN	Write signal
29	RD	IN	Read signal
30	Vcc	IN	+5V supply
31	Vss	IN	GND 0V supply
32	φL	IN	1.229MHz clock
33	MX/MN	IN	Refresh cycle determination. Fixed to MN MN: GND 1.5ms
34	RES	IN	System reset signal
35	AS	In	Address bus AS = A16
36	AH8 ~ AH0	IN	System address bus (A8 ~ A15) AH8: GND
44	AL8 ~ AL5	IN	System address bus (A5 ~ A7) AL8: GND



2-9. PRINTER-CNTL SCB85G (64-p) signal description

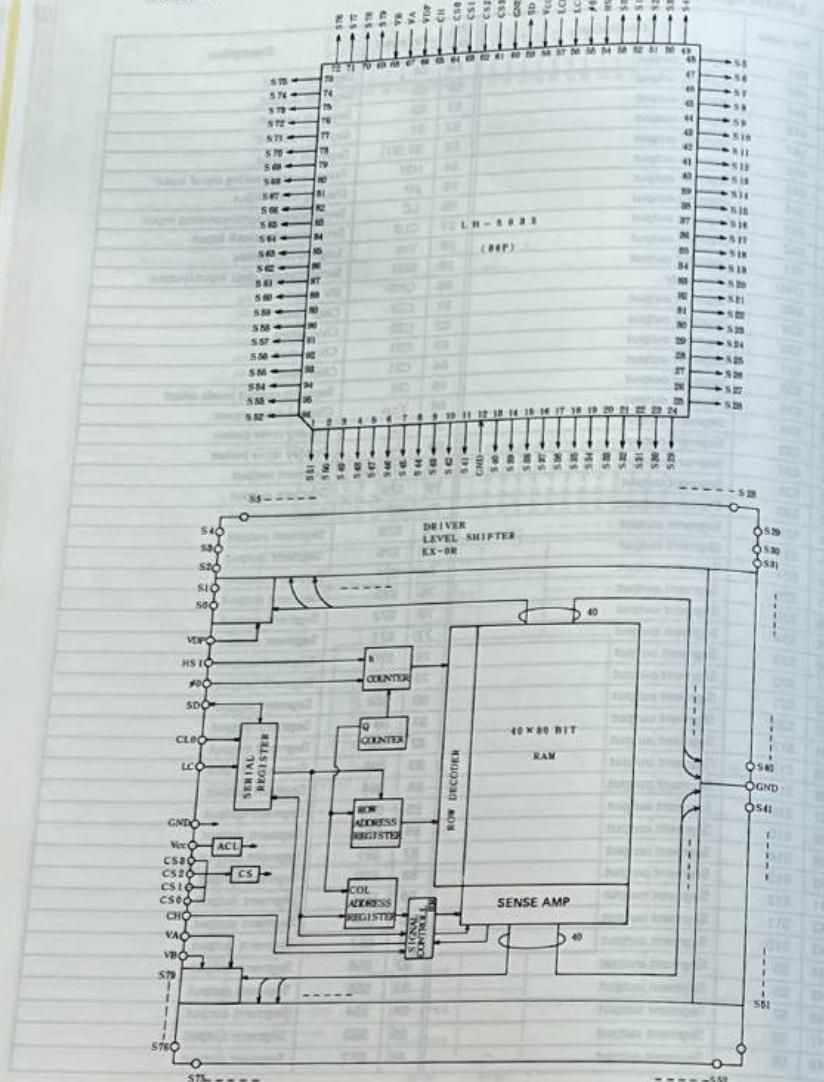
Pin No.	Signal name	IN/OUT	Description
1	NC		
2	D3	IN/OUT	Data bus line
5	DO		
6	INT1	IN	Ton time count signal
7	INT0	IN	Print signal (ATTP)
8	NC		
9	WR	OUT	Write signal
10	RD	OUT	Read signal
11	LUS	IN	Shift up detect signal
12	PAS	IN	Paper detect signal
13	HUS	IN	Head up signal
14	LES	IN	Left end sensor signal
15	RES	IN	Ribbon end detect signal
16	TON	IN	Current carrying time determining signal (dependent on thermal voltage)
17	REL	IN	Hardware test signal
18	NC		
21			
22		IN	Reset signal (RESL)
23	X2		Oscillator resistance connecting pins
24	X1		
25	GND	IN	0V supply
26	NC		
27	00	OUT	Pulse shift motor start signal
28	01	OUT	Shift motor lift signal
29	PMON	OUT	Pulse motor signal (active high)
30	F	OUT	CR motor (DC motor with FG) forward drive signal
31	R	OUT	CR motor (DC motor with FG) reverse drive signal
32	HCR	OUT	High speed carriage return signal
33	READY	OUT	Ready signal
34	HON	OUT	Ready signal
35	PB0	OUT	Thermal head pin signal
42	~ PB7	OUT	
43	A0	OUT	Address bus (thermal head pin signal)
57	~ A14	OUT	
58	Vcc	IN	+5 supply
59	A15	OUT	Address bus (thermal head pin signal)
60	NC		
61	D7	IN/OUT	Data bus line
64	~ D4	IN/OUT	
65	BP13	Common output	
66	BP12	Common output	
67	BP10	Common output	
68	BP9	Common output	
69	BP8	Common output	
70	BP7	Common output	
71	BP6	Common output	
72	BP5	Common output	
73	BP4	Common output	
74	BP3	Common output	
75	BP2	Common output	
76	BP1	Common output	





2-11. LH5035 signal description (96-p)

Pin No.	Pin name	Description	Pin No.	Pin name	Description
1	S51	Segment output	49	S4	Segment output
2	S50	Segment output	50	S3	Segment output
3	S49	Segment output	51	S2	Segment output
4	S48	Segment output	52	S1	Segment output
5	S47	Segment output	53	S0 (S1)	Segment output
6	S46	Segment output	54	HSI	Frame synchronizing signal input
7	S45	Segment output	55	φ0	Display clock input
8	S44	Segment output	56	LC	Serial transfer synchronizing input
9	S43	Segment output	57	CL0	Serial transfer clock input
10	S42	Segment output	58	Vcc	Logic driver power
11	S41	Segment output	59	SD0	Serial transfer data input/output
12	GND	0V supply	60	GND	0V supply
13	S40	Segment output	61	CS3	Chip select
14	S39	Segment output	62	CS2	Chip select
15	S38	Segment output	63	CS1	Chip select
16	S37	Segment output	64	CS1	Chip select
17	S36	Segment output	65	CH	Segment output mode select
18	S35	Segment output	66	V _{DD}	Display drive power
19	S34	Segment output	67	VA	Display drive power
20	S33	Segment output	68	V _B	Display drive power
21	S32	Segment output	69	S79 (B0)	Segment output
22	S31	Segment output	70	S78	Segment output
23	S30	Segment output	71	S77	Segment output
24	S29	Segment output	72	S76	Segment output
25	S28	Segment output	73	S75	Segment output
26	S27	Segment output	74	S74	Segment output
27	S26	Segment output	75	S73	Segment output
28	S25	Segment output	76	S72	Segment output
29	S24	Segment output	77	S71	Segment output
30	S23	Segment output	78	S70	Segment output
31	S22	Segment output	79	S69	Segment output
32	S21	Segment output	80	S68	Segment output
33	S20	Segment output	81	S67	Segment output
34	S19	Segment output	82	S66	Segment output
35	S18	Segment output	83	S65	Segment output
36	S17	Segment output	84	S64	Segment output
37	S16	Segment output	85	S63	Segment output
38	S15	Segment output	86	S62	Segment output
39	S14	Segment output	87	S61	Segment output
40	S13	Segment output	88	S60	Segment output
41	S12	Segment output	89	S59	Segment output
42	S11	Segment output	90	S58	Segment output
43	S10	Segment output	91	S57	Segment output
44	S9	Segment output	92	S56	Segment output
45	S8	Segment output	93	S55	Segment output
46	S7	Segment output	94	S54	Segment output
47	S6	Segment output	95	S53	Segment output
48	S5	Segment output	96	S52	Segment output



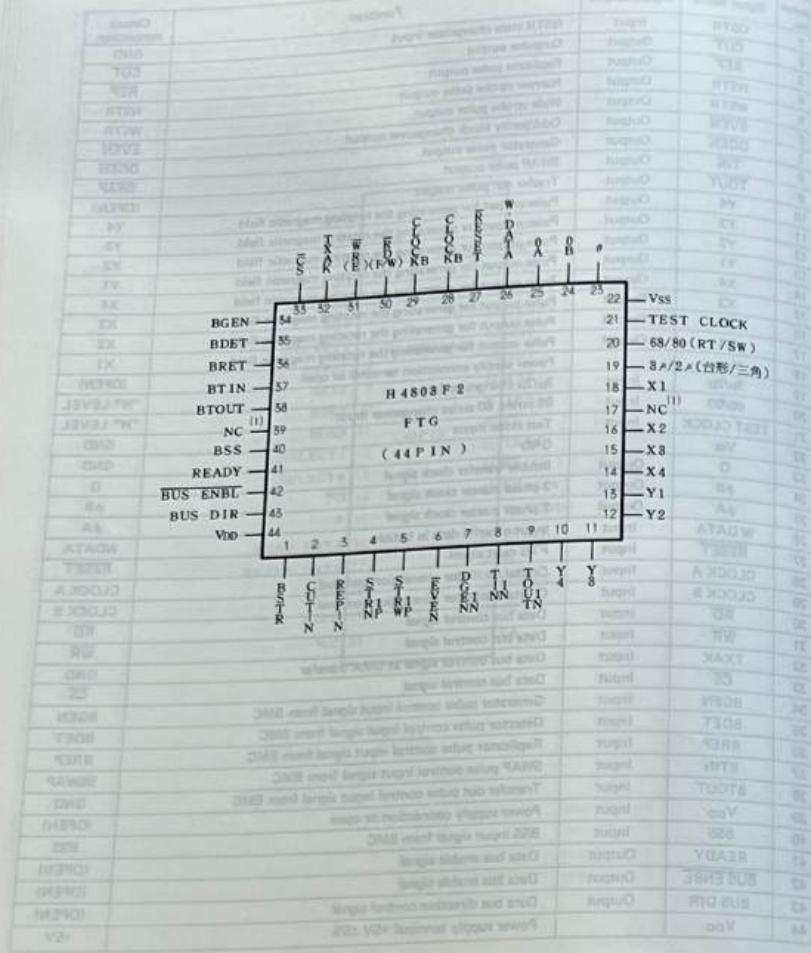
2-12. HD46507PA23 Signals and functions of BMC (40-pin)

Terminal No.	Signal Name	Input/Output	Function	Circuit connection
1	GND		GND	
2	D3	Input/Output	Bidirectional databus	D3
3	D2	Input/Output	Bidirectional databus	D2
4	D1	Input/Output	Bidirectional databus	D1
5	D0	Input/Output	Bidirectional databus LSB	D0
6	BSS	Output	Control signal used to generate rotating field to be applied to the bubble	BSS
7	SELECT 2	Output	Selection signal of bubble device and block	(OPEN)
8	BSWAP	Output	Control signal used to generate SWAP pulse	BSWAP
9	BRET	Output	Control signal used to generate replicate pulse	BREP
10	BDEP	Output	Control signal used to generate strobe pulse against sense amplifier	BDEP
11	BGEN	Output	Control signal used to generate strobe pulse against sense amplifier	BGEN
12	SELECT1	Output	Selection signal of bubble device and block	(OPEN)
13	SELECT0	Output	Selection signal of bubble device and block	SELECT 0
14	PD	Input	Signal to maintain the contents of the bubble when the power supply fail or disconnected	PD
15	θ	Input	Clock signal to create rotating magnetic field	θ
16	READ DATA	Input	Input of readout data from bubble memory	RDATA
17	WRITE DATA	Output	Output of write data in bubble memory	WDATA
18	IRQ	Output	Request for interruption against host system	(OPEN)
19	TXRO	Output	Request for data transfer against DMA controller	(OPEN)
20	Vcc		Power supply +5V ± 5%	+5V
21	φA	Input	2-phase clock to operate BMC	φA
22	φB	Input	2-phase clock to operate BMC	φB
23	PORES	Input	Signal to initialize the internal contents of BMC	PORES
24	NC		Unoccupied pin	(OPEN)
25	TESTA 1	Input	Changeover signal of normal mode ("H") and free mode ("L")	TESTA 1
26	80/68	Input	Changeover signal of 80 series and 68 series	Vcc
27	RD	Input	Timing for reading out the contents of BMC internal register	RD
28	WR	Input	Timing for writing data in BMC internal register	WR
29	TXAK	Input	Acknowledgement signal to TXRO in DMA mode	GND
30	CS	Input	Selection signal of BMC	CS
31	TESTA	Input	LIS test terminal	GND
32	RS2	Input	Selection signal of BMC internal register	RS2
33	RS1	Input	Selection signal of BMC internal register	RS1
34	RS0	Input	Selection signal of BMC internal register	RS0
35	TESTY	Input	LIS test terminal	GND
36	TESTX	Input	LIS test terminal	GND
37	D7	Input/Output	Bidirectional data bus MSB	D7
38	D6	Input/Output	Bidirectional data bus	D6
39	D5	Input/Output	Bidirectional data bus	D5
40	D4	Input/Output	Bidirectional data bus	D4

Pin	Description	Pin	Description
GND		1	analog input
DD		2	analog input
SD		3	analog input
PD		4	analog input
DO		5	analog input
SWB		6	analog input
TRIPRO		7	analog input
PLA100		8	analog input
PLA101		9	analog input
PLA102		10	analog input
PLA103		11	(40 PIN)
PLA104		12	
PLA105		13	
PLA106		14	
PLA107		15	
PLA108		16	
PLA109		17	
PLA110		18	
PLA111		19	
PLA112		20	Vcc
PLA113		21	0A
PLA114		22	0B
PLA115		23	PORES
PLA116		24	NC
PLA117		25	
PLA118		26	
PLA119		27	RD(R-W)
PLA120		28	WR(E)
PLA121		29	TXAK
PLA122		30	CS
PLA123		31	TESTA
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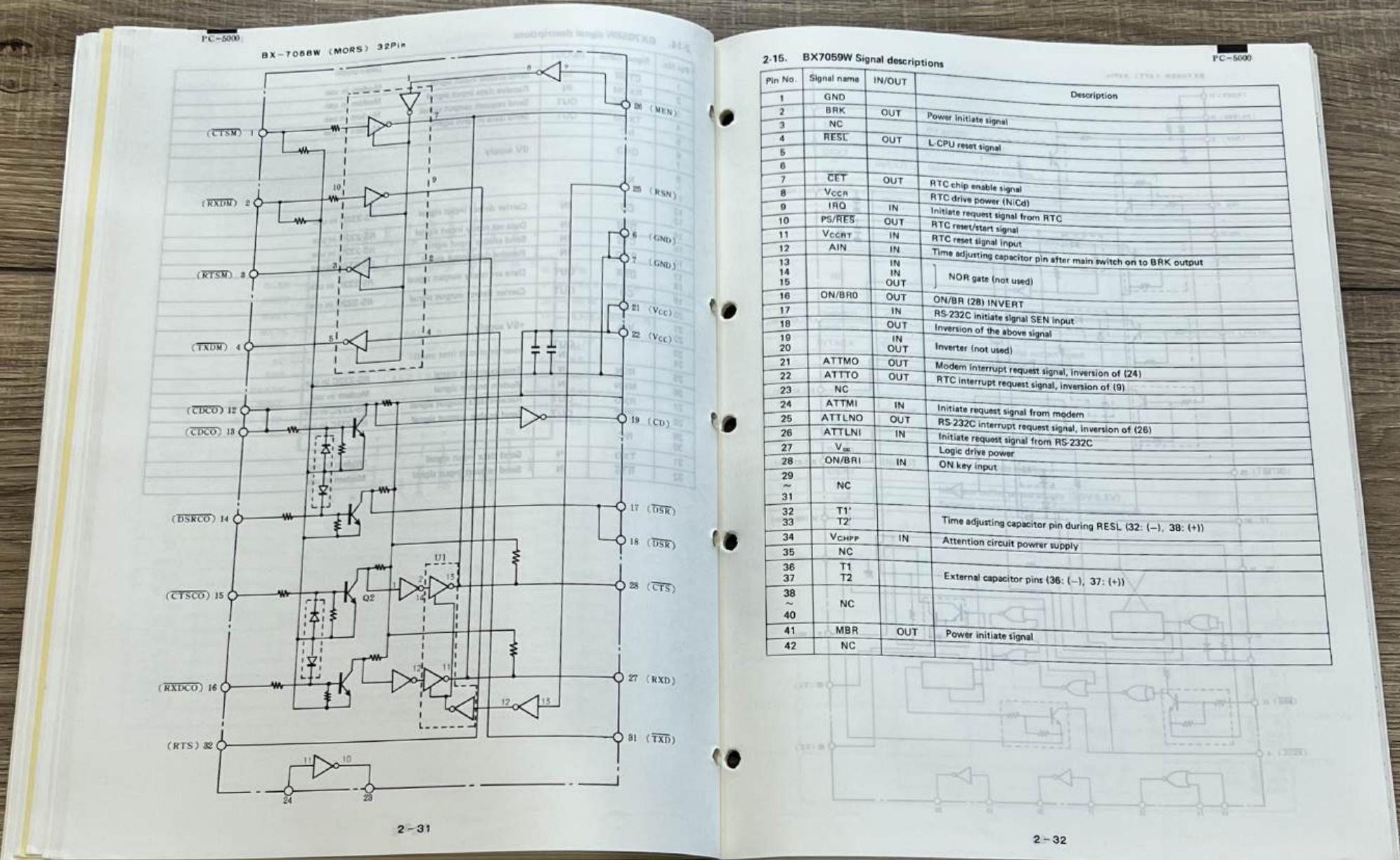
2-13. H4803F2 Signals and functions of FTG (44-p)

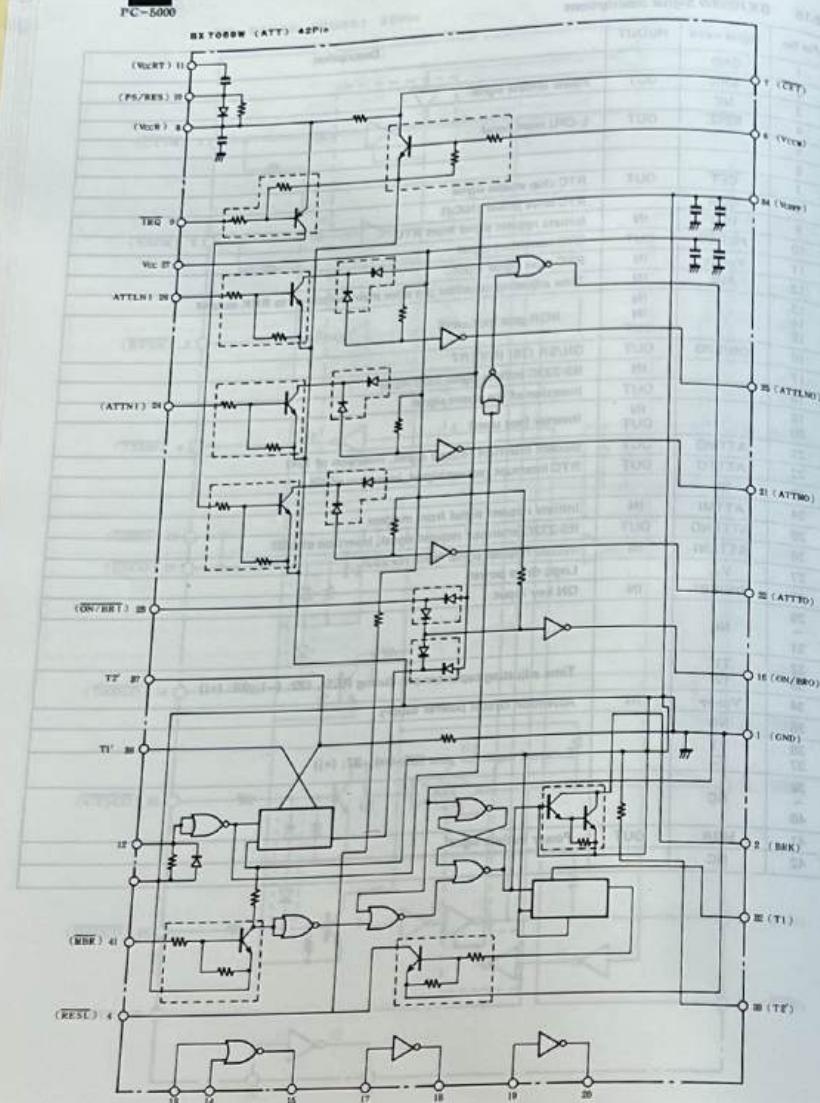
Terminal No.	Signal Name	Input/Output	Function	Circuit connection
1	OSTR	Input	NSTR state changeover input	GND
2	CUT	Output	Cutpulse output	CUT
3	REP	Output	Replicate pulse output	REP
4	NSTR	Output	Narrow strobe pulse output	NSTR
5	WSTR	Output	Wide strobe pulse output	WSTR
6	EVEN	Output	Odd/parity block changeover output	EVEN
7	DGEN	Output	Generator pulse output	DGEN
8	TIN	Output	SWAP pulse output	SWAP
9	TOUT	Output	Transfer out pulse output	(OPEN)
10	Y4	Output	Pulse output for generating the rotating magnetic field	Y4
11	Y3	Output	Pulse output for generating the rotating magnetic field	Y3
12	Y2	Output	Pulse output for generating the rotating magnetic field	Y2
13	Y1	Output	Pulse output for generating the rotating magnetic field	Y1
14	X4	Output	Pulse output for generating the rotating magnetic field	X4
15	X3	Output	Pulse output for generating the rotating magnetic field	X3
16	X2	Output	Pulse output for generating the rotating magnetic field	X2
17	X1	Output	Pulse output for generating the rotating magnetic field	X1
18	V _{DD}		Power supply connection terminal or open	(OPEN)
19	3μ/2μ	Input	3μ/2μ changeover input	"H" LEVEL
20	60/80	Input	68 series, 80 series changeover input	"H" LEVEL
21	TEST CLOCK	Input	Test clock input	GND
22	V _{SS}		GND	GND
23	Q	Output	Bubble transfer clock signal	Q
24	φB	Output	2-phase master clock signal	φB
25	φA	Output	2-phase master clock signal	φA
26	W DATA	Input	Input of write data in bubble	W DATA
27	RESET	Input	FTG reset signal	RESET
28	CLOCK A	Input	Crystal oscillator connection terminal	CLOCK A
29	CLOCK B	Input	Crystal oscillator connection terminal	CLOCK B
30	RD	Input	Data bus control signal	RD
31	WR	Input	Data bus control signal	WR
32	TXAK	Input	Data bus control signal at DMA transfer	GND
33	CS	Input	Data bus control signal	CS
34	BGEN	Input	Generator pulse control input signal from BMC	BGEN
35	BDET	Input	Detector pulse control input signal from BMC	BDET
36	BREP	Input	Replicator pulse control input signal from BMC	BREP
37	BTIN	Input	SWAP pulse control input signal from BMC	BSWAP
38	BTOUT	Input	Transfer out pulse control input signal from BMC	GND
39	V _{DD}	Input	Power supply connection or open	(OPEN)
40	BSS	Input	BSS input signal from BMC	BSS
41	READY	Output	Data bus enable signal	(OPEN)
42	BUS ENBL	Output	Data bus enable signal	(OPEN)
43	BUS DIR	Output	Data bus direction control signal	(OPEN)
44	V _{DD}		Power supply terminal +5V ±5%	+5V



2-14. BX7058W signal descriptions

Pin No.	Signal name	IN/OUT	Description
1	CTSM	IN	Send enable input signal Modem in use
2	RXDM	IN	Receive data input signal Modem in use
3	RTSM	OUT	Send request output signal Modem in use
4	TXDM	OUT	Send data output signal Modem in use
5	NC		
6	GND		0V supply
7			
8	NC		
11			
12	CD	IN	Carrier detect input signal RS-232C in use
13			
14	DSR	IN	Data set ready input signal RS-232C in use
15	CTS	IN	Send enable input signal RS-232C in use
16	RXD	IN	Receive data input signal RS-232C in use
17	DSR	OUT	Data set ready output signal RS-232C in use
18			
19	CD	OUT	Carrier detect output signal RS-232C in use
20	NC		
21	Vcc		+5V supply
22			
23		OUT	
24		IN	Inverter circuit (not used)
25	RSN	IN	Receive enable signal RS-232C in use
26	MEN	IN	Modem enable signal Modem in use
27	RXD	OUT	Receive data output signal RS-232C in use
28	CTS	OUT	Send enable output signal RS-232C in use
29	NC		
30			
31	TXD	IN	Send data input signal Modem in use
32	RTS	IN	Send request input signal Modem in use





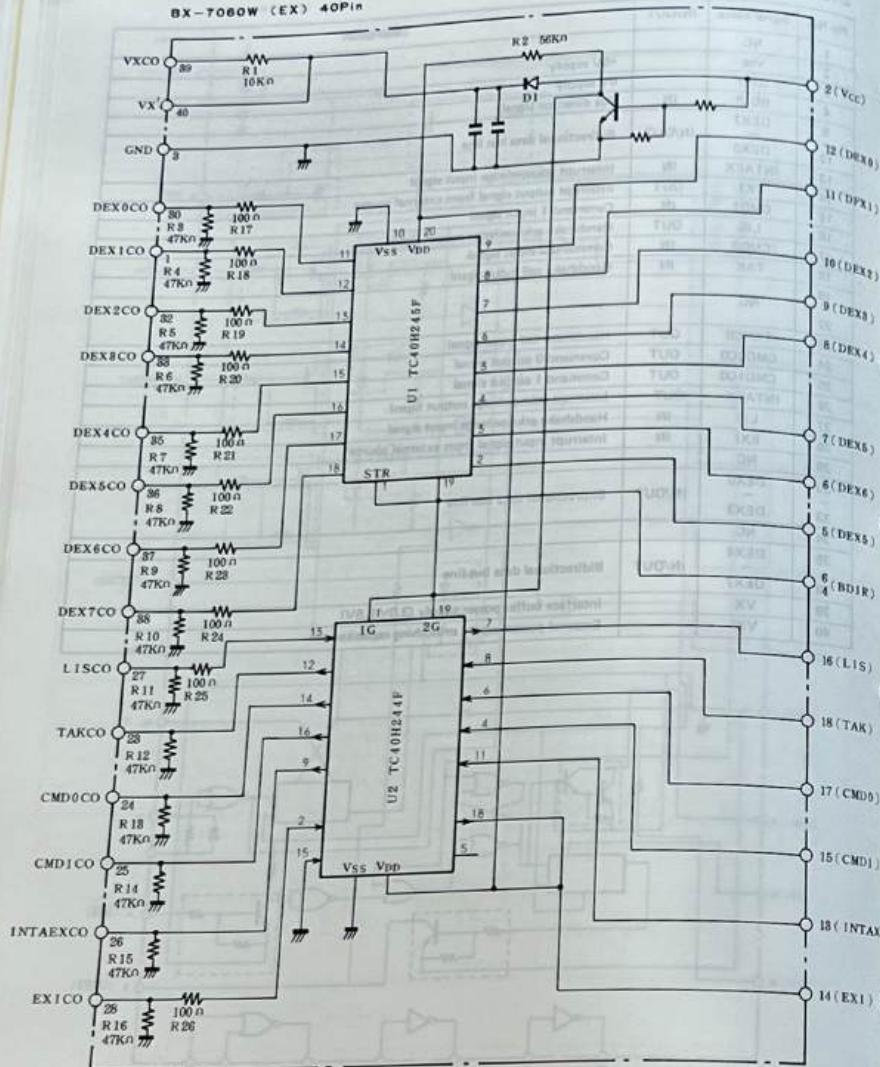
2 - 33

2-16. BX7060W signal descriptions

Pin No.	Signal name	IN/OUT	Description
1	NC		
2	Vcc		
3	GND		+5V supply
4	BDIR	IN	0V supply
5	DEX7		Bus direction signal
~	DEX0	IN/OUT	
12			Bidirectional data bus line
13	INTAEX	IN	
14	EX1	OUT	Interrupt acknowledge input signal
15	CMD1	IN	Interrupt output signal from external source
16	LIS	OUT	Command 1 input signal
17	CMD0	IN	Handshake acknowledge output signal
18	TAK	IN	Command 0 input signal
19			Handshake call input signal
~	NC		
22			
23	TAK0	OUT	
24	CMD0C0	OUT	Handshake call input signal
25	CMD1C0	OUT	Command 0 output signal
26	INTAEX	OUT	Command 1 output signal
27	LIS	IN	Interrupt acknowledge output signal
28	EXI	IN	Handshake acknowledge input signal
29	NC		Interrupt input signal from external source
30	DEX0		
~	DEX3	IN/OUT	
33			Bidirectional data bus line
34	NC		
35	DEX4		
~	DEX7	IN/OUT	
38			Bidirectional data bus line
39	VX		Interface buffer power supply (3.0V-5.5V)
40	VX'		External power supply smoothing capacitor pin

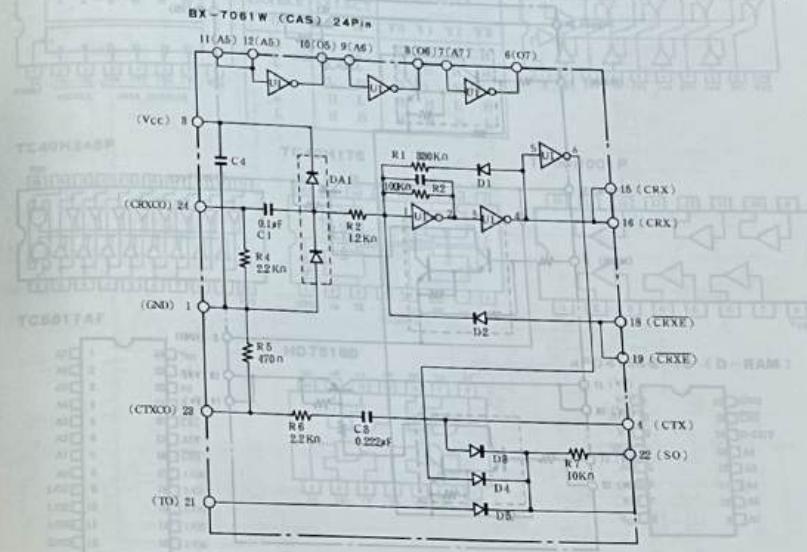
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BX-TOBOW (EX) 40Pin

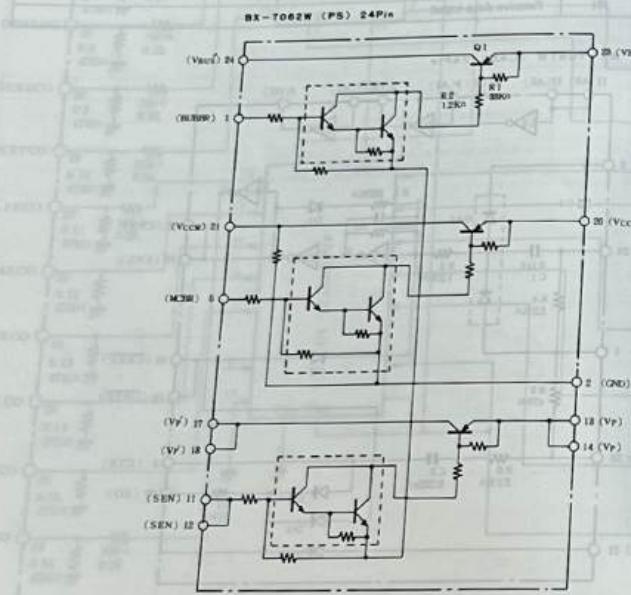


2-17. BX7061W Signal descriptions

Pin No.	Signal name	IN/OUT	Function	Description
1	GND		0V supply	
2	NC			
3	V _{cc}		+5V supply	
4	CTX	IN	Send data input	
5	NC			
6		OUT		
7		IN	Inverter circuit (not used)	
8		OUT		
9		IN	Inverter circuit (not used)	
10		OUT		
11		IN		
12		IN	Inverter circuit (not used)	
13	NC			
14				
15	CRX	OUT	Receive data output	
16				
17	NC			
18	CRXE	IN	CRX level control signal	
19	NC			
20				
21	TO	IN	Audio input	
22	SO	OUT	Audio output	
23	CTXCO	OUT	Send data output	
24	CRXCO	IN	Receive data input	

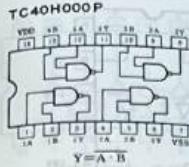


2-18. BX7062W signal descriptions			
Pin No.	Signal name	IN/OUT	Description
1	BUBBR	IN	Bubble memory power initiate signal
2	GND		
3	NC		
4			
5	MCBR	IN	M-CPU power initiate signal
6			
~			
10	NC		
11			
12	SEN	IN	RS-232C transmission power initiate signal
13			
14	VP	IN	VP' supply
15			
16	NC		
17			
18	VP	OUT	RS-232C transmission power
19	NC		
20	Vcc	In	VCCM power
21	VccM	OUT	M-CPU power
22	NC		
23	VB	IN	VBUB power
24	Vbus	OUT	Bubble memory power

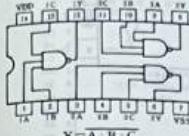


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2.19. PIN CONFIGURATION OF IC



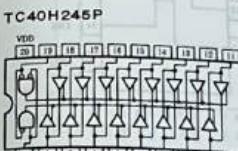
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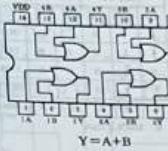
- 2 - 18H1308

FUNCTION TABLE

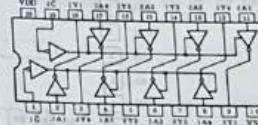
INPUTS		OUTPUTS				
ENABLE	SELECT		Y0	Y1	Y2	Y3
G	B A		H	H	H	H
H	X X		H	H	H	H
L	L L		L	H	H	H
L	L H		H	L	H	H
L	H L		H	H	L	H
L	H H		H	H	H	L



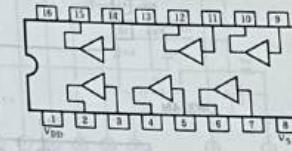
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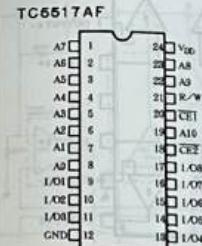
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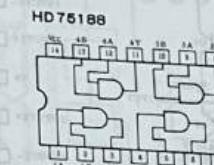
TC50H001P



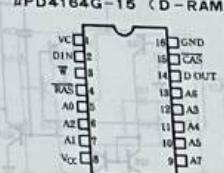
μPD4164G-15 (D-RAM)



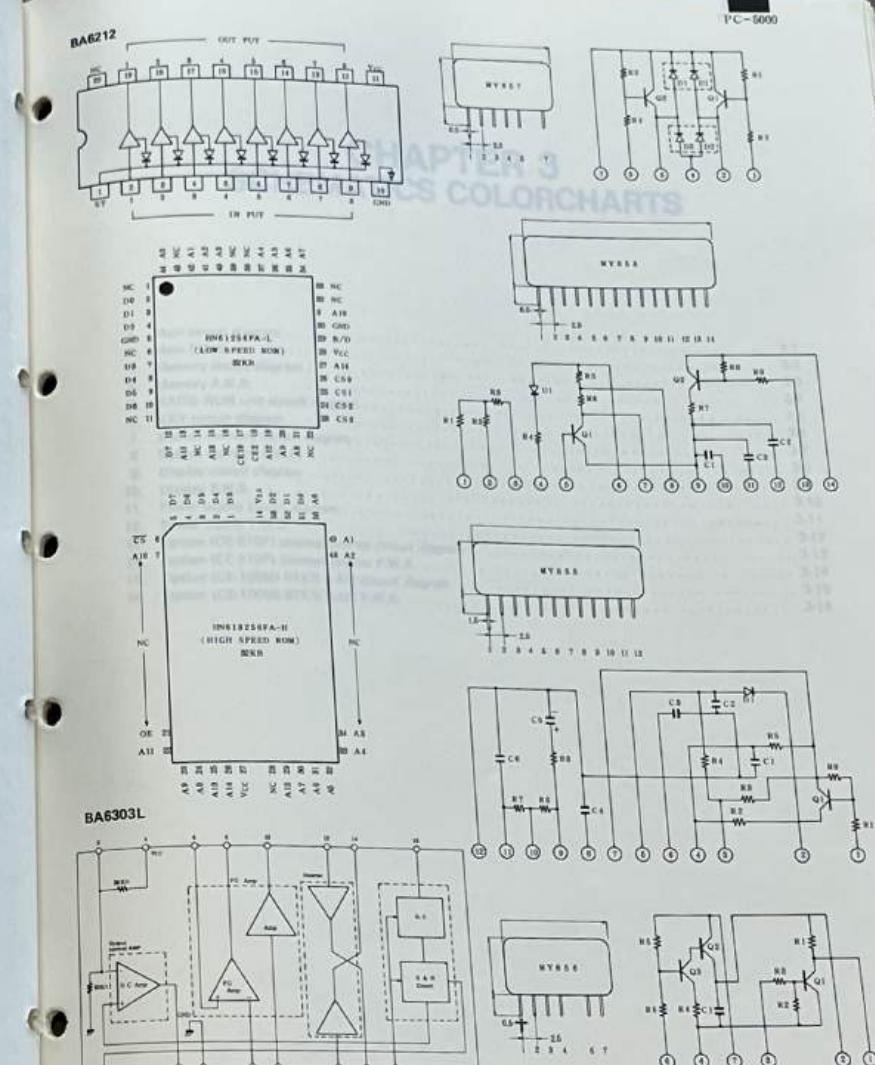
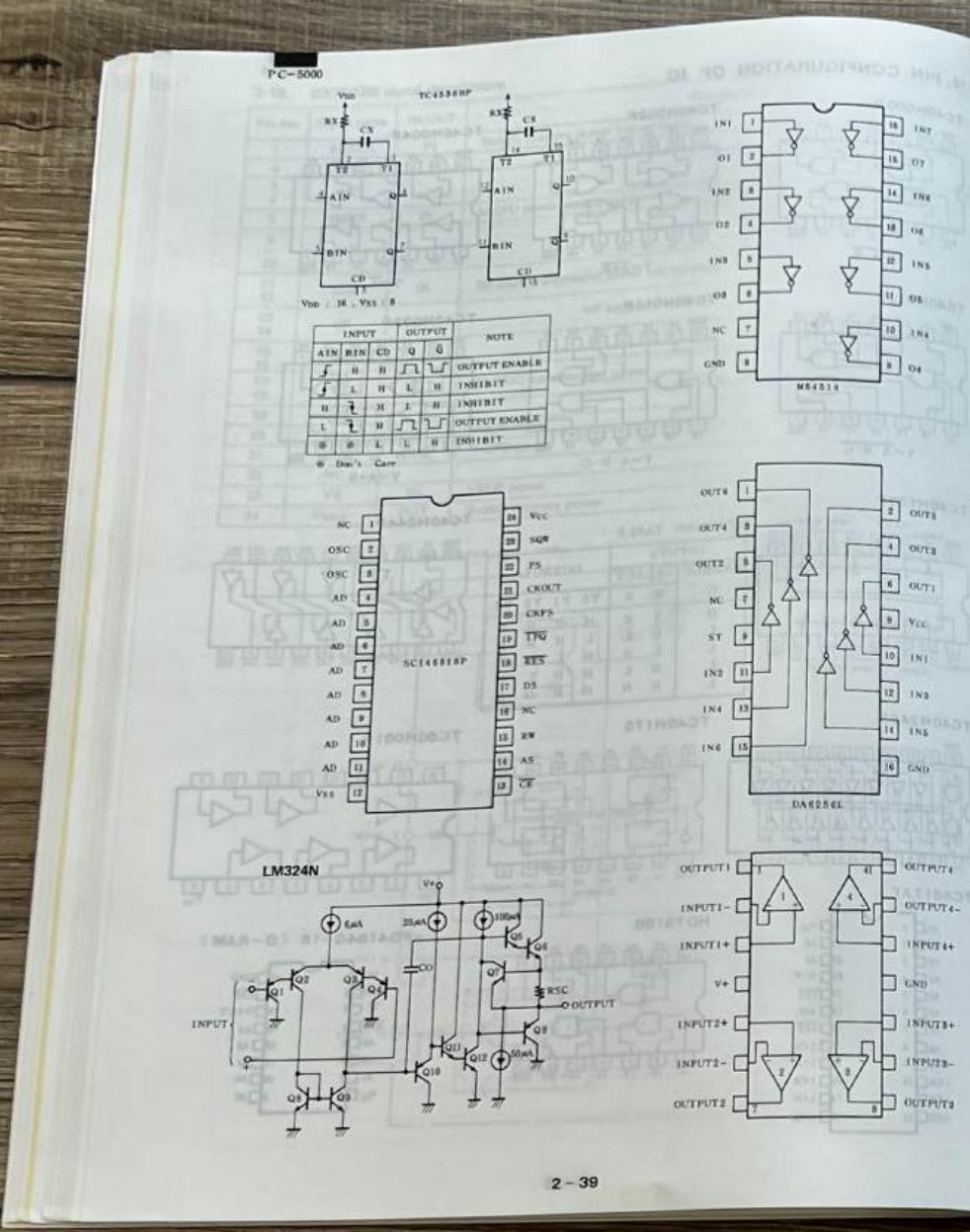
24 Yes



HD751

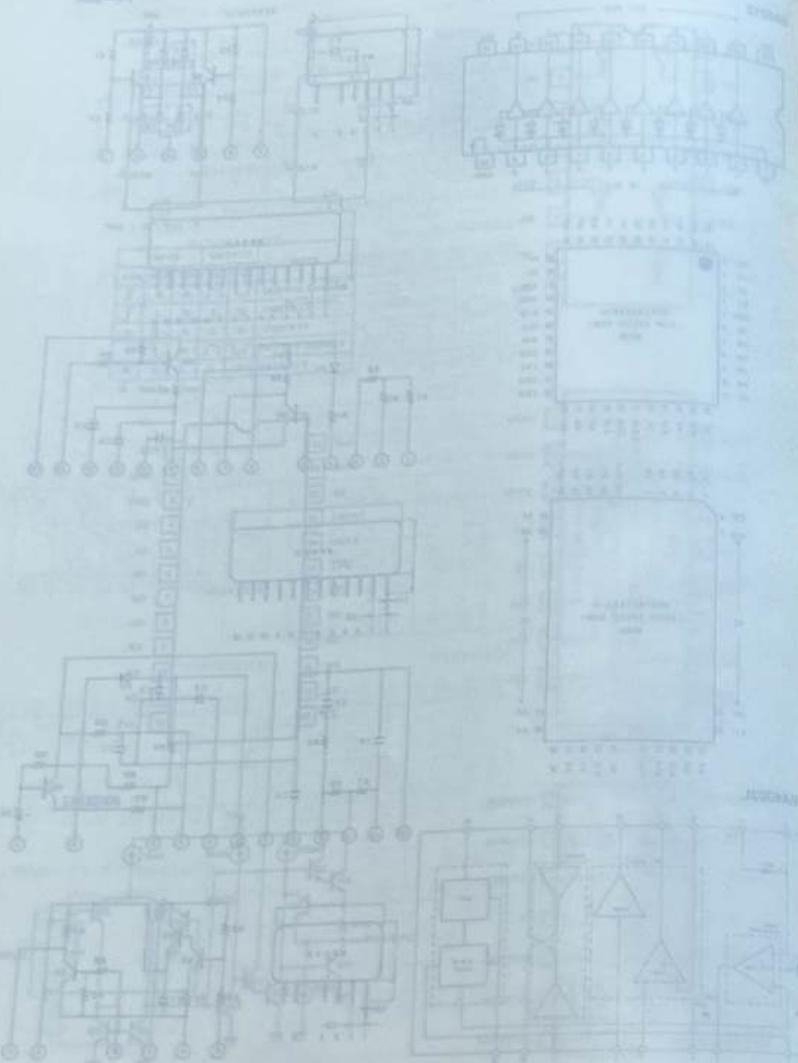


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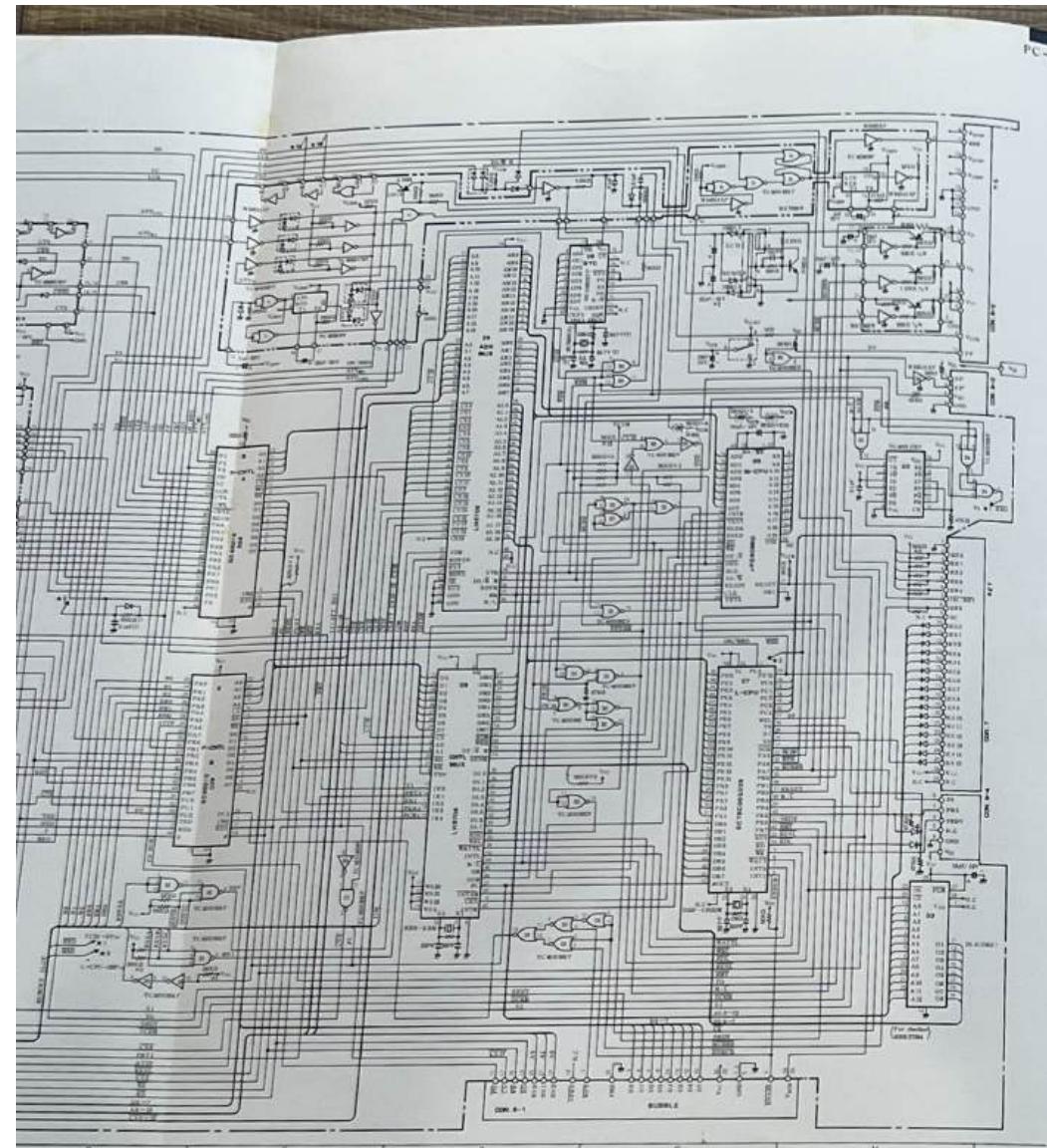
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CHAPTER 3
SCHEMATIC CIRCUITS



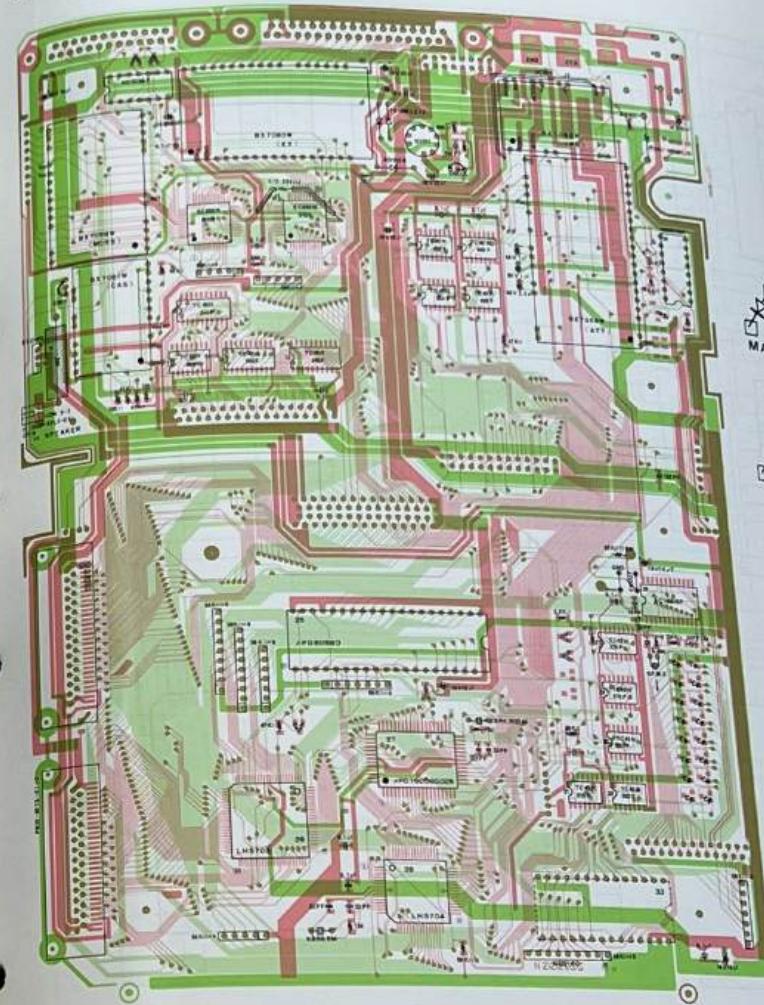


3-1

PC-5000

2. メイン基板図
2. MAIN P.W.B.

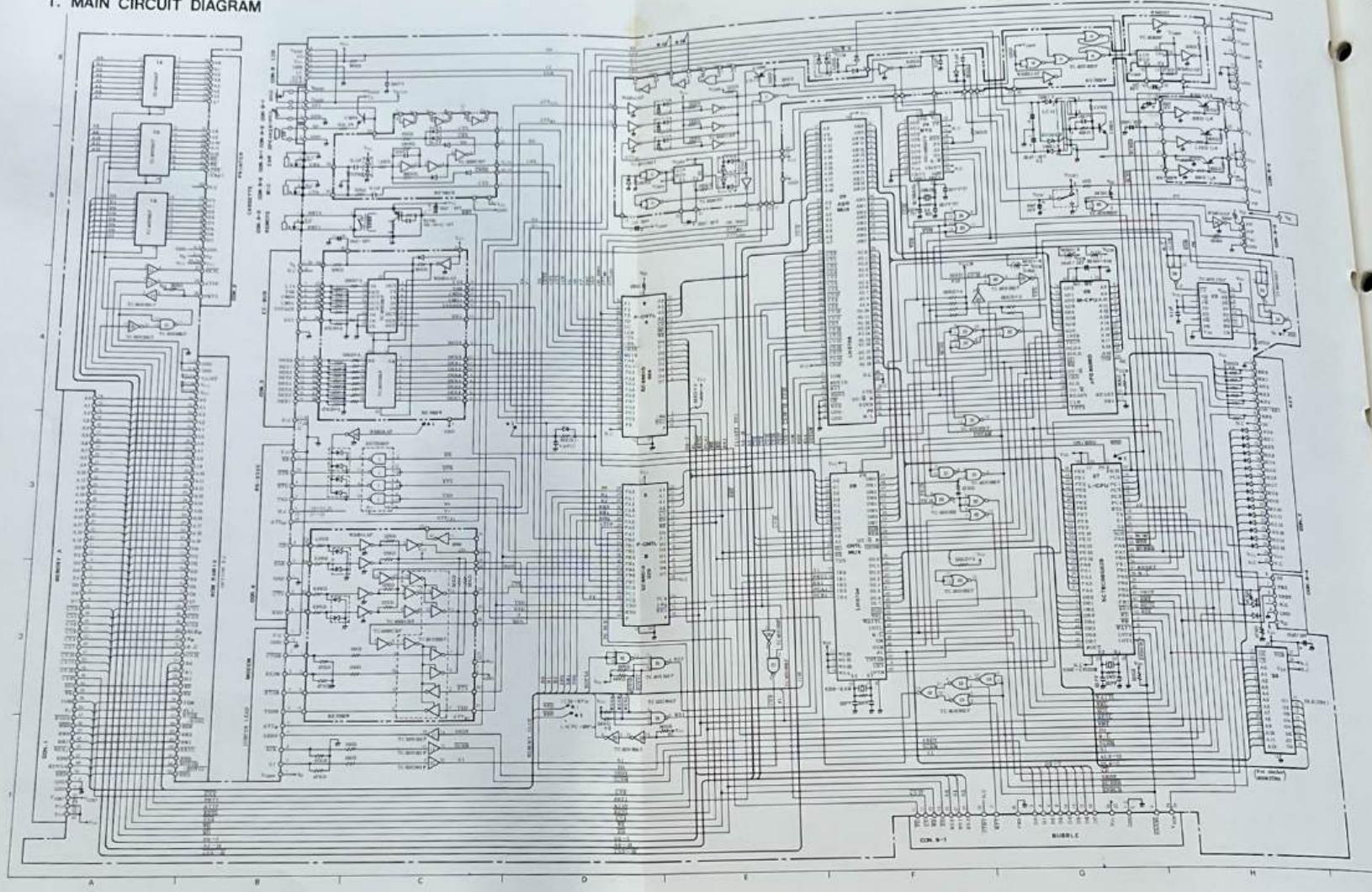
PARTS SIDE



3-2



1. メイン回路図
1. MAIN CIRCUIT DIAGRAM

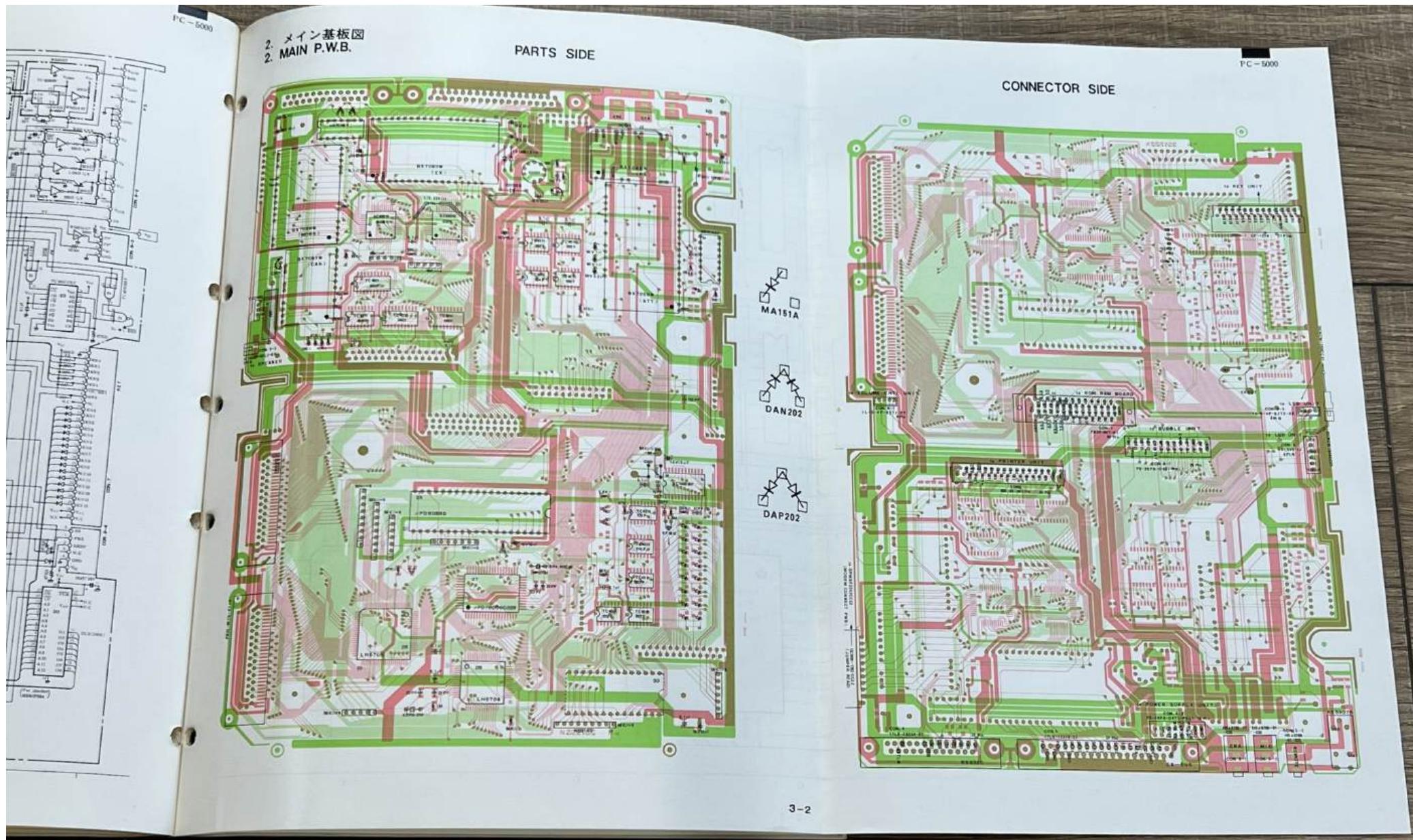


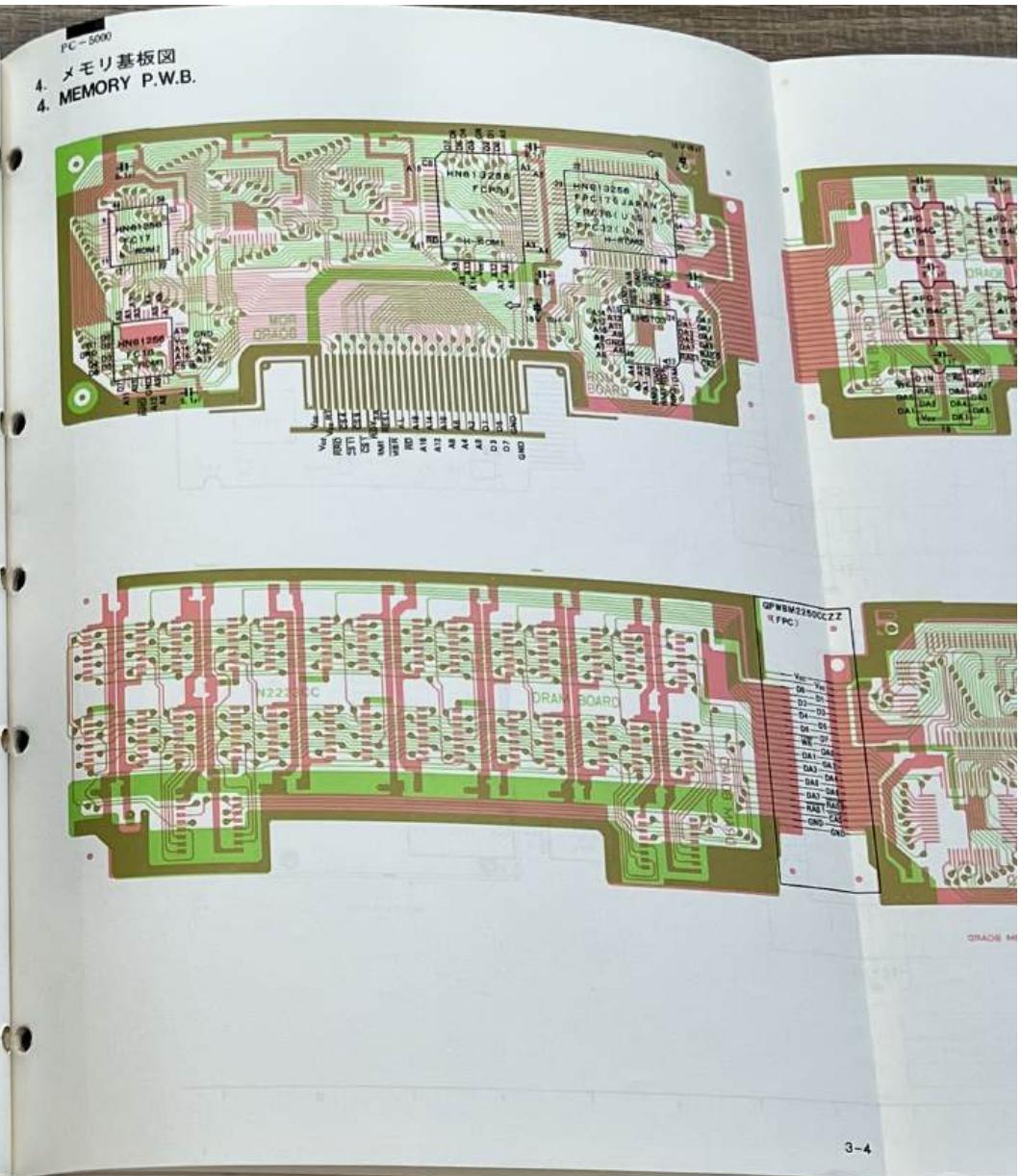
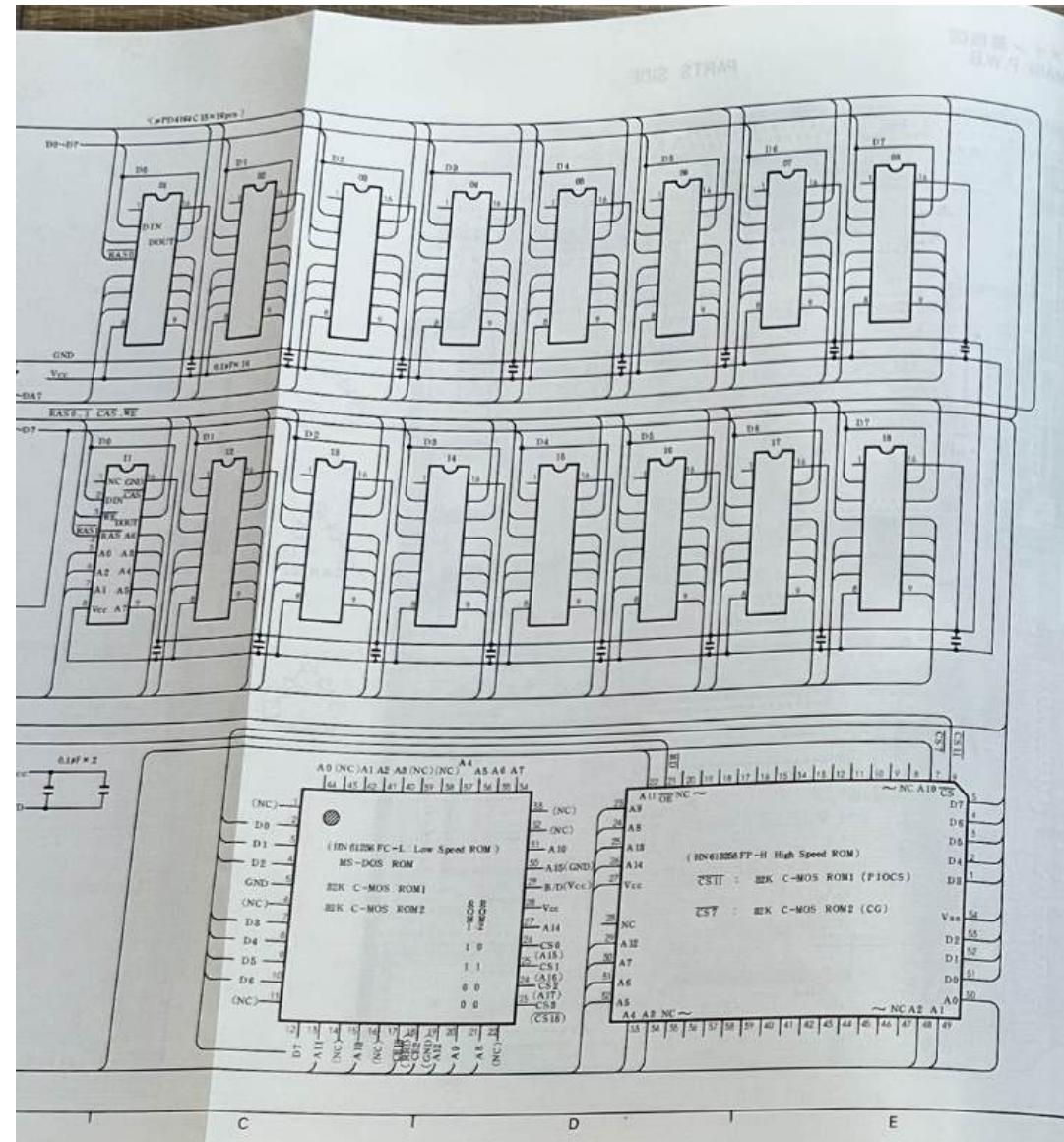
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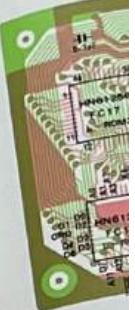
PC-500

2. メイン基板
2. MAIN P.W.



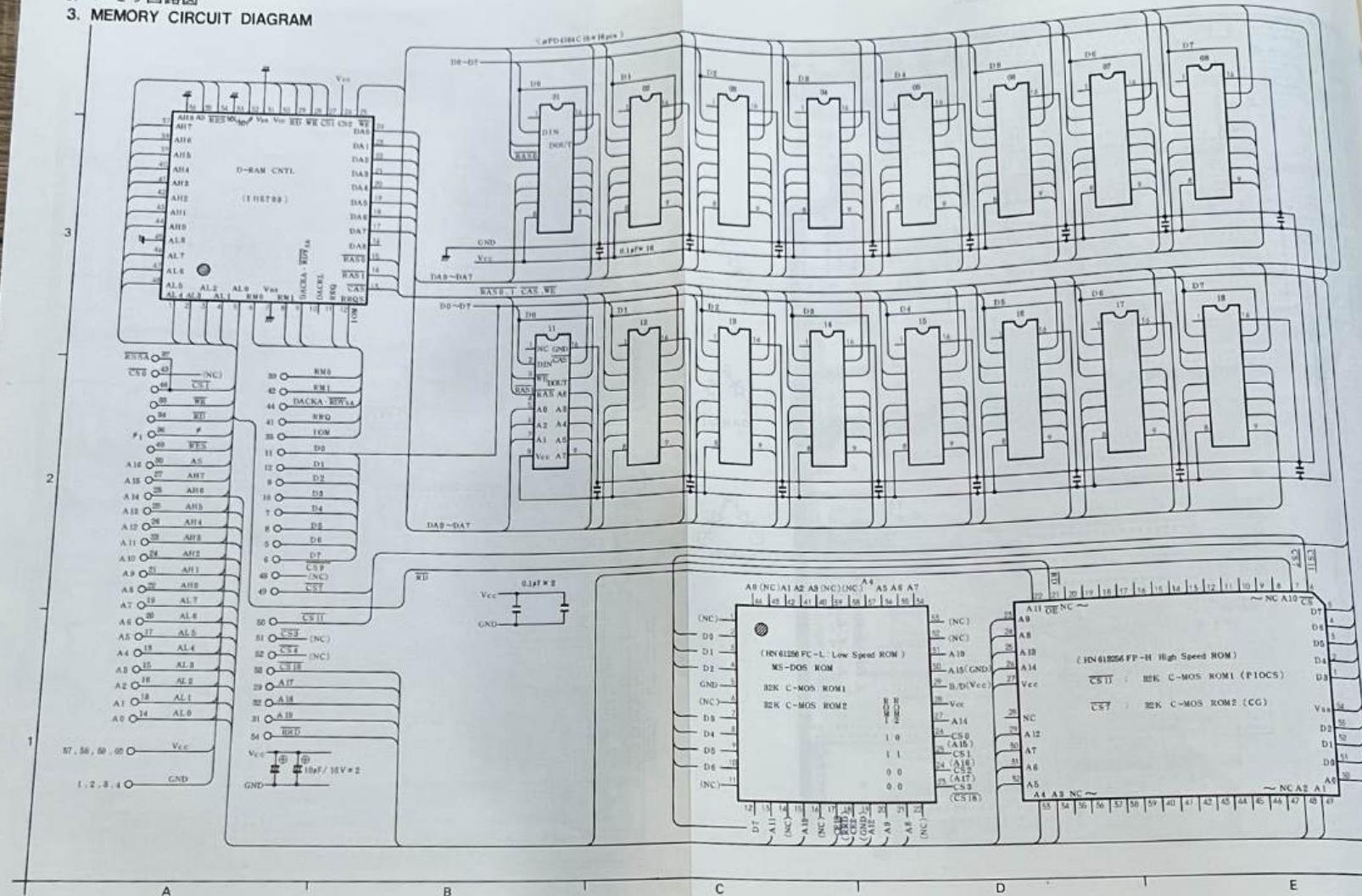




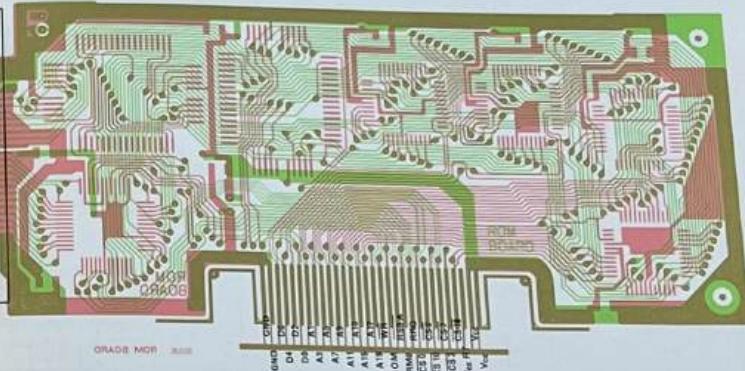
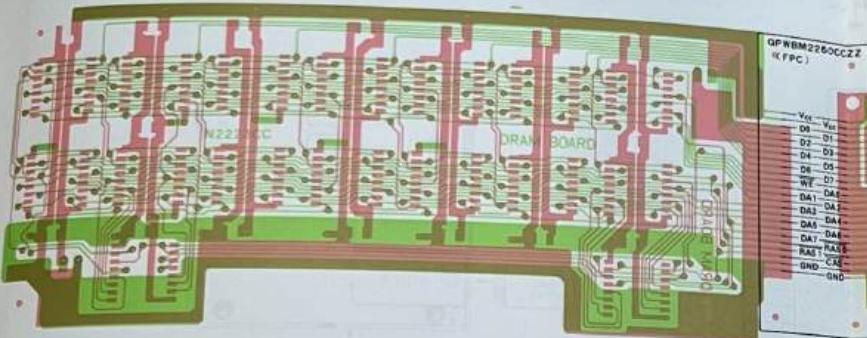
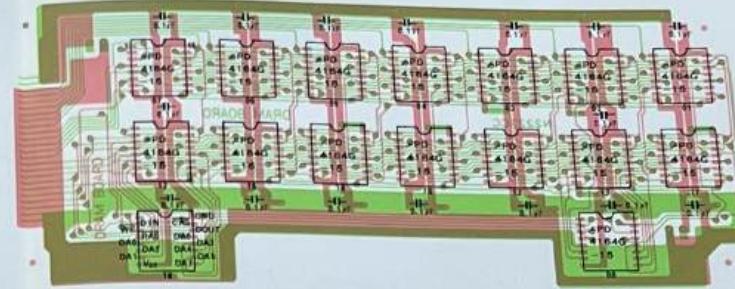
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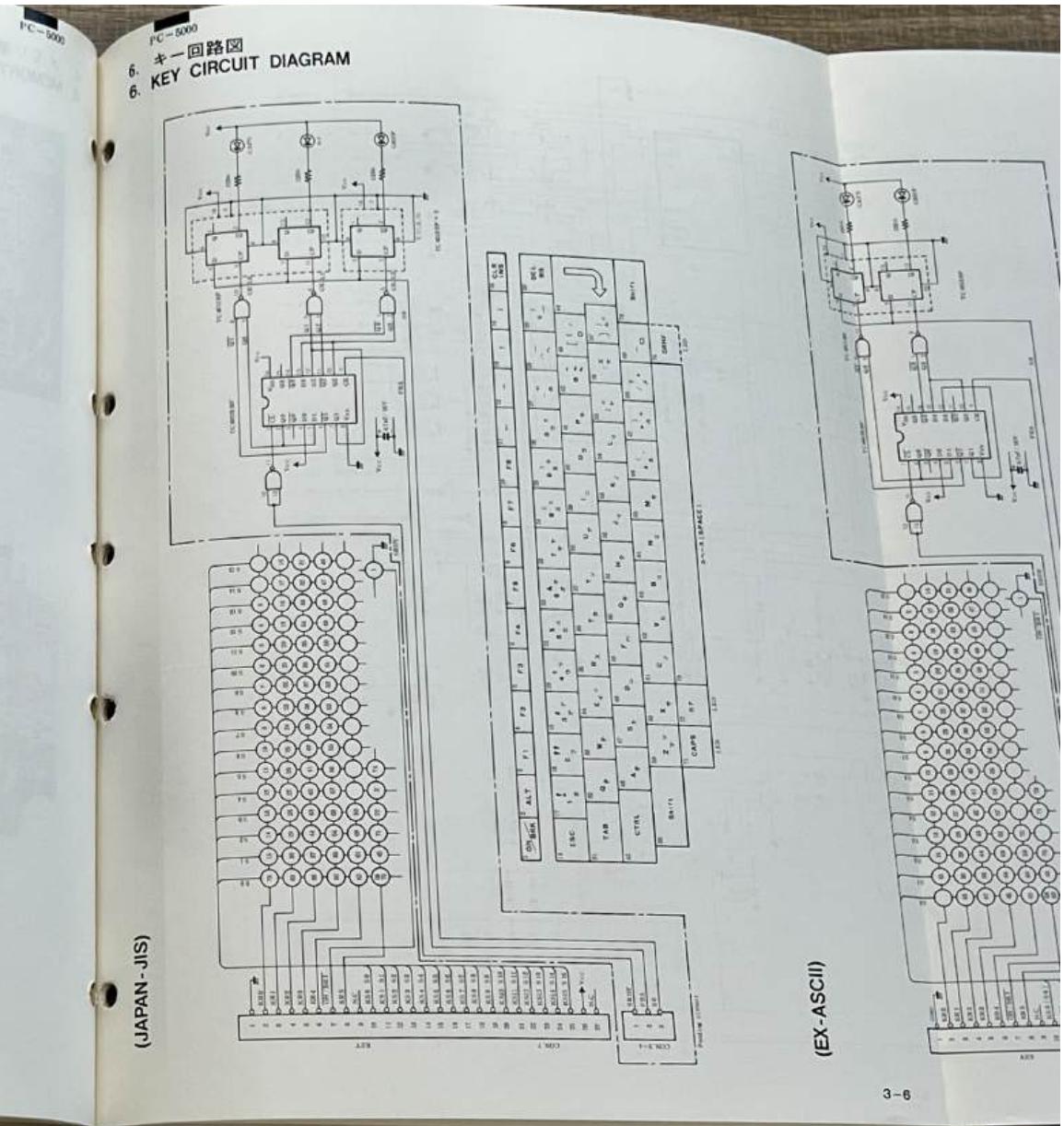
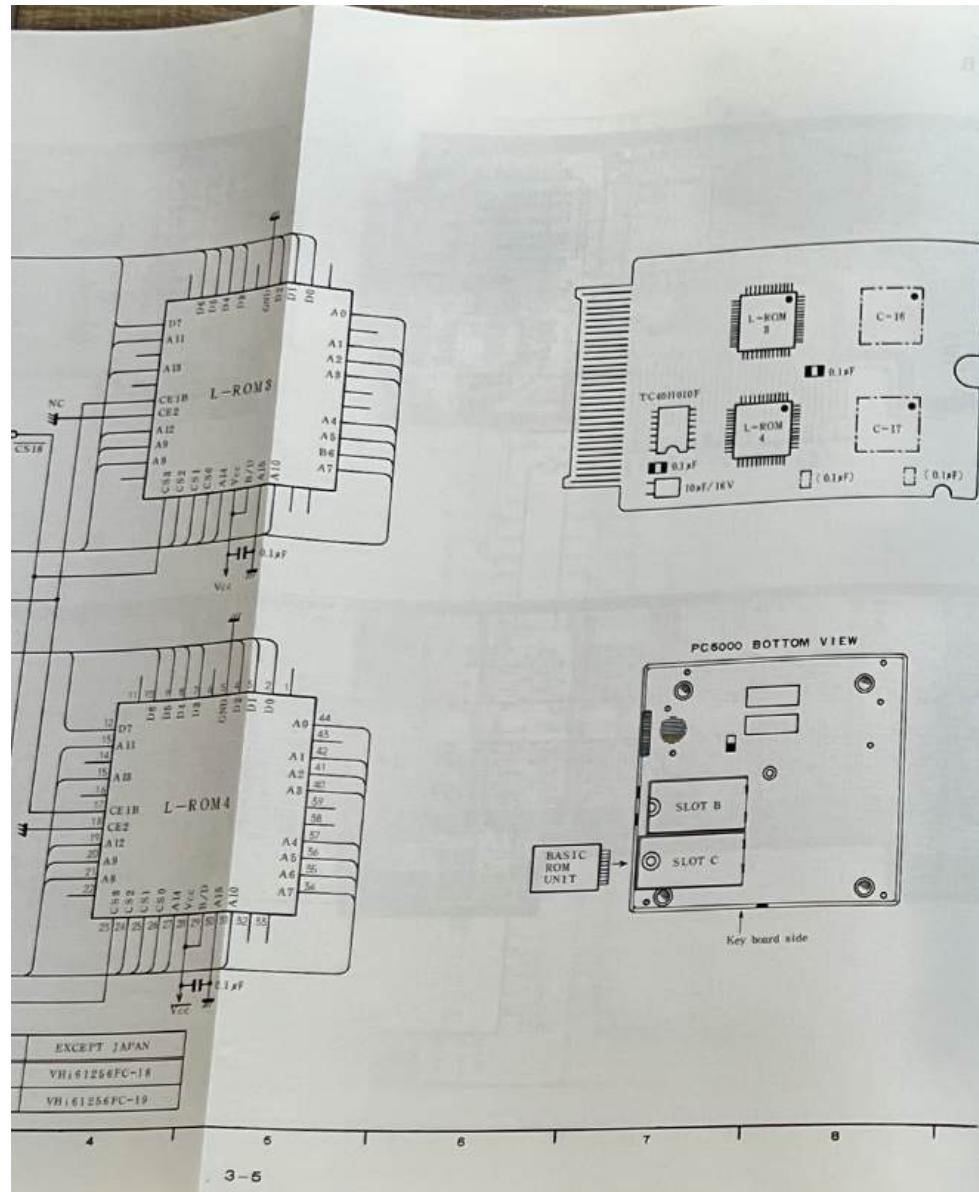
PC-5000

3. メモリ回路図
3. MEMORY CIRCUIT DIAGRAM

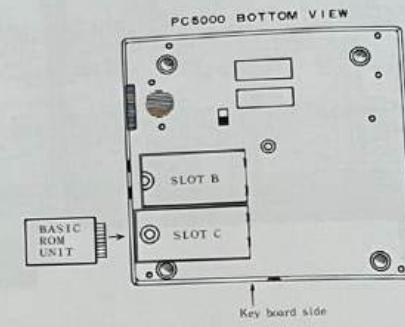
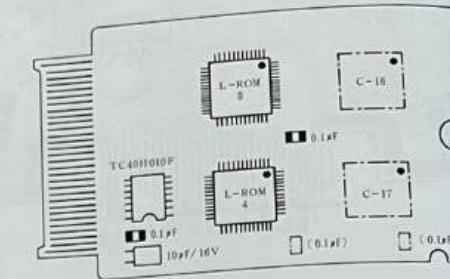
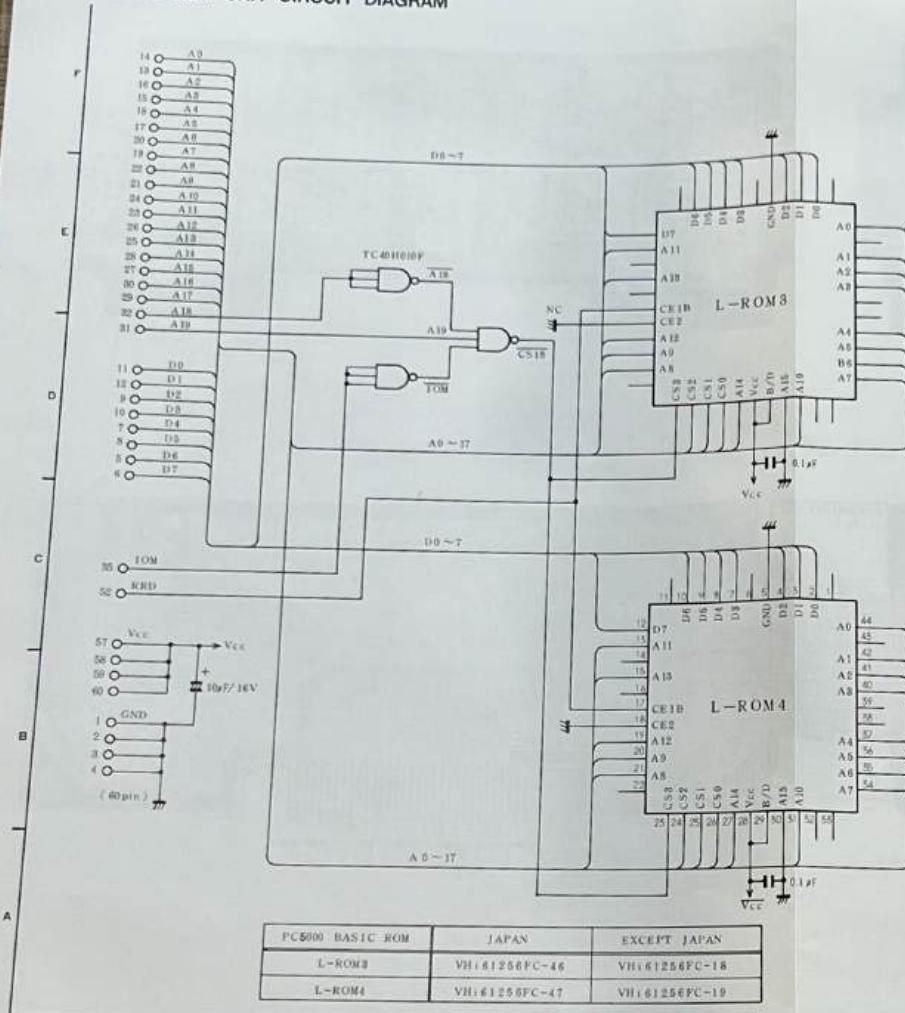


PC-8000
4. メモリ基板図
MEMORY P.W.B.



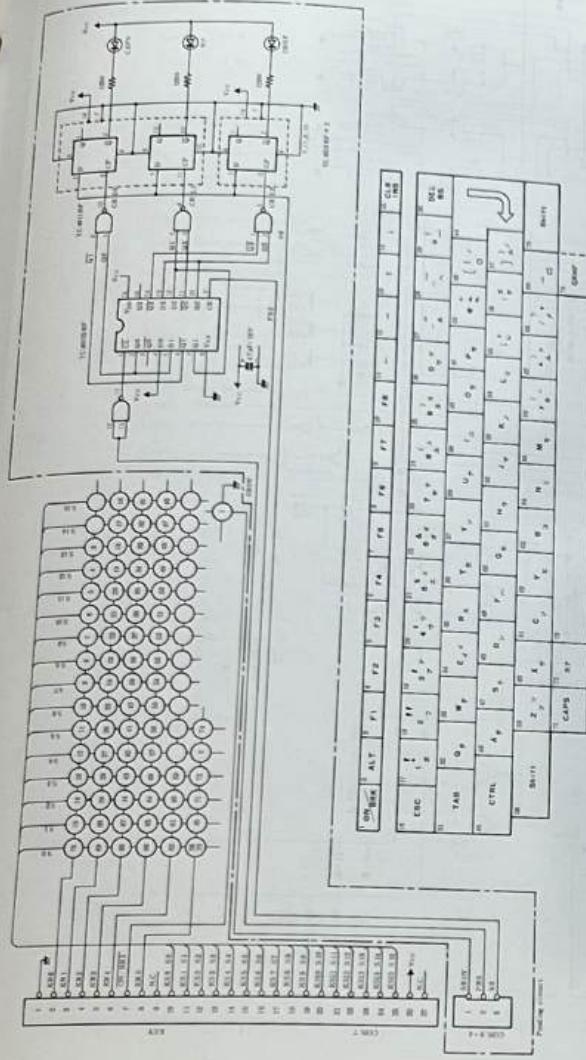


5. BASIC ROM ユニット回路図
5. BASIC ROM UNIT CIRCUIT DIAGRAM

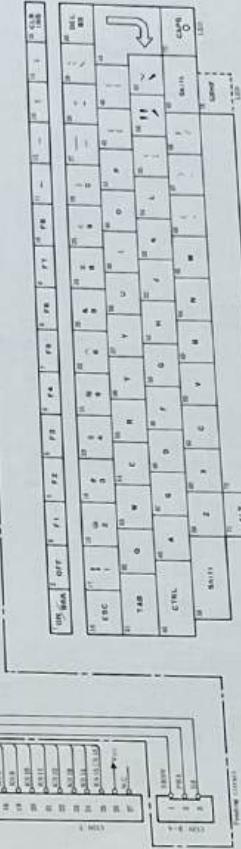
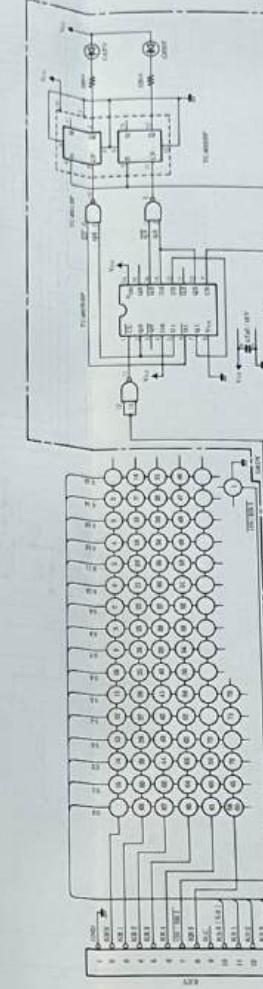


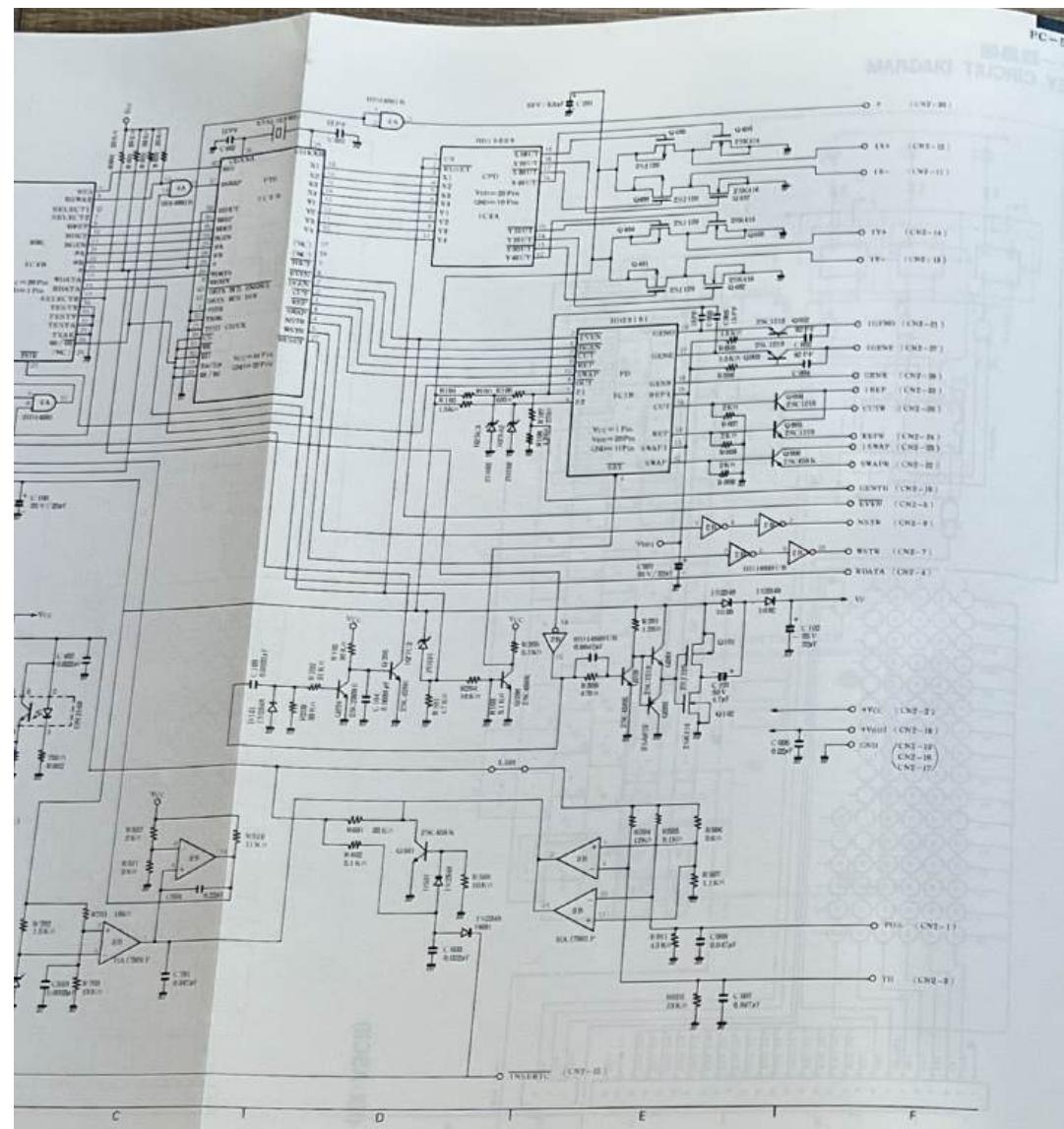
PC-5000
PC-5000
6. キーワード
6. KEY CIRCUIT

第一回路図
KEY CIRCUIT DIAGRAM

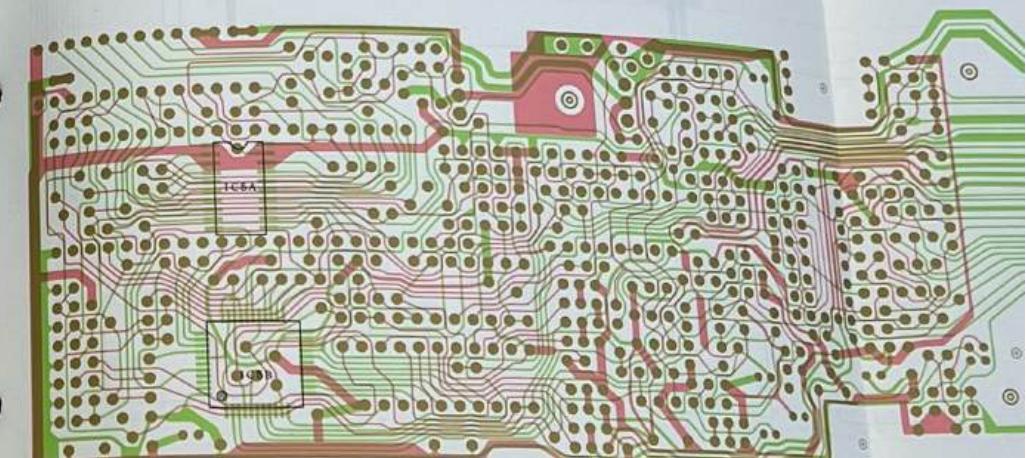
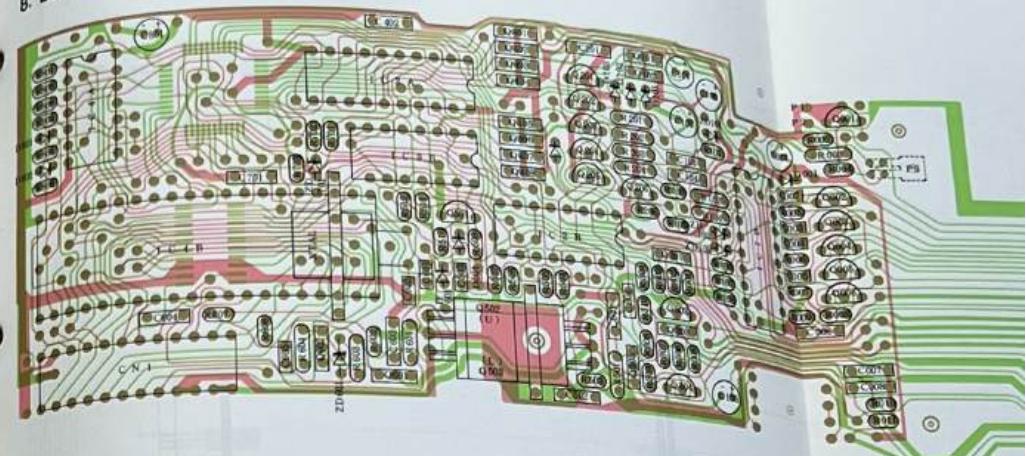


(EX-ASC))



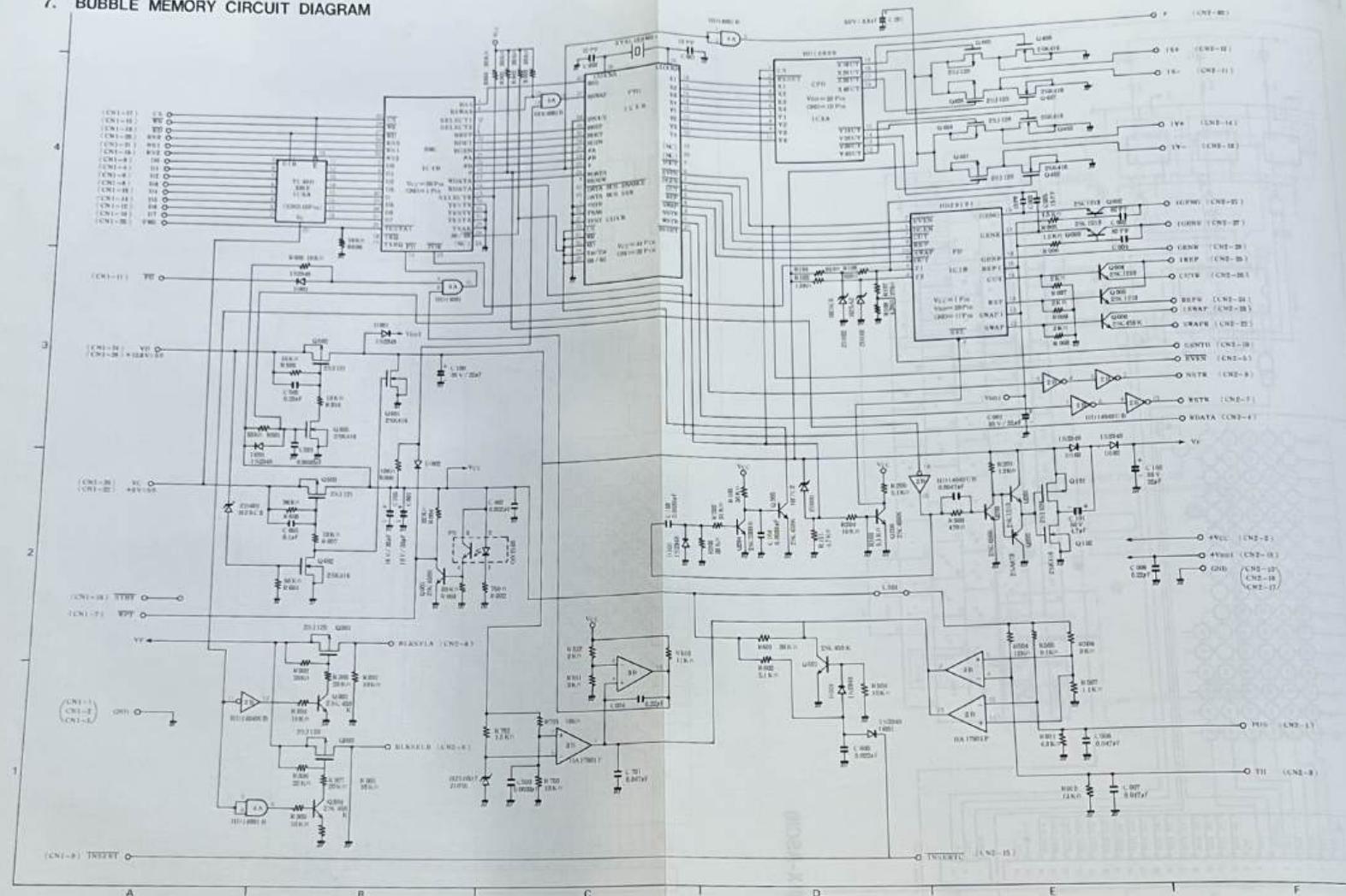


PC-5000
8. バブルメモリ基板図
8. BUBBLE MEMORY P.W.B

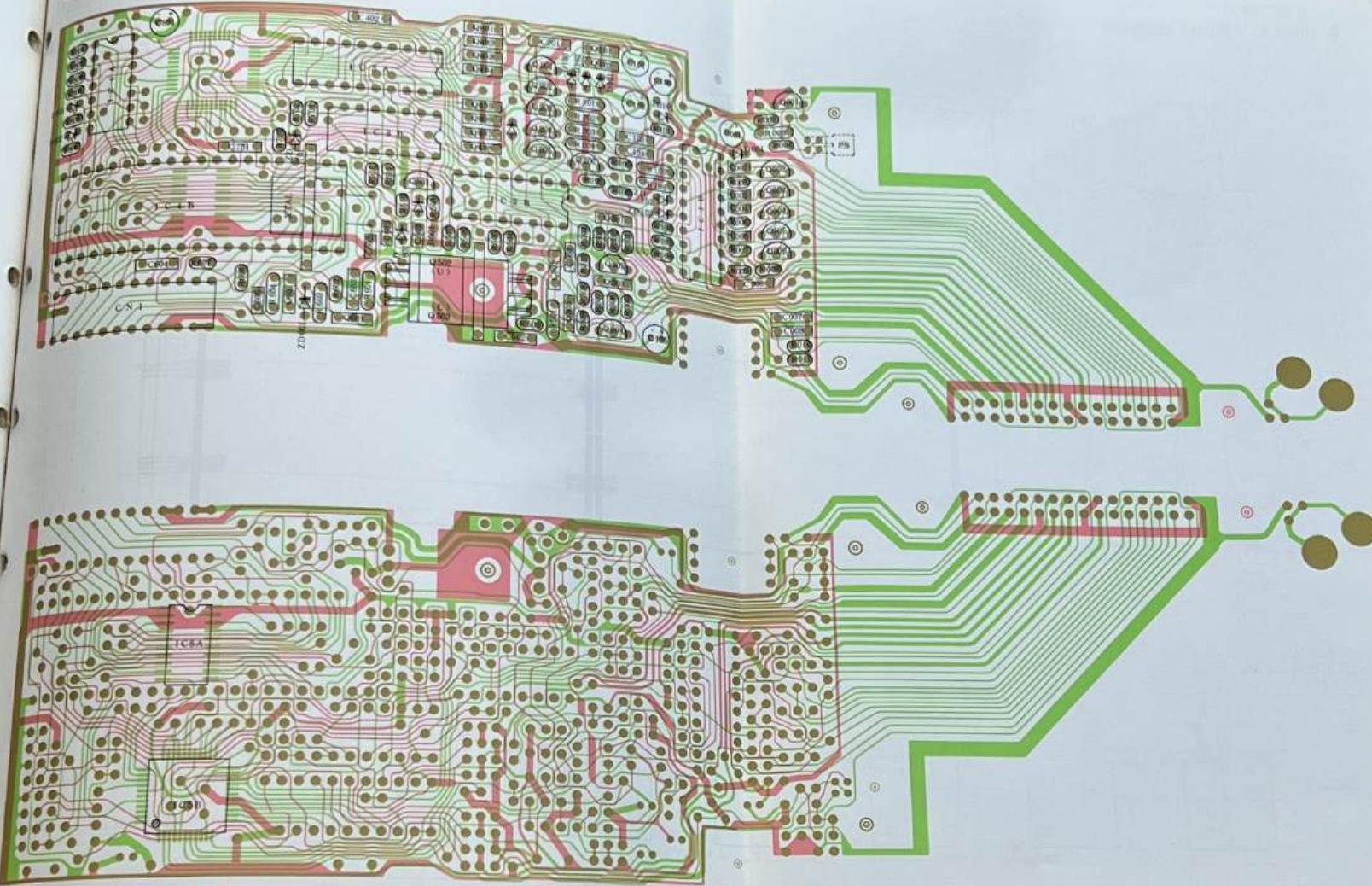


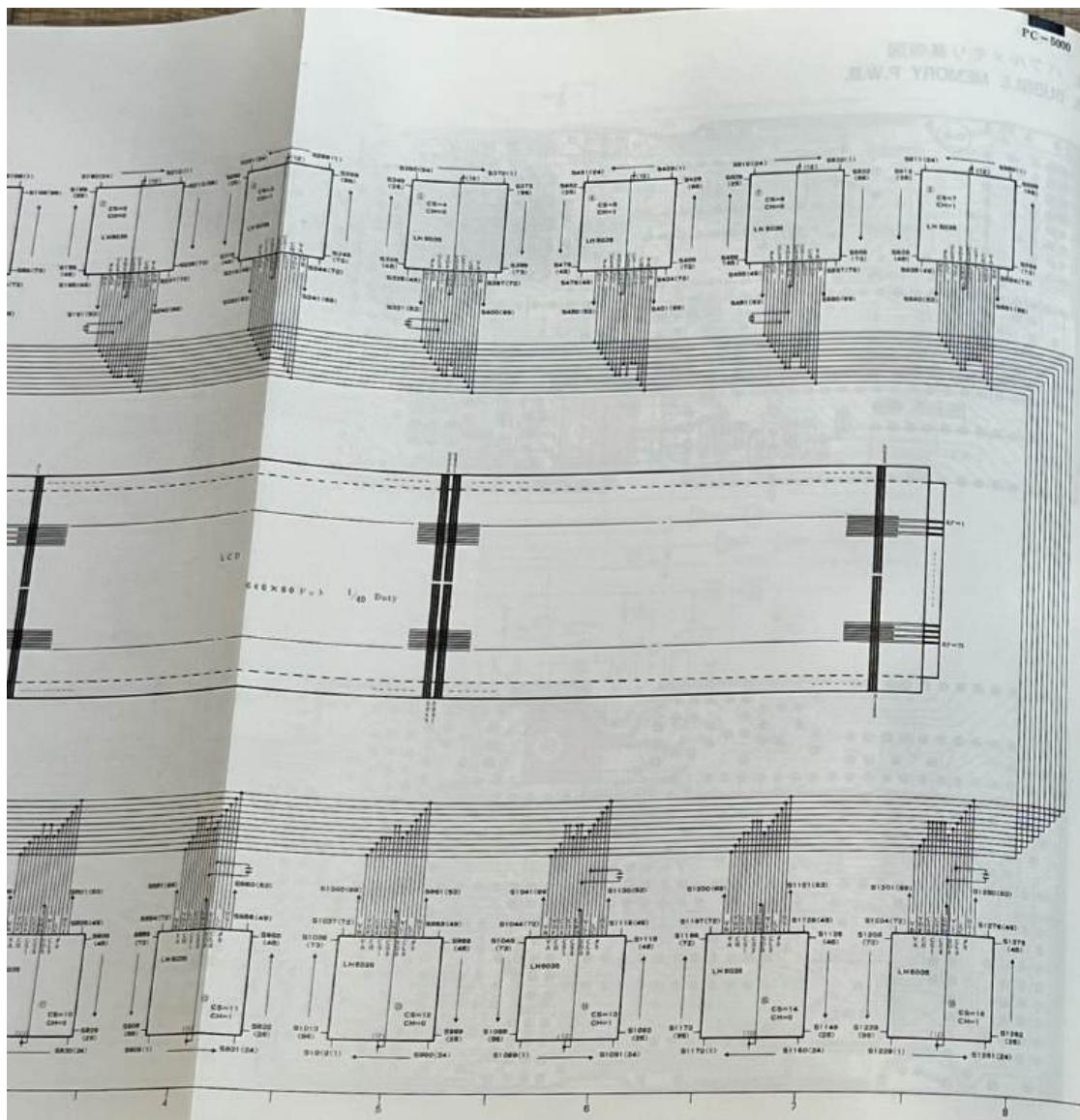
7. バブルメモリ回路図

7. BUBBLE MEMORY CIRCUIT DIAGRAM



PC-5000
B. バブルメモリ基板図
B. BUBBLE MEMORY P.W.B.

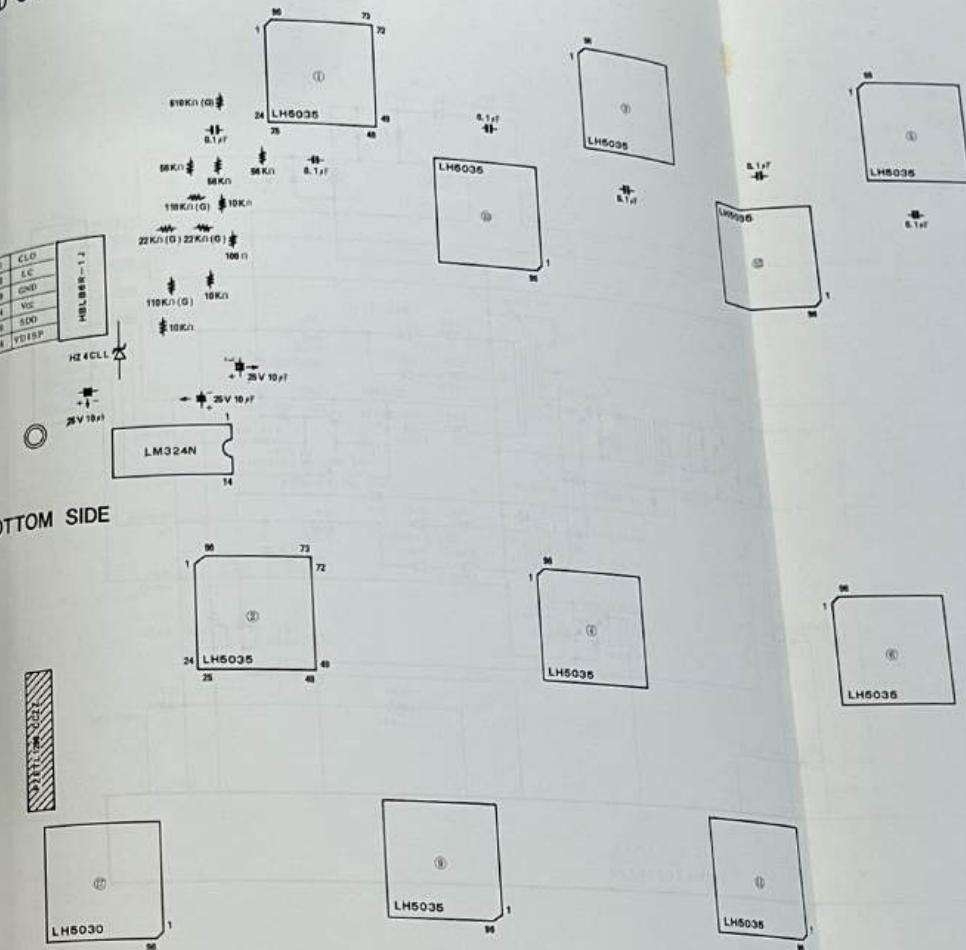




3-9

10. DISPLAY P.W.B.
LCD SIDE
表示基板図
PC-5000

LCD SID



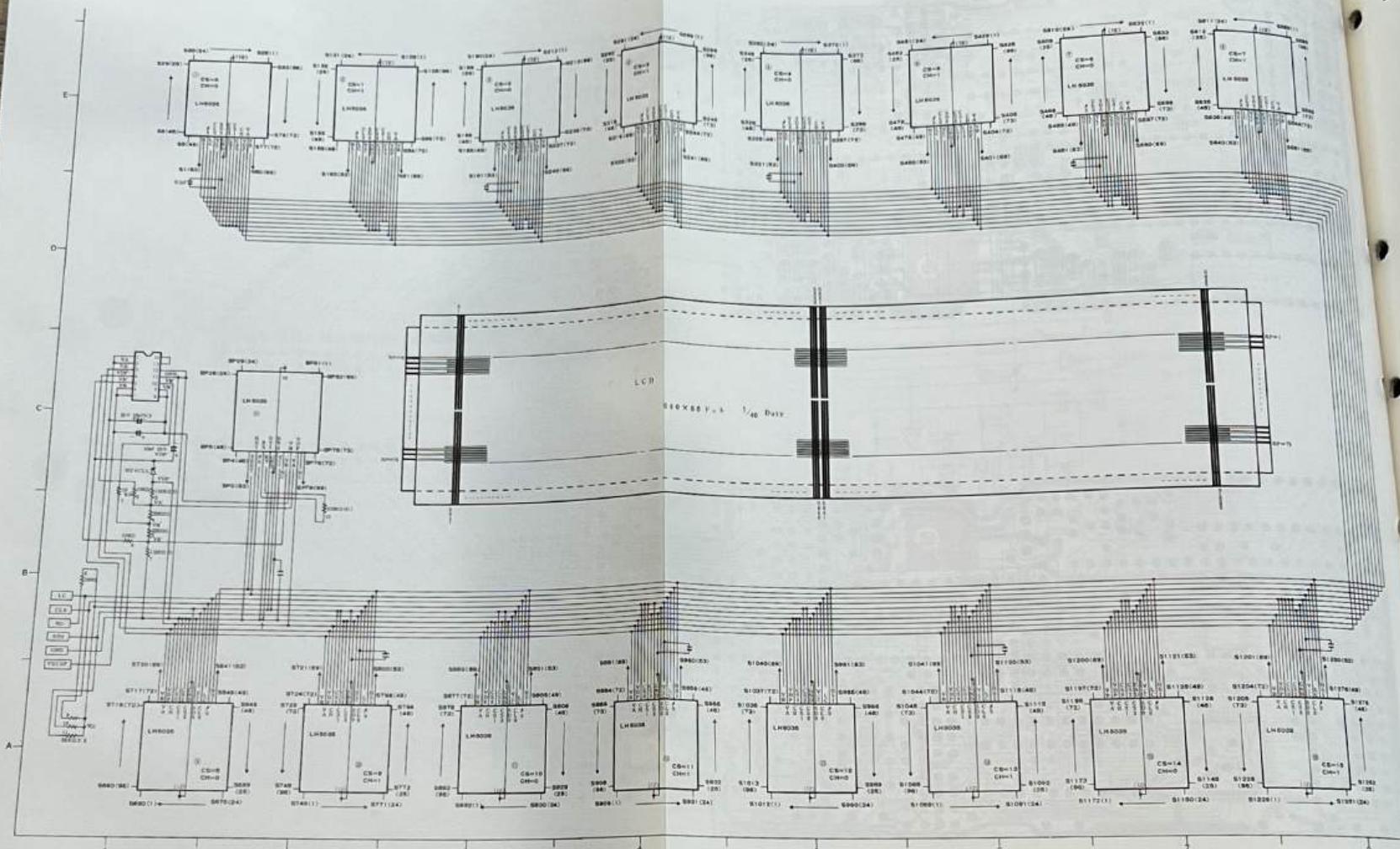
3-10

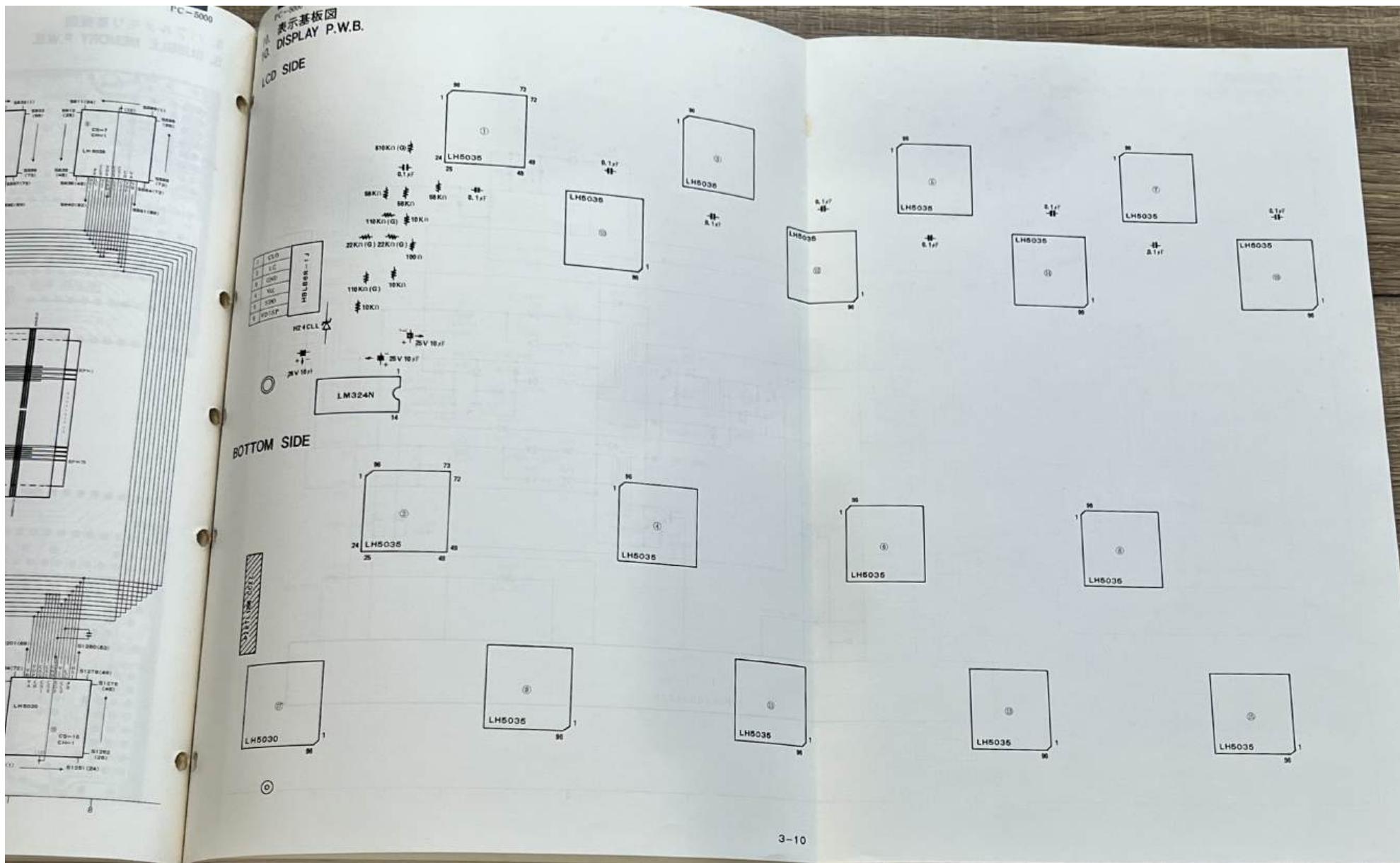
PC-5000
LCD SIDE
10. DISPLAY P.W.B

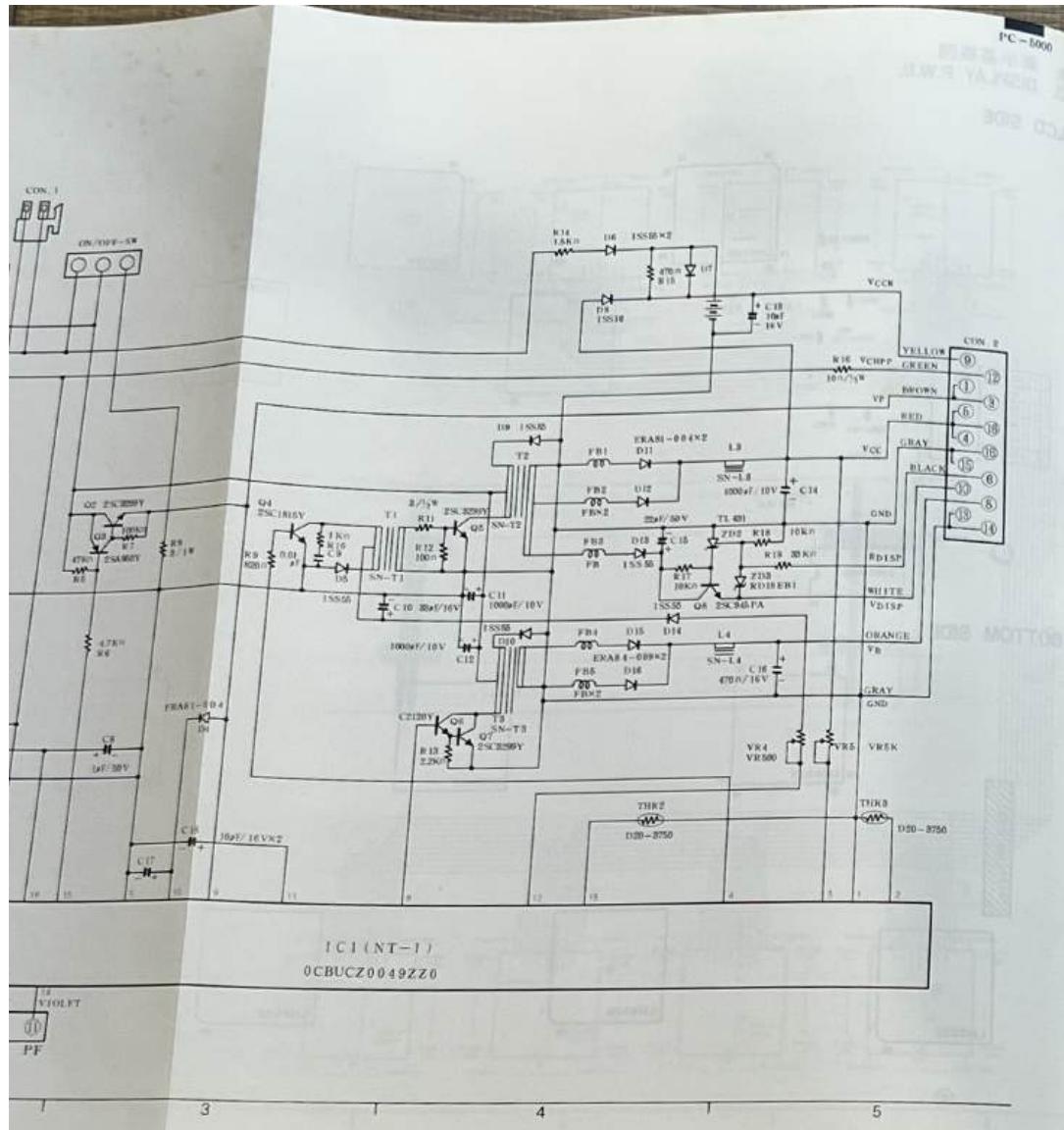
1	CLO
2	LC
3	GND
4	WC
5	SDO
6	VDISP

BOTTOM S

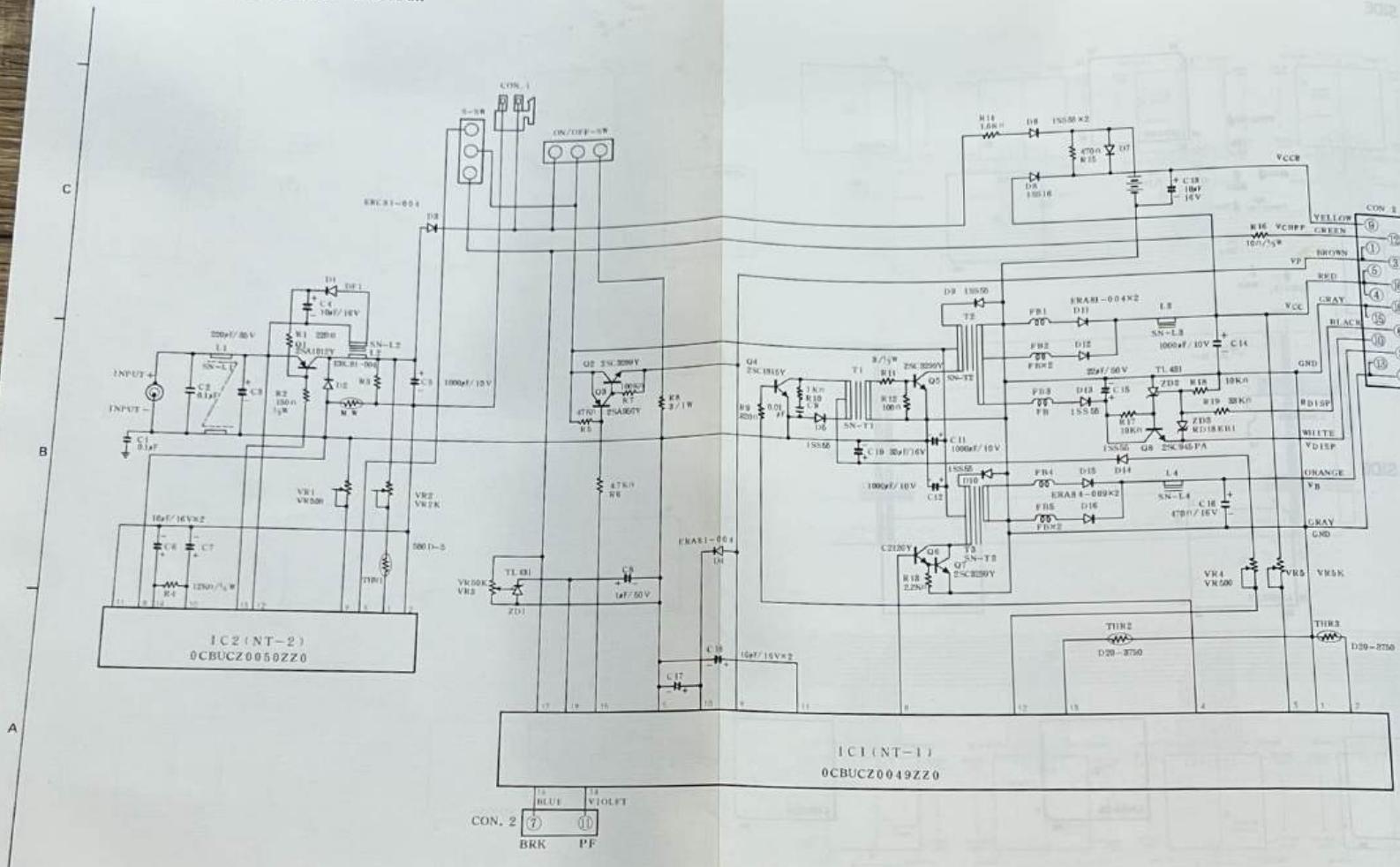
9. 表示回路図
9. DISPLAY CIRCUIT DIAGRAM



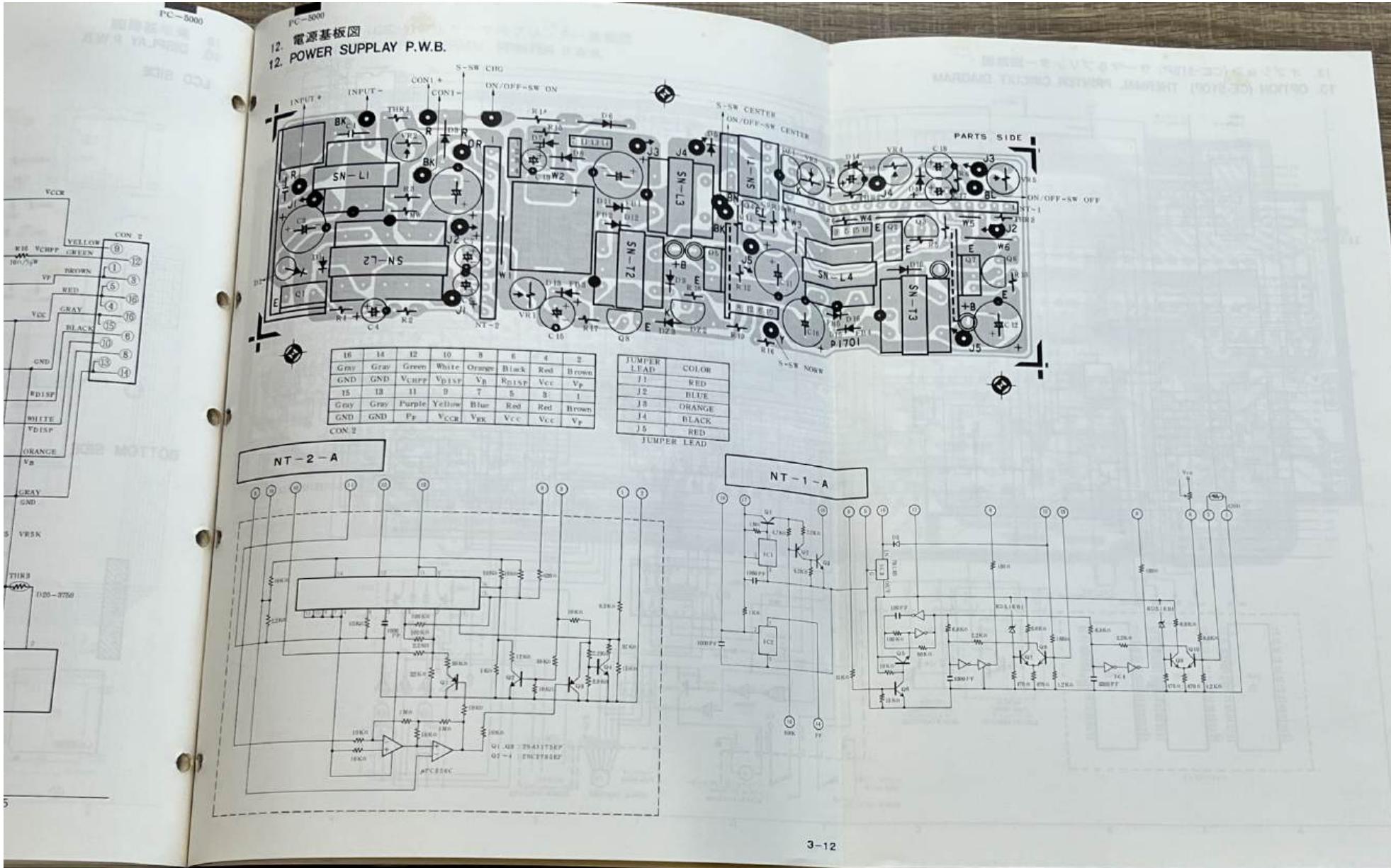


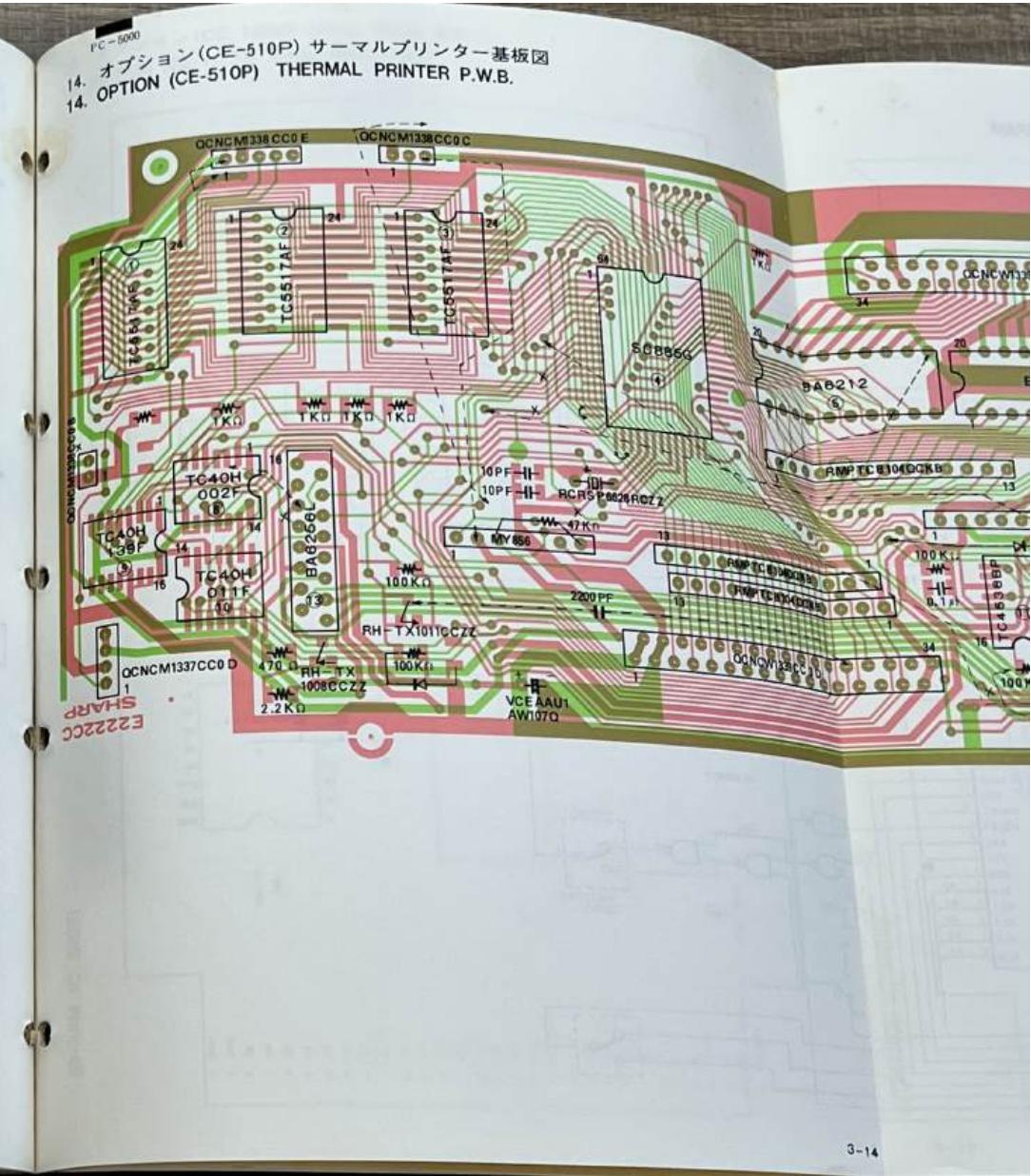
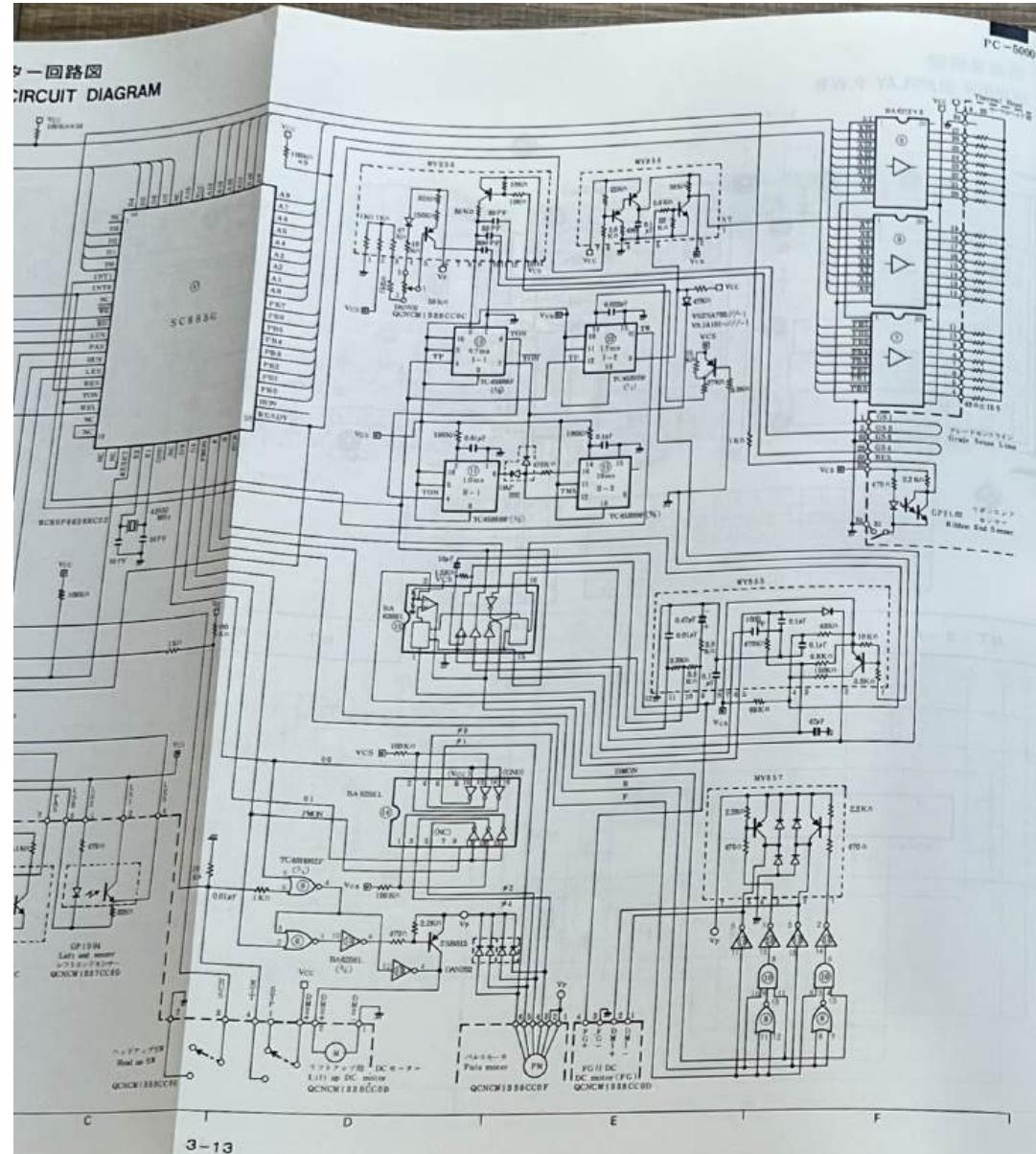


11. 電源回路図 11. POWER SUPPLY CIRCUIT DIAGRAM

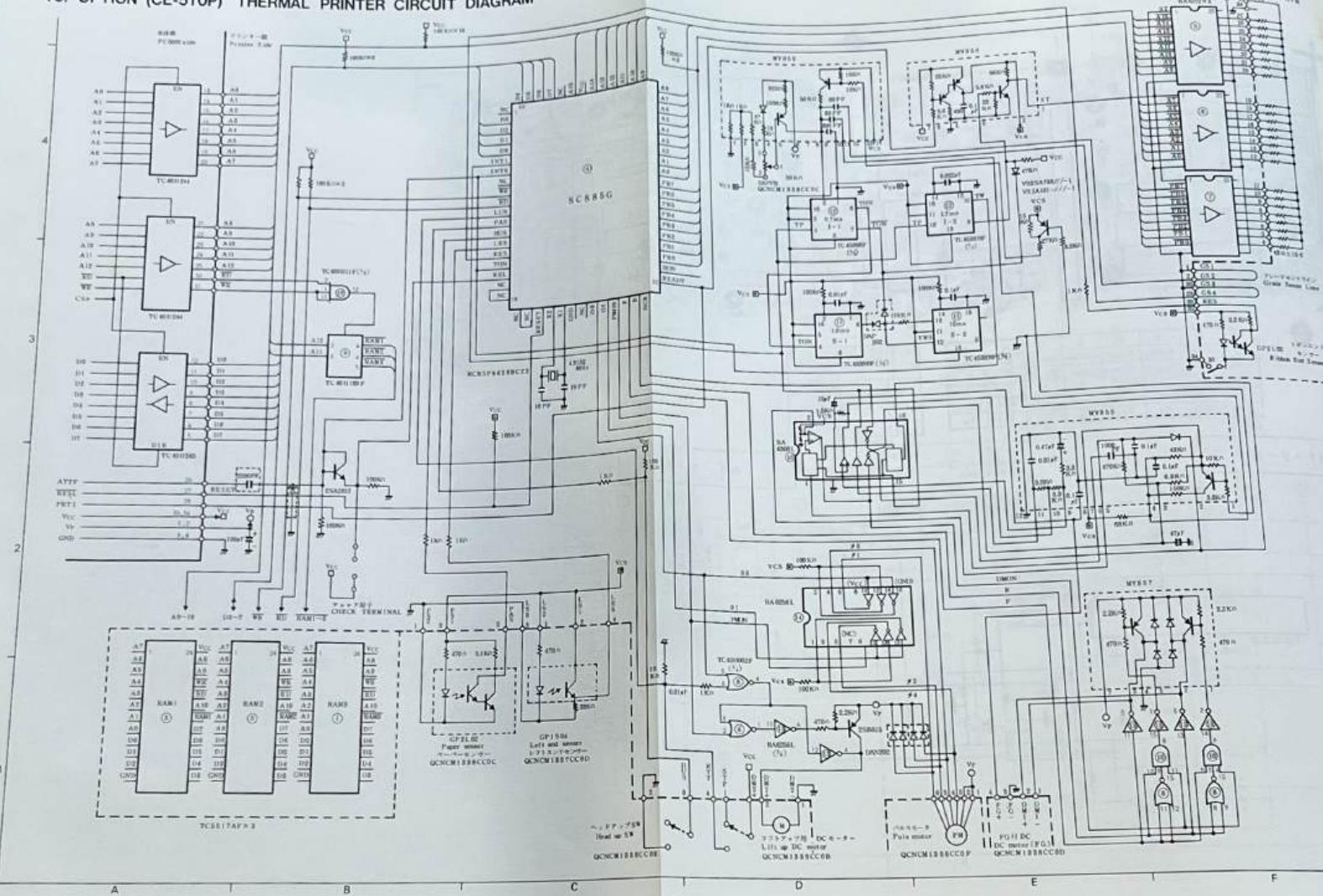


3-11



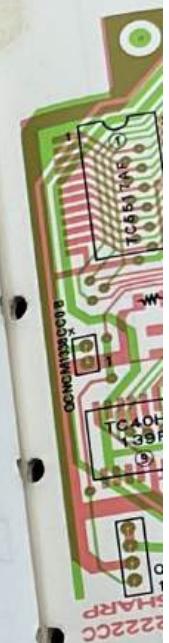


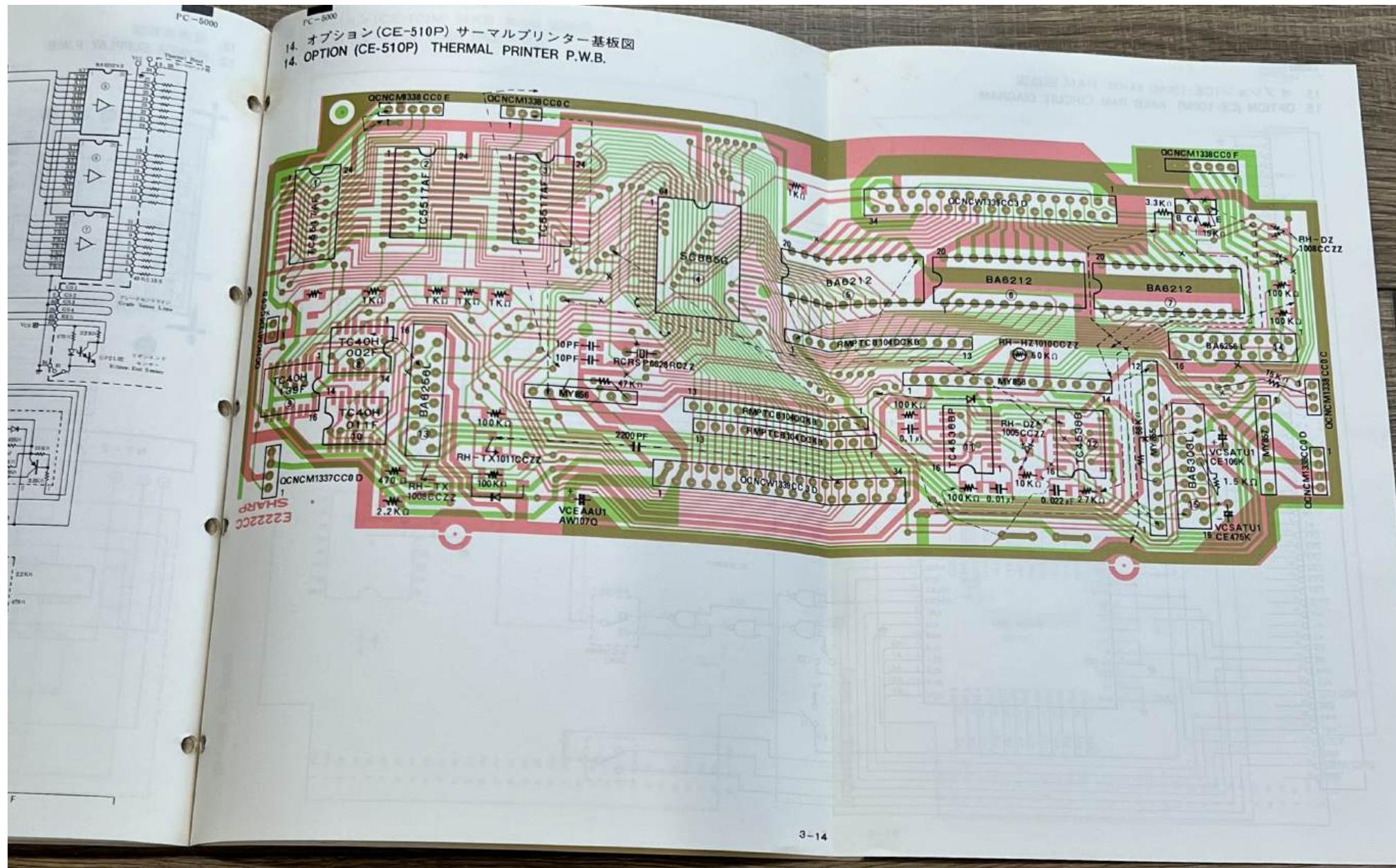
13. オプション(CE-510P) サーマルプリンター回路図
 13. OPTION (CE-510P) THERMAL PRINTER CIRCUIT DIAGRAM

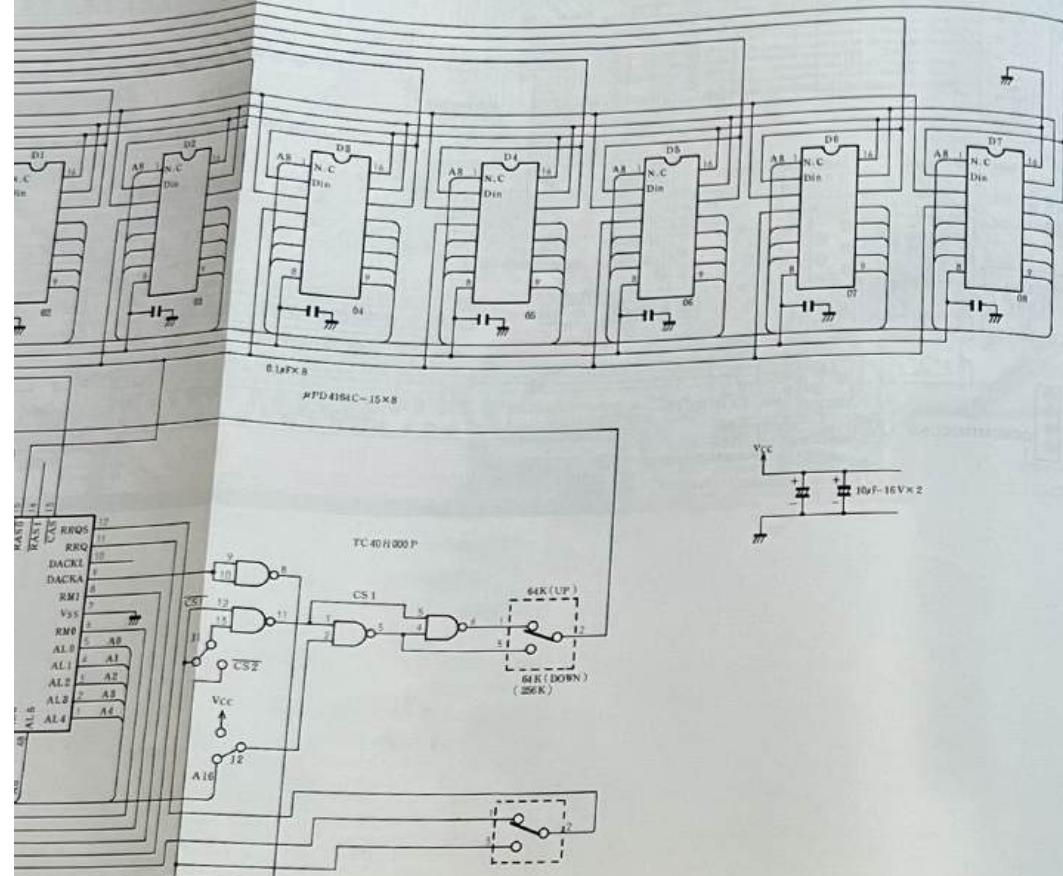


3-13

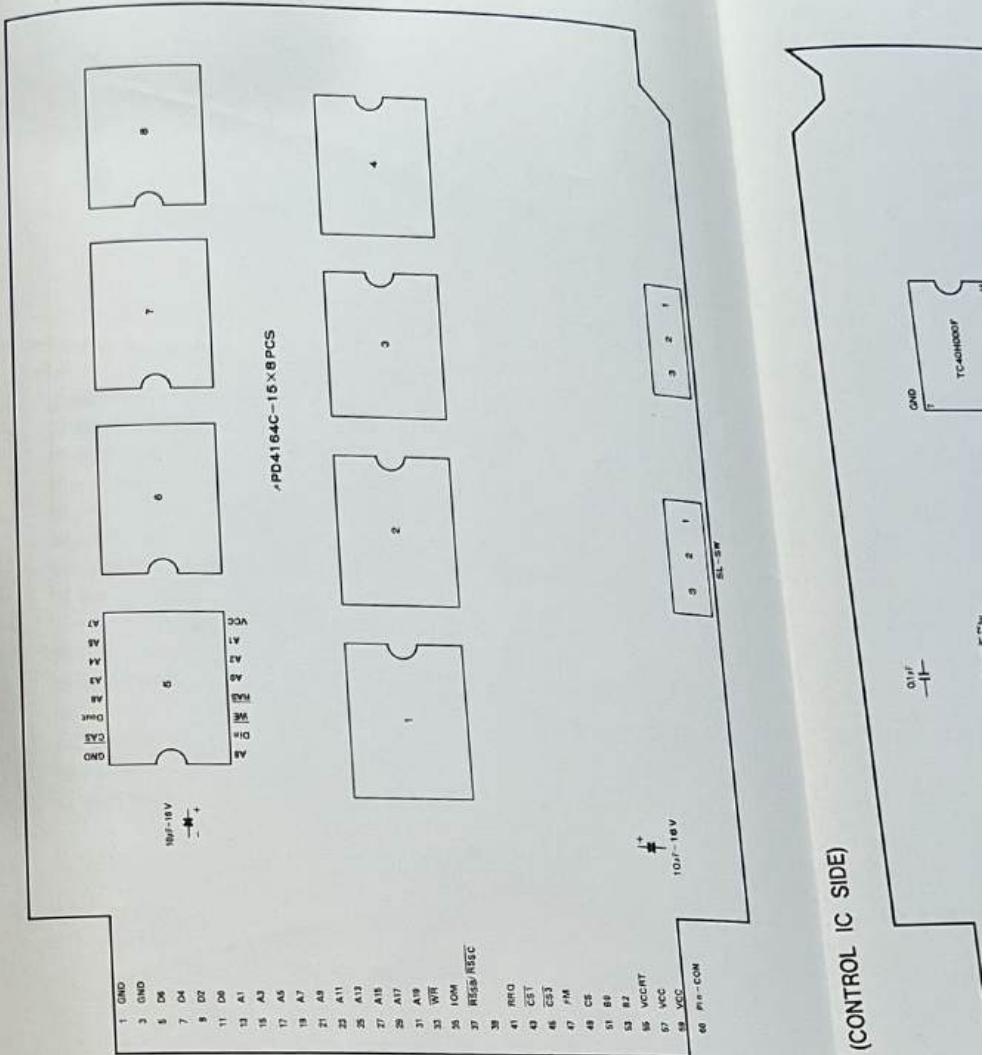
I'C - 5000
 14. オプション
 14. OPTION (C)

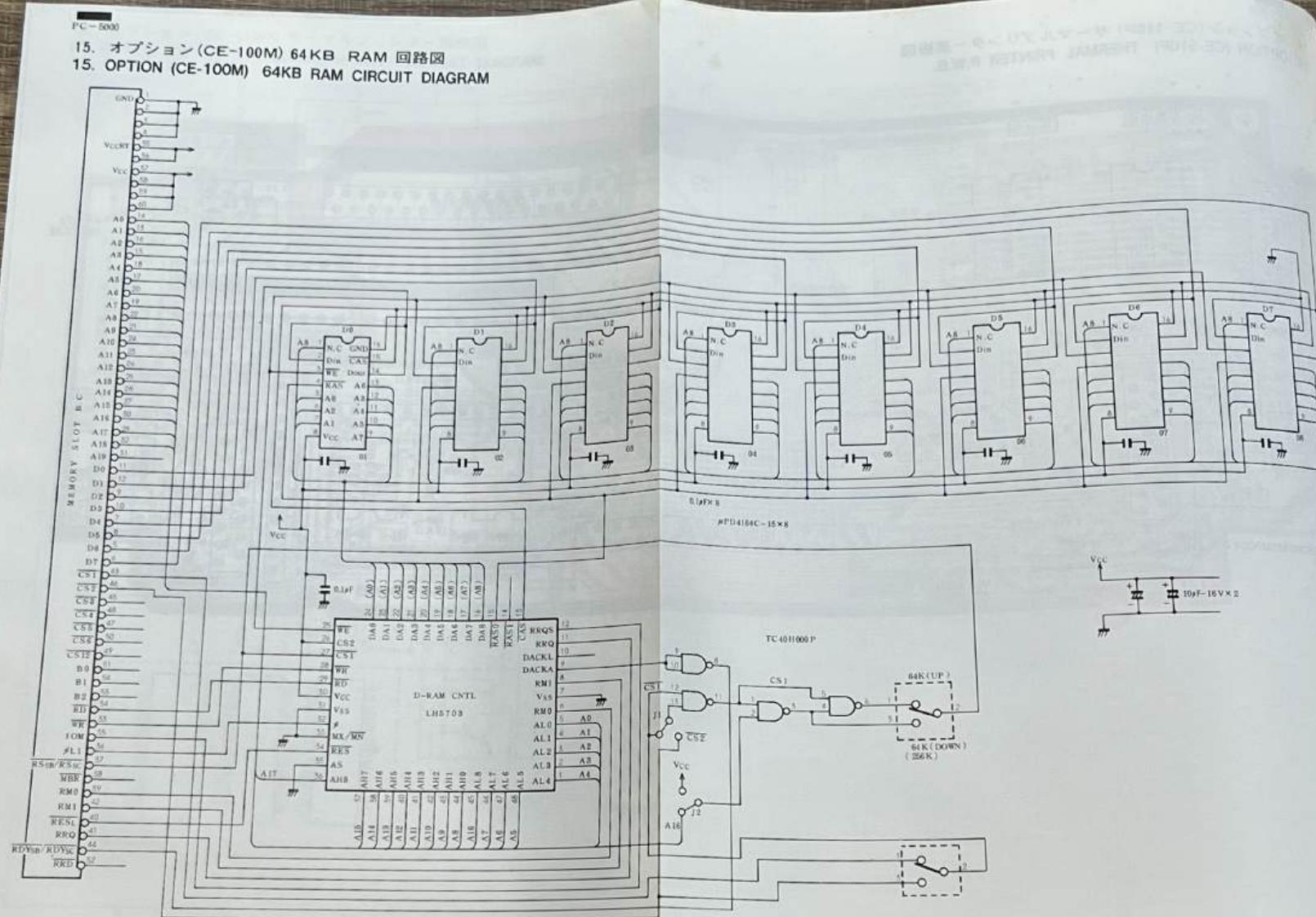


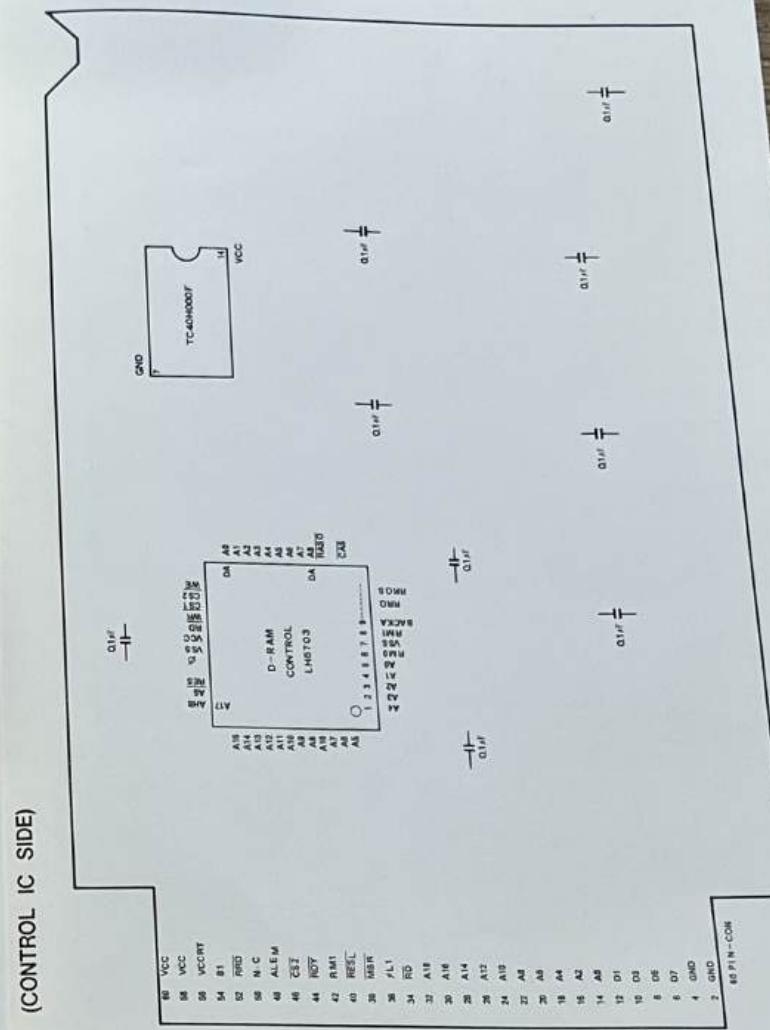
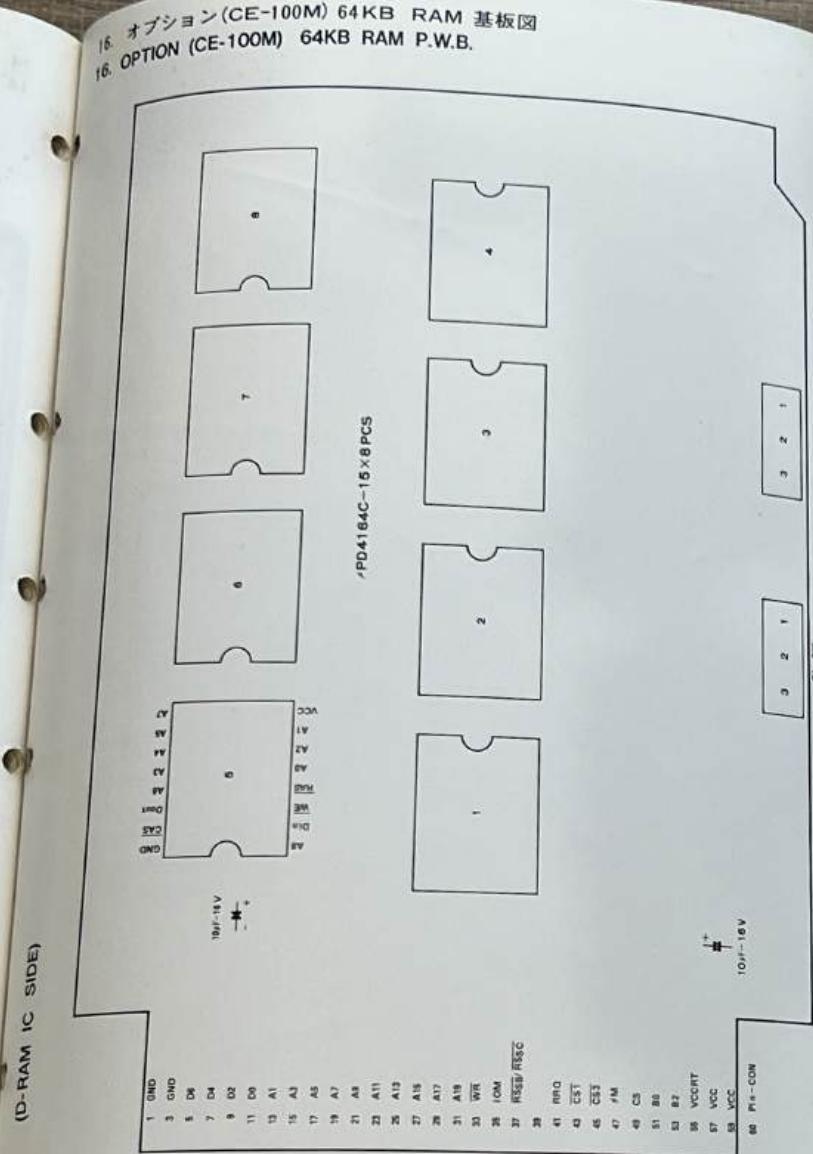




16. オプション(CE-100M) 64KB RAM 基板図
16. OPTION (CE-100M) 64KB RAM P.W.B.







IV. パーツガイド&リスト (PARTS LIST & GUIDE)

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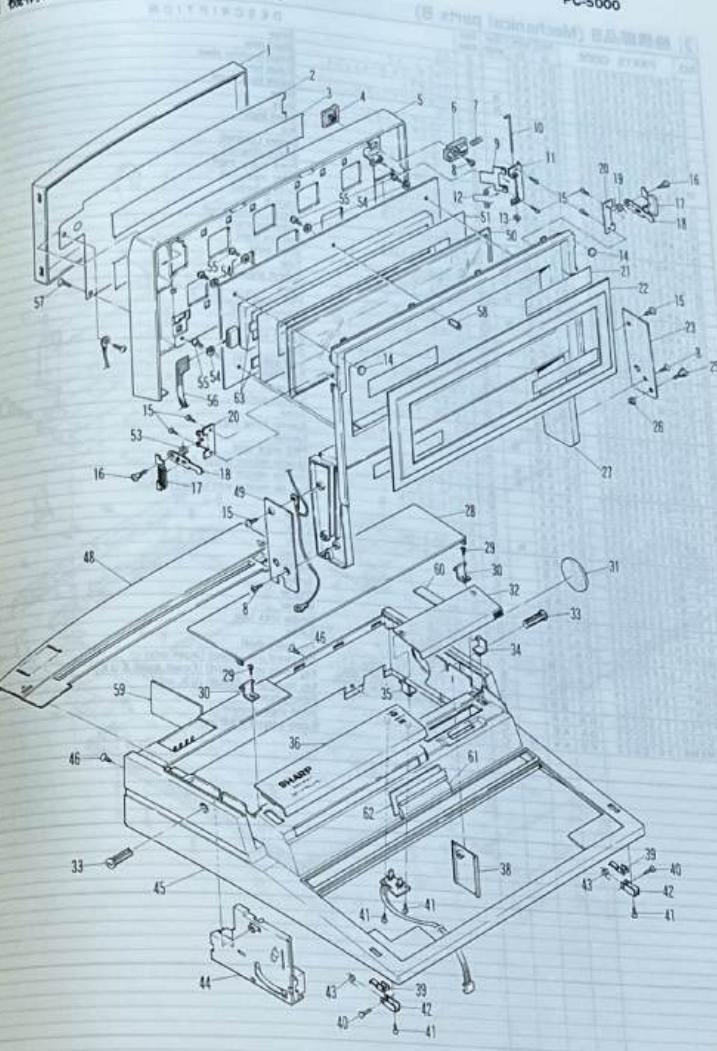
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① 機構部品A (Mechanical parts A)

NO.	PARTS CODE	PRICE RANK	NEW PART	DESCRIPTION
1	GC0VA1389CCZ2	DY AK	N	Cバー
2	PSLDLH1414CCZ2	DW AD	N	セパレーター
3	PTRH1218CCZ2	DB AB	N	カセットリリースラバー
4	JKNB2183CCZ2	EX AR	N	ロックボタン
5	GGARC1220CCZ2	DB AB	N	ディスプレイカバー
6	MSPRC1220CCZ2	DA AA	N	カセットロッカーリード
7	XUSSD26P0700	DA AA	N	スクリュ
8	MLEV1041CCZ2	DD AD	N	カセットリリースバー
9	LPINS1818CCZ2	DD AC	N	カセットリリースバー
10	LANGF1529CCZ2	DD AC	N	カセットリリースバー
11	MSPRC1220CCZ2	DD AC	N	カセットリリースバー
12	TW1001AF2	DA AA	C	スプリング
13	GLEGG1014CCZ2	DA AA	C	スクリュー
14	XUPSD26P0680	DA AA	C	スクリュー
15	LX-BZ1195CCZ2	DA AA	C	スクリュー
16	XNESD0-3206	DA AA	C	スクリュー
17	JKNB21376CCZ2	DA AB	N	カセットリリースラン
18	MLEV1044CCZ2	DB AB	N	カセットリリースラン
19	MSPRC1233CCZ2	DB AB	N	カセットリリースラン
20	PTPH1222CCZ2	DE AC	N	カセットリリースラバー
21	INDECA2138CCZ2	ET AQ	N	カセットリリースラバー
22	GC0VA1383CCZ2	DW AF	N	カセットカバー
23	GC0VA1384CCZ2	DG AF	N	スクリュー
24	LX-BZ1164CCZ2	DG AF	C	ナット
25	XNESD0-3206	DA AA	C	スクリュー
26	GCABD2713CCZ2	DO AF	N	ディスプレイカバートリ
27	GCABD2713CCZ2	DO AF	D	ブリッジアタッチ
28	GC0VA1383CCZ2	DO AF	C	スクリュー
29	XUSSD26P0590	DA AA	C	ナット
30	LPINS1818CCZ2	DA AA	N	カセットリリースバー
31	GC0VA1381CCZ2	DB AB	D	カセットリリースバー
32	GC0VA1389CCZ2	DE AC	N	ハーフカバー
33	LPINS1819CCZ2	DB AB	N	カセットリリースバー
34	LHLDZ1192CCZ2	DB AB	N	ホルダーライト
35	LHLDZ1191CCZ2	DB AB	N	ホルダーライト
36	GCABB2733CCZ2	DX AR	C	カセットトラン
37	GITAS1808CCZ2	DC AB	N	ヒューズカバーリング
38	GFTAT1255CCZ2	DG AD	N	カセットリリースラン
39	LPINS1818CCZ2	DA AA	N	カセットリリースラン
40	MSPRC1220P090	DA AA	C	スクリュー
41	LANGK1531CCZ2	DC AB	N	カセットラン
42	MSPRC1299CCZ2	DB AB	N	カセットラン
43	MSPRC1299CCZ2	DB AB	C	カセットラン
44	DUNT-4108CCZ2	EY AR	E	カセットラン
45	GCABB2732CCZ2	FW AX	N	カセットトラン A
46	XBSSC30P0690	DA AA	C	カセットトラン A
47	GC0VA1381CCZ2	DS AG	D	カセットリリースナット
48	GC0VA1384CCZ2	DN AF	N	カセットカバー
49	PFILWL1481CCZ2	FJ AU	N	フィルターフィルター
50	PSLDP1413CCZ2	DS AG	C	ディスプレイマスク
51	MSPPC1233CCZ2	DB AB	C	カセットリリースラン
52	LX-W21009CCZ2	DA AA	C	ワッシャー
53	XBPSD13P1000	DA AA	C	スクリュー
54	QPWBMT229CCZ2	EE AM	N	FPC (EP)
55	XBSSC30P1400	DA AA	C	スクリュー
56	QPWBMT229CCZ2	EE AM	N	スクリュー
57	XBSSC30P1400	DA AA	C	ナット
58	LX-NZ1019CCZ2	DA AA	N	シート
59	PSHEP1220CCZ2	DA AA	N	シート
60	LANGK1539CCZ2	DA AA	N	アンダル
61	LHLDZ11817CCZ2	DF AD	N	テンブレートラン
62	PTPEH1180CCZ2	DA AB	N	テープ
63	PSPAF1248CCZ2	DC AB	N	スペーサー

- 1 -

① 機構部品A (Mechanical parts A)

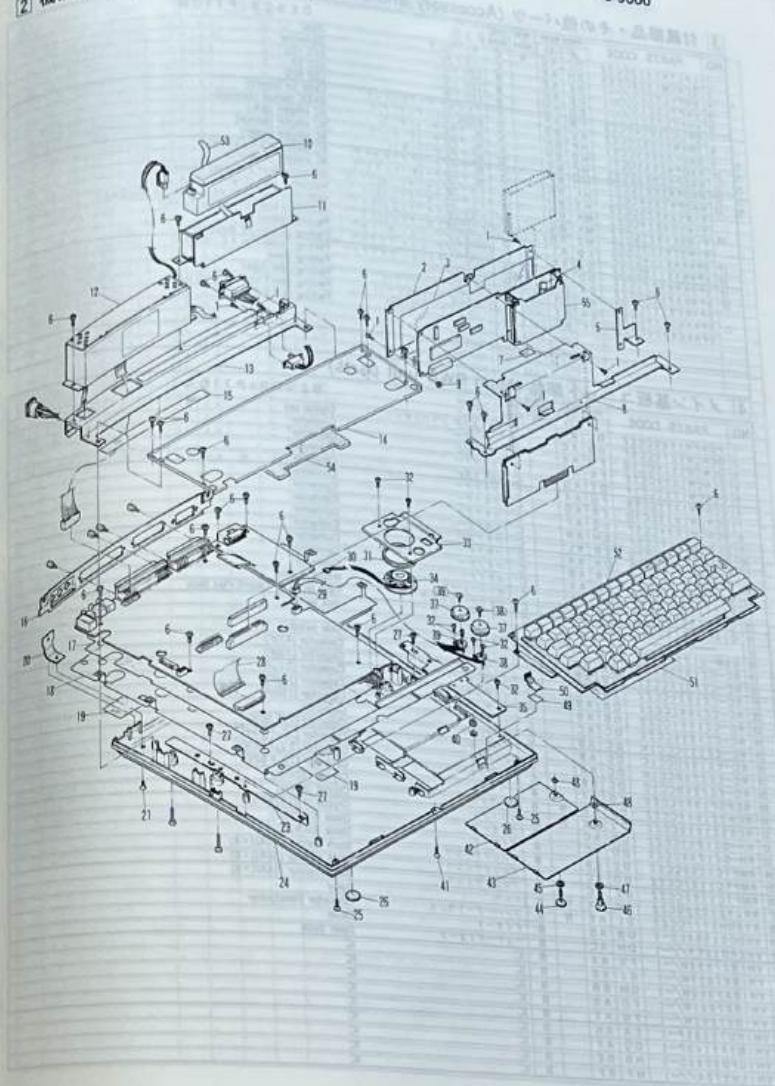


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② 機構部品B (Mechanical parts B)

NO.	PARTS CODE	PRICE	RANK	NET WT.	PART	MANUFACTURER	DESCRIPTION
1	XBPSD22P85000	DA A	C	2.5			Screw
2	PSLDC1422CC2Z	DF A	C	0.2			Panel sheet
3	PZEY1448CC2Z	DB AB	C	0.1			Bubble insulator sheet
4	JKNBZ1832CC2Z	DA AA N	C	0.1			Bubble bottom
5	ZBPSD1372CC2Z	DE AC N	C	0.1			Bubble fixing angle
6	PZETL174CC2Z	DA AA	C	0.1			Screw
7	PZETL174CC2Z	DA AA	C	0.1			Sheet
8	LANGF1521CC2Z	FA AK	N	0.1			Angle angle
9	XNESD20-16000	DA AA	C	0.1			Nut
10	CBATZ9082CC2Z	HN BG	B	0.1			Battery (Japanese)
11	CBATZ9082CC2Z	HN BG	B	0.1			Battery (English)
12	DUNY137180CC2Z	DP AF	N	0.1			Power supply angle
13	LANGT1532CC2Z	EA AK	N	0.1			Power supply unit
14	LANGF1582CC2Z	DM AF	N	0.1			Battery chassis
15	PZETL1503CC2Z	DB AB	C	0.1			Angle B
16	LANGT1499CC2Z	DV AH	N	0.1			Chassis cushion sheet
17	GG1019CC2Z	DF AD	N	0.1			Insulator sheet
18	PLDLC1493CC2Z	EG AN	N	0.1			Shield panel
19	PTEH1211CC2Z	TA HN	D	0.1			Tape
20	LANGK1525CC2Z	DB AC N	C	0.1			Cabinet angle left
21	XBSST30P6600	DA AA	C	0.1			Screw
22	LANGT1503CC2Z	DH AD	N	0.1			PWB angle left
23	GA6A2731CC01	FT AW	C	0.1			Cabinet bottom
24	XBSST30P18000	DA AA	C	0.1			Screw
25	XBSST30P18000	DA AA	C	0.1			Rubber foot
26	GG1019CC2Z	DB AB	C	0.1			Screw
27	XUPD0310P00005	DA AA	C	0.1			Lead wire (27P)
28	QCNW1323CC01	DA AK	N	0.1			Connector
29	QCNW1323CC01	DA HN	D	0.1			Connector
30	QCNW1324CC01	DD AC	C	0.1			Speaker
31	PCUSS1244CC2Z	DB AB	C	0.1			Speaker cushion
32	XUPSD16P85000	DA AA	C	0.1			Screw
33	LANGT1505CC2Z	DF AD	N	0.1			Speaker fixing angle
34	VSP0038P268A	EG AM	A	0.1			Speaker
35	GG1019CC2Z	DG AD	N	0.1			Speaker angle right
36	JKNBZ1105CC2Z	DA AA	C	0.1			Variable resistor button A
37	RVR-M340P00002	DA AB	B	0.1			Variable resistor with screw (30KΩ)
38	RVR-C1550PQZ7	DR AF	B	0.1			Variable resistor with screw (100KΩ)
39	XNESD20-74800	DA AA	C	0.1			Nut
40	XBPSF16P18000	DA AA	C	0.1			Screw
41	XBPSF16P18000	DA AA	C	0.1			Cover
42	GC0VA1383CC2Z	DX AH	N	0.1			Cover
43	GC0VA1394CC2Z	DV AK	C	0.1			Washer
44	LX-BZ1151CC2Z	DC AB	C	0.1			Screw
45	LX-WZ1009CC2Z	DA AA	C	0.1			Washer
46	LX-BZ1157CC2Z	DB AB	C	0.1			Screw
47	LX-WZ1008CC2Z	DA AA	C	0.1			Washer
48	LX-WZ1007CC2Z	DA AA	C	0.1			Washer
49	PTPEC1219CC2Z	DA AA	C	0.1			Outer stick tape
50	MSPR0104CC2Z	DA AA	C	0.1			Spring
51	PZETL1499CC2Z	DB AB	C	0.1			Key board sheet
52	DUNT-7535CC2Z	LV BN	E	0.1			Key board unit (Japan) (Japan only)
53	DUNT-7535CC2Z	LV BN	E	0.1			Key board unit (Export) (Japan & U.K.)
54	PTPEC1219CC2Z	DA AA	C	0.1			Key board unit (Export) (U.K. only)
55	PCUSG1223CC2Z	DK AE	C	0.1			Battery tape
	RMEMR1007CC2Z	VD *** N	C	0.1			Shield angle cushion

② 機構部品B (Mechanical parts B)



3) 付属部品・その他パーツ (Accessory and other parts)

NO.	PARTS CODE	PRICE RANK	NEW PART	DESCRIPTION
Ja	Ex	MARK	RANK	
1	LPIZK1113CCZZ	DC A C	N	C リードホールド
2	QCNW1128CCZZ	DL A C		Connector
4	VHPTL1V1//	DE A C	B	LED ホワイト
5	VHPTLG21//	DE A C	B	LED グリーン
6	VHPTLR21//	DD A C	B	LED レッド
7	QPLGJ1014CCZZ	F B A R	C	カセット用カバーハルス
8	RADPA1051CCZZ	GU BD	D	BASIC manual (Japanese)
9	RADPA1052CCZZ	GP BH	C	ACアダプタ (ヨーロッパ)
10	RADPA1053CCZZ	HQ BD	C	ACアダプタ (ヨーロッパ)
11	RADPA1054CCZZ	HO BF	C	ACアダプタ (ヨーロッパ)
12	RADPA2003CC01	HH BF	C	ACアダプタ (アメリカ)
13	RADPA2004CC01	HL BG	C	ACアダプタ (アメリカ)
14	TINSJ4023CCZZ	HT BH	D	インストラクション (日本語)
15	TINSJ4024CCZZ	MK BQ	D	インストラクション (英語)
16	TINSJ4025CCZZ	MN BQ	D	インストラクション (ヨーロッパ)
17	SPAKA1114CCZZ	EB AL	D	エアクッションシート (ヨーロッパ)
18	SPAKA1115CCZZ	DL AF	D	エアクッションシート (ヨーロッパ)
19	SPAKA8333CCZZ	DO AC	D	エアクッションシート (ヨーロッパ)
20	SPAKAB3334CCZZ	DA RA	D	パッケージ
21	SPAKC8113CCZZ	GA AY	D	パッケージ (ヨーロッパ)
22	SPAKC8116CCZZ	GA AY	D	パッケージ (ヨーロッパ)
23	SPAKC8308CCZZ	HE BF	D	パッケージ (USA)

4) メイン基板ユニット部品 (Main PWB unit parts)

NO.	PARTS CODE	PRICE RANK	NEW PART	DESCRIPTION
Ja	Ex	MARK	RANK	
1	PCAPH1386CCZZ	DL A F	C	リードホルダーカップ
2	QCNCW11330CCF	DL A C	C	コネクター
3	QCNCW11330CCG	FU D	C	コネクター
4	QCNCW11330CC2K	FK A U	C	コネクター
5	QCNCM11331CC1F	DT A G	C	コネクター
6	QCNCW11332CC6B	FU AX	C	コネクター
7	QCNCW11333CC3D	ER A Q	C	コネクター
8	QCNCM11334CC1F	DQ AF	C	コネクター
9	QCNCM11334CC2F	EH AN	C	コネクター
10	QCNCW11336CC2G	EB AL	C	コネクター
11	QCNCM11337CC0B	DA AA	C	コネクター
12	QCNCM11337CCD	DA AB	C	コネクター
13	QCNCW11343CC6B	FW AX	C	コネクター
14	PZETL1497CC01	DA A I	C	ガラス
15	QJAKC1013CCZZ	DD AG	C	コネクターボックス
16	QJAKC1016CCZZ	DH AC	C	ジャック
17				
18	QSW-S1358CCZZ	DG AD	B	スライドスイッチ
19	RC-CZ1015CCZZ	DB AB	C	コンデンサー
20	RC-CZ1019CCZZ	DB AB	C	コンデンサー
21	RC-CZ1021CCZZ	DB AB	C	コンデンサー
22	RC-CZ1041CCZZ	DB AB	C	コンデンサー
23	RC-CZ1052CCZZ	DB AB	C	コンデンサー
24	RC-CZ1056CCZZ	DC AC	C	コンデンサー
25	RC-EZ1055CC1H	DC AB	C	コンデンサー
26	RC-EZ1060CC1C	DC AB	C	コンデンサー
27	RC-EZ1065CC1H	DC AB	C	コンデンサー
28	RC-EZ2258CC1H	DC AB	C	コンデンサー
29	RC-EZ2228BCC1C	DC AB	C	コンデンサー
30	RCRSP1010CCZZ	F A T	B	クリスタル
31	RCRSZ1049CCZZ	DJ AE	N	クリスタル
32	RCRSZ1050CCZZ	DJ AE	N	クリスタル
33	RH-DZ1060CCZZ	DD AC	B	ダイオード
34	RH-DZ1090CCZZ	DD AC	B	ダイオード
35	RMPTC1105CCZZ	DC AB	B	ブロブタイコウ
36	RMPTC1107CCZZ	DD AC	B	ブロブタイコウ
37	RMPTC1116CCZZ	DE AC	B	ブロブタイコウ
38	RRLYZ3200CCZZ	FW AX	N	リレー
39	RTRNH1777CCZZ	DL AE	B	コンバータトランジ
40	VHDD5158L2//	DB AB	B	ディオード
41	VHERD1059//	DH AC	B	ゼンタリオード
42	VHIBX7055W//	FX AX	B	IC
43	VHIBX7055W//	GJ AB	B	IC
44	VHIBX7056W//	GM BB	B	IC
45	VHIBX7056W//	FD AS	B	IC
46	VHIBX7056W//	FG AT	B	IC
47	VHM5451AAP//	EA AK	B	IC
48	VHIBUP60880//	DQ AF	B	IC
49	VHILH5704//	HB SE	B	IC
				IC

4) メイン基板ユニット部品 (Main PWB unit parts)

NO.	PARTS CODE	PRICE RANK	NEW PART	DESCRIPTION
Ja	Ex	MARK	RANK	
50	VH1LH1105//	HR BH	B	IC
51	VH1SC10631BP1	TR AW	B	IC
52	VH1SC10630BP2	TR AW	B	IC
53	VH1SC10630BP3	HR BE	B	IC
54	VH1TC48H10027H	DS AG	B	IC
55	VH1TC48H10047H	DP AF	B	IC
56	VH1TC48H10047H	DP AF	B	IC
57	VH1TC48H10047H	DP AF	B	IC
58	VH1TC48H10047H	DP AF	B	IC
59	VH1TC48H10047H	DP AF	B	IC
60	VH1TC48H10047H	DP AF	B	IC
61	VH1TC48H10047H	DP AF	B	IC
62	VH1TC48H10047H	DP AF	B	IC
63	VH1TC48H10047H	DP AF	B	IC
64	VH1TC48H10047H	DP AF	B	IC
65	VH1TC48H10047H	DP AF	B	IC
66	VH1TC48H10047H	DP AF	B	IC
67	VH1TC48H10047H	DP AF	B	IC
68	VH1TC48H10047H	DP AF	B	IC
69	VH1TC48H10047H	DP AF	B	IC
70	VH1TC48H10047H	DP AF	B	IC
71	VH1TC48H10047H	DP AF	B	IC
72	VH1TC48H10047H	DP AF	B	IC
73	VH1TC48H10047H	DP AF	B	IC
74	VH1TC48H10047H	DP AF	B	IC
75	VH1TC48H10047H	DP AF	B	IC
76	VH1TC48H10047H	DP AF	B	IC
77	VH1TC48H10047H	DP AF	B	IC
78	VH1TC48H10047H	DP AF	B	IC
79	VH1TC48H10047H	DP AF	B	IC
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86	VH1TC48H10047H	DP AF	B	IC
87	VH1TC48H10047H	DP AF	B	IC
88	VH1TC48H10047H	DP AF	B	IC
89	VH1TC48H10047H	DP AF	B	IC
90	VH1TC48H10047H	DP AF	B	IC
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95	VH1TC48H10047H	DP AF	B	IC
96	VH1TC48H10047H	DP AF	B	IC
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101	VH1TC48H10047H	DP AF	B	IC
102	VH1TC48H10047H	DP AF	B	IC
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106	VH1TC48H10047H	DP AF	B	IC
107	VH1TC48H10047H	DP AF	B	IC
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119	VH1TC48H10047H	DP AF	B	IC
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179	VH1TC48H10047H	DP AF	B	IC
180	VH1TC48H10047H	DP AF	B	IC
181	VH1TC48H10047H	DP AF	B	IC
182	VH1TC48H10047H	DP AF	B	IC
183	VH1TC48H10047H	DP AF	B	IC
184	VH1TC48H10047H	DP AF	B	IC
185	VH1TC48H10047H	DP AF	B	IC
186	VH1TC48H10047H	DP AF	B	IC
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189	VH1TC48H10047H	DP AF	B	IC

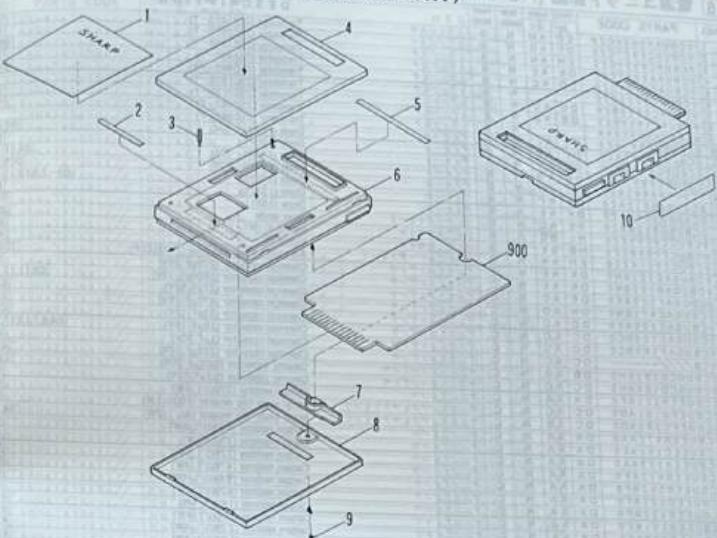
5 メモリー基板ユニット部品 (Memory PWB unit parts)

NO.	PARTS CODE	PRICE RANK Ja Ex	NEW MARK	PART RANK	DESCRIPTION
1	RC-C21021CC2Z	D B A B	C	コネクター	Capacitor (0.1μF)
2	VH161256FC-1	G H B A	B	IC	IC
3	VH161256FC-4	G H B A	B	IC	IC
4	VH161256FC-6	G H B A	B	IC	IC (Capacitor (Japan only))
5	VH161256FC-7	G H B A	B	IC	IC (Export) (Except Japan & U.K.)
6	VH161256FC17	G W B D	B	IC	IC (Export) (U.K. only)
7	VH161256FC18	G W B D	B	IC	IC
8	VH161256FC32	G W B D	B	IC	Double stick tape
9	VH161256FC33	D G A B	B	IC	Memory PWB sheet
10	PTPEH1049CC2Z	D A A A	C	メモリーパンクレー	Capacitor
11	PZETL1495CC2Z	D C A B N	C	コネクター	Screw
12	RC-EZ106DCC1C	D C A B	C	コネクター	Nut
13	XKPS020P0500B	D A A A	C	ダブル	
14	XKPS020-16800	D A A A	C	ダブル	
					(Unit)
901	DUNTK7783CC2Z	Z Z ***	E		メモリー基板ユニット (HS)
	DUNTK7783CC2Z	Z Z ***	E		メモリー基板ユニット (ASLJ)
	DUNTK7783CC2Z	Z Z ***	E		メモリー基板ユニット (ASCD)

6 BASIC ROMユニット (BASIC ROM UNIT)

NO.	PARTS CODE	PRICE RANK Ja Ex	NEW MARK	PART RANK	DESCRIPTION
1	T LABZ1946CCZZ	D D A C N	D	ラベル	Label
2	PTPEH1137CCZZ	D A A A	D	テープ	Tape
3	MSPRC1181CCZZ	D A A A	C	スプリング	Spring
4	GCABB2754CCZZ	D K A E	D	アルミパネルウエ	Panel top
5	PTPEH1127CCZZ	D A A A	C	テープ	Tape
6	LCHSS1151CCZZ	D E A C	C	シャーシ	Chassis
7	LHLDFF1195CCZZ	D D A C	C	PWBナサ	Holder
8	GCABA2753CCZZ	D K A E	D	アルミパネルシコ	Panel bottom
9	LX-BZ1098CCZZ	D A A A	C	タッピングネジ	Screw
10	T LABZ1946CCZZ	D A A A N	D	ラベル	Label
	VH161256FC-46	G H B A N B	L.S.I. ニホン	L.S.I.	for Japan
	VH161256FC-18	G H B A N B	L.S.I. Ex	L.S.I.	Except Japan
	VH161256FC-47	G H B A N B	L.S.I. ニホン	L.S.I.	for Japan
	VH161256FC-19	G H B A N B	L.S.I. Ex	L.S.I.	Except Japan
	VH1TC40T01OFN	D P A F	B	i. C.	i. C.
	RC-CZ1021CCZZ	D B A B	C	チップコンデンサー 0.1μF	Capacitor 0.1μF
	RC-EZ106DCC1C	D C A B	C	コンデンサー 10μF 16V	Capacitor 10μF 16V
901	DUNTK7783CCZZ	H B	N	E	PWBユニット ニホン
	DUNTK7775CCZZ	H B	B E	N	PWBユニット Ex

6 BASIC ROMユニット (BASIC ROM UNIT)



7 LCD基板ユニット部品 (LCD PWB unit parts)

NO.	PARTS CODE	PRICE RANK Ja Ex	NEW MARK	PART RANK	DESCRIPTION
1	PZETL1756CCZZ	D A A A	C	シート B	Sheet B
2	QCNOW1380CC09	D D A C	C	コネクター	Connector
3	RC-C21021CCZZ	D B A B	C	コネクター	Capacitor (0.1μF)
4	RC-EZ106DCC1E	D C A B	C	コネクター	Capacitor (0.1μF 25V)
5	RK-K21056CCZZ	D A A A	C	ダイコウ	Resistor (22kΩ ± 2% chip)
6	RK-K21059CCZZ	D A A A	C	ダイコウ	Resistor (110kΩ ± 2% chip)
7	RK-K21080CCZZ	D A A A	C	ダイコウ	Resistor (510kΩ ± 2% chip)
8	VHEHZ4CLL//1	D L A E	L	ヒュードライバー	Driver
9	VH1LH503B//1	G E A Z	B	IC	IC
10	VH1LH5035//1	D Z A K	B	IC	IC
11	VH1LH524N//1	E D A K	B	IC	IC
12	VRS-TP2BD101J	D A A A	C	ダイコウ	Resistor (1/BW 1000 ± 5%)
13	VRS-TP2BD103J	D A A A	C	ダイコウ	Resistor (1/BW 10kΩ ± 5%)
14	VRS-TP2BD563J	D A A A	C	ダイコウ	Resistor (1/BW 56kΩ ± 5%)
901	DUNTK7393CCZZ	Z Z ***	E	LCDユニット	LCD unit

8 電源ユニット部品 (P.S. unit)

NO.	PARTS CODE	PRICE	RANK	NEW	PART	DESCRIPTION
1	OCBUAA8030CZ0	ED-A	M	N	B	トランジスタ Transistor (2SA1012-Y)
2	OCBUAC8030CZ0	ED-A	M	N	B	トランジスタ Transistor (2SC3220-Y)
3	OCBUAC8030CZ0	ED-A	M	N	B	トランジスタ Transistor (2SA1012-Y)
4	OCBUAA8037CZ0	DK-A	E	N	B	トランジスタ Transistor (2SA1015-PA)
5	OCBUAC8004DZ0	DD-A	C	N	B	トランジスタ Transistor (2SA1015-Y)
6	OCBUAC8004DZ0	DD-A	C	N	B	トランジスタ Transistor (2SC2120-Y)
7	OCBUAC8060BZ0	DG-A	D	N	B	トランジスタ Transistor (2SA882-E)
8	OCBUAC8060BZ0	DG-A	D	N	B	トランジスタ Transistor (2SA882-P)
9	OCBVX00128XXBZ0	DB-A	B	N	B	Diode (EBC81)
10	OCBUUC8087A20	EC-A	L	N	B	Diode (1N4001)
11	OCBUUC8017A20	DL-A	E	N	B	Diode (1N4001)
12	OCBUUC8007BZ0	DM-A	E	N	B	Diode (1N4001)
13	OCBUUC8093A20	DR-A	G	N	B	Diode (1N555)
14	OCBUAB6005AZ0	DC-A	B	N	B	Diode (1SS16)
15	OCBUAB6005AZ0	DC-A	B	N	B	Diode (10E1)
16	OCBUAB6005AZ0	DC-A	B	N	B	Zener diode
17	OCBU0001288820	DE-A	C	N	B	Hybrid IC (NT-1-A)
18	OCBUZ001288820	HL-B	G	N	B	Hybrid IC (NT-1-A)
19	OCBUZ200502X0	HB-B	N	B	Adjustable shunt regulator (TL431CLP)	
20	OCBUZ200142X0	EH-A	N	C	Chemical capacitor (220pF/35V)	
21	OCBUGAE212BN0	DK-A	E	N	C	Chemical capacitor (1000pF/10V)
22	OCBUGAF102BN0	DK-A	E	N	C	Chemical capacitor (22pF/50V)
23	OCBUGAC102AK0	DK-A	E	N	C	Chemical capacitor (470pF/6V)
24	OCBUGAC102AK0	DK-A	E	N	C	Chemical capacitor (33pF/16V)
25	OCBUGAC102AK0	DC-A	C	N	C	Chemical capacitor (100pF/6V)
26	OCBUGAC108BC0	DC-A	C	N	C	Chemical capacitor (220pF/10V)
27	OCBUGAF108BC0	DC-A	C	N	C	Capacitor (0.01μF/50V)
28	OCB//	DC-A	C	N	C	Capacitor (0.01μF/50V)
29	OCBUGCD103AH0	DB-A	B	N	C	Carbon resistor (220Ω/1.4W)
30	OCBUGCO104AH0	DC-A	C	N	C	Carbon resistor (220Ω/1.4W)
31	OCBUWE2212A0	DA-A	A	N	C	Metal oxide film resistor (1000Ω/1W)
32	OCBUWE2212A0	DC-A	B	N	C	Metal oxide film resistor (30Ω/1.2W)
33	OCBUGFC007AD0	DC-A	B	N	C	Carbon resistor (4.7kΩ/1.6W)
34	OCBUCEEA7AA0	DA-A	A	N	C	Carbon resistor (150Ω/1W)
35	OCBUCEC151AA0	DA-A	A	N	C	Carbon resistor (1.2MΩ/1W)
36	OCBUCEA123AA0	DA-A	A	N	C	Carbon resistor (4.0Ω/1.4W)
37	OCBUCEB1473AF0	DA-A	A	N	C	Carbon resistor (5.6kΩ/1.4W)
38	OCBUFEFB562AF0	DA-A	A	N	C	Carbon resistor (820Ω/1.4W)
39	OCBUFEDE021AF0	DA-A	A	N	C	Carbon resistor (1kΩ/1.4W)
40	OCBUCEB102AF0	DA-A	A	N	C	Carbon resistor (1000Ω/1.4W)
41	OCBUCEEB101AE0	DA-A	A	N	C	Carbon resistor (1.5kΩ/1.4W)
42	OCBUCEEB101AE0	DA-A	A	N	C	Carbon resistor (1.5kΩ/1.4W)
43	OCBUCEEB101AF0	DA-A	A	N	C	Carbon resistor (4700Ω/1.4W)
44	OCBUCEB471AF0	DA-A	A	N	C	Carbon resistor (10Ω/1.2W)
45	OCBUCEC101AE0	DA-A	A	N	C	Carbon resistor (10kΩ/1.4W)
46	OCBUCEB100AF0	DA-A	A	N	C	Carbon resistor (33kΩ/1.4W)
47	OCBUCEEB313AF0	DA-A	A	N	C	Carbon resistor (680Ω/1.4W)
48	OCBUCEB681AF0	DA-A	A	N	C	Thermistor (5000Ω~5Ω)
49	OCBU00011220	DX-A	H	N	B	Thermistor (D20~3540)
50	OCBU00011220	EX-A	K	N	B	Variable resistor (2kΩ)
51	OCBUFCD202AA0	DL-A	E	N	B	Variable resistor (50kΩ)
52	OCBUFCD503AA0	DL-A	E	N	B	Variable resistor (500Ω)
53	OCBUFCD501AA0	DL-A	E	N	B	Variable resistor (5kΩ)
54	OCBUFCD507A00	DL-A	E	N	C	Input noise filter
55	OCB8298000340	EZ-A	A	N	C	Chopper choke coil
56	OCB8298000350	EZ-A	A	N	C	Choke coil (SN-L3)
57	OCB8298000360	EZ-A	A	N	C	Choke coil (SN-L4)
58	OCB8298000370	EZ-A	A	N	B	Driver transformer (SN-T2)
59	OCB8298000310	EZ-A	A	N	B	Power Transformer (SN-T2)
60	OCB8298000320	EZ-A	A	N	B	Power Transformer (SN-T3)
61	OCB8298000330	EZ-A	A	N	B	Power Transformer (SN-T3)
ユニット (Unit)						
601	DUNT-7411CCZZ	TX	B	Z	E	アンサンユーニット

PS unit

9 バブル・メモリ基板 (Bubble memory P.W.B.)

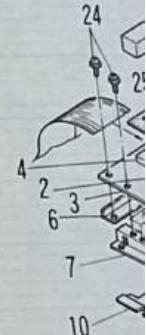
NO.	PARTS CODE	PRICE	RANK	NEW	PART	DESCRIPTION
1	OCBUH4779501	MH-B	Q	N	B	LSI (HD46107PA23)
2	OCBUH4779501	MV-B	R	N	B	LSI (HD46107PA23)
3	OCBUH4779504	DL-A	F	B	IC	LSI (HD46107PA23)
4	OCBUH4779505	GG-A	A	N	B	LSI (HD46107PA23)
5	OCBUH4779505	DA-A	A	N	B	LSI (HD46107PA23)
6	OCBUH4779505	FD-A	S	N	B	LSI (HD46107PA23)
7	OCBUH4779505	DK-AH	H	N	B	LSI (HD46107PA23)
8	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
9	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
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41	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
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43	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
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55	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
56	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
57	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
58	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
59	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
60	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
61	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
62	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
63	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
64	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
65	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
66	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
67	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
68	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
69	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
70	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
71	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
72	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
73	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
74	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
75	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
76	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
77	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
78	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
79	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
80	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
81	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
82	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
83	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
84	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
85	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
86	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
87	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
88	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
89	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
90	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
91	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
92	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
93	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
94	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
95	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
96	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
97	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
98	OCBUH4779505	ES-AQ	N	B	LSI (HD46107PA23)	
99</						

10 キーボードユニット (Keyboard unit)

NO.	PARTS CODE	PRICE	NAME	NEW PART	DESCRIPTION	
					IN	EX
1	DOPVFL19503-2	DT	G	B	スイッチ	Push switch
2	DOPVFL19503-2	DT	G	B	スイッチ	P.W.B. (Japan only)
3	DOPVFL19503-2	HEB	N	B	P.W.B. (コネクタ)	P.W.B. (Export)
4	DOPVFL19503-2	HEB	N	B	P.W.B. (コネクタ)	Connector
5	DOP2SKF028B	FGAT	N	C	スイッチ	Insulator (Japan only)
6	DOP2SKF028B	FGAT	N	C	スイッチ	Insulator (Export)
7	DOP2SKF028B	FGAT	N	C	スイッチ	Angle
8	DOP2SKF028B	FGAT	N	C	スイッチ	Angle
9	DOP2SKF028B	FGAT	N	C	スイッチ	Angle
10	DOP2SKF028B	FGAT	N	C	スイッチ	Angle
11	DOP2SKF028B	FGAT	N	C	スイッチ	Angle
12	DOP2SKF028B	FGAT	N	C	スイッチ	Angle
13	DOP2SKF028B	DEAC	N	C	スイッチ	Key guide
14	DOP2SKF028B	DEAC	N	C	スイッチ	Key guide
15	DOP2SKF028B	DRAG	N	C	スイッチ	Key guide
16	DOP2SKF028B	DRAG	N	C	スイッチ	Key guide pin
17	DOP2SKF028B	DRAG	N	C	スイッチ	Spring
18	DOP2SKF028B	DRAG	N	C	スイッチ	Key top (Japan only) (Space)
19	DOP2SKF028B	ERQ	N	C	スイッチ	Key top (Export) (Space)
20	DOP2SKF028B	ERQ	N	C	スイッチ	Lever
21	DOP2SKF028B	ERQ	N	C	スイッチ	Lever
22	DOP2SKF028B	ERQ	N	C	スイッチ	Screw
23	DOP3D041040	DCAC	N	C	スイッチ	Screw
24	DOP3D041040	DBAB	N	C	スイッチ	Screw
25	DOP2IKF013A	DFAD	N	C	スイッチ	Screw
101	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (ON/BRK)
102	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (OFF) オフ位置
103	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (F1)
104	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (F2)
105	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (F3)
106	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (F4)
107	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (F5)
108	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (F6)
109	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (F7)
110	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (F8)
111	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (-)
112	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (-)
113	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (-)
114	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (CLR INS)
115	DOP2IKF013A	ERAK	N	C	スイッチ	Key top (ESC)
116	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (1#)
117	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (1#)
118	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (2#)
119	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (2#)
120	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (3#)
121	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (3#)
122	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (4#)
123	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (4#)
124	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (5#)
125	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (5#)
126	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (6#)
127	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (6#)
128	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (-)
129	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (-)
130	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (-)
131	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (DEL BS)
132	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (TAB)
133	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (Q#)
134	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (Q#)
135	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (W#)
136	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (W#)
137	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (E#)
138	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (E#)
139	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Japan only) (R#)
140	DOP8N3C123005	ERAK	N	C	スイッチ	Key top (Export) (R#)

キーボードユニット (Key board unit)

10 キーボードユニット



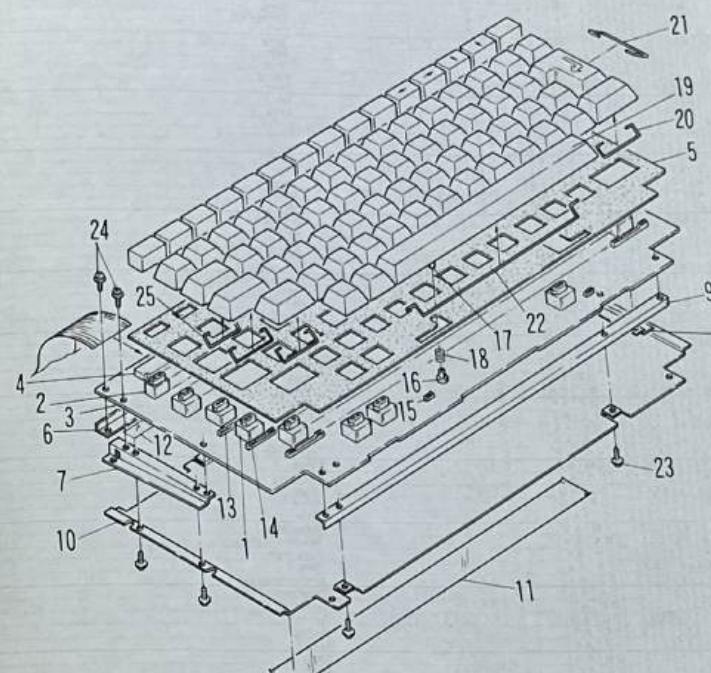
10 キーボードユニット (Key board unit)

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NO.	PARTS CODE	ITEM	ITEM RANK	DESCRIPTION
1	DOPF8N1C01018	EA AK N C	1	キー - ブコナイヨウ Key top (Japan only) (Y)
2	DOPF8N1C01025	EA AK N C	2	キー - ブコナイヨウ Key top (Export) (1)
3	DOPF8N1C01019	EA AK N C	3	キー - ブコナイヨウ Key top (Japan only) (Y)
4	DOPF8N1C01057	EA AK N C	4	キー - ブコナイヨウ Key top (Export) (Y)
5	DOPF8N1C01020	EA AK N C	5	キー - ブコナイヨウ Key top (Japan only) (U)
6	DOPF8N1C01068	EA AK N C	6	キー - ブコナイヨウ Key top (Japan only) (U)
7	DOPF8N1C01022	EA AK N C	7	キー - ブコナイヨウ Key top (Japan only) (L)
8	DOPF8N1C01073	EA AK N C	8	キー - ブコナイヨウ Key top (Export) (1)
9	DOPF8N1C01023	EA AK N C	9	キー - ブコナイヨウ Key top (Japan only) (D)
10	DOPF8N1C01024	EA AK N C	10	キー - ブコナイヨウ Key top (Japan only) (D)
11	DOPF8N1C01074	EA AK N C	11	キー - ブコナイヨウ Key top (Japan only) (P)
12	DOPF8N1C01075	EA AK N C	12	キー - ブコナイヨウ Key top (Japan only) (P)
13	DOPF8N1C01076	EA AK N C	13	キー - ブコナイヨウ Key top (Export) (W)
14	DOPF8N1C01077	EA AK N C	14	キー - ブコナイヨウ Key top (Japan only) (W)
15	DOPF8N1C01078	EA AQ N C	15	キー - ブコナイヨウ Key top (Export) (W)
16	DOPF8N1C01079	EA AK N C	16	キー - ブコナイヨウ Key top (CTRI)
17	DOPF8N1C01070	EA AK N C	17	キー - ブコナイヨウ Key top (Japan only) (A)
18	DOPF8N1C01027	EA AK N C	18	キー - ブコナイヨウ Key top (Export) (A)
19	DOPF8N1C01075	EA AK N C	19	キー - ブコナイヨウ Key top (Japan only) (S)
20	DOPF8N1C01028	EA AK N C	20	キー - ブコナイヨウ Key top (Export) (S)
21	DOPF8N1C01076	EA AK N C	21	キー - ブコナイヨウ Key top (Japan only) (D)
22	DOPF8N1C01029	EA AK N C	22	キー - ブコナイヨウ Key top (Export) (D)
23	DOPF8N1C01077	EA AK N C	23	キー - ブコナイヨウ Key top (Japan only) (F)
24	DOPF8N1C01078	EA AK N C	24	キー - ブコナイヨウ Key top (Export) (F)
25	DOPF8N1C01079	EA AK N C	25	キー - ブコナイヨウ Key top (Japan only) (G)
26	DOPF8N1C01031	EA AK N C	26	キー - ブコナイヨウ Key top (Japan only) (G)
27	DOPF8N1C01071	EA AK N C	27	キー - ブコナイヨウ Key top (Japan only) (H)
28	DOPF8N1C01032	EA AK N C	28	キー - ブコナイヨウ Key top (Japan only) (H)
29	DOPF8N1C01082	EA AK N C	29	キー - ブコナイヨウ Key top (Japan only) (J)
30	DOPF8N1C01033	EA AK N C	30	キー - ブコナイヨウ Key top (Export) (J)
31	DOPF8N1C01081	EA AK N C	31	キー - ブコナイヨウ Key top (Japan only) (K)
32	DOPF8N1C01084	EA AK N C	32	キー - ブコナイヨウ Key top (Export) (K)
33	DOPF8N1C01082	EA AK N C	33	キー - ブコナイヨウ Key top (Japan only) (L)
34	DOPF8N1C01035	EA AK N C	34	キー - ブコナイヨウ Key top (Japan only) (L)
35	DOPF8N1C01083	EA AK N C	35	キー - ブコナイヨウ Key top (Export) (L)
36	DOPF8N1C01036	EA AK N C	36	キー - ブコナイヨウ Key top (Japan only) (L)
37	DOPF8N1C01084	EA AK N C	37	キー - ブコナイヨウ Key top (Export) (L)
38	DOPF8N1C01085	EA AK N C	38	キー - ブコナイヨウ Key top (Japan only) (L)
39	DOPF8N1C01086	EA AK N C	39	キー - ブコナイヨウ Key top (Export) (L)
40	DOPF8N1C01088	EA AK N C	40	キー - ブコナイヨウ Key top (Japan only) (Z)
41	DOPF8N1C01089	EA AK N C	41	キー - ブコナイヨウ Key top (Export) (Z)
42	DOPF8N1C01087	EA AK N C	42	キー - ブコナイヨウ Key top (Japan only) (X)
43	DOPF8N1C01040	EA AK N C	43	キー - ブコナイヨウ Key top (Export) (X)
44	DOPF8N1C01088	EA AK N C	44	キー - ブコナイヨウ Key top (Japan only) (C)
45	DOPF8N1C01041	EA AK N C	45	キー - ブコナイヨウ Key top (Export) (C)
46	DOPF8N1C01089	EA AK N C	46	キー - ブコナイヨウ Key top (Japan only) (Y)
47	DOPF8N1C01042	EA AK N C	47	キー - ブコナイヨウ Key top (Export) (Y)
48	DOPF8N1C01080	EA AK N C	48	キー - ブコナイヨウ Key top (Japan only) (B)
49	DOPF8N1C01043	EA AK N C	49	キー - ブコナイヨウ Key top (Export) (B)
50	DOPF8N1C01091	EA AK N C	50	キー - ブコナイヨウ Key top (Japan only) (N)
51	DOPF8N1C01044	EA AK N C	51	キー - ブコナイヨウ Key top (Export) (N)
52	DOPF8N1C01092	EA AK N C	52	キー - ブコナイヨウ Key top (Japan only) (M)
53	DOPF8N1C01045	EA AK N C	53	キー - ブコナイヨウ Key top (Export) (M)
54	DOPF8N1C01093	EA AK N C	54	キー - ブコナイヨウ Key top (Japan only) (< , >)
55	DOPF8N1C01046	EA AK N C	55	キー - ブコナイヨウ Key top (Export) (< , >)
56	DOPF8N1C01094	EA AK N C	56	キー - ブコナイヨウ Key top (Japan only) (< , >)
57	DOPF8N1C01047	EA AK N C	57	キー - ブコナイヨウ Key top (Export) (< , >)
58	DOPF8N1C01095	EA AK N C	58	キー - ブコナイヨウ Key top (Japan only) (< , >)
59	DOPF8N1C0123004	EA AQ N C	59	キー - ブ Key top (SHIFT) Key top (CAPS)
60	DOPF8N1C0123008	EA AK N C	60	キー - ブ Key top (Japan only) (ALT)
61	DOPD2K003802	EA AK N C	61	キー - ブコナイヨウ Key top (Export) (ALT)
62	DOPF8N1C0123007	EA AK N C	62	キー - ブコナイヨウ Key top (Japan only) (-)
63	DOPF8N1C0123048	EA AK N C	63	キー - ブコナイヨウ Key top (Japan only) (-)
64	DOPF8N1C0123009	EA AK N C	64	キー - ブコナイヨウ Key top (Japan only) (-)
65	DOPF8N1C0123009	EA AK N C	65	キー - ブコナイヨウ Key top (Japan only) (-)
66	エントリ			
67	DUNT-7555CCZZ	LV BN	E	キーボードユニット JIS Key board unit (Japan)
68	DUNT-7394CCZZ	LV BN	E	キーボードユニット ASCII Key board unit (Except Japan & U.K.)
69	DUNT-7717CCZZ	LV BN	E	キーボードユニット ASCII Key board unit (U.K.)

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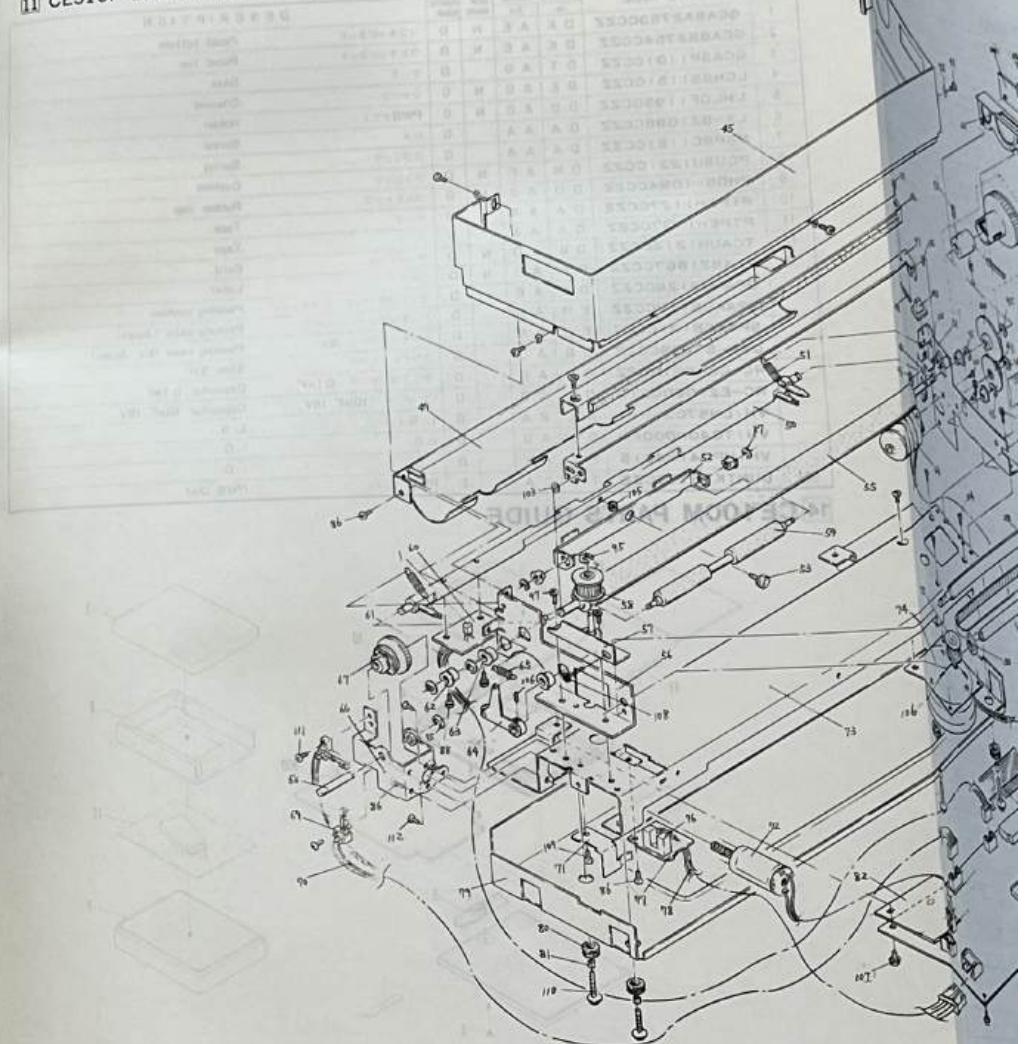
10 キーボードユニット (Key board unit)



II CE510P 機構部 (CE510P Mechanical parts)

NO.	PARTS CODE	PRICE RANK J1 E2	NEW PART MARK	PART RANK	DESCRIPTION
85	XBP5C23P03000	DA AA	C	ビス	Screw
86	XBP5D10P03K50	DA AA	C	ビス	Screw
87	XRESPL50	DA AA	C	ビス	Screw
88	XBPSD10P03K50	DA AA	C	ビス	Screw
89	XBPSD10P03K50	DA AA	C	ビス	Screw
90	XBPSD02-05000	DA AA	C	ワッシャー	Washer
91	XBPSD02-05000	DA AA	C	ビス	Screw
92	XWNP-0202P03000	DA AA	C	ビス	Screw
93	XXXSP10P03075	DA AA	C	ビス	Screw
94	XRESPL50	DA AA	C	ビス	Screw
95	XRESPL50-04000	DA AA	C	ビス	Screw
96	XRESPL50-04000	DA AA	C	ビス	Screw
97	XRESPL50-04000	DA AA	C	ビス	Screw
98	XBPSD03P03K50	DA AA	C	ビス	Screw with washer and spring washer
99	XBPSD03P03K50	DA AA	C	ビス	Washer
100	LX-B216CCZ2	DA AA	C	ビス	Screw
101	XBS5D24P03000	DA AA	C	ビス	Screw
102	LX-WZ1011CCZ2	DA AA	C	ワッシャー	Washer
103	LX-WZ5001BCZ2	DA AA	C	ワッシャー	Washer
104	XBS5D10P05000	DA AA	C	ビス	Screw
105	LX-S1011HCZ2	DA AA	C	ワッシャー	Washer
106	XXXSP10P03000	DA AA	C	ビス	Screw
107	XBPSD02P03000	DA AA	C	ビス	Screw
108	XBPSD02P03000	DA AA	C	ビス	Screw
109	XBPSD02P03K50	DA AA	C	ビス	Screw with washer and spring washer
110	XBPSD02P03K50	DA AA	C	ビス	Washer
111	XBPSD10P03K50	DA AA	C	ビス	Screw
112	LX-B216CCZ2	DA AA	C	ビス	Screw
113	VRO-2728Y222J	DA AA	C	ダイコク	Resistor (1.8W 2.2KΩ ±5%)
114	VRO-2728Y333J	DA AA	C	ダイコク	Resistor (1.8W 3.3KΩ ±5%)
115	VRO-2728Y333J	DA AA	C	ダイコク	Resistor (1.8W 3.3KΩ ±5%)
116	VRO-2728Y512J	DA AA	C	ダイコク	Resistor (1.8W 5.1KΩ ±5%)
201	CRBN11014C5F	D	リボンケーブル (日本語)		ribbon cable (Japanese only)
202	GCOV1181CCZ2	DS AB	D	プリントカバー	Printer cover
203	GCOV1181CCZ2	EV AR	D	プリントカバー	Printer cover
204	TINSM4928CCZ2		D	トランザクションマニュアル (英語)	Transaction manual (English)
			D	トランザクションマニュアル (日本語)	Transaction manual (Japanese)
205	UKGOD1004CCZ2	DW AH	D	ドライバ (L型)	Driver (+ -)
206	UKGDL1057CCZ2	DK AE	D	ドライバレンチ	Wrench
207	SPAKA1180CCZ2	FC AS	D	パッキンクラシナー	Packing cushion
208	SPAKA1180CCZ2	FC AS	D	パッキンクラシナー	Packing cushion
209	SPAKA8335CCZ2	DH AE	D	パッキンクラシナー	Packing cushion
210	SPAKA8335CCZ2	DB AB	D	パッキンクラシナー	Packing case (Japan)
211	SPAKC8120CCZ2	EB AL	D	パッキンケース (英語)	Packing case (English)
212	SPAKC8120CCZ2	EC AL	D	パッキンケース (日本語)	Packing case (Japanese)

II CE510P 機構部 (CE510P Mechanical parts)



II CE510P 機構部 (CE510P Mechanical parts)

NO	PARTS CODE	PRICE RANK	NEW PART MARK	DESCRIPTION
1	VHPDZL2B/-	D Y AH	B	フォトダイオダブスター
2	QWPBE2220CCZ	D A AA	C	RE- PWBモジュール RE- sensor PWB
3	LHLDZ1188CCZ	D C AB	C	センサー
4	PLTM1001CCZ	D A AA	C	RE- PWBモジュール
5	PLTM1001CCZ	D A AA	C	リボルバセード
6	CHEDZ1101CCZ	D A AA	C	リボルバモータ
7	CHLDZ1189CCZ	G A Y	C	リボルバモータ
8	MSPRC1246CCZ	D B AB	C	スプリング
9	CSL12024CC9	F U AX	C	キャリッジユニット
10	CSL12024CC9	F U AX	C	カートリッジユニット
11	MSPRP1001CCZ	D B AB	C	シリンダー
12	NSFTZ1053CCZ	D A AA	C	シグニオサ
13	MSPRC1232CCZ	D B AB	C	スプリング
14	LSHZ1109CCZ	D D AB	C	ゲイターリング
15	NROL1P1023CCZ	D E AC	C	ペーパーローラー
16	NGERZ1303CCZ	D A AA	C	ギア
17	NGERZ1303CCZ	D G AC	C	ギヤドライブユニット
18	NSFTZ1037CCZ	D B AB	C	スプリング
19	CPYLC1101CC9	D F AB	C	シャフト
20	NGERZ1232CCZ	D W AB	C	ギヤー
21	PFLT-1056CCZ	D B AB	C	ボルト
22	PTNPT101CCZ	D A AA	C	角度
23	MSPRC1221CCZ	D R AB	C	スプリング
24	NSFTZ1056CCZ	D X AH	C	セイリング
25	GTAF11297CCZ	D B AB	C	カプラ
26	LSHZ11063CCZ	D B AB	C	リード
27	NSFTZ1056CCZ	F T AT	C	ギヤ
28	NBLTM1066CCZ	E C AL	C	ベルト
29	NSFTZ1057CCZ	E F AM	C	ギヤドライブ
30	PGUMR1487CCZ	D C AC	C	ストップゴム
31	GTAS1004CC9	E C AL	C	ガイドユニット
32	DUINT1001CCZ	D A AA	C	ガイドユニット
33	QWPBL1001CCZ	D A AA	C	ガイドユニット
34	QWPBL1055CCZ	D A AB	C	ガイドユニット
35	QNCW1327CC9	D F AD	C	VTR PWB
36	DUINT1040CCZ	D W AH	C	ホルダ
37	NGERZ1104CCZ	D C AC	C	メカニズム
38	NGERZ1105CCZ	D B AB	C	PF ギア
39	MLEVT1041CCZ	D T AG	C	PF ギア
40	JXBNBZ11857CCZ	D A AA	C	リリースレバー
41	CMOTA1007CC9	G U BB	B	リリースモード
42	NROL1P1025CCZ	D C AS	C	セーフティフレーム
43	LANGR11515CCZ	D K AE	C	チャージング
44	MSPRC1230CCZ	D B AB	C	チャージャーモジュール
45	PG10M1034CCZ	E N AP	C	ペーパーガード
46	CSFTZ1067CC9	G M BB	C	PKシングル
47	MSPRC1277CCZ	D C AC	C	スプリング
48	LANGK11514CCZ	D F AD	C	PRアンブル
49	LX-BZ1102CCZ	D R AG	C	ビス
50	NROL1P1025CCZ	E C AL	C	セーフティ
51	NSR1024CCZ	F M AV	C	ゴムローラー
52	CF10097CCZ	D X AH	C	ゴムローラー
53	ANOKR1101CCZ	D N AT	C	ゴムローラー
54	NPLYD1010CCZ	F M IV	C	ゴムローラー
55	QCNW11751CCZ	D Z AK	C	ゴムローラー
56	QFWBL21218CCZ	D A AA	C	ペーパーリミッタ
57	QCNW1327CCZ	D F AD	C	コネクター
58	LSHZ1101CCZ	D C AC	C	ギヤアシスト
59	LSHZ1102CCZ	D C AC	C	ギヤアシスト
60	CLEVF1042CC9	D Z AK	C	ギヤアシスト
61	MSPRC1225CCZ	D B AB	C	ギヤアシスト
62	CMOTM1008CC9	D M AP	C	ギヤアシスト
63	QCNW1328CCZ	D J AE	C	ギヤアシスト
64	QCNW1329CCZ	D J AE	C	ギヤアシスト
65	MSPRC1233CCZ	D B AB	C	ギヤアシスト
66	LANGK11012CCZ	D J AE	C	ギヤアシスト
67	MCAMP1106CCZ	D C AB	C	ウォームキール カム
68	NSFTZ1053CCZ	D H AE	C	ウォームキール シフ
69	QSW-M1354CCZ	D F AD	B	マイクロスイッチ
70	QCNW1329CCZ	D J AE	C	コネクター
71	MSPRF1233CCZ	D B AB	C	エラストワスツリ
72	CMOTM1008CC9	F V AX	B	リフトモータユニット
73	G-TAU1005CCZ	E M AP	C	ソフタ
74	CMOTP1009CC9	L Q BN	B	キャリッジモータユニット
75	NPLYD1010CCZ	E A AK	C	キャリッジモーター
76	VHPGP1504//	D Y AK	B	フォトダイオダ
77	QWPBE2219CCZ	D C AB	C	LEセイリング
78	QCNW1328CCZ	D F AD	C	コネクター
79	LCH551145CCZ	F L AU	C	ベースフレーム 2
80	PCUSG1213CCZ	D B AB	C	ゴムフレーム
81	PCLR-1001CCZ	D C AB	C	フックガード
82	PCOVA1029CCZ	D C AB	C	PWBカバー F
83	XBPSD26P19K09	D A AA	C	ビス
84	XBPSD26P04909	D A AA	C	ビス

II CE510P 機構部 (CE510P Mechanical parts)

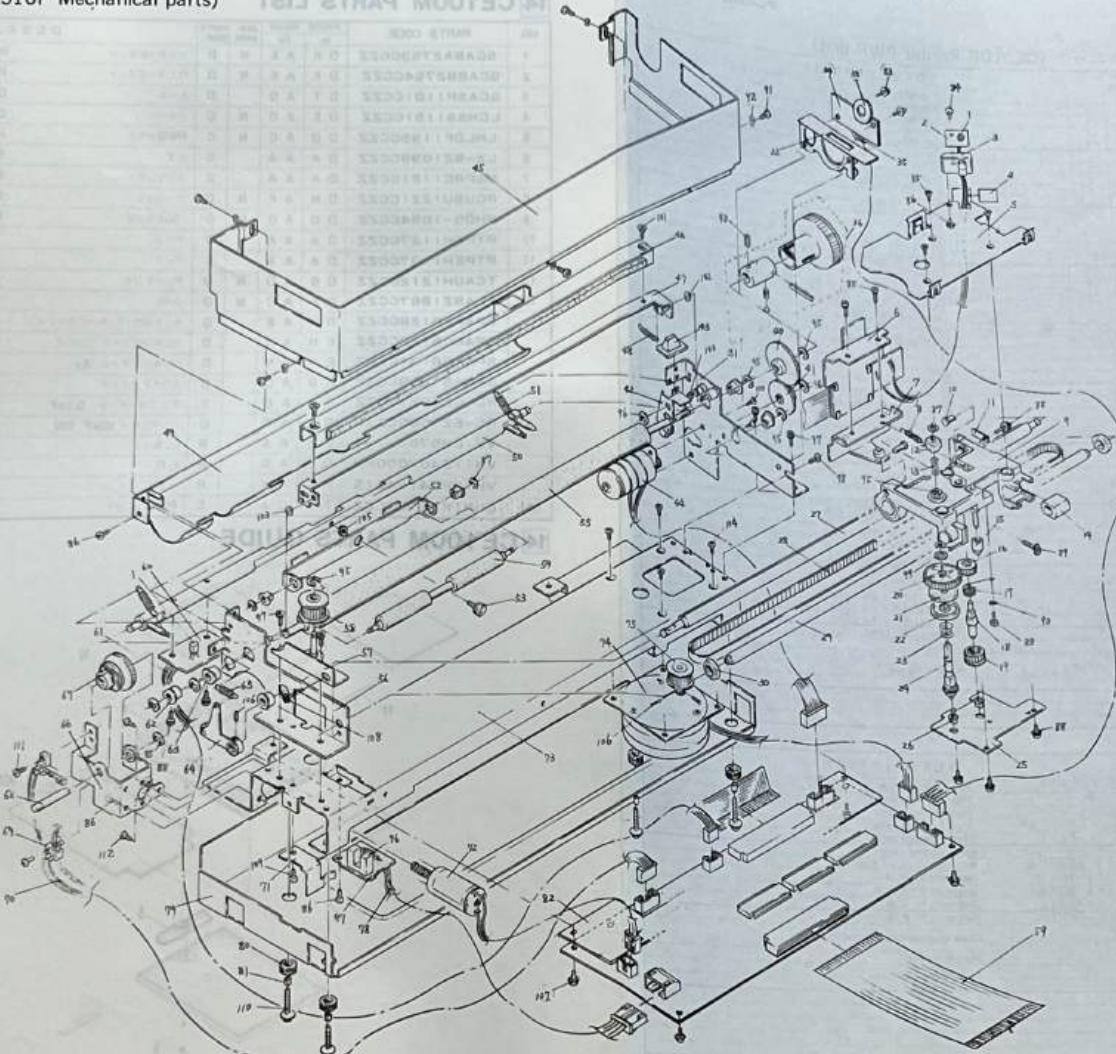
NO	PARTS CODE	PRICE RANK	NEW PART MARK	DESCRIPTION
81	KHSSC10P06E003	D A AA	C	Screw
82	KBPSD10P06K005	D A AA	C	E type ring
83	SPAKS13-04900	D A AA	C	Screw
84	KHSD10P06K000	D A AA	C	Screw
85	KBPSD10P06K000	D A AA	C	Screw
86	KWHD1D20-1500	D A AA	C	ワッシャー
87	KWHD1D20-1500	D A AA	C	Screw
88	KWHD1D20-1500	D A AA	C	ワッシャー
89	KWHD1D20-1500	D A AA	C	Screw
90	KWHD1D20-1500	D A AA	C	ワッシャー
91	KWHD1D20-1500	D A AA	C	Screw
92	KWHD1D20-1500	D A AA	C	ワッシャー
93	KWHD1D20-1500	D A AA	C	Screw
94	KWHD1D20-1500	D A AA	C	E type ring
95	KWHD1D20-1500	D A AA	C	E type ring
96	KWHD1D20-1500	D A AA	C	Screw
97	KBPSD10P14K002	D A AA	C	Screw with washer and spring washer
98	XBPSD26P14K002	D A AA	C	Washer
99	XW-2116216CCZ	D A AA	C	Screw
100	XW-2116216CCZ	D A AA	C	Washer
101	XW-2116216CCZ	D A AA	C	Washer
102	XW-2116216CCZ	D A AA	C	Washer
103	LX-W255010BCZ	D A AA	C	ワッシャー
104	XBPSD10P15E000	D A AA	C	Washer
105	LX-W211611HCZ	D A AA	C	ワッシャー
106	XXXSP76L1404006	D A AA	C	Screw
107	XBPSD26P15K005	D A AA	C	Screw
108	XBPSD26P15K005	D A AA	C	Screw with washer and spring washer
109	XBPSD26P15K005	D A AA	C	Screw
110	XBT5050P08E000	D A AA	C	Screw
111	LX-Z11616CCZ	D A AA	C	ビス
112	LX-B211616CCZ	D A AA	C	ビス
113	VRD-ST10Y22J	D A AA	C	Resistor (L-BW 2.2KΩ ±5%)
114	VRD-ST10Y22J	D A AA	C	Resistor (L-BW 3.3KΩ ±5%)
115	VRD-ST10Y22J	D A AA	C	Resistor (L-BW 4.7KΩ ±5%)
116	VAD-212BY47J	D A AA	C	Resistor (L-BW 5.1KΩ ±5%)
201	CRBN11116GF	Z A	S	Ribbon cassette unit (Japan only)
202	GC0VAL1810CGZ	D S AG	D	Printer cover
203	GC0VA1382CCZ	E V AR	D	Printer cover
204	TINSM4028CCZ	D	D	トリアゴラセイツイシヨウ (イギヤク) Instruction book (Export)
	TINSM4028CCZ	D	D	トリアゴラセイツイシヨウ (コナイヨウ) Instruction book (Japan)
205	UKGOD1006E002	DW AH	D	ドライバー (+)
206	UQGL1006E002	D W AE	D	ローラ
207	SPAKA81119CCZ	D G AS	D	パッキンテープ
208	SPAKA81119CCZ	D G AD	D	パッキンテープ
209	SPAKA8315CCZ	D H AE	D	パッキンテープ
210	SPAKA8336CCZ	D B AB	D	パッキンテープ
211	SPAKC8128CCZ	E B AL	D	パッキンテープ (トクトク)
212	SPAKC8122CCZ	E C AL	D	パッキンテープ (カイガイヨウ)

OPTION

11 CE510P 機構部 (CE510P Mechanical parts)

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12 CE510P プリンタ基板ユニット (CE510P Printer PWB unit)

NO	PARTS CODE	PRICE RANK Jp Ex	NEW PART MARK RANK	DESCRIPTION
1	QCNM1133CC00	D 9 A B	C	コネクター Connector
2	QCNM1133CC08	D A A A	C	コネクター Connector
3	QCNM1133CC09	D A A A	C	コネクター Connector
4	QCNM1133CC0D	D A A A	C	コネクター Connector
5	QCNM1133CC0E	D B A B	C	コネクター Connector
6	QCNM1133CC0F	D B A B	C	コネクター Connector
7	QCNW1133CC30	E F A M	C	コネクター Connector
8	RC-C21021CC22	D B A B	C	コンデンサー Capacitor (0.1μF)
9	RC-C21021CC22	D B A B	C	コンデンサー Capacitor (0.1μF)
10	RC-C21021CC22	D B A B	C	コンデンサー Capacitor (0.1μF)
11	RC-C21048CC22	D B A B	C	コンデンサー Capacitor (0.022μF)
12	RC-C21058CC22	D B A B	C	コンデンサー Capacitor
13	RC-C21091CC22	D B A B	C	コンデンサー Capacitor
14	RC-C21098CC22	D B A B	C	コンデンサー Capacitor
15	RH-TC45186CCZ	D G A T	B	クリスタル Crystal (4.9152MHz)
16	RH-D21085CCZ	D D A C	B	ブリッジダイオード Diode (DAP202)
17	RH-D21085CCZ	D D A C	B	ブリッジダイオード Diode (DAN202)
18	RH-TX1083CCZ	D D A C	B	トランジスター Transistor (2SB815-B6)
19	RH-TX1083CCZ	D D A C	B	トランジスター Transistor (2SC2813 LS)
20	YGEAUU1AW107Q	D B A B	C	コンデンサー Capacitor (10WV 100pF)
21	VCEA1CE195K	D H A D	C	コンデンサー Capacitor (16WV 10pF)
22	VESATU1CE475K	D H A D	C	コンデンサー Capacitor (16WV 4.7pF)
23	VH1BA511L	F N	B	コンデンサー Capacitor
24	VH1BA521L	D Z A K	B	コンデンサー Capacitor
25	VH1BA531U	L C A L	B	IC
26	VH1MY853//-/	F A A R	B	IC
27	VH1MY853//-/	E H A N	B	IC
28	VH1MY853//-/	E N A P	B	IC
29	VH1TC45186CCZ	E N A P	B	IC
30	VH1TC45186CCZ	E N A P	B	IC
31	VH1TC45186CCZ	D R A F	B	IC
32	VH1TC45186CCZ	E S A Q	B	IC
33	VH1TC45186BF-1	F K A N	B	IC
34	VH1TC5517AF-7	G C A Z	B	LSI
35	VH1SC885G//-/	G Y B E	B	LSI
36	VRD-S728Y152J	D A A A	C	ダイオード Diode
37	VRS-TP2BD0182J	D A A A	C	ダイオード Diode
38	VRS-TP2BD0182J	D A A A	C	ダイオード Diode
39	VRS-TP2BD0184J	D A A A	C	ダイオード Diode
40	VRS-TP2BD0153J	D A A A	C	ダイオード Diode
41	VRS-TP2BD0222J	D A A A	C	ダイオード Diode
42	VRS-TP2BD0273J	D A A A	C	ダイオード Diode
43	VRS-TP2BD332J	D A A A	C	ダイオード Diode
44	VRS-TP2BD471J	D A A A	C	ダイオード Diode
45	VRS-TP2BD473J	D A A A	C	ダイオード Diode
46	VRS-TP2BD683J	D A A A	C	ダイオード Diode
47	VSHA181//-/	D B A B	B	トランジスター Transistor
901	DUNTK7780CCZZ	U D C B	E	プリンタ基板ユニット Printer PWB unit

13 治工具 (Tool)

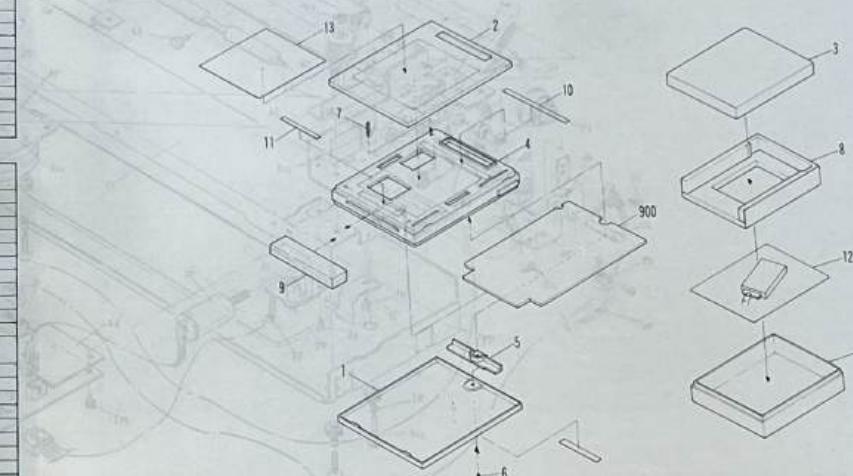
NO	PARTS CODE	PRICE RANK Jp Ex	NEW PART MARK RANK	DESCRIPTION
1	UK0GG0082CS2Z	E C A L	N	4ビン エニコネクターブル 4pin Extension cable
2	UK0GG0083CS2Z	F W A X	N	16ビン エニコネクターブル 16pin Extension cable
3	UK0GG0084CS2Z	G H B A	N	26ビン エニコネクターブル 26pin Extension cable
4	UK0GG0085CS2Z	E W A R	N	37ビン エニコネクターブル 37pin Extension cable
5	UK0GG00886CS2Z	F F A S	N	34ビン エニコネクターブル 34pin Extension cable
6	UK0GG0087CS2Z	D V A H	N	6ビン エニコネクターブル 6pin Extension cable
7	UK0GG00888CS2Z	H B B F	N	レバートップ ROM用 ICソケット 28pin Lev-top top P-ROM IC socket 28pin
8	UK0GCJ095CS2Z	H Y B K	N	シエラリオ P-ROM (A) Sierra Rio P-ROM (A)
9	UK0GCJ095CS01	H Y B K	N	シエラリオ P-ROM (B) Sierra Rio P-ROM (B)
10	UK0GCJ095CS02	H Y B K	N	シエラリオ P-ROM (L) Sierra Rio P-ROM (L)
11	UK0GCJ095CS03	H Y B K	N	シエラリオ P-ROM (D) Sierra Rio P-ROM (D)
12	UK0GCJ008CS2Z	V R * * N	E	ランサモ Check program bubble cassette
13	QS0CZ6428ACZZ	D L A E	C	28ビン ICノケット 28pin IC socket

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NO	PARTS CODE	PRICE RANK Jp Ex	NEW PART MARK RANK	PARTS RANK	DESCRIPTION
1	GCABA2753CCZZ	D K A E	N	D	ノコキナビネット Panel bottom
2	GCABBB2754CCZZ	D K A E	N	D	エキナビネット Panel top
3	GCASPI101CCZZ	D T A D	O	D	カース Case
4	LCH551151CCZZ	D E A C	N	O	シャープ Holder
5	LHLOFI1195CCZZ	D D A C	N	O	PWBオサエ Screw
6	LX-BZ1098CCZZ	D A A A	O	O	ビス Screw
7	MSPRC1181CCZZ	D A A A	O	C	スプリング Spring
8	PCUSU1221CCZZ	D N A F	N	D	クッション Cushion
9	PHDG-1094CCZZ	D D A C	N	O	ゴムキャップ Rubber cap
10	PTPEHI127CCZZ	D A A A	O	C	テープ Tape
11	PTPEHI137CCZZ	D A A A	O	C	テープ Tape
12	TCAUH1212CCZZ	D G A D	N	D	チュイシ Label
13	TLABZ1867CCZZ	D E A C	N	D	セッショウパッキングクッション Packing cushion
	SPAKA8128CCZZ	D K A E	D	D	セッショウパッキングクッション Packing case (Japan)
	SPAKCB129CCZZ	E H A N	D	D	パッキングケース (日本) Packing case (Japan)
	SPAKCB131CCZZ	E H A N	D	D	パッキングケース (Ex.) Packing case (Ex. Japan)
	QSW-S1359CCZZ	D G A D	B	B	スライドスイッチ Slide-SW
	RC-CZ1021CCZZ	D B A B	C	C	チップコンデンサー 0.1μF Capacitor 0.1μF
	RC-EZ106DCCIC	D C A B	O	B	コンデンサー 10μF 16V Capacitor 10μF 16V
	VH1LH5703/-/1	O K B A	B	L.S.	L.S.
	VH1TC40H000FN	D S A G	B	I.C.	I.C.
	VH1UPD4164G15	F Z A Y	B	I.C.	I.C.
901	DUNTK7780CCZZ	T Y C A	E	PWB Unit	PWB Unit

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