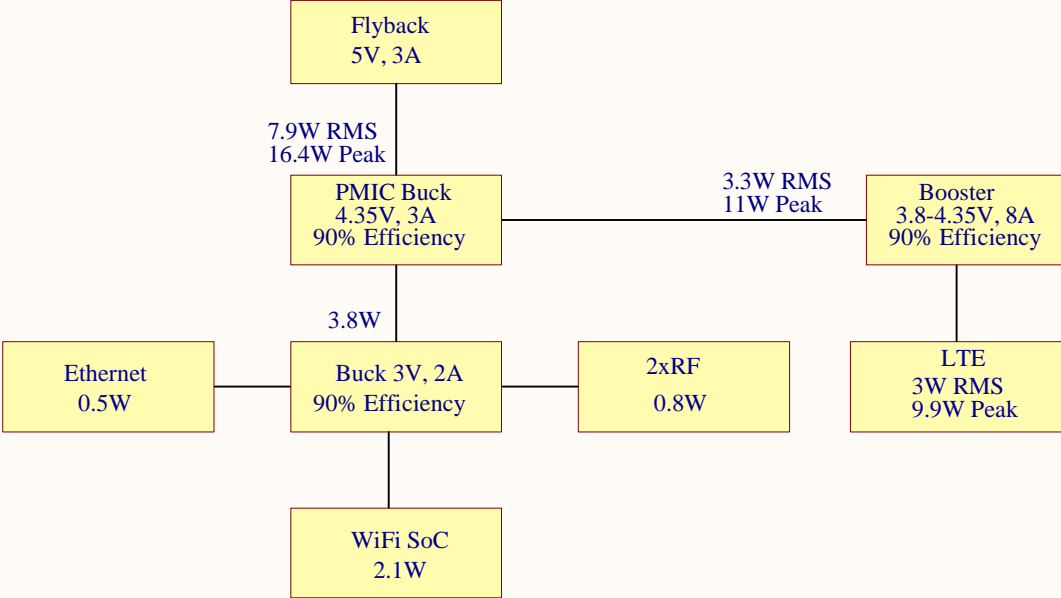
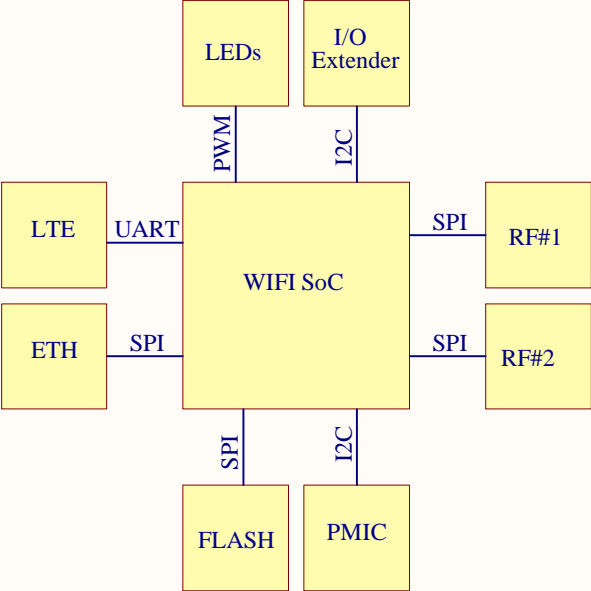
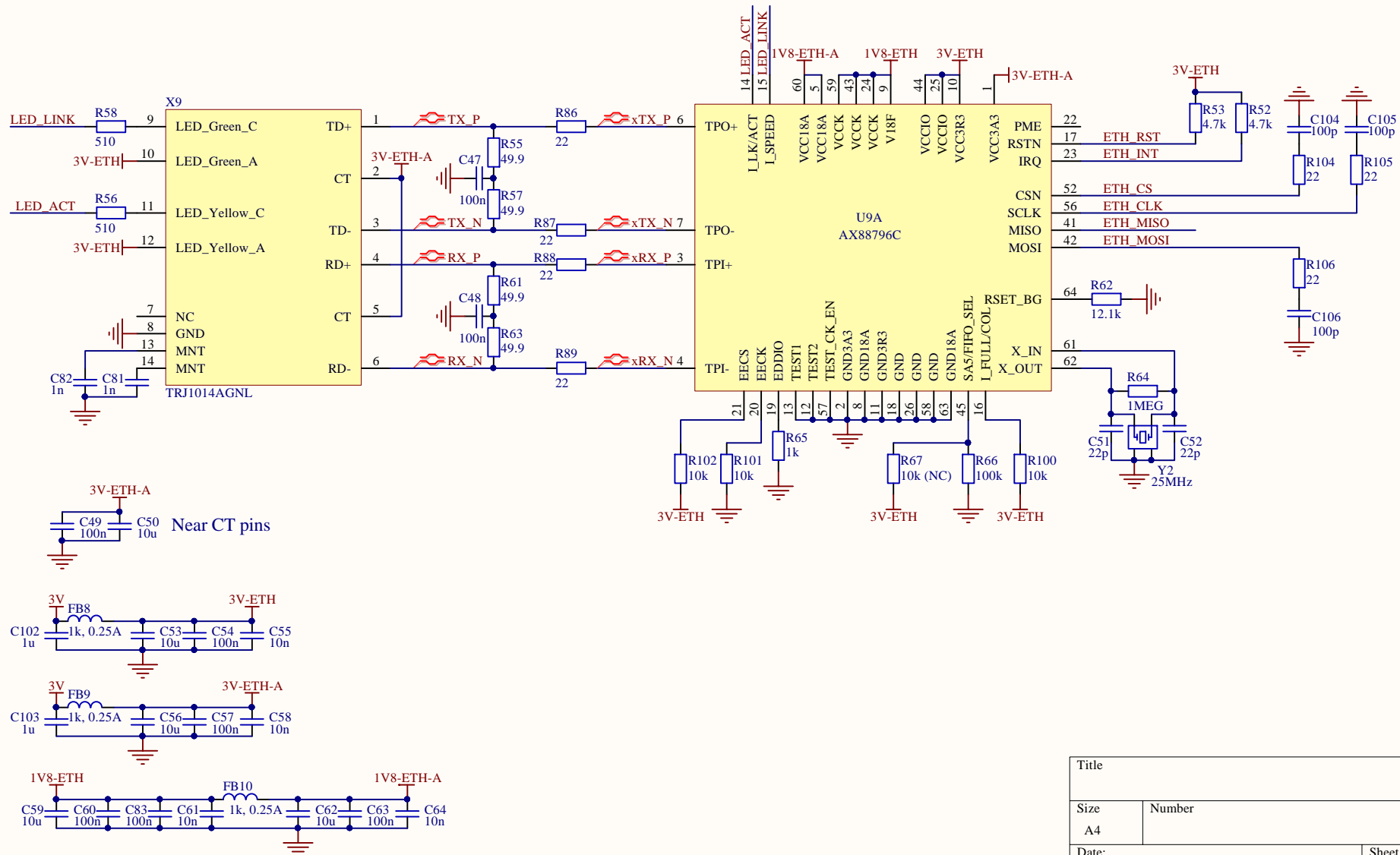


BLOCK DIAGRAM



Title		
Size A4	Number	Revision
Date:	Sheet of	
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ETHERNET



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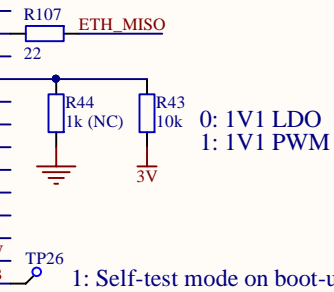
INTERFACES

U6B

PA0/MIC_BIAS/I2S_SD_RX/QDEC_IDX/SGPIO/BT_UART_RTS/ANT_SEL_P	4	JWL01_RDIO0
PA1/MIC2_N/I2S_SD_TX0	7	JWL02_RDIO2
PA2/MIC2_P/I2S_CLK/QDEC_PHB/SGPIO_OUT/BT_UART_TXD/TRSW_P	6	JWL02_RDIO4
PA4/MIC1_P/I2S_WS/QDEC_PHA/BT_UART_RXD/TRSW_N	5	JWL01_RDIO2
PA5/AUXIN_L/SD_WP/TRSW_P	8	JWL01_RDIO4
PA6/AUXIN_R/SD_CD/TRSW_N	9	JWL02_RFSW
PA9	30	JWL02_RDIO0
PA10	31	JWL02_RDIO5
PA11	32	TAMPER
PA12/LP_UART_TXD/SPI1_MOSI/HS_PWM0/LP_PWM0/I2S_MCLK/ANT_SEL_N/GRANT_BT/EN_EXLNA/KEY_ROW0/LGPIO0	33	JWL02_MOSI
PA13/LP_UART_RXD/SPI1_MISO/HS_PWM1/LP_PWM1/I2S_SD_TX1/ANT_SEL_P/GRANT_BT_N/EN_EXPA/KEY_ROW1/LGPIO1	34	JWL02_MISO
PA14/LP_UART_RTS/SPI1_CLK/I2S_SD_TX2/ANT_SEL_N/SICK_BT_DIS/RTC_OUT/KEY_ROW2/LGPIO2	35	JWL02_SCK
PA15/LP_UART_CTS/SPI1_CS/ANT_SEL_P/SIDD/BT_WAKE_HOST/RTC_EXT_32K/KEY_ROW3/KEY_COL6/LGPIO3	36	JWL02_NSS
PA16/HS_UART0_RTS/SPI0_MOSI/BT_FW_LOG_TXD/ANT_SEL_N/HOST_WAKE_BT/KEY_ROW4/KEY_COL5	37	JWL01_MOSI
PA17/HS_UART0_CTS/SPI0_MISO/ANT_SEL_P/BT_CLK_REQ/KEY_ROW6/KEY_COL3	38	JWL01_MISO
PA18/HS_UART0_TXD/SPI0_CLK/JTAG_CLK/MBOX_I2C_SDA/RTC_OUT/KEY_ROW5/KEY_COL4	39	JWL01_SCK
PA19/HS_UART0_RXD/SPI0_CS/LCD_D0/JTAG_TRST/MBOX_I2C_SCL/KEY_COL2	40	JWL01_NSS
PA20/LCD_D1/KEY_COL7	41	EXP_INT
PA21/HS_UART0_TXD/HS_USI_UART_RTS/KEY_ROW7	42	LTE_RX
PA22/HS_UART0_RXD/HS_USI_UART_CTS	43	LTE_TX
PA23/HS_USI_UART_TXD/HS_UART0_RTS/HS_USI_I2C_SCL/HS_PWM2/LP_PWM2/LCD_D2	44	PMIC_INT
PA24/HS_USI_UART_RXD/HS_UART0_CTS/HS_USI_I2C_SDA/HS_PWM3/LP_PWM3/LCD_D3	47	ETH_INT
PA25/HSDM/LP_UART_RXD/HS_USI_SPL_MOSI/IR_TX/LP_I2C_SCL/HS_PWM4/LP_PWM4/LCD_D9/BT_I2C_SCL/MBOX_I2C_INT/KEY_COL5	55	ETH_MOSI
PA26/HSDP/LP_UART_TXD/HS_USI_SPL_MISO/IR_RX/LP_I2C_SDA/HS_PWM5/LP_PWM5/LCD_D8/BT_I2C_SDA/BT_ACT/KEY_COL6	54	ETH_CS
PA28/RREF/LP_UART_CTS/HS_USI_SPL_CS/HS_PWM6/LP_PWM6/LCD_D7/BT_CLK	53	ETH_CLK
PA30/VBUS_OTG/SPS_SEL/HS_USI_SPL_CLK/HS_PWM7/LP_PWM1/LCD_D6/EXTBT_UART_RTS	51	ETH_CLK
PA31/LP_I2C_SCL/LCD_D4	49	SCL
PB0/LP_I2C_SDA/LCD_D5	50	SDA
PB1/LP_UART_TXD/DMIC_CLK/SGPIO_OUT/BT_GPIO[1]/ANT_SEL_N/BT_STE/EN_EXLNA/HS_TIM4_TRIG	57	PWR_SW
PB2/ADC_CH5/LP_UART_RXD/DMIC_DATA/SGPIO/BT_GPIO[0]/ANT_SEL_P/PCM_CLK/EN_EXPA/HS_TIM5_TRIG	56	JWL02_RST
PB4/TOUCH_KEY0/ID_OTG/SPI1_MOSI/RTC_EXT_32K/HS_PWM8/LP_PWM2/I2S_SD_TX1/JTAG_TDI/PCM_IN/HS_TIM4_TRIG	59	ON_HOLD
PB5/TOUCH_KEY1/SPI1_MISO/RTC_OUT/LP_I2C_SCL/HS_PWM9/LP_PWM3/I2S_SD_TX2/JTAG_TDO/PCM_OUT/HS_TIM5_TRIG	60	BAT_LOAD
PB6/TOUCH_KEY2/SPI1_CLK/LP_TIM4_TRIG/LP_I2C_SDA/JTAG_TMS/EXTBT_UART_TXD	61	ETH_RST
PB7/TOUCH_KEY3/SPI1_CS/LP_TIM5_TRIG/HS_PWM17/LP_PWM5/BT_LED/EXTBT_UART_RXD	62	LTE_PWR_SW
PB18/HS_UART0_RXD/HS_USI_UART_RTS/SPI0_MOSI/SPL_CS/SD_D2/HS_PWM10/LP_PWM4/SWD_CLK/LCD_D14	77	LED_LOGO_B
PB19/HS_UART0_TXD/HS_USI_UART_CTS/SPI0_MISO/SPL_DATA1/SD_D3/HS_PWM11/LP_PWM5/SWD_DATA/I2S_SD_TX0/LCD_D15	78	LED_LOGO_R
PB20/HS_USI_UART_TXD/HS_UART0_CTS/SPI0_CLK/SPL_DATA0/HS_USI_I2C_SCL/SD_CMD/HS_PWM12/LP_PWM0/I2S_CLK/LCD_VSYNC_TE	79	LED_LOGO_G
PB21/LCD_VSYNC_TE/HS_UART0_RTS/SPI0_CS/SPL_CLK/HS_USI_I2C_SDA/SD_CLK/HS_PWM13/LP_PWM1/I2S_WS/LCD_RS/QDEC_IDX	80	LTE_ON
PB22/ID_OTG/LP_TIM4_TRIG/IR_RX/SPL_DATA3/SD_D0/HS_PWM14/LP_PWM2/I2S_SD_RX/LCD_RD/QDEC_PHB/SGPIO_OUT/EXTBT_UART_CTS	81	VPSU_DET
PB23/LP_TIM5_TRIG/IR_TX/SPL_DATA2/SD_D1/HS_PWM15/LP_PWM3/I2S_MCLK/LCD_WR/QDEC_PHA/SGPIO_OUT/EXT_32K	82	JWL01_RDIO5
PB28/LCD_CS	85	JWL01_RFSW
PB29/IR_RX/I2S_CLK/SGPIO/TRSW_P	84	JWL01_RST
PB30/AOUTN_L	86	PMIC_#CE
PB31/AOUTP_L/IR_TX/I2S_WS/QDEC_PHA/SGPIO/BT_UART_CTS	87	PMIC_STAT

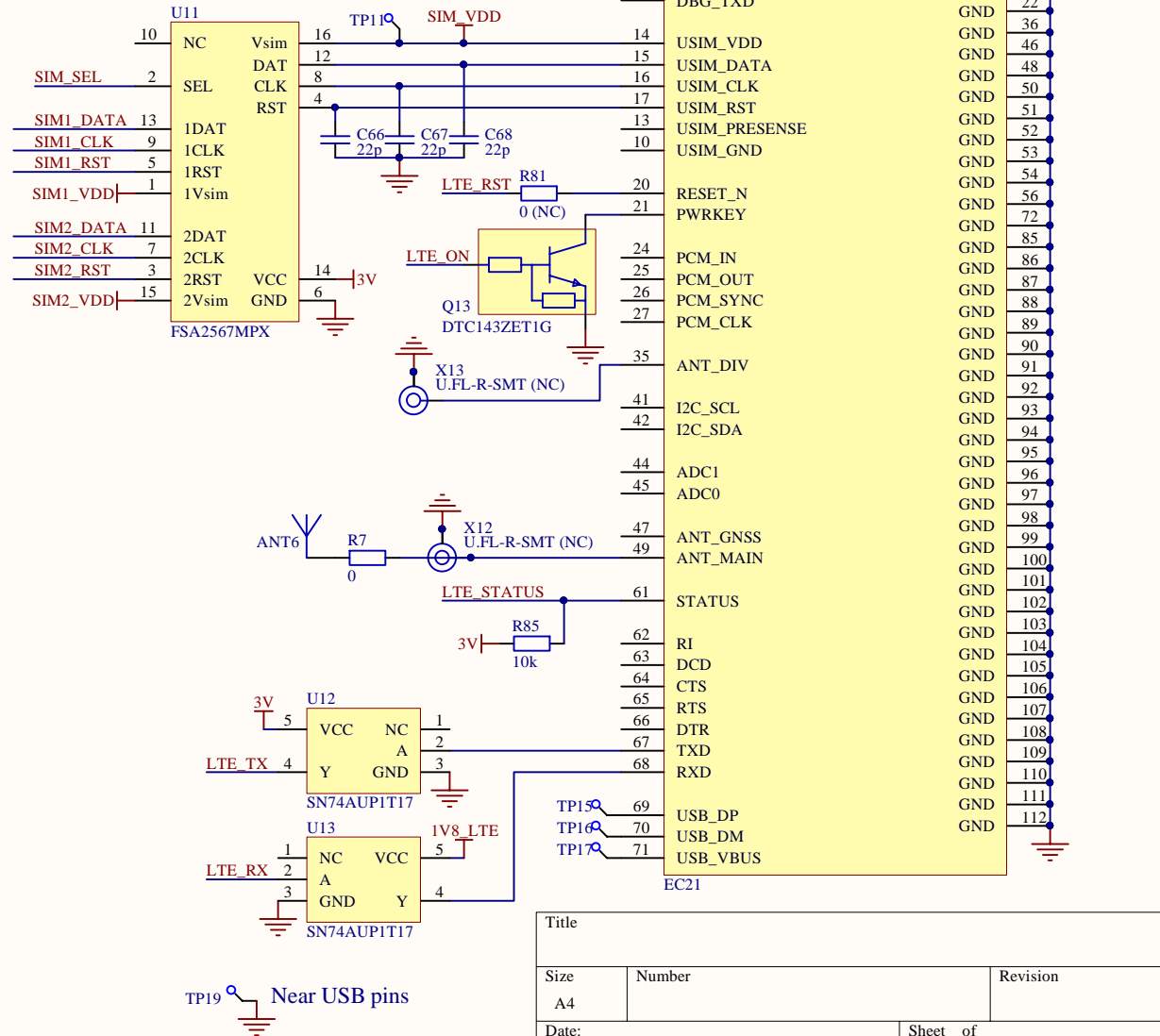
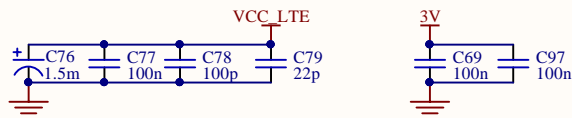
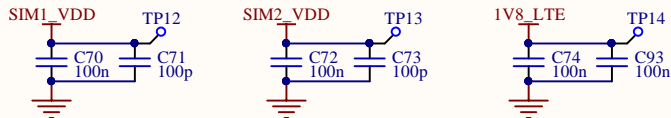
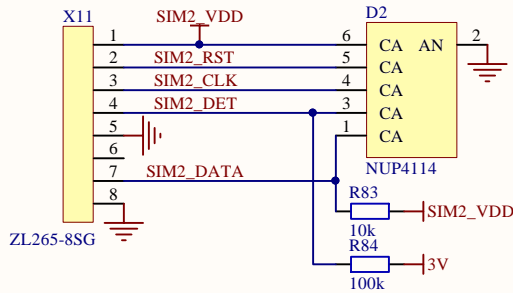
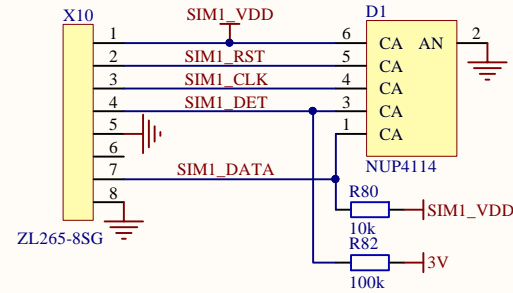
RTL8722CSM

Only PORT A pins are interrupt-capable!



Title		
Size A4	Number	Revision
Date:	Sheet of	
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LTE MODULE

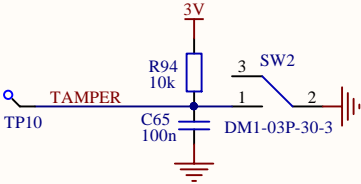
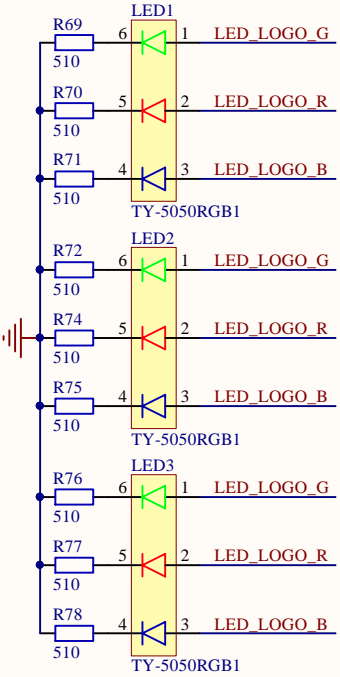
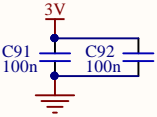
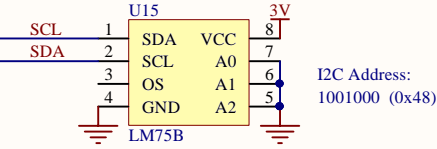
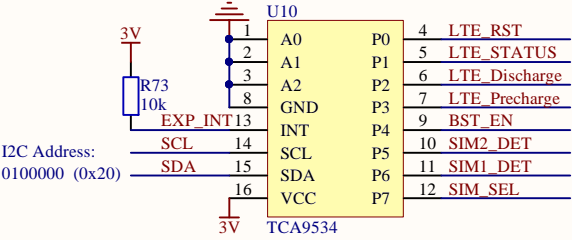


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MISCELLANEOUS

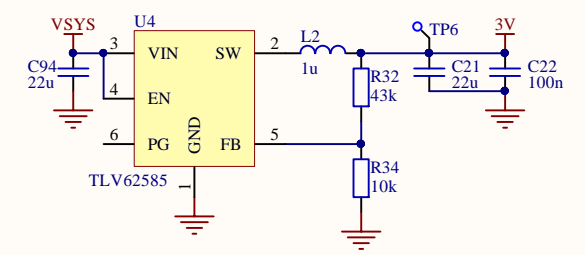
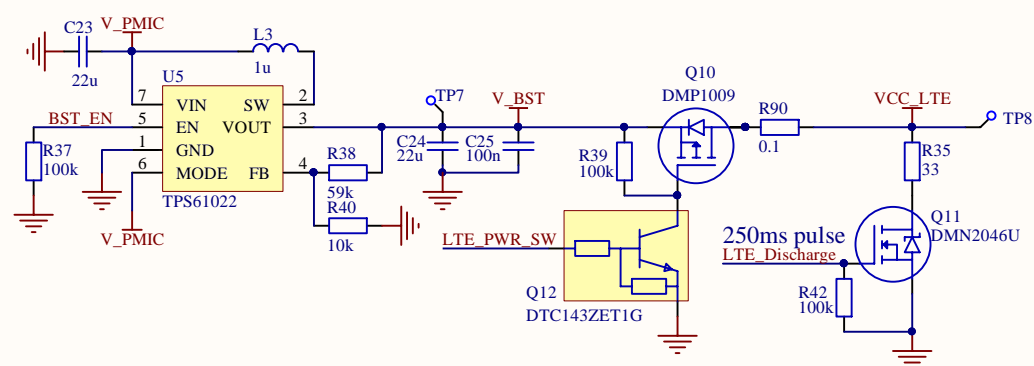
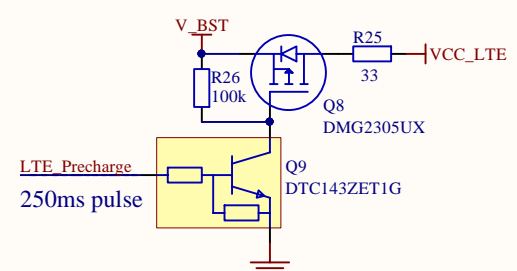
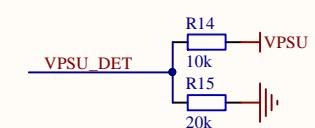
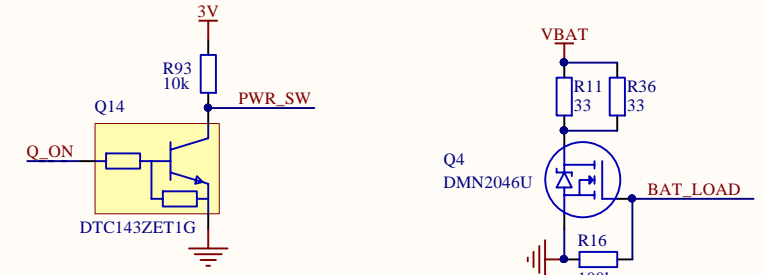
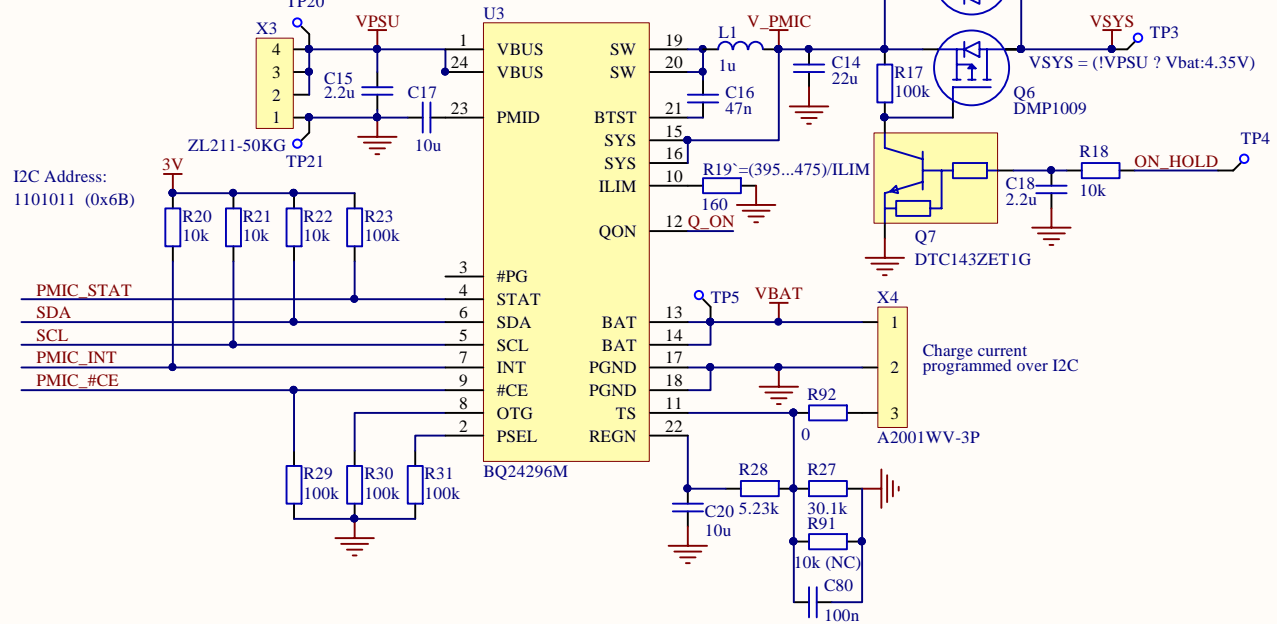
GREEN&BLUE draws 2mA each @3V
RED draws 1mA each @3V

I/O Extender



Title		
Size	Number	Revision
A4		
Date:		Sheet of
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POWER



Title		
Size	Number	Revision
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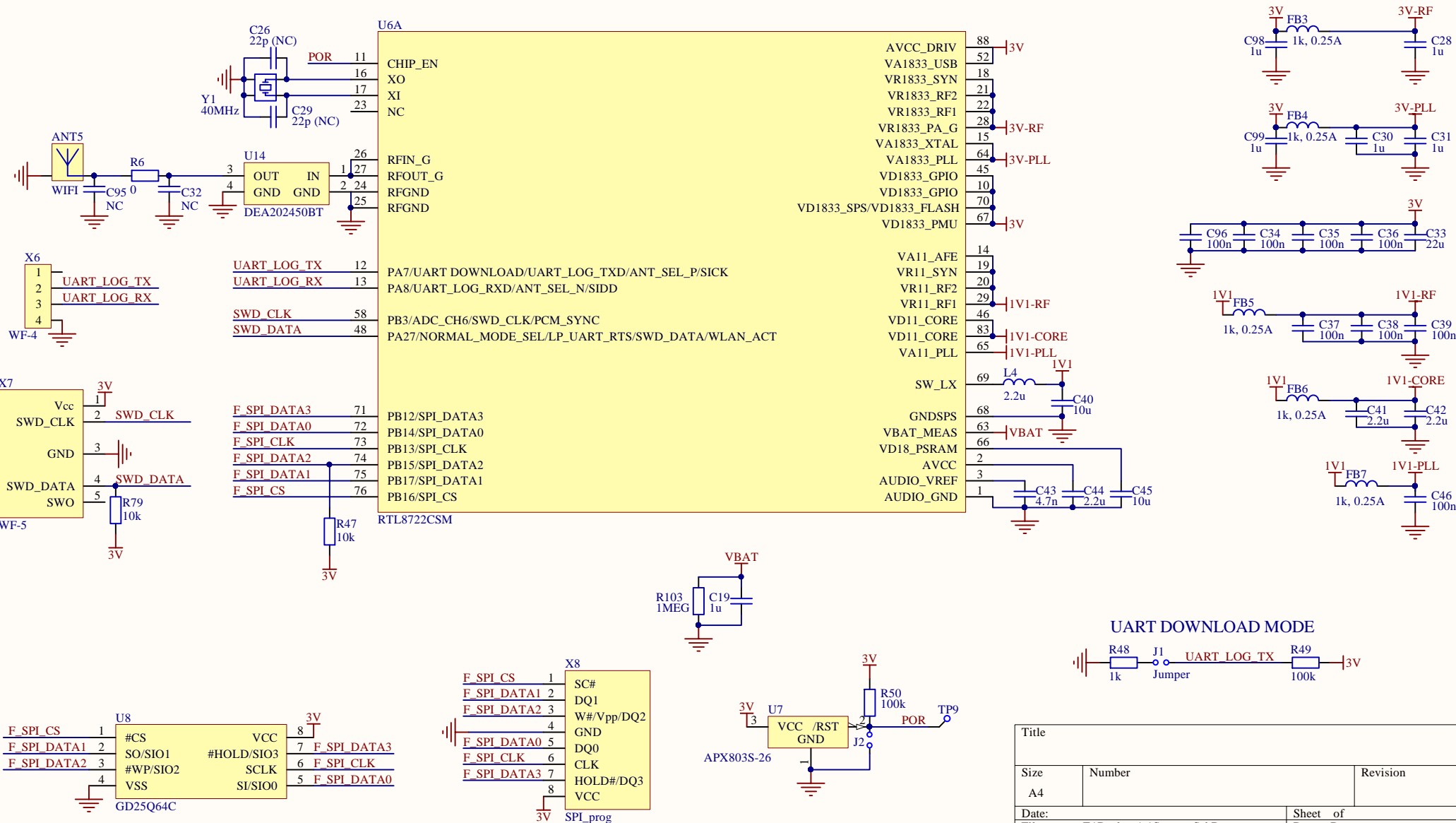
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D



SYSTEM



Title		
Size	Number	Revision
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