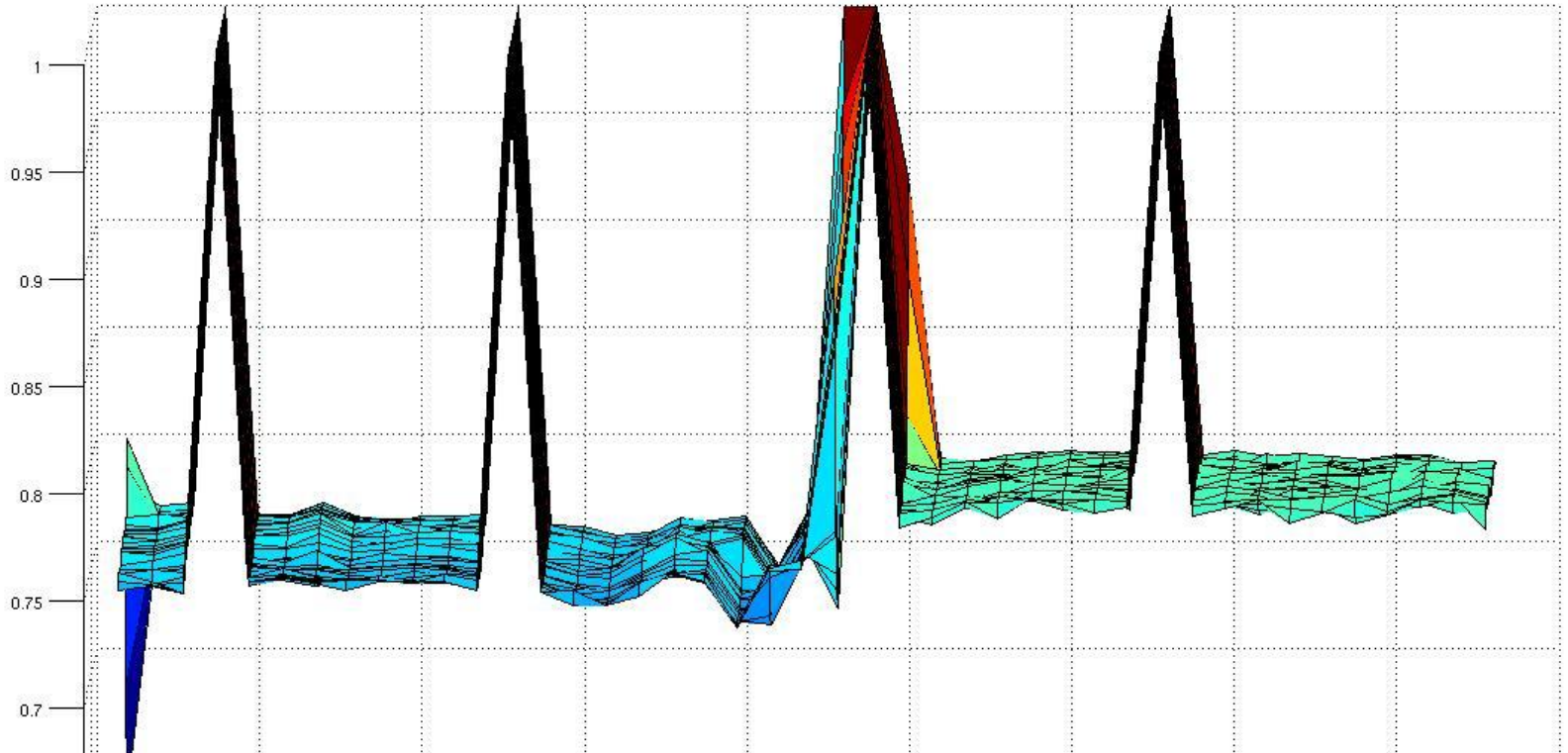
An Automated Flow for Intra-Die Power Variation Measurement in FPGAs

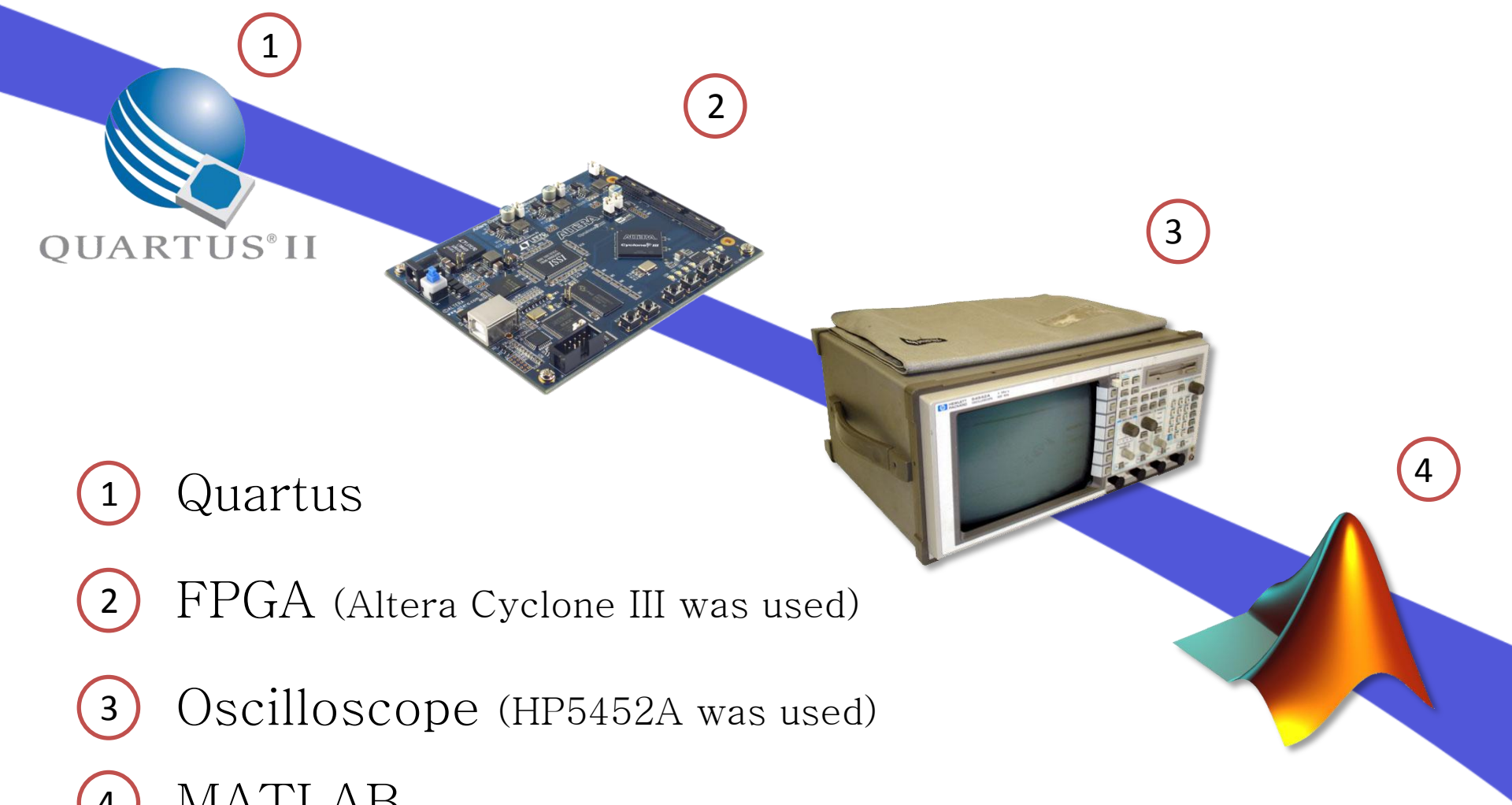
- Vikram Voleti



Motivation

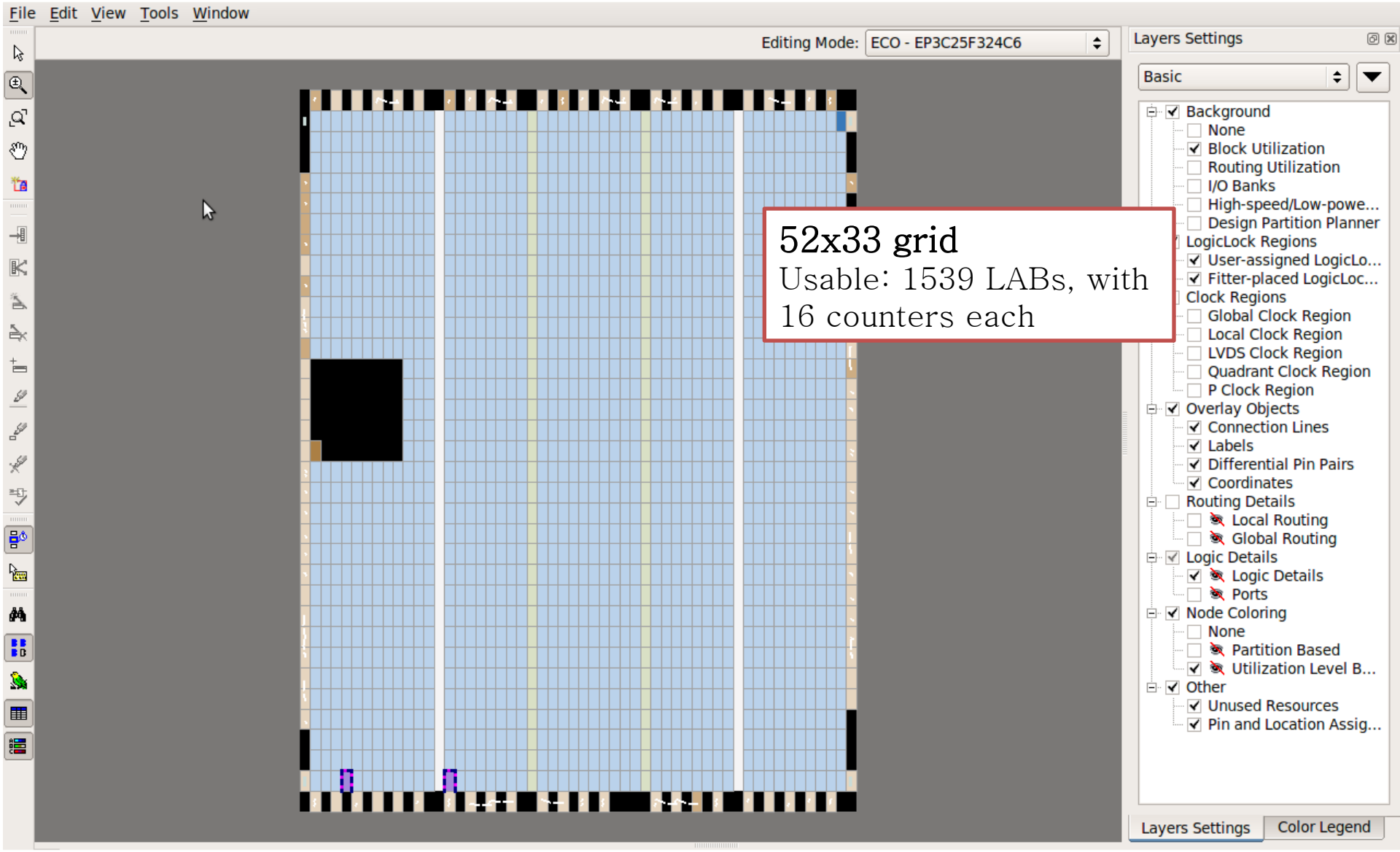
- Intra-Die Variation is ever increasing in Sub-nm CMOS
- We need to take Process Variation into account during design flow.
- This flow is a building block of such a design scheme.
- Will be useful for analysis of sub-nm variation maps in FPGAs.

The Flow

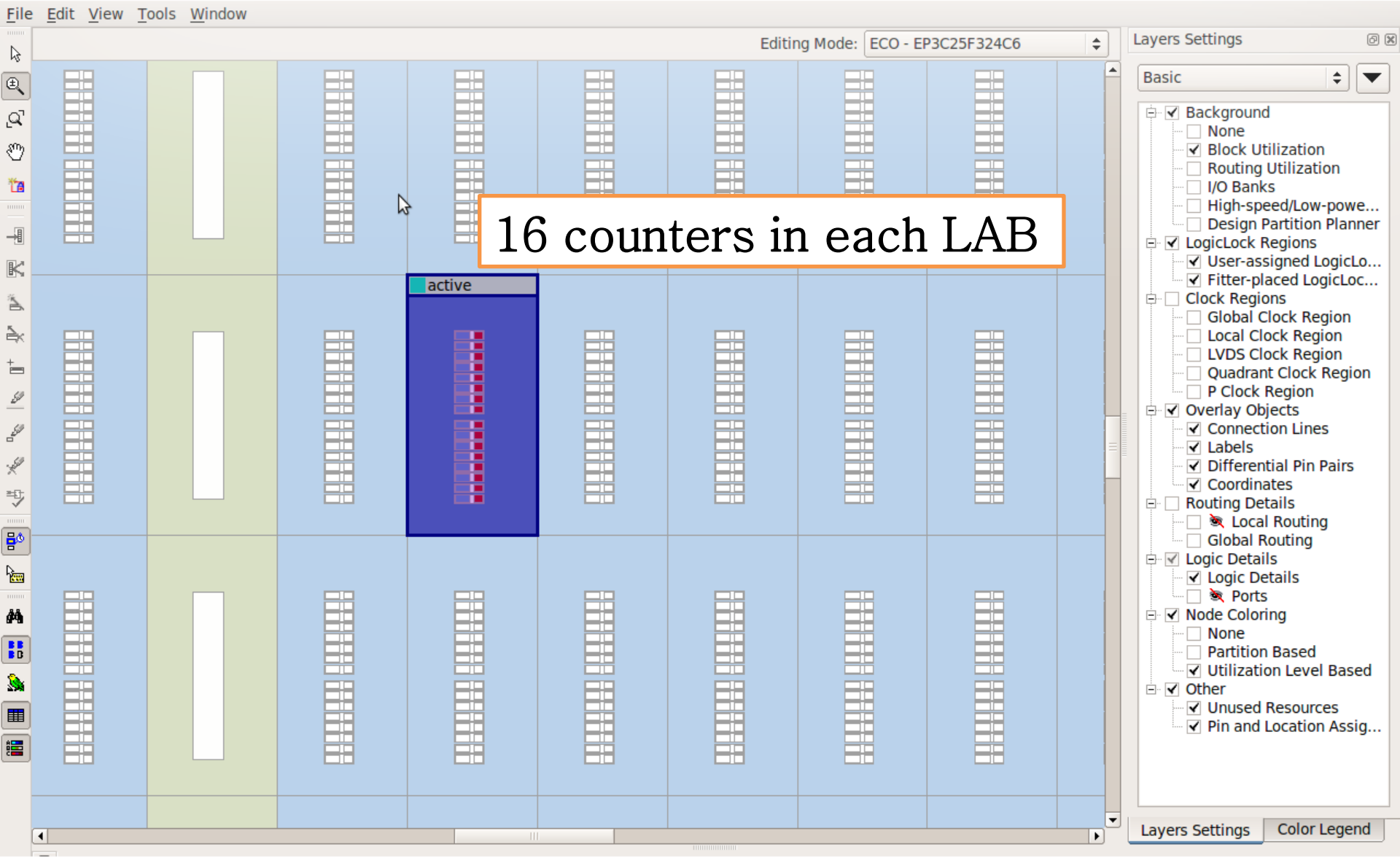


1. Quartus
2. FPGA (Altera Cyclone III was used)
3. Oscilloscope (HP5452A was used)
4. MATLAB

1 Quartus


File Edit View Tools Window
Editing Mode: ECO - EP3C25F324C6
52x33 grid
Usable: 1539 LABs, with 16 counters each
Layers Settings
Basic
Background
None
Block Utilization
Routing Utilization
I/O Banks
High-speed/Low-powe...
Design Partition Planner
LogicLock Regions
User-assigned LogicLo...
Fitter-placed LogicLoc...
Clock Regions
Global Clock Region
Local Clock Region
LVDS Clock Region
Quadrant Clock Region
P Clock Region
Overlay Objects
Connection Lines
Labels
Differential Pin Pairs
Coordinates
Routing Details
Local Routing
Global Routing
Logic Details
Logic Details
Ports
Node Coloring
None
Partition Based
Utilization Level B...
Other
Unused Resources
Pin and Location Assig...
Layers Settings
Color Legend

1 Quartus

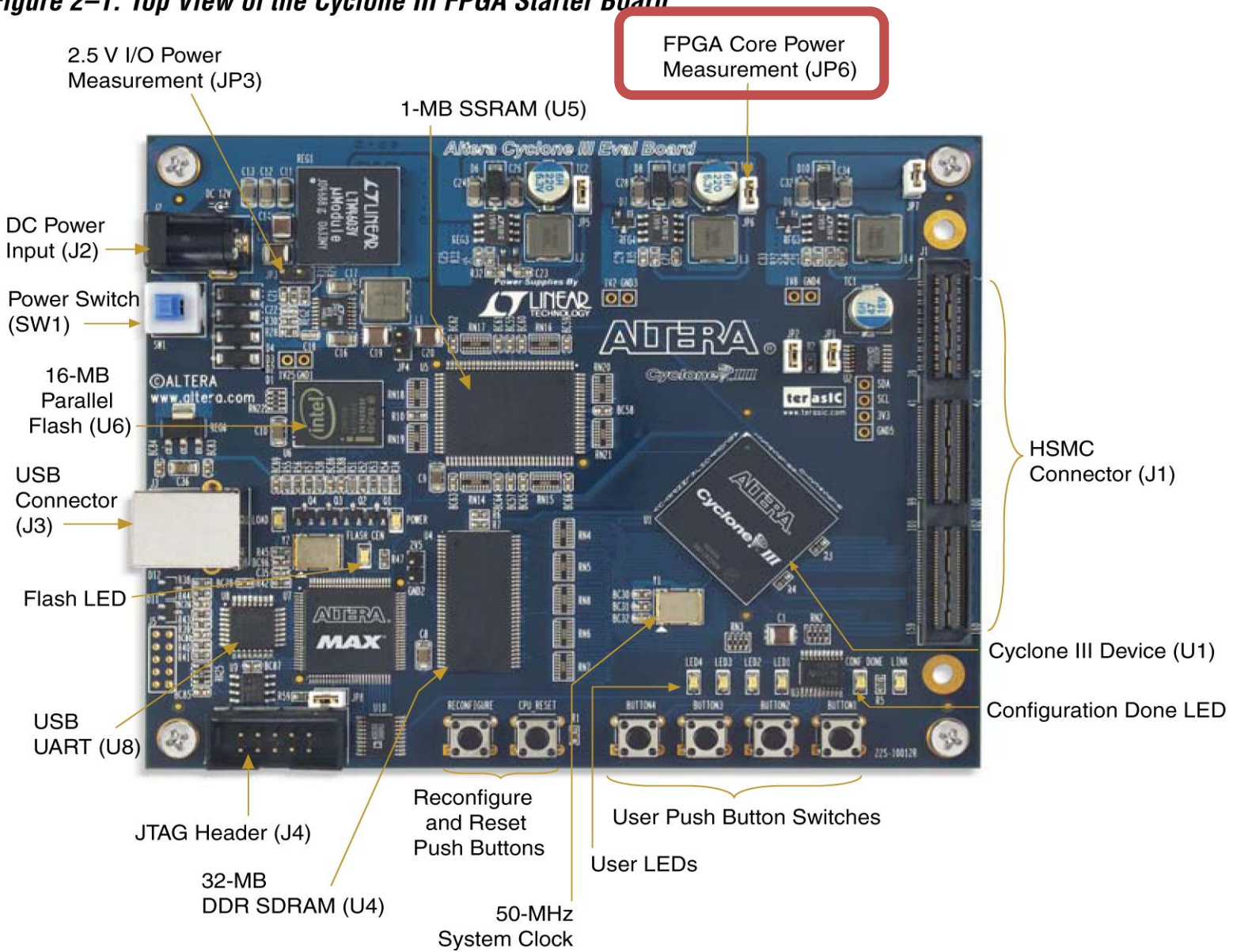

File
Edit
View
Tools
Window
Editing Mode:
ECO - EP3C25F324C6
16 counters in each LAB
active
Layers Settings
Basic
Background
None
Block Utilization
Routing Utilization
I/O Banks
High-speed/Low-powe...
Design Partition Planner
LogicLock Regions
User-assigned LogicLo...
Fitter-placed LogicLoc...
Clock Regions
Global Clock Region
Local Clock Region
LVDS Clock Region
Quadrant Clock Region
P Clock Region
Overlay Objects
Connection Lines
Labels
Differential Pin Pairs
Coordinates
Routing Details
Local Routing
Global Routing
Logic Details
Logic Details
Ports
Node Coloring
None
Partition Based
Utilization Level Based
Other
Unused Resources
Pin and Location Assig...
Layers Settings
Color Legend

1 Quartus

- Compile the configuration for each location of the LAB
- Generate *.sof file
- Program the FPGA

2 FPGA

Figure 2–1. Top View of the Cyclone III FPGA Starter Board



3 Oscilloscope

HP 54542A

RATINGS OF PROBES USED:

CHAN1, CHAN2 – 150 MHz
Ext. Trigger – 60 MHz

Order of Commands:

- **TIMEBASE:**
  Trigger-mode;
  Repetitive sampling;
  200ns window, 500 points

- **CHANNEL:** (set equal for both channels)
  72 mV/div;
  1.2V DC Offset;
  DC Coupling

- **TRIGGER:**
  Edge-triggered

- **ACQUIRE:**
  1024 averages of 500 points

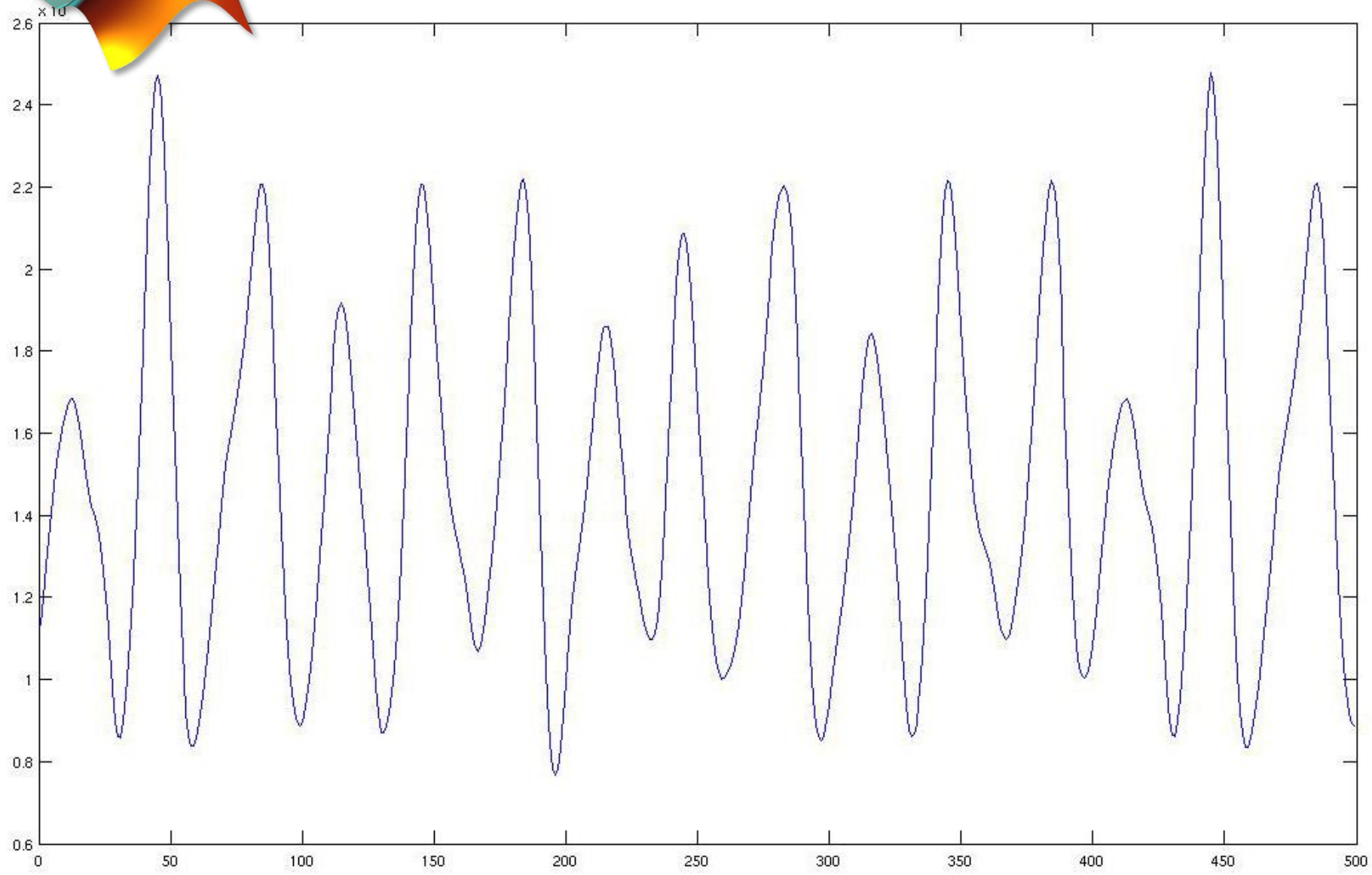
- **FORMAT:**
  16 bit ASCII

3 Oscilloscope

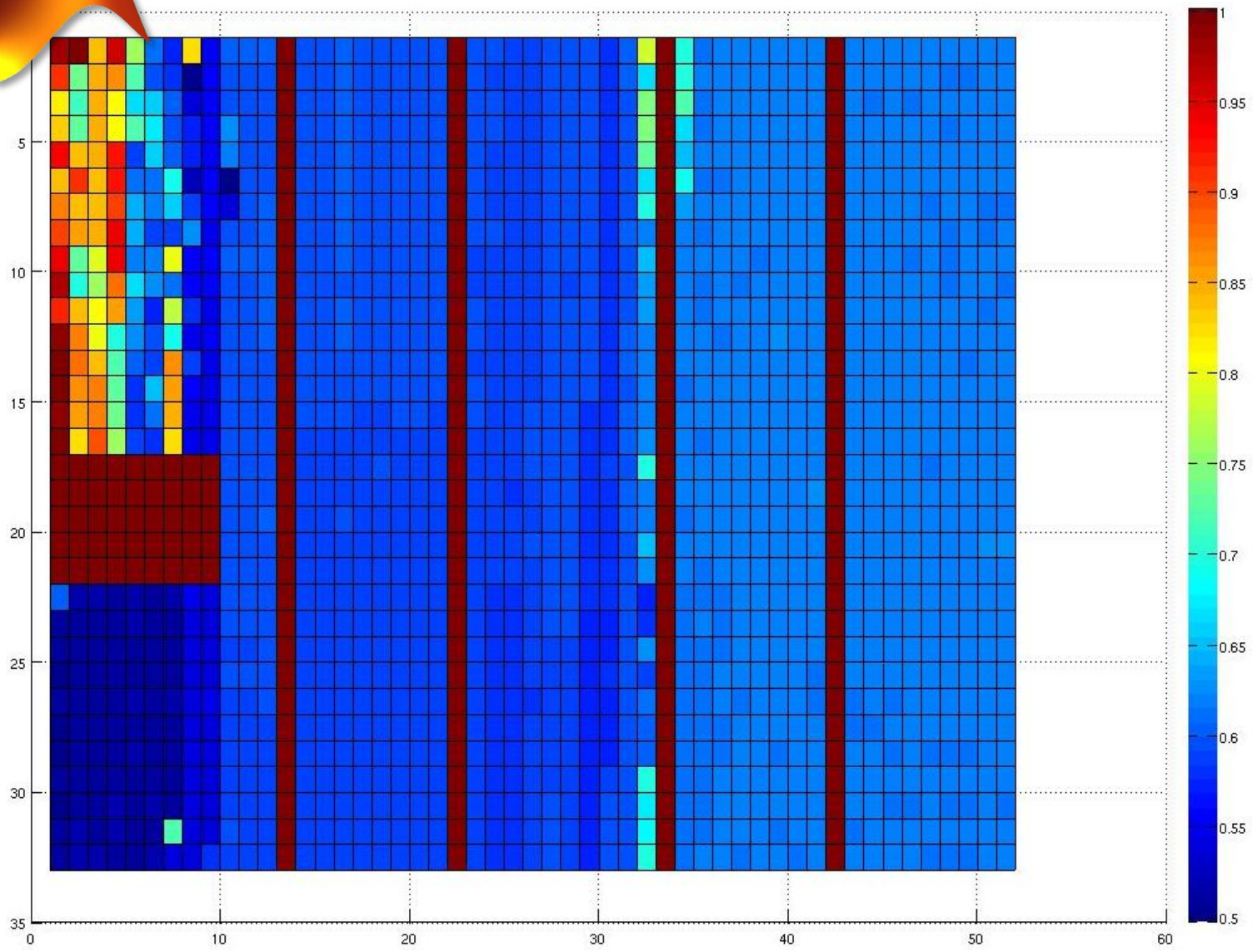
Get the waveform as a file.

11327 12012 12805 13447 14076 14734 15273 15716 16095 16384 16664 16801 16827 16681 16347 15994 15474 15000 14594 14231
14087 13839 13507 12996 12305 11700 10731 9791 9006 8607 8589 8998 9603 10458 11468 12579 14018 15582 17145 19019 20829
22452 23724 24541 24728 24475 23471 22052 20204 18200 16491 14773 12977 11353 10034 9195 8654 8390 8374 8570 8930 9403
9921 10502 11122 11786 12514 13129 13901 14609 15214 15656 15966 16382 16744 17207 17710 18183 18823 19537 20255 20981
21627 22053 22068 21772 20943 19761 18154 16438 15151 13695 12354 11194 10271 9673 9234 8971 8880 8965 9307 9764 10278
10961 11691 12572 13488 14259 15239 16219 17236 18034 18683 19059 19166 19044 18616 17999 17233 16405 15635 14852 14099
13391 12468 11648 10715 9840 9148 8713 8718 8868 9203 9672 10259 11165 12175 13528 15041 16527 18260 19719 20893 21696
22065 22016 21536 20845 19889 18885 17951 17109 16306 15504 14780 14319 13896 13577 13305 12911 12665 12238 11764 11275
10855 10733 10673 10861 11214 11719 12306 12892 13577 14278 15115 15995 16838 17974 19124 20077 20887 21584 22083 22203
21864 21189 19884 18227 16199 14453 12689 10968 9539 8442 7834 7665 7817 8339 9092 9952 10904 11695 12283 12765 13217
13706 14205 14775 15512 16205 16928 17615 18150 18554 18592 18591 18230 17722 16981 16150 15442 14818 14184 13538 13075
12748 12376 12062 11657 11328 11143 10961 10991 11146 11478 12168 13155 14430 15778 17104 18508 19676 20403 20838 20863
20562 19929 19014 17899 16747 15687 14739 13639 12426 11578 10991 10461 10196 10015 10038 10168 10265 10455 10750 11106
11623 12213 12885 13765 14548 15319 15933 16488 17170 17796 18619 19417 20143 20854 21350 21754 21940 22028 21900 21551
20878 19759 18325 16515 15047 13503 11913 10584 9515 8909 8610 8505 8646 8993 9397 9962 10465 10985 11435 11882 12477
13069 13736 14333 15152 15991 16818 17495 18014 18371 18427 18237 17854 17304 16704 16053 15317 14581 13753 13004 12160
11183 10187 9341 8782 8625 8685 8931 9407 10105 11085 12273 13701 15271 16853 18536 19997 21122 21890 22174 22081 21513
20703 19720 18608 17620 16725 15846 15063 14389 13942 13589 13402 13201 13022 12809 12445 12025 11552 11244 11071 10966
11042 11272 11686 12144 12590 13133 13783 14569 15505 16417 17405 18630 19639 20514 21243 21856 22164 22016 21532 20460
19019 17268 15718 14319 12808 11645 10766 10311 10094 10034 10135 10398 10811 11361 12015 12805 13460 14111 14793 15252
15744 16125 16419 16699 16774 16855 16690 16421 15987 15470 14997 14581 14305 14061 13823 13478 12959 12365 11698 10732
9756 8992 8635 8604 8986 9563 10423 11447 12590 13957 15558 17110 19030 20833 22411 23725 24564 24771 24507 23487 22122
20254 18283 16505 14811 13029 11399 10110 9211 8666 8356 8341 8585 8920 9376 9856 10446 11126 11793 12443 13096 13861
14615 15208 15604 15989 16357 16784 17187 17672 18235 18804 19550 20235 20963 21640 22041 22101 21812 21046 19787 18231
16488 15223 13779 12351 11242 10300 9693 9209 8940 8866

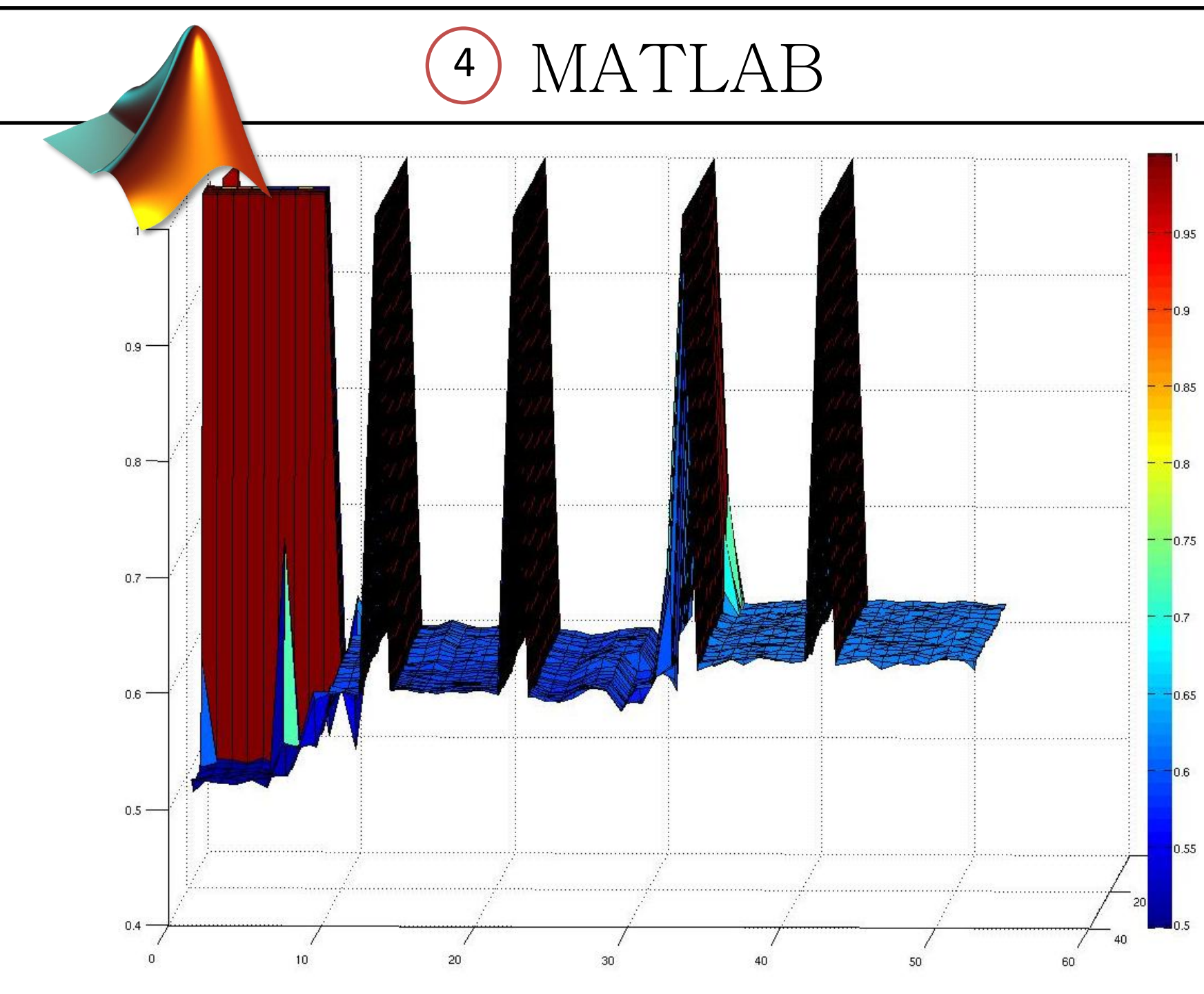
4 MATLAB


x 10
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0
50
100
150
200
250
300
350
400
450
500

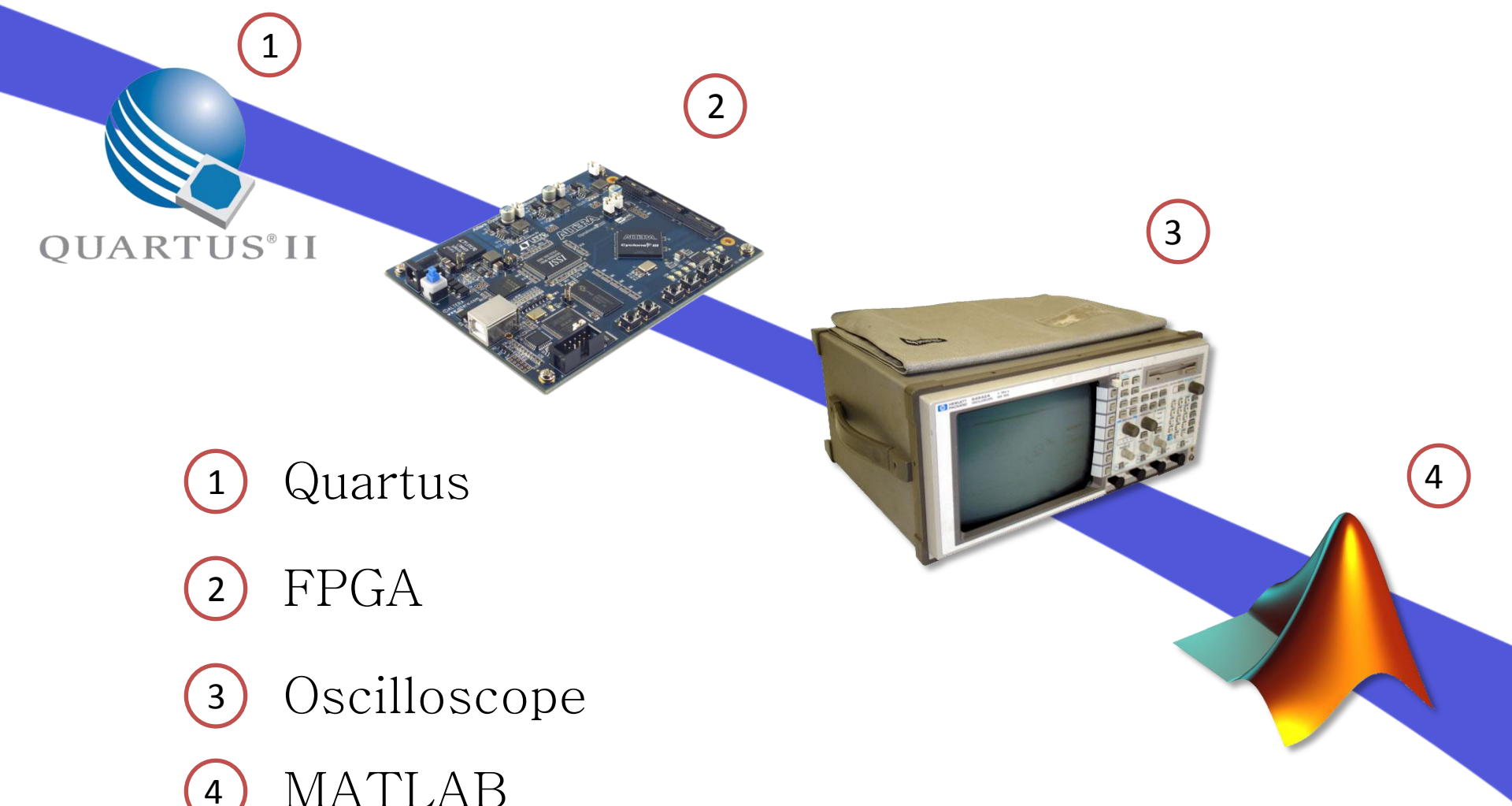
4 MATLAB


5
10
15
20
25
30
35
0
10
20
30
40
50
60
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5

4 MATLAB


1
0.9
0.8
0.7
0.6
0.5
0.4
0
10
20
30
40
50
60
20
40
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5

The Flow



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Limitations

- **Number of counters used:**
  - Need sufficient number of counters to get proper waveform
  - Maximum number of counters that can be used is 196 due to limited number of I/O ports

- **Trigger:**
  - Trigger needs to be given from the clock in the FPGA
  - Trigger needs to be sychronised
  - Trigger level needs to be checked

- **Time:**

  It takes about 97 seconds for each configuration (for compilation, programming and capture of waveforms) for 1024 averages

- **50 MHz:**

  An oscilloscope appropriate for 50 MHz (for Cyclone III) is required

Future Enhancements

- Differential probe can be used to increase accuracy
- Variation map for different V_{DD}'s using Source Meter
- Can be packaged to be platform-independent