

**SPECIFICATION
FOR
LCD Module
KD040WVFBD003-C005A**

MODULE:	KD040WVFBD003-C005A
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2016.09.05

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CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

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常备库存
Stock For Sale

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range

[illegible]

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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 4.0'TFT-LCD contains 480X800 pixels, and can display up to 65K colors.

* Features

- Low Input Voltage: 3.3V(TYP)
- Display Colors of TFT LCD: 65K colors
- TFT Interface: 1 MCU 8/16BIT interface
- CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	51.84(H)*86.4(V) (4.0inch)	mm	-
CTP View area	96.04(H)*54.86(V)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K	colors	-
Number of pixels	480(RGB)*800	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.108(H)*0.108(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9806	-	-
CTP Driver IC	GT911	-	-
Display mode	Transmissive/Normally Black	-	-
Touch mode	Five point and Gestures	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		58.26		mm	-
	Vertical(V)		98.1		mm	-
	Depth(D)		3.63		mm	-
Weight			TBD		g	-

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常备库存
Stock For Sale

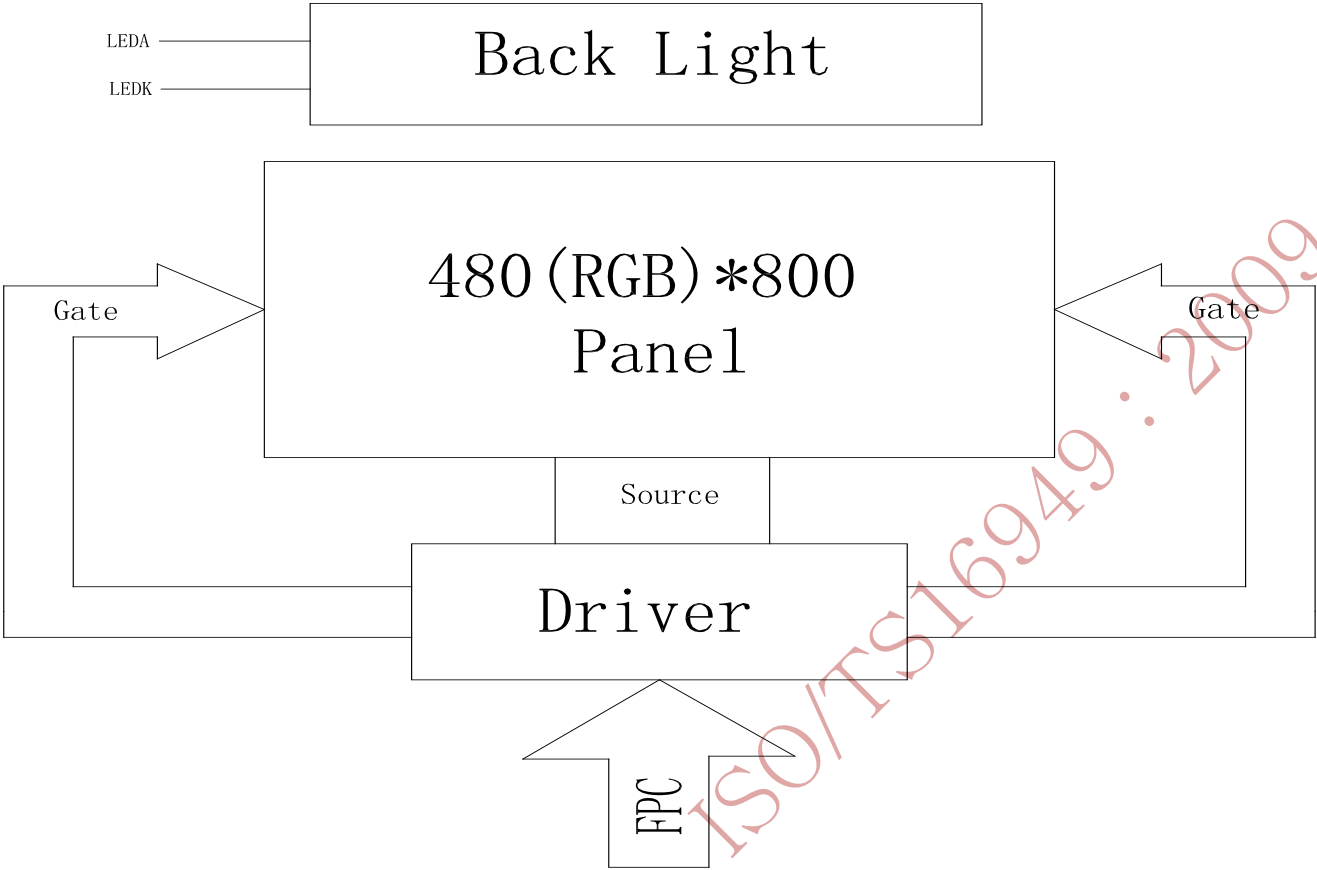
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1. Block Diagram



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Stock For Sale	Long Time supply	NO MOQ	In Full Range	

3. Input terminal Pin Assignment

3.1 TFT

Pin NO.	Symbol	Function	I/O
1	YU(NC)	Touch panel Top Film Terminal	A/D
2	XR(NC)	Touch panel Right Glass Terminal	A/D
3	YD(NC)	Touch panel Bottom Film Terminal	A/D
4	XL(NC)	Touch panel LIFT Glass Terminal	A/D
5	GND	Ground.	P
6	GND	Ground.	P
7	VCI	Supply voltage (3.3V).	P
8	VCI	Supply voltage (3.3V).	P
9-16	NC		
17-32	DB15-DB0	16-bit parallel bi-directional data bus for MCU system interface mode . Fix to GND level when not in use	I/O
33-35	NC		
36	IM0	Interface Select	I
37	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.	I
38	CS	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed.	I
39	RS	Data / Command Selection pin	I
40	WR	Write enable clock input pin	I
41	RD	Read enable clock input pin	I

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42-48	NC		
49	LEDA	Anode pin of backlight.	P
50	LEDK	Cathode pin of backlight.	P

3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	NC	NC	
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

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NO MOQ

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4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	550	800	--		
Response time	Rising	T _R		--	35	--	msec	
	Falling	T _F						
Color gamut		S(%)		--	70	--	%	
Color Filter Chromaticity	White	W _X		0.277	0.292	0.307		
		W _Y		0.318	0.333	0.348		
	Red	R _X		0.650	0.665	0.680		
		R _Y		0.308	0.323	0.338		
	Green	G _X		0.257	0.272	0.287		
		G _Y		0.573	0.588	0.613		
	Blue	B _X		0.119	0.134	0.149		
		B _Y		0.106	0.121	0.136		
Viewing angle	Hor.	Θ_L	CR>10	80	85	--		
		Θ_R		80	85	--		
	Ver.	Θ_U		80	85	--		
		Θ_D		80	85	--		
		Option View Direction		ALL				

4.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: $25 \pm 2^\circ\text{C}$
- 15min. warm-up time.

4.3 Measuring Equipment

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).
2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer
4. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
5. The electro-optical response time measurements shall be made as FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_d .

ISO9001:2015

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Figure 1. The Definition of V_{th} & V_{sat}

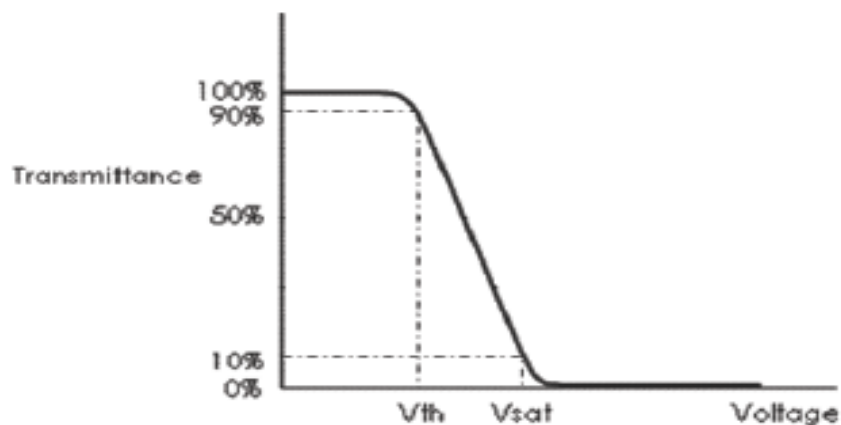


Figure 2. Measurement Set Up

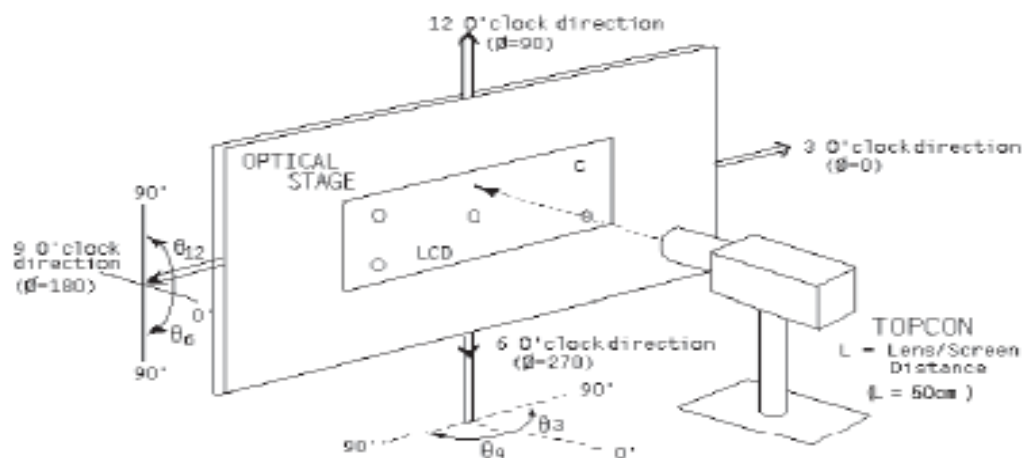
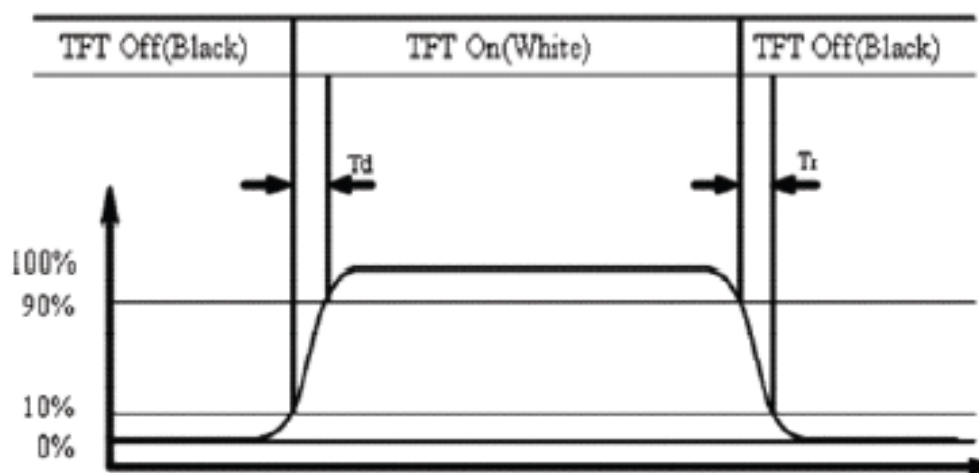


Figure 3. Response Time Testing



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5. Electrical Characteristics

5.1 Absolute Maximum Rating ($T_a=25$ VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	2.5	3.6	V
Operating temperature	T_{OP}	-20	+70	°C
Storage temperature	T_{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.5	2.8	3.6	V	
Normal mode Current consumption	IDD	--	30	--	mA	
Level input voltage	V_{IH}	$0.7V_{DDIO}$		VDDIO	V	
	V_{IL}	GND		$0.3V_{DDIO}$	V	
Level output voltage	V_{OH}	$0.8V_{DDIO}$		VDDIO	V	
	V_{OL}	GND		$0.2V_{DDIO}$	V	

5.3 LED Backlight Characteristics

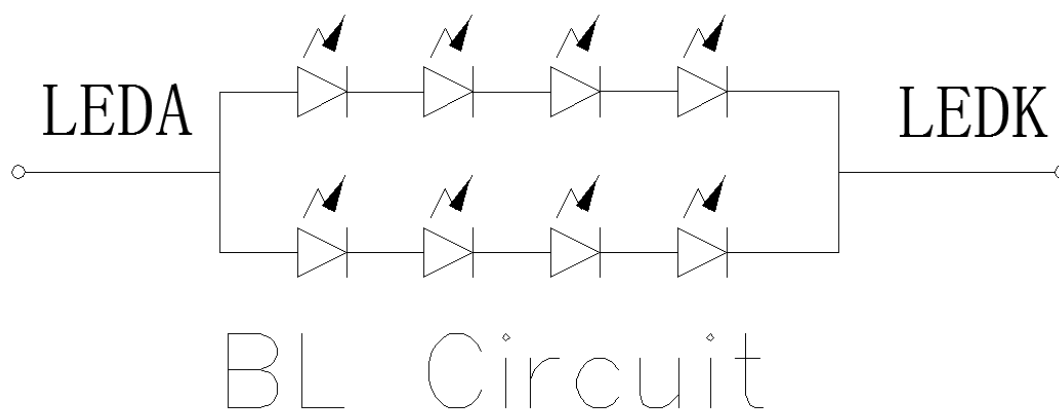
The back-light system is edge-lighting type with 8 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	30	40	--	mA	
Forward Voltage	V_F	--	28.8	--	V	
LCM Luminance	L_V	--	400	--	cd/m ²	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

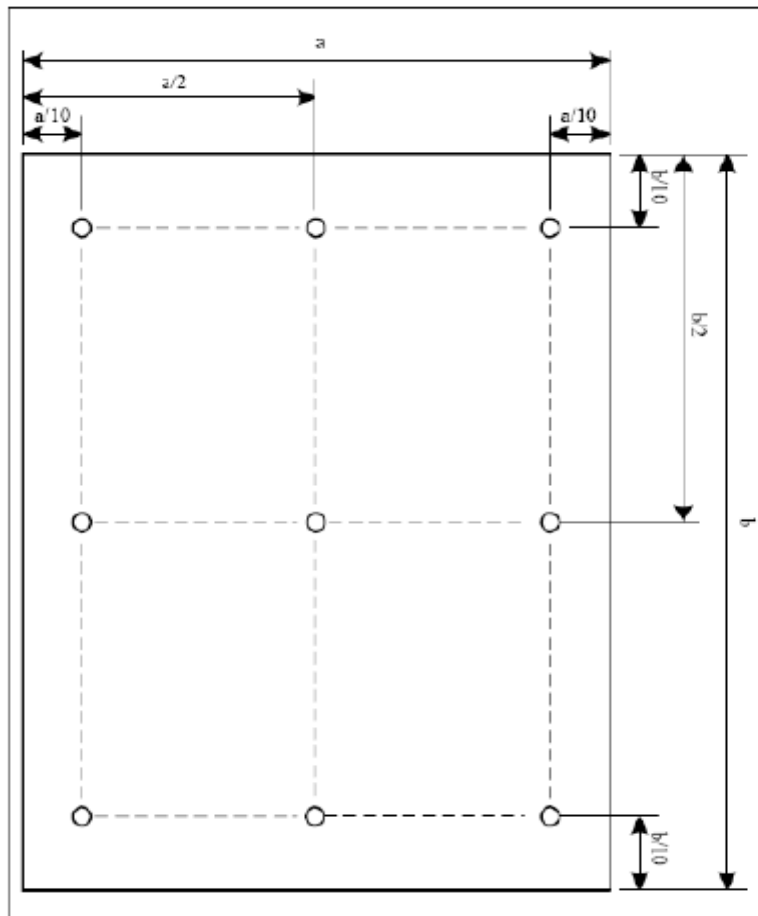
$T_a = 25 \pm 3^\circ \text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at $T_a = 25^\circ \text{C}$ and $I_L = 40 \text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 40mA. The constant current driving method is suggested.





NOTE 3: Luminance Uniformity of these 9 points is defined as below:



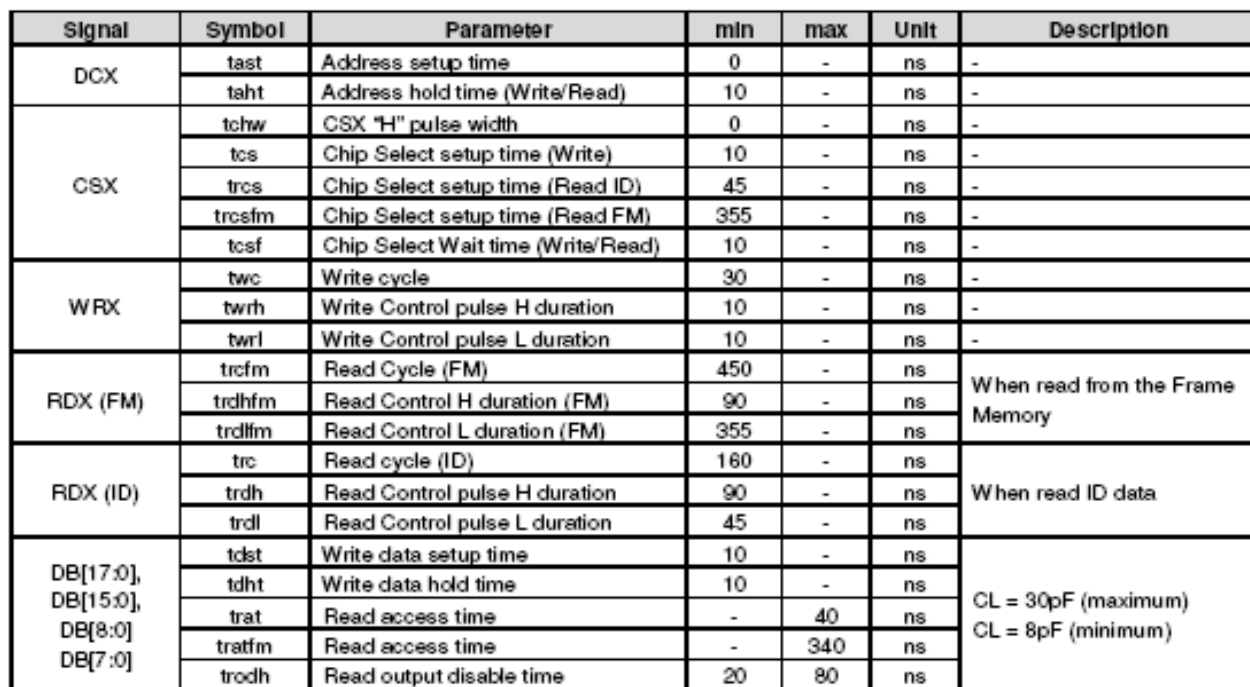
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

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常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	



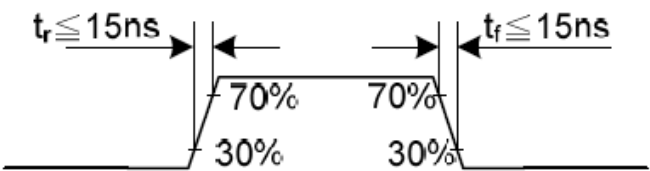
6.1 Display Parallel 16/8-bit Interface Timing Characteristics (8080- I system)



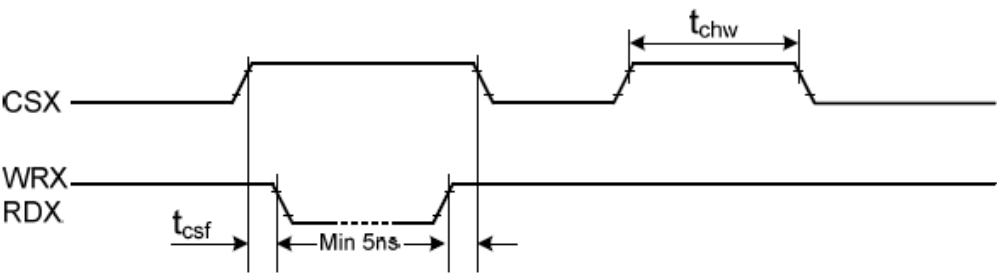
品种齐全
In Full Range

Notes:

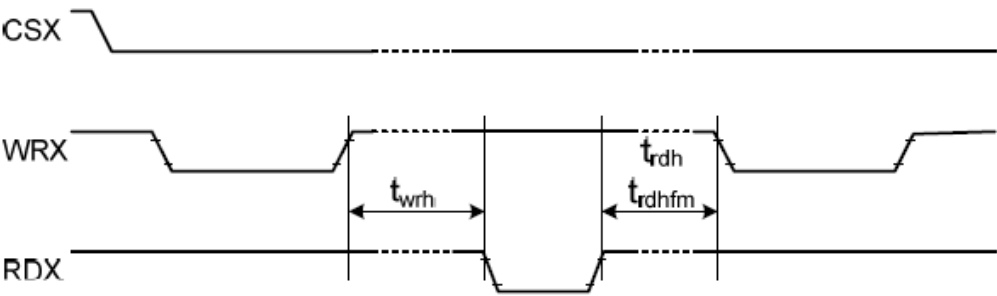
1. Ta = -30 to 70℃, VDDI = 1.65V to 3.3V, VDDA = 2.6V to 4.8V, VSSAM = GND= 0V
2. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.
3. Input signal rising and falling time:



4. The CSX timing:



5. The Write-to-Read or the Read-to-Write timing:



ISU

6.2 Reset input timing

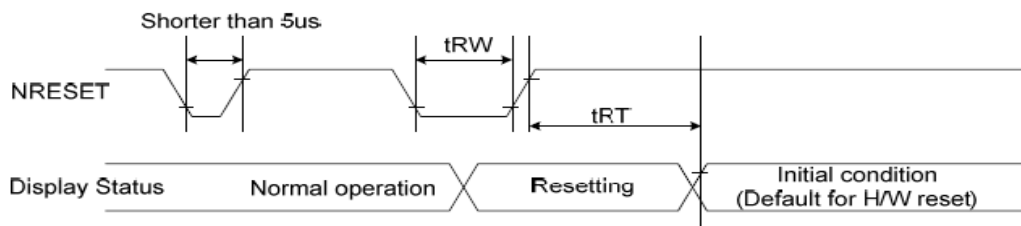


Figure 180: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5 (note 1,5) 120 (note 1,6,7)	ms

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. A spike due to an electrostatic discharge on the RESX line does not cause irregular system reset, according to the Table 48.

Table 48: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains blank in the Sleep In mode.), and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse as shown below:

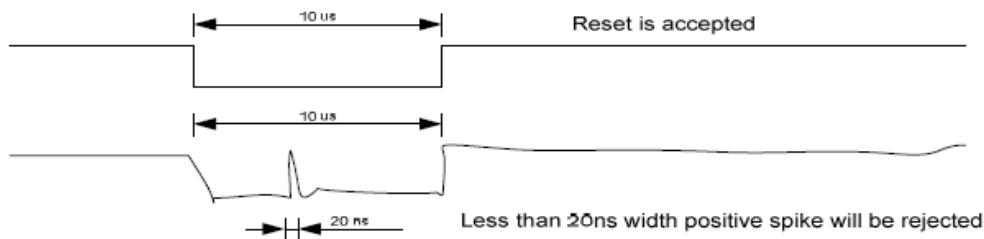


Figure 181: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing the RESX before sending commands. Moreover, the Sleep Out command cannot be sent in 120msec.

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.66	3.47	V	--
Operating temperature	T _{OP}	-40	+85	°C	--
Storage temperature	T _{ST}	-60	+125	°C	--
Welding temperature (10s)	--	--	300	°C	--
ESD protection voltage (HB Model)	--	--	±2	KV	--

7.1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient temperature:25°C, AVDD=2.8V, VDDIO=1.8V or VDDIO=AVDD)

Item	Min.	Typ.	Max.	Unit	Note
Normal mode operating current	--	8	14.5	mA	
Green mode operating current	--	3.3	--	mA	
Sleep mode operating current	70	--	120	uA	
Doze mode operating current	--	0.78	--	mA	
Digital Input low voltage/VIL	-0.3	--	0.25*VDDIO	V	
Digital Input high voltage/VIH	0.75*VDDIO	--	VDDIO+0.3	V	
Digital Output low voltage/VOL	--		0.15*VDDIO	V	
Digital Output high voltage/VOH	0.85*VDDIO			V	

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常备库存
Stock For Sale

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range

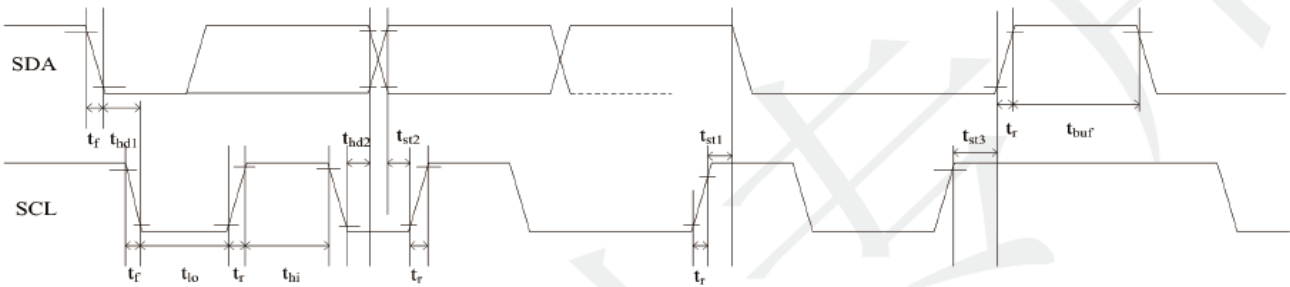
7.1.3 AC Characteristics

(Ambient temperature:25℃, AVDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit
OSC oscillation frequency	59	60	61	MHZ
I/O output rise time,low to high	-	14	-	ns
I/O output rfall time,high to low	-	14	-	ns

7.2 I2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

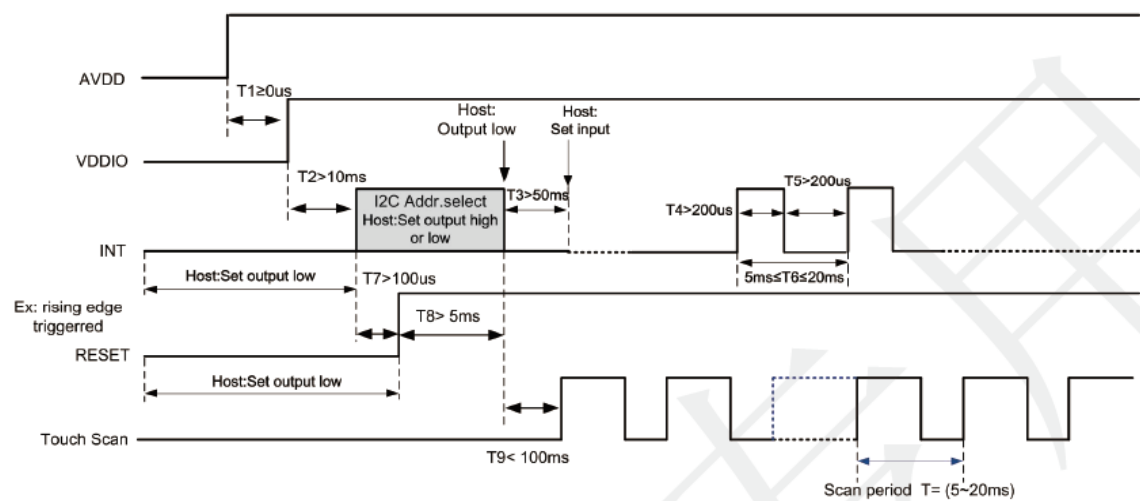
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

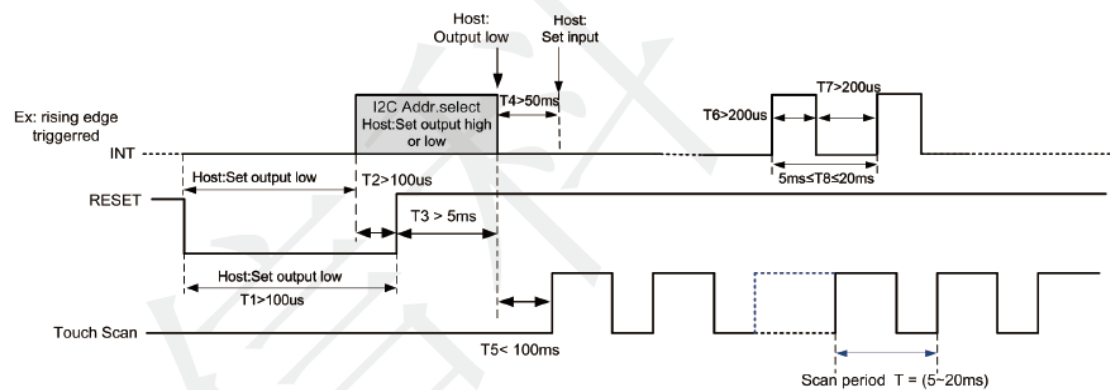
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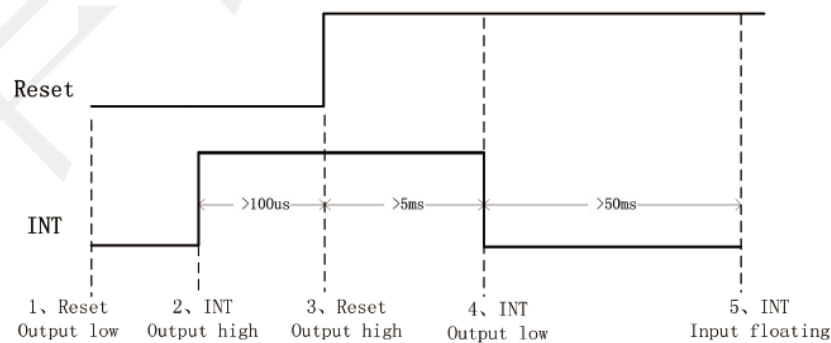
Power-on Timing:



Timing for host resetting GT911:

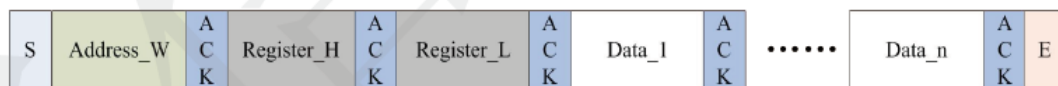


Timing for setting slave address to 0x28/0x29:





Timing diagram for the 74VHC141 showing Reset and INT signals. The diagram is divided into five numbered sections: 1. Reset (Output low), 2. INT (Output low), 3. Reset (Output high), 4. INT (Output low), and 5. INT (Input floating). Timing constraints are shown: >100us for the low pulse in section 2, >5ms for the high pulse in section 3, and >50ms for the low pulse in section 4.



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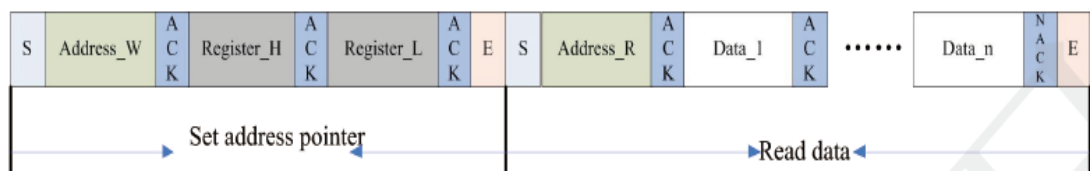
The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example: device address is 0xBA/0xBB)



Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0xBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

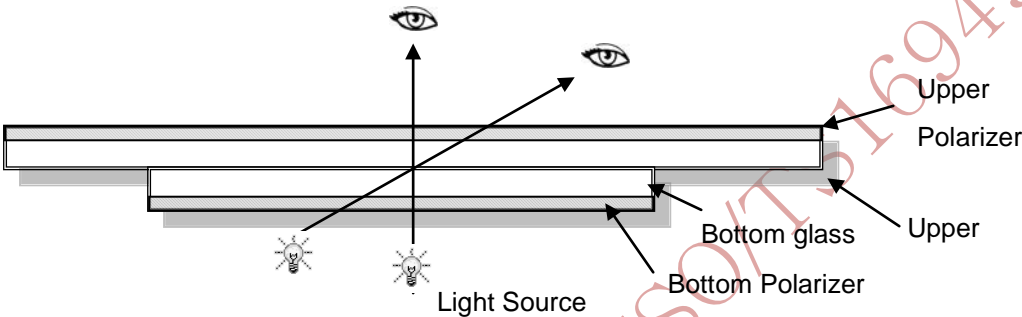
8 LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

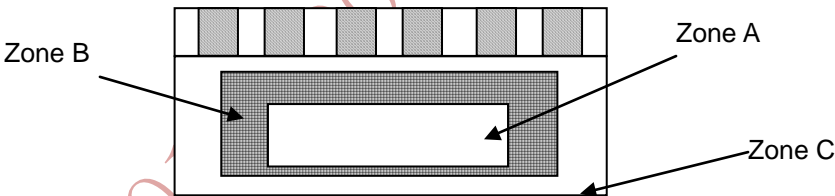
8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : 25±5℃
- Humidity : 65%±10%RH
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance:30-50cm



8.1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
- Zone B : Viewing Area except Zone A
- Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

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		支持小量 NO MOQ		

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

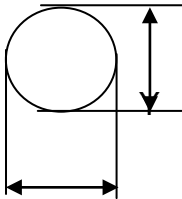
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

8.1.4 Criteria (Visual)

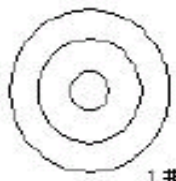
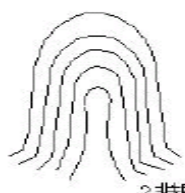

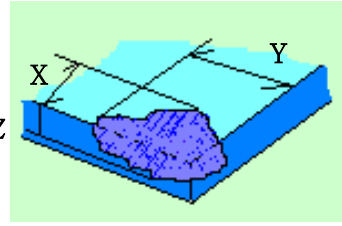
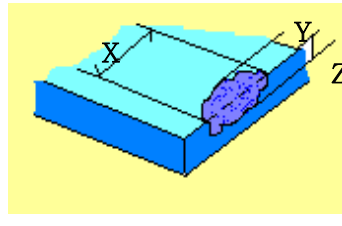
Number	Items	Criteria(mm)
1.0 LCD Crack/Broken 		

Number	Items	Criteria (mm)																													
2.0	<div>Spot defect</div> <div></div> <div>X</div> <div>Φ=(X+Y)/2</div>	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)																													
		<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.10</td><td colspan="3">Ignore</td></tr><tr><td>0.10<Φ≤0.20</td><td colspan="3">3(distance ≥ 10mm)</td></tr><tr><td>0.20<Φ≤0.25</td><td colspan="3">2</td></tr><tr><td>Φ > 0.25</td><td colspan="3">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.10	Ignore			0.10<Φ≤0.20	3(distance ≥ 10mm)			0.20<Φ≤0.25	2			Φ > 0.25	0								
		Zone Size (mm)		Acceptable Qty																											
			A	B	C																										
		Φ≤0.10	Ignore																												
		0.10<Φ≤0.20	3(distance ≥ 10mm)																												
		0.20<Φ≤0.25	2																												
		Φ > 0.25	0																												
		②Dim spot (LCD/TP/Polarizer dim dot, light leakage、 dark spot)																													
		<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.1</td><td colspan="3">Ignore</td></tr><tr><td>0.10<Φ≤0.20</td><td colspan="3">3(distance ≥ 10mm)</td></tr><tr><td>0.20<Φ≤0.30</td><td colspan="3">2</td></tr><tr><td>Φ > 0.30</td><td colspan="3">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.1	Ignore			0.10<Φ≤0.20	3(distance ≥ 10mm)			0.20<Φ≤0.30	2			Φ > 0.30	0								
Zone Size (mm)	Acceptable Qty																														
	A	B	C																												
Φ≤0.1	Ignore																														
0.10<Φ≤0.20	3(distance ≥ 10mm)																														
0.20<Φ≤0.30	2																														
Φ > 0.30	0																														
③ Polarizer accidented spot																															
<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.2</td><td colspan="3">Ignore</td></tr><tr><td>0.3<Φ≤0.5</td><td colspan="3">2(distance ≥ 10mm)</td></tr><tr><td>Φ>0.5</td><td colspan="3">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.2	Ignore			0.3<Φ≤0.5	2(distance ≥ 10mm)			Φ>0.5	0														
Zone Size (mm)		Acceptable Qty																													
	A	B	C																												
Φ≤0.2	Ignore																														
0.3<Φ≤0.5	2(distance ≥ 10mm)																														
Φ>0.5	0																														
Line defect (LCD/TP /Polarizer black/white line, scratch, stain)	<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="3">Ignore</td></tr><tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="3">N≤2</td></tr><tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="3">N≤2</td></tr><tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr></table>			Width(mm)	Length(mm)	Acceptable Qty			A	B	C	Φ≤0.03	Ignore	Ignore			0.03<W≤0.05	L≤3.0	N≤2			0.05<W≤0.08	L≤2.0	N≤2			0.08<W	Define as spot defect			
	Width(mm)	Length(mm)	Acceptable Qty																												
			A	B	C																										
	Φ≤0.03	Ignore	Ignore																												
	0.03<W≤0.05	L≤3.0	N≤2																												
	0.05<W≤0.08	L≤2.0	N≤2																												
0.08<W	Define as spot defect																														

3.0	Polarizer Bubble	<div><div>Zone</div><div>Size (mm)</div></div>	Acceptable Qty		
		A	B	C	
		Ignore		Ignore	
		3(distance ≥ 10□m)			
		2			
		0			

4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.
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		TP bubble/ accidented spot	<table><tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr><tr><td>A</td><td>B</td><td>C</td></tr><tr><td>$\Phi \leq 0.1$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.1 < \Phi \leq 0.25$</td><td colspan="2">3 (distance \geq</td></tr><tr><td>$0.25 < \Phi \leq 0.3$</td><td colspan="2">2</td></tr><tr><td>$0.3 < \Phi$</td><td colspan="2">0</td></tr></table>			Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.1$	Ignore		Ignore	$0.1 < \Phi \leq 0.25$	3 (distance \geq		$0.25 < \Phi \leq 0.3$	2		$0.3 < \Phi$	0	
Size Φ (mm)	Acceptable Qty																								
	A		B	C																					
$\Phi \leq 0.1$	Ignore		Ignore																						
$0.1 < \Phi \leq 0.25$	3 (distance \geq																								
$0.25 < \Phi \leq 0.3$	2																								
$0.3 < \Phi$	0																								
		Assembly deflection	beyond the edge of backlight $\leq 0.15\text{mm}$																						

5.0	TP Related	Newton Ring	Newton Ring area>1/3 TP area NG			 1 规律性					
			Newton Ring area≤1/3 TP area OK				 2 非规律性				
					 似牛顿环						
TP corner broken		<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thicknes</td></tr></table>	X	Y	Z	X≤3.0mm	Y≤3.0mm	Z<LCD thicknes			
X	Y	Z									
X≤3.0mm	Y≤3.0mm	Z<LCD thicknes									
TP edge broken		<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thicknes</td></tr></table>	X	Y	Z	X≤6.0mm	Y≤2.0mm	Z<LCD thicknes			
X	Y	Z									
X≤6.0mm	Y≤2.0mm	Z<LCD thicknes									

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

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常备库存
Stock For Sale

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range

9. Reliability Test Result

9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	-30℃, 96HR	3ea	pass	-
ESD test	150pF, 330Ω, ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

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常备库存
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NO MOQ

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10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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11. Packing

----TBD-----

ISO9001 : 2008 ISO/TS16949 : 2009

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