Rzeszów 2010

Problem report document

Dcoument Revision V1_0

Problem report oryginator	Michał Wołowik	Problem report date	16.XII.2010
PCB,Schematic revision	V3_0	Project name	Laboratory supply
Software revision	V1_0 testing	OS revision	FreeRTOS V6.0.5

1. Document abstract

Intention of current document is describe in detail problem which appear for enginnering problem during construction and testing phase.

Document should consist of:

- Regarding to hardware part
 - Current schematic screen of schematic where located problem.
 - Current pcb document screen of part where located problem.
- Regarding to software part
 - Source code where is probability of bad working and related with it necessary code
 - Functional algorithms

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2. Problem description

Hardware part:

During testing of power board version V3_0 found a few following problems:

1. Problem with voltage regulator. Part of schematic figured below.

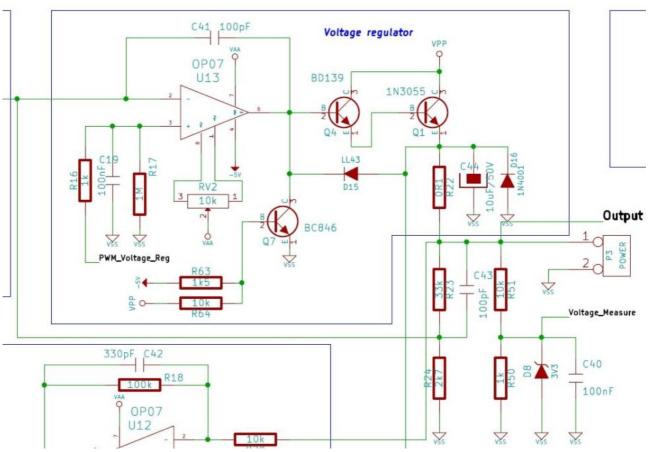


Figure 1. Voltage regulation part

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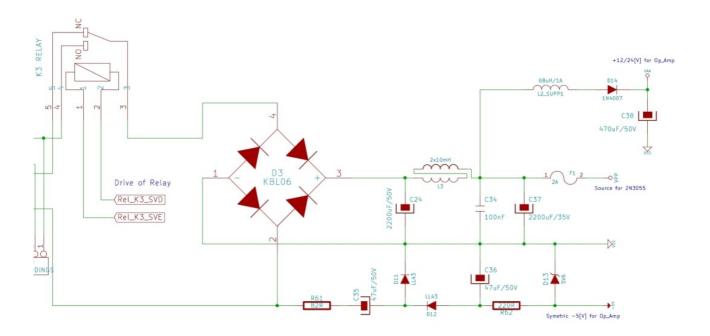


Figure 2. Transformer and rectifier part

Problem description in detail.

During first run of power regulation module occure bad working of U13 chip (OP07). Problem appear when relay switch from ~24[V] to ~12[V]. This voltage reduction casue problem. When voltage is near low comparator limit and if comparator turn on lower windings ~12[V] during transition operation relay generate peek which go to – input of U13. After that U13 very quickly increment voltage about few voltage and active again comparator, after that when capacitor discharging comparator again connect to lower windings of transformer and all process again. The result is not stabil voltage, amplifier became generator. To see relay commutation look at below figures.

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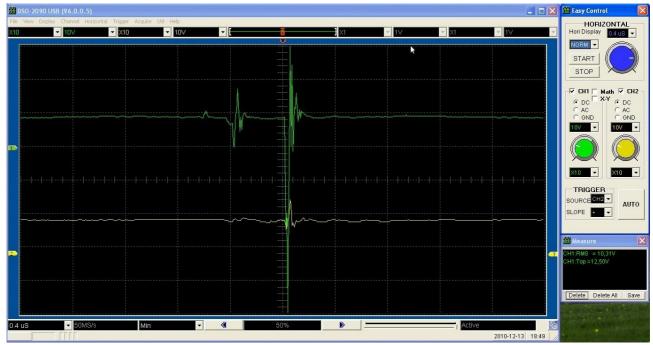


Figure 3. Relay gitter – very high peek on output

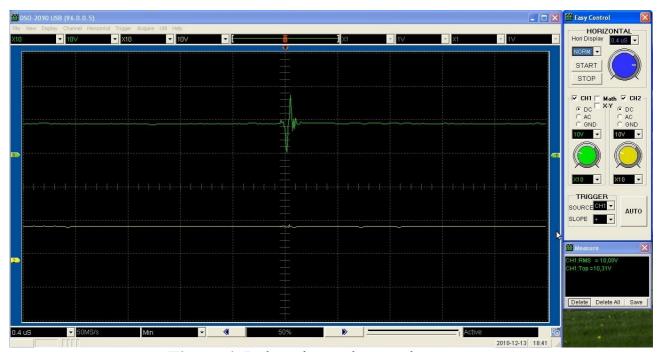


Figure 4. Relay gitter – low peek on output

Solution proposition.

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