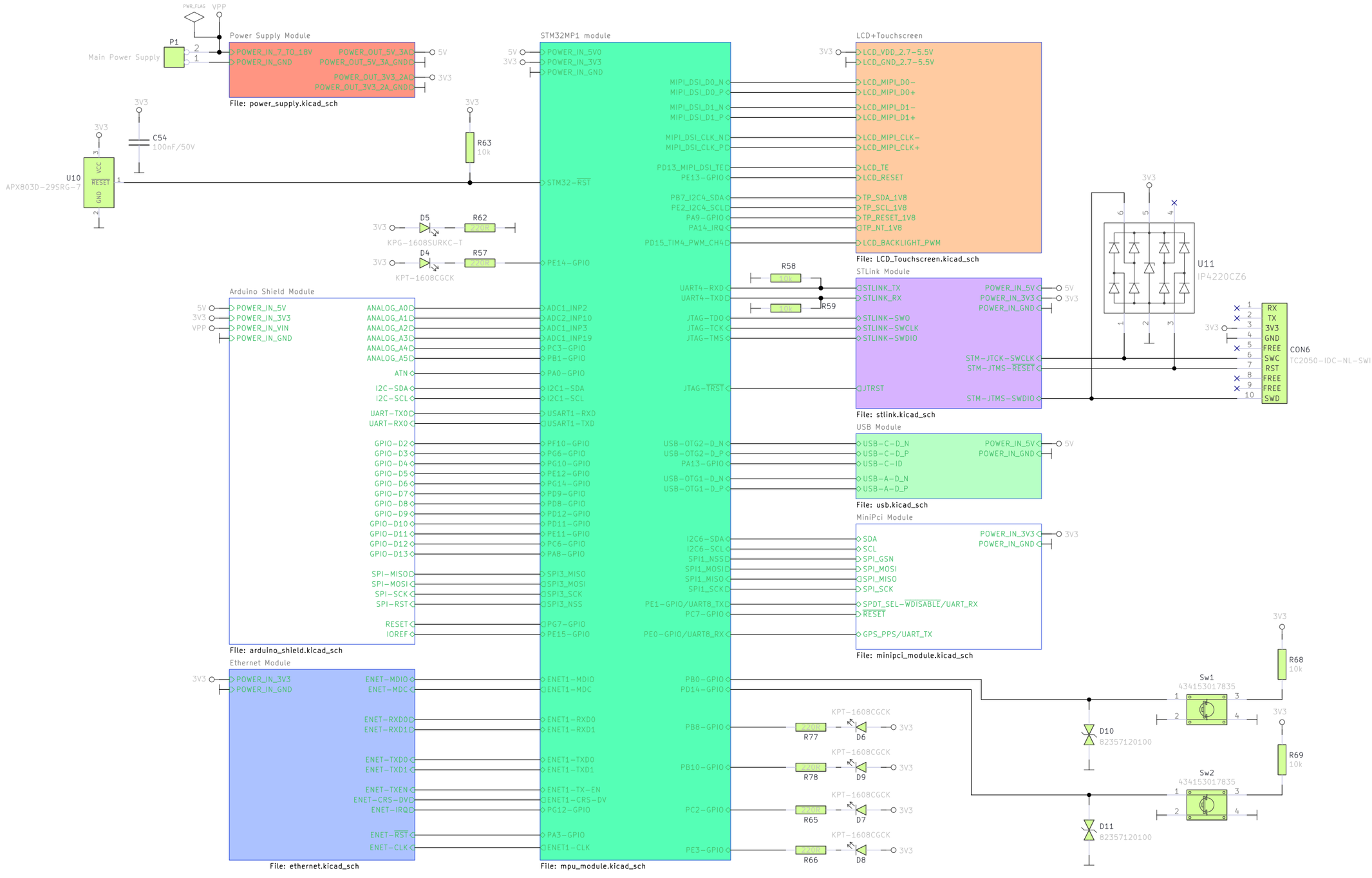


KiCad Logo

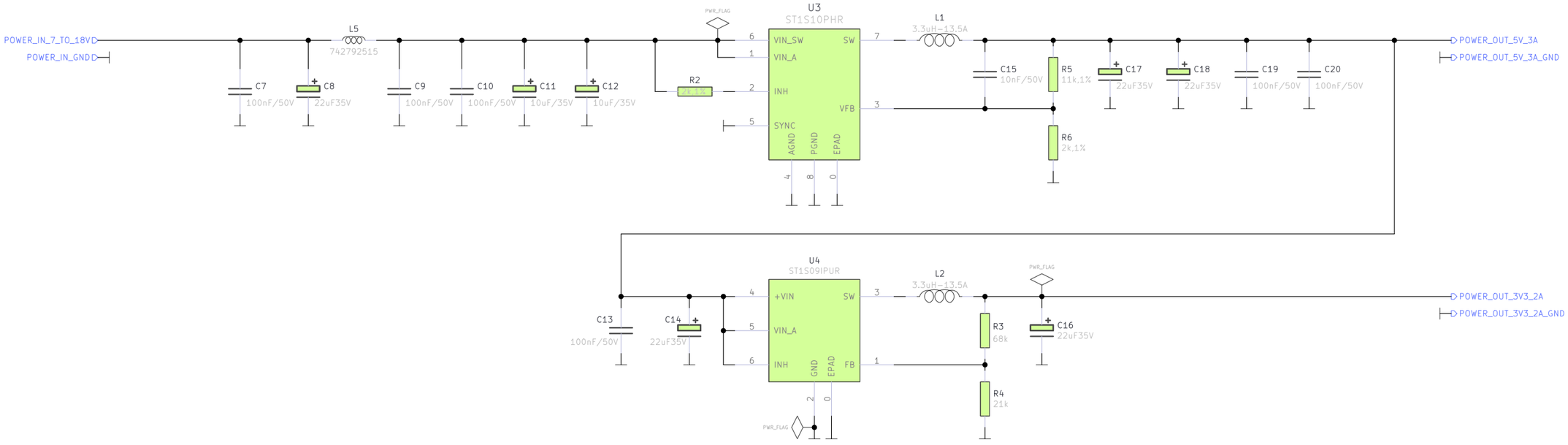
Sofjan

Sheet: /

File: stm32mp1-custom-devboard.kicad_sch

Title: stm32mp1-custom-devboard

Size: A3	Date: 2020-12-19	**Rev: V3.0**
KiCad E.D.A. kicad (6.0.0)		Id: 1/11

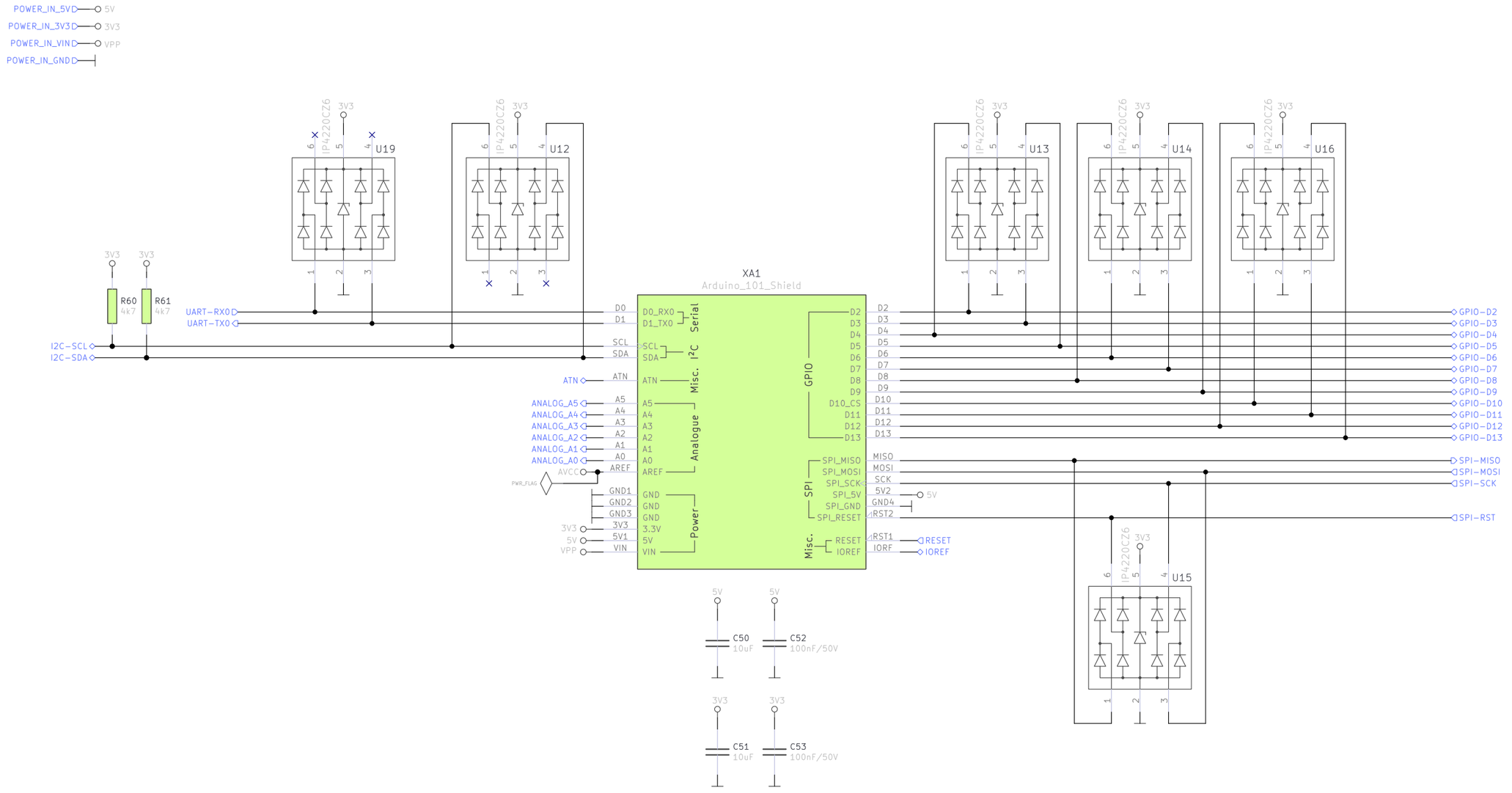


Embedded System Labs

Sheet: /Power Supply Module/
File: power_supply.kicad_sch

Title: Power Supply Module 5V/3V3

Size: A3	Date: 2020-12-19	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.0)		Id: 2/11

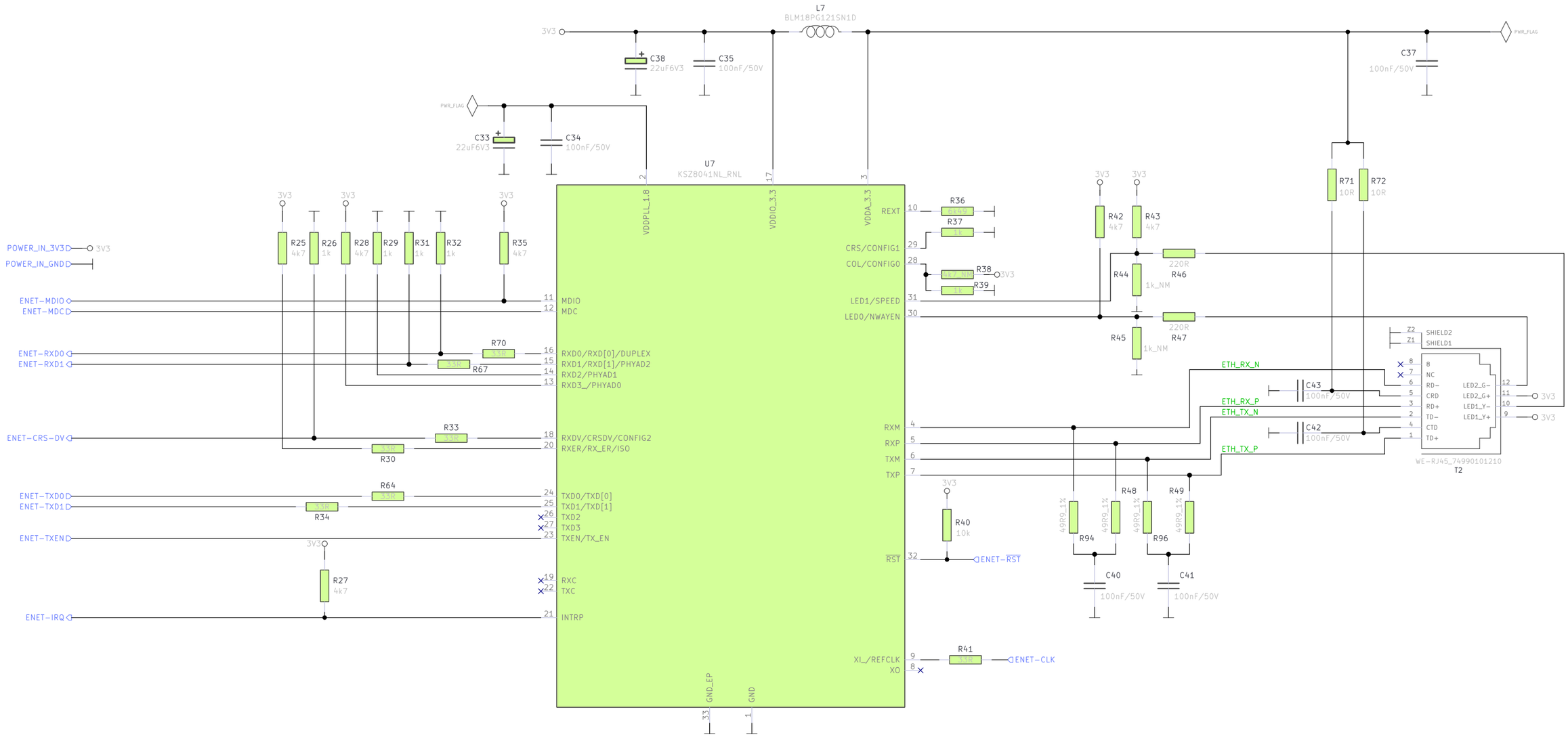


Embedded System Module

Sheet: /Arduino Shield Module/
File: arduino_shield.kicad_sch

Title: Arduino Shield Module

Size: A3	Date: 2020-12-20	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.0)		Id: 3/11



Track width 4.75mil for all

PHYAD2	Ipd/O	The PHY Address is latched at power-up or reset and is configurable to any value from 1 to 7. The default PHY Address is 00001. PHY Address bits [4:3] are always set to '00'.
PHYAD1	Ipd/O	
PHYAD0	Ipu/O	

MII and RMII Routing Guidelines

All connections on a PCB in MII and RMII routing are point-to-point connections. Although MII and RMII use relatively low data rates, the limiting parameter that determines whether a trace can act as a transmission line is the signal rise/fall time. Unless your board is very large or your signal switching speed is very fast, reflections at the end of each connection can be ignored.
The recommended trace impedance in MII is 50 Ohms +/- 10%.
Although the trace length between the PHY and MAC is generally short enough to ignore transmission line effects, you should pay attention to impedance when routing the signal and clock traces when the traces are electrically long.
Since MII and RMII require clock signals between the PHY and MAC, best practices for routing clock signals should be used with longer traces. Generally, you should avoid the use of vias on traces carrying clock signals on board with impedance control as the trace impedance can be different between layers. However, as long as the impedance in each layer is carefully controlled to the right value, then the clock signals can certainly be routed through vias. This will prevent signal reflections on longer clock traces.
For the above reasons, all MII/RMII signal traces should be routed as short as possible on a single layer, and traces should be routed in a straight path. If you must turn a corner with a signal trace, the trace should bend by no more than 45 degrees.
Clock lines should also be shielded with GND lines to prevent crosstalk through capacitive coupling, especially when longer traces are necessary. Because the TX and RX data signals are triggered by the rising edge of the clock, communication in MII and RMII is synchronous. Thus, the data lines and the clock line between the MAC and PHY should be length matched. The allowed deviation in length matching depends on the rise/fall time for digital signals between these two elements, although it is generally recommended that any deviation be less than 10 mm as MII and RMII use TTL logic.
Again, the allowed trace length mismatch depends on the rise/fall time of digital signals.

CONFIG[2:0]	Mode
000	MII (default)
001	RMII
010	Reserved - not used
011	Reserved - not used
100	MII 100 Mbps Preamble Restore
101	Reserved - not used
110	Reserved - not used
111	Reserved - not used

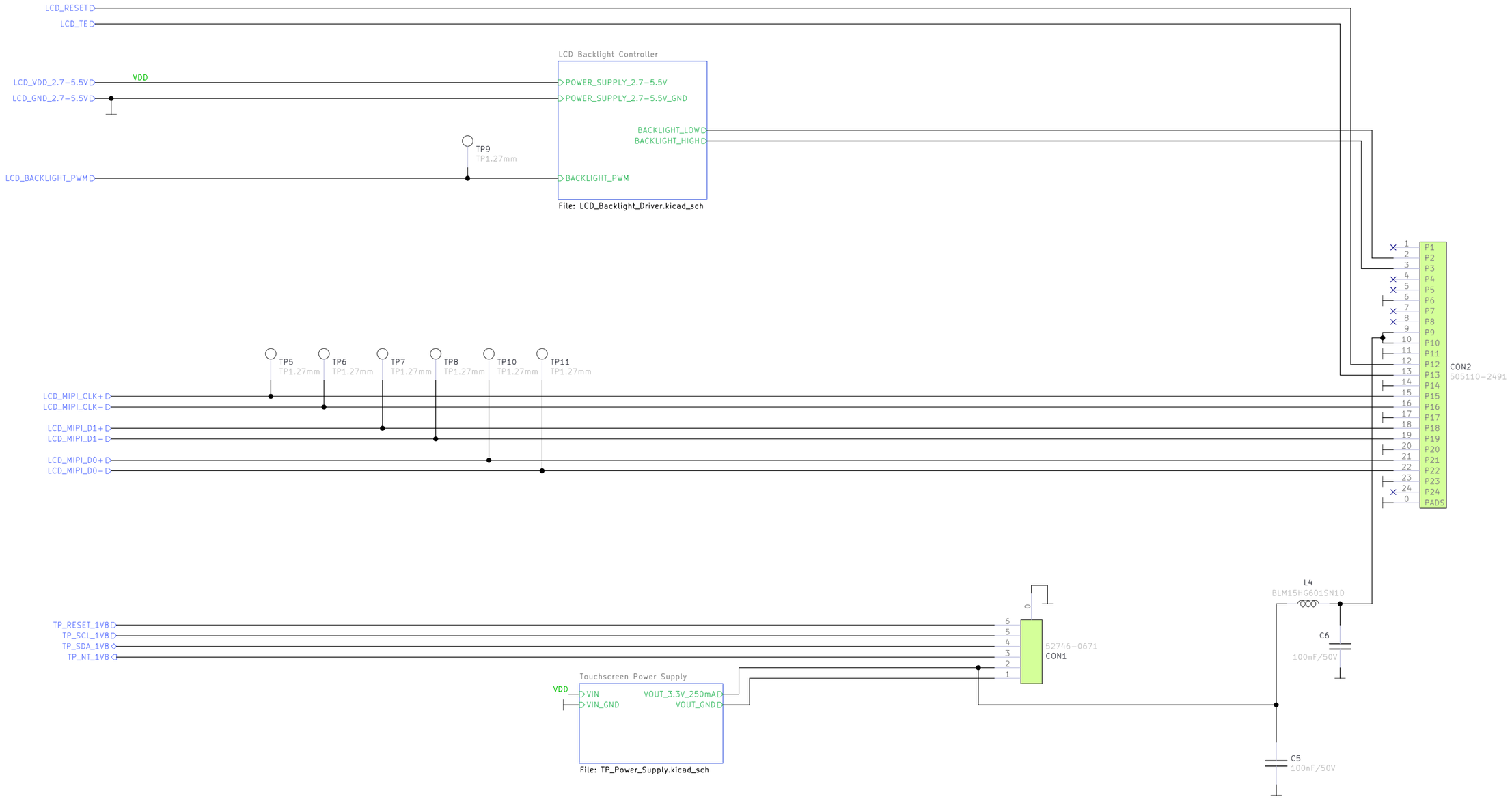
Embedded System Labs

Sheet: /Ethernet Module/
File: ethernet.kicad_sch

Title: Ethernet

Size: A3	Date: 2021-01-13	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.0)		Id: 4/11

SOM1A
VisionSOM-STM32MP1
POWER_IN_5V0
POWER_IN_3V3
POWER_IN_GND
5V
3V3
NC
GND
VDD_3V3
VDD_COIN_3V
+3.3VOUT
+5VIN
PWR_FLAG
C55
C56
100nF/50V
F1
FF_PW_1A0
Boot Mode | BOOT2 | BOOT1 | BOOT0
Recovery | 0 | 0 | 0
NOR | 0 | 0 | 1
eMMC | 0 | 1 | 0
NAND | 0 | 1 | 1
Reserved | 1 | 0 | 0
SD-Card | 1 | 0 | 1
Recovery | 1 | 1 | 0
SPI-NAND | 1 | 1 | 1
R51 10k
R53 10k
R55 10k
R52 10k
R54 10k
R56 10k
BOOT0
BOOT1
BOOT2
PWR_ON
PWR_LP
JTAG_TDI
JTAG_TMS
JTAG_nTRST
JTAG_TDO
JTAG_TCK
STM32_nRST
PADS
SOM1B
VisionSOM-STM32MP1
SOM1D
VisionSOM-STM32MP1
ENET1-MDIO
ENET1-CRS-DV
ENET1-CLK
PA3-GPIO
PA8-GPIO
PA9-GPIO
PA14_IRQ
PA13-GPIO
SPI3_NSS
SPI1_NSS
ADC1_INP3
ADC1_INP19
I2C6-SDA
I2C6-SCL
PA0-GPIO
PA2_TIM2_CH3,TIM5_CH3,LPTIM4_OUT,TIM15_CH1,USART2_TX,SAI2_SCK_B,SDMMC2_D0DIR,_ETH1_MDIO,_MDIOS_MDIO,_LCD_R1,_EVENTOUT,_ADC1_INP14,_WKUP2
PA7_TIM1_CH1N,TIM3_CH2,TIM8_CH1N,SAI4_D1,SPI1_MOSI/I2S1_SDO,SPI6_MOSI,TIM14_CH1,QUADSPI_CLK,ETH1_GMII_RX_DV/ETH1_MII_RX_DV/ETH1_RGMII_RX_CTL/ETH1_RMII_CRS_DV,SAI4_SD_A,_EVENTOUT,ADC1_INP7,ADC1_INN3,ADC2_INP7,ADC2_INN3
PA1_ETH_CLK,TIM2_CH2,TIM5_CH2,LPTIM3_OUT,TIM15_CH1N,USART2_RTS/USART2_DE,UART4_RX,QUADSPI_BK1_IO3,SAI2_MCLK_B,ETH1_GMII_RX_CLK/ETH1_MII_RX_CLK/ETH1_RGMII_RX_CLK/ETH1_RMII_REF_CLK,LCD_R2,EVENTOUT,ADC1_INP17,ADC1_INN16
PA3_TIM2_CH4,TIM5_CH4,LPTIM5_OUT,TIM15_CH2,USART2_RX,LCD_B2,ETH1_GMII_COL/ETH1_MII_COL,LCD_B5,EVENTOUT,ADC1_INP15,PVD_IN
PA8_MCO1,TIM1_CH1,TIM8_BKIN2,I2C3_SCL,SPI3_MOSI/I2S3_SDO,USART1_CK,SDMMC2_CKIN,SDMMC2_D4,OTG_FS_SOF/OTG_HS_SOF,SAI4_SD_B,UART7_RX,LCD_R6,EVENTOUT,
PA9_TIM1_CH2,I2C3_SMBA,SPI2_SCK/I2S2_CK,USART1_TX,SDMMC2_CDIR,SDMMC2_D5,DCMI_D0,LCD_R5,EVENTOUT
PA14_DBTRGO,DBTRGI,MCO2,EVENTOUT
PA13_DBTRGO,DBTRGI,MCO1,UART4_TX,EVENTOUT,BOOTFAILN
PA10_TIM1_CH3,SPI3_NSS/I2S3_WS,USART1_RX,MDIOS_MDIO,SAI4_FS_B,DCMI_D1,LCD_B1,EVENTOUT,OTG_FS_ID,OTG_HS_ID
PA4_HDP0,TIM5_ETR,SAI4_D2,SPI1_NSS/I2S1_WS,SPI3_NSS/I2S3_WS,USART2_CK,SPI6_NSS,SAI4_FS_A,DCMI_HSYNC,LCD_VSYNC,EVENTOUT,ADC1_INP18,ADC2_INP18,DAC_OUT1
PA6_TIM1_BKIN,TIM3_CH1,TIM8_BKIN,SAI4_CK2,SPI1_MISO/I2S1_SDI,SPI6_MISO,TIM13_CH1,MDIOS_MDC,SAI4_SCK_A,DCMI_PIXCLK,LCD_G2,EVENTOUT,ADC1_INP3,ADC2_INP3
PA5_TIM2_CH1/TIM2_ETR,TIM8_CH1N,SAI4_CK1,SPI1_SCK/I2S1_CK,SPI6_SCK,SAI4_MCLK_A,LCD_R4,EVENTOUT,ADC1_INP19,ADC1_INN18,ADC2_INP19,ADC2_INN18,DAC_OUT2
PA12_TIM1_ETR,I2C6_SDA,I2C5_SDA,UART4_TX,USART1_RTS/USART1_DE,SAI2_FS_B,FDCAN1_TX,LCD_R5,EVENTOUT,OTG_FS_DP
PA11_TIM1_CH4,I2C6_SCL,I2C5_SCL,SPI2_NSS/I2S2_WS,UART4_RX,USART1_CTS/USART1_NSS,FDCAN1_RX,LCD_R4,EVENTOUT,OTG_FS_DM
PA0_TIM2_CH1/TIM2_ETR,TIM5_CH1,TIM8_ETR,TIM15_BKIN,USART2_CTS/USART2_NSS,UART4_TX,SDMMC2_CMD,SAI2_SD_B,ETH1_GMII_CRS/ETH1_MII_CRS,EVENTOUT
SOM1E
VisionSOM-STM32MP1
SPI1_SCK
USART1-RXD
SPI1_MISO
USART1-TXD
PB8-GPIO
UART4-RXD
I2C1-SCL
I2C1-SDA
PB10-GPIO
PB0-GPIO
ENET1-TXD1
SPI1_MOSI
ENET1-TX-EN
PB1-GPIO
PB7_I2C4_SDA
R7 4k7
PB3_TRACED9,TIM2_CH2,SAI4_CK1,SPI1_SCK/I2S1_CK,SPI3_SCK/I2S3_CK,SPI6_SCK,SDMMC2_D2,SAI4_MCLK_A,UART7_RX,EVENTOUT
PB15_RTC_REFIN,TIM1_CH3N,TIM12_CH2,TIM8_CH3N,USART1_RX,SPI2_MOSI/I2S2_SDO,DFSDM1_CKIN2,SDMMC2_D1,EVENTOUT
PB4_TRACED8,TIM16_BKIN,TIM3_CH1,SAI4_CK2,SPI1_MISO/I2S1_SDI,SPI3_MISO/I2S3_SDI,SPI2_NSS/I2S2_WS,SPI6_MISO,SDMMC2_D3,SAI4_SCK_A,UART7_TX,EVENTOUT
PB14_TIM1_CH2N,TIM12_CH1,TIM8_CH2N,USART1_TX,SPI2_MISO/I2S2_SDI,DFSDM1_DATIN2,USART3_RTS/USART3_DE,SDMMC2_D0,EVENTOUT
PB8_HDP6,TIM16_CH1,TIM4_CH3,DFSDM1_CKIN7,I2C1_SCL,SDMMC1_CKIN,I2C4_SCL,SDMMC2_CKIN,UART4_RX,FDCAN1_RX,SDMMC2_D4,ETH1_GMII_TXD3/ETH1_MII_TXD3/ETH1_RGMII_TXD3,SDMMC1_D4,DCMI_D6,LCD_B6,_EVENTOUT
PB2_TRACED4,RTC_OUT2,SAI1_D1,DFSDM1_CKIN1,USART1_RX,I2S_CKIN,SAI1_SD_A,SPI3_MOSI/I2S3_SDO,UART4_RX,QUADSPI_CLK,EVENTOUT
PB6_TIM16_CH1N,TIM4_CH1,I2C1_SCL,_CEC,I2C4_SCL,USART1_TX,FDCAN2_TX,QUADSPI_BK1_NCS,DFSDM1_DATIN5,UART5_TX,DCMI_D5,EVENTOUT
PB9_HDP7,TIM17_CH1,TIM4_CH4,DFSDM1_DATIN7,I2C1_SDA,SPI2_NSS/I2S2_WS,I2C4_SDA,SDMMC2_CDIR,UART4_TX,FDCAN1_TX,SDMMC2_D5,SDMMC1_CDIR,SDMMC1_D5,DCMI_D7,LCD_B7,EVENTOUT
PB10_TIM2_CH3,LPTIM2_IN1,I2C2_SCL,SPI2_SCK/I2S2_CK,DFSDM1_DATIN7,USART3_TX,QUADSPI_BK1_NCS,ETH1_GMII_RX_ER/ETH1_MII_RX_ER,LCD_G4,EVENTOUT
PB0_TIM1_CH2N,TIM3_CH3,TIM8_CH2N,DFSDM1_CKOUT,UART4_CTS,LCD_R3,ETH1_GMII_RXD2/ETH1_MII_RXD2/ETH1_RGMII_RXD2,MDIOS_MDIO,LCD_G1,EVENTOUT,ADC1_INP9,ADC1_INN5,ADC2_INP9,ADC2_INN5
PB13_TIM1_CH1N,DFSDM1_CKOUT,LPTIM2_OUT,SPI2_SCK/I2S2_CK,DFSDM1_CKIN1,USART3_CTS/USART3_NSS,FDCAN2_TX,ETH1_GMII_TXD1/ETH1_MII_TXD1/ETH1_RGMII_TXD1/ETH1_RMII_TXD1,UART5_TX,EVENTOUT
PB5_ETH_CLK,TIM17_BKIN,TIM3_CH2,SAI4_D1,I2C1_SMBA,SPI1_MOSI/I2S1_SDO,I2C4_SMBA,SPI3_MOSI/I2S3_SDO,SPI6_MOSI,FDCAN2_RX,SAI4_SD_A,ETH1_PPS_OUT,UART5_RX,DCMI_D10,LCD_G7,EVENTOUT
PB11_TIM2_CH4,LPTIM2_ETR,I2C2_SDA,DFSDM1_CKIN7,USART3_RX,ETH1_GMII_TX_EN/ETH1_MII_TX_EN/ETH1_RGMII_TX_CTL/ETH1_RMII_TX_EN,DSI_TE,LCD_G5,EVENTOUT
PB1_TIM1_CH3N,TIM3_CH4,TIM8_CH3N,DFSDM1_DATIN1,LCD_R6,ETH1_GMII_RXD3/ETH1_MII_RXD3/ETH1_RGMII_RXD3,MDIOS_MDC,LCD_G0,EVENTOUT,ADC1_INP5,ADC2_INP5
PB7_TIM17_CH1N,TIM4_CH2,I2C1_SDA,I2C4_SDA,USART1_RX,SDMMC2_D1,DFSDM1_CKIN5,FMC_NL,DCMI_VSYNC,EVENTOUT
SOM1F
VisionSOM-STM32MP1
PC7-GPIO
SPI3_SCK
PC2-GPIO
ENET1-RXD1
ENET1-RXD0
ADC2_INP10
ENET1-MDC
PC3-GPIO
PC6-GPIO
PC7_HDP4,TIM3_CH2,TIM8_CH2,DFSDM1_DATIN3,I2S3_MCK,USART6_RX,SDMMC1_D123DIR,SDMMC2_D123DIR,SDMMC2_D7,SDMMC1_D7,DCMI_D1,LCD_G6,EVENTOUT
PC10_TRACED2,DFSDM1_CKIN5,SPI3_SCK/I2S3_CK,USART3_TX,UART4_TX,QUADSPI_BK1_IO1,SAI4_MCLK_B,SDMMC1_D2,DCMI_D8,LCD_R2,EVENTOUT
PC2_DFSDM1_CKIN1,SPI2_MISO/I2S2_SDI,DFSDM1_CKOUT,ETH1_GMII_TXD2/ETH1_MII_TXD2/ETH1_RGMII_TXD2,DCMI_PIXCLK,EVENTOUT,ADC1_INP12,ADC1_INN11
PC5_SAI1_D3,DFSDM1_DATIN2,SAI4_D4,_SAI1_D4,SPDIFRX_IN3,ETH1_GMII_RXD1/ETH1_MII_RXD1/ETH1_RGMII_RXD1/ETH1_RMII_RXD1,_SAI4_D3,EVENTOUT,ADC1_INP8,ADC1_INN4,ADC2_INP8,ADC2_INN4
PC4_DFSDM1_CKIN2,I2S1_MCK,SPDIFRX_IN2,ETH1_GMII_RXD0/ETH1_MII_RXD0/ETH1_RGMII_RXD0/ETH1_RMII_RXD0,EVENTOUT,ADC1_INP4,ADC2_INP4
PC0_DFSDM1_CKIN0,LPTIM2_IN2,DFSDM1_DATIN4,SAI2_FS_B,QUADSPI_BK2_NCS,LCD_R5,EVENTOUT,ADC1_INP10,ADC2_INP10
PC1_TRACED0,SAI1_D1,DFSDM1_DATIN0,DFSDM1_CKIN4,SPI2_MOSI/I2S2_SDO,SAI1_SD_A,SDMMC2_CK,ETH1_MDC,MDIOS_MDC,EVENTOUT,ADC1_INP11,ADC1_INN10,ADC2_INP11,ADC2_INN10,TAMP_IN3,WKUP6
PC3_TRACECLK,DFSDM1_DATIN1,SPI2_MOSI/I2S2_SDO,ETH1_GMII_TX_CLK/ETH1_MII_TX_CLK,EVENTOUT,ADC1_INP13,ADC1_INN12
PC6_HDP1,TIM3_CH1,TIM8_CH1,DFSDM1_CKIN3,I2S2_MCK,USART6_TX,SDMMC1_D0DIR,SDMMC2_D0DIR,SDMMC2_D6,DSI_TE,SDMMC1_D6,DCMI_D0,LCD_HSYNC,EVENTOUT
R8 4k7
PE2_I2C4_SCL
PE3-GPIO
PE13-GPIO
PE14-GPIO
PE0-GPIO/UART8_RX
PE1-GPIO/UART8_TX
PE12-GPIO
PE11-GPIO
PE15-GPIO
PE3_TRACED0,TIM15_BKIN,SAI1_SD_B,SDMMC2_CK,FMC_A19,EVENTOUT
PE13_HDP2,TIM1_CH3,DFSDM1_CKIN5,SPI4_MISO,SAI2_FS_B,FMC_D10/FMC_DA10,DCMI_D6,LCD_DE,EVENTOUT
PE14_TIM1_CH4,SPI4_MOSI,UART8_RTS/UART8_DE,SAI2_MCLK_B,SDMMC1_D123DIR,FMC_D11/FMC_DA11,LCD_G0,LCD_CLK,EVENTOUT
PE2_TRACECLK,SAI1_CK1,I2C4_SCL,SPI4_SCK,SAI1_MCLK_A,QUADSPI_BK1_IO2,ETH1_GMII_TXD3/ETH1_MII_TXD3/ETH1_RGMII_TXD3,FMC_A23,EVENTOUT
PE0_LPTIM1_ETR,TIM4_ETR,LPTIM2_ETR,SPI3_SCK/I2S3_CK,SAI4_MCLK_B,UART8_RX,SAI2_MCLK_A,FMC_NBL0,DCMI_D2,EVENTOUT
PE1_LPTIM1_IN2,I2S2_MCK,SAI3_SD_B,UART8_TX,FMC_NBL1,DCMI_D3,EVENTOUT
PE12_TIM1_CH3N,DFSDM1_DATIN5,SPI4_SCK,SDMMC1_D0DIR,SAI2_SCK_B,FMC_D9/FMC_DA9,LCD_B4,EVENTOUT
PE11_TIM1_CH2,DFSDM1_CKIN4,SPI4_NSS,USART6_CK,SAI2_SD_B,FMC_D8/FMC_DA8,DCMI_D4,LCD_G3,EVENTOUT
PE15_HDP3,TIM1_BKIN,TIM15_BKIN,USART2_CTS/USART2_NSS,UART8_CTS,FMC_NCE2,FMC_D12/FMC_DA12,LCD_R7,EVENTOUT
SOM1H VisionSOM-STM32MP1
SOM1C
VisionSOM-STM32MP1
USB-OTG2-D_P
USB-OTG2-D_N
USB-OTG1-D_P
USB-OTG1-D_N
USB_OTG2_VBUS
USB_OTG2_DP
USB_OTG2_DN
USB_OTG1_DP
USB_OTG1_DN
SOM1I
VisionSOM-STM32MP1
ADC1_INP2
PF10-GPIO
PG6-GPIO
PG10-GPIO
PG7-GPIO
UART4-TXD
PG12-GPIO
ENET1-TXD0
PG14-GPIO
PF11_SPI5_MOSI,SAI2_SD_B,DCMI_D12,LCD_G5,EVENTOUT,ADC1_INP2
PF10_PF10_TIM16_BKIN,SAI1_D3,SAI4_D4,SAI1_D4,QUADSPI_CLK,SAI4_D3,DCMI_D11,_LCD_DE,EVENTOUT
PG6_TRACED14,TIM17_BKIN,SDMMC2_CMD,DCMI_D12,LCD_R7,EVENTOUT
PG10_TRACED10,UART8_CTS,LCD_G3,SAI2_SD_B,QUADSPI_BK2_IO2,FMC_NE3,DCMI_D2,LCD_B2,EVENTOUT
PG7_TRACED5,_SAI1_MCLK_A,_USART6_CK,_UART8_RTS/UART8_DE,_QUADSPI_CLK,_QUADSPI_BK2_IO3,_DCMI_D13,_LCD_CLK,_EVENTOUT
PG11_TRACED11,USART1_TX,UART4_TX,SPDIFRX_IN0,ETH1_GMII_TX_EN/ETH1_MII_TX_EN/ETH1_RGMII_TX_CTL/ETH1_RMII_TX_EN,DCMI_D3,LCD_B3,_EVENTOUT
PG12_LPTIM1_IN1,SPI6_MISO,SAI4_CK2,USART6_RTS/USART6_DE,SPDIFRX_IN1,LCD_B4,SAI4_SCK_A,ETH1_PHY_INTN,FMC_NE4,LCD_B1,EVENTOUT
PG13_TRACED0,LPTIM1_OUT,SAI1_CK2,SAI4_CK1,SPI6_SCK,SAI1_SCK_A,USART6_CTS/USART6_NSS,SAI4_MCLK_A,ETH1_GMII_TXD0/ETH1_MII_TXD0/ETH1_RGMII_TXD0/ETH1_RMII_TXD0,FMC_A24,LCD_R0,EVENTOUT
PG14_TRACED1,LPTIM1_ETR,SPI6_MOSI,_SAI4_D1,USART6_TX,QUADSPI_BK2_IO3,SAI4_SD_A,ETH1_GMII_TXD1/ETH1_MII_TXD1/ETH1_RGMII_TXD1/ETH1_RMII_TXD1,FMC_A25,LCD_B0,EVENTOUT
SOM1J
VisionSOM-STM32MP1
MIPI_DSI_CLK_P
MIPI_DSI_CLK_N
MIPI_DSI_D1_P
MIPI_DSI_D1_N
MIPI_DSI_D0_P
MIPI_DSI_D0_N
DSI_CKP
DSI_CKN
DSI_D1P
DSI_D1N
DSI_D0P
DSI_D0N
SOM1G
VisionSOM-STM32MP1
PD15_TIM4_PWM_CH4
PD9-GPIO
PD8-GPIO
PD13_MIPI_DSI_TE
SPI3_MOSI
SPI3_MISO
PD12-GPIO
PD11-GPIO
PD14-GPIO
PD15_TIM4_CH4,SAI3_MCLK_A,UART8_CTS,FMC_D1/FMC_DA1,LCD_R1,EVENTOUT
PD9_DFSDM1_DATIN3,SAI3_SD_B,USART3_RX,FMC_D14/FMC_DA14,DCMI_HSYNC,LCD_B0,EVENTOUT
PD8_DFSDM1_CKIN3,SAI3_SCK_B,USART3_TX,SPDIFRX_IN1,FMC_D13/FMC_DA13,LCD_B7,EVENTOUT
PD13_LPTIM1_OUT,TIM4_CH2,I2C4_SDA,I2C1_SDA,I2S3_MCK,QUADSPI_BK1_IO3,SAI2_SCK_A,FMC_A18,DSI_TE,EVENTOUT
PD6_TIM16_CH1N,SAI1_D1,DFSDM1_CKIN4,DFSDM1_DATIN1,SPI3_MOSI/I2S3_SDO,SAI1_SD_A,USART2_RX,FMC_NWAIT,DCMI_D10,LCD_B2,EVENTOUT
PD10_RTC_REFIN,TIM16_BKIN,DFSDM1_CKOUT,I2C5_SMBA,SPI3_MISO/I2S3_SDI,SAI3_FS_B,USART3_CK,FMC_D15/FMC_DA15,LCD_B3,EVENTOUT
PD12_LPTIM1_IN1,TIM4_CH1,LPTIM2_IN1,I2C4_SCL,I2C1_SCL,USART3_RTS/USART3_DE,QUADSPI_BK1_IO1,SAI2_FS_A,FMC_ALE/FMC_A17,EVENTOUT
PD11_LPTIM2_IN2,I2C4_SMBA,I2C1_SMBA,USART3_CTS/USART3_NSS,QUADSPI_BK1_IO0,SAI2_SD_A,FMC_CLE/FMC_A16,EVENTOUT
PD14_TIM4_CH3,_SAI3_MCLK_B,UART8_CTS,FMC_AD0/FMC_D0,_EVENTOUT
Embedded System Labs
Sheet: /STM32MP1 module/
File: mpu_module.kicad_sch
Title: STM32MP1 Module
Size: A3
Date: 2020-12-19
Rev: V1.0
KiCad E.D.A. kicad (6.0.0)
Id: 5/11

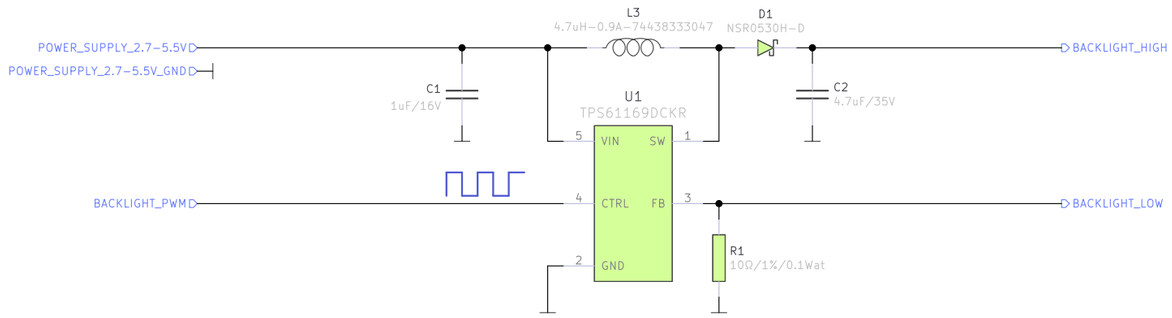


5.0 IPS 720X1280 MIPI +CTP
PH720128T004-ZBC02
Embedded System Labs

Sheet: /LCD+Touchscreen/
File: LCD_Touchscreen.kicad_sch

Title: LCD MiPi and Touchscreen module

Size: A3	Date: 2020-12-19	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.0)		Id: 6/11

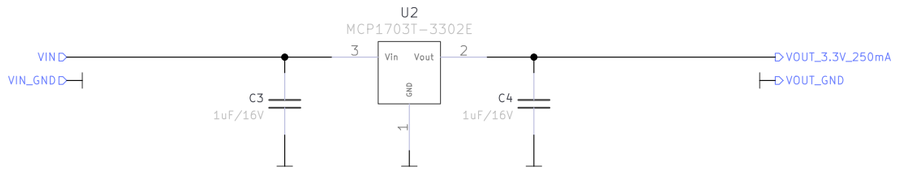


Embedded System Labs

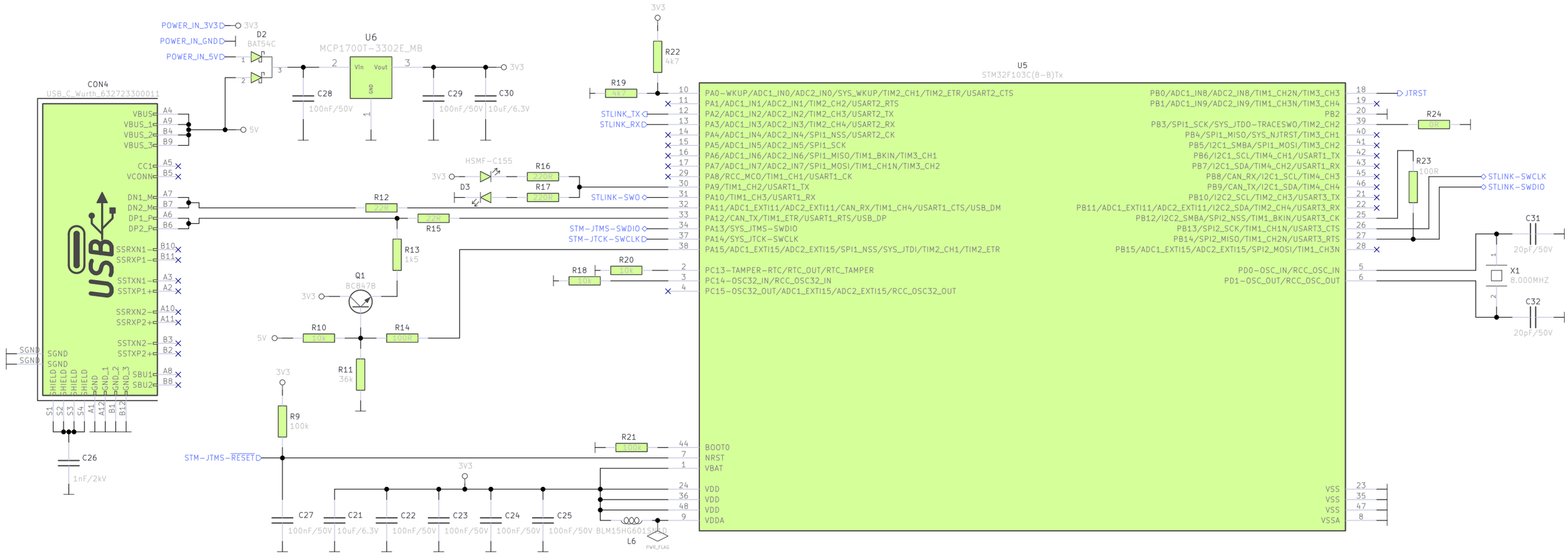
Sheet: /LCD+Touchscreen/LCD Backlight Controller/
File: LCD_Backlight_Driver.kicad_sch

Title: LCD Backlight Controller

Size: A3	Date: 2020-12-19	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.0)		Id: 7/11



Embedded System Labs		
Sheet: /LCD+Touchscreen/Touchscreen Power Supply/		
File: TP_Power_Supply.kicad_sch		
Title: 2.8V LDO Regulator		
Size: A3	Date: 2020-12-19	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.0)		Id: 8/11

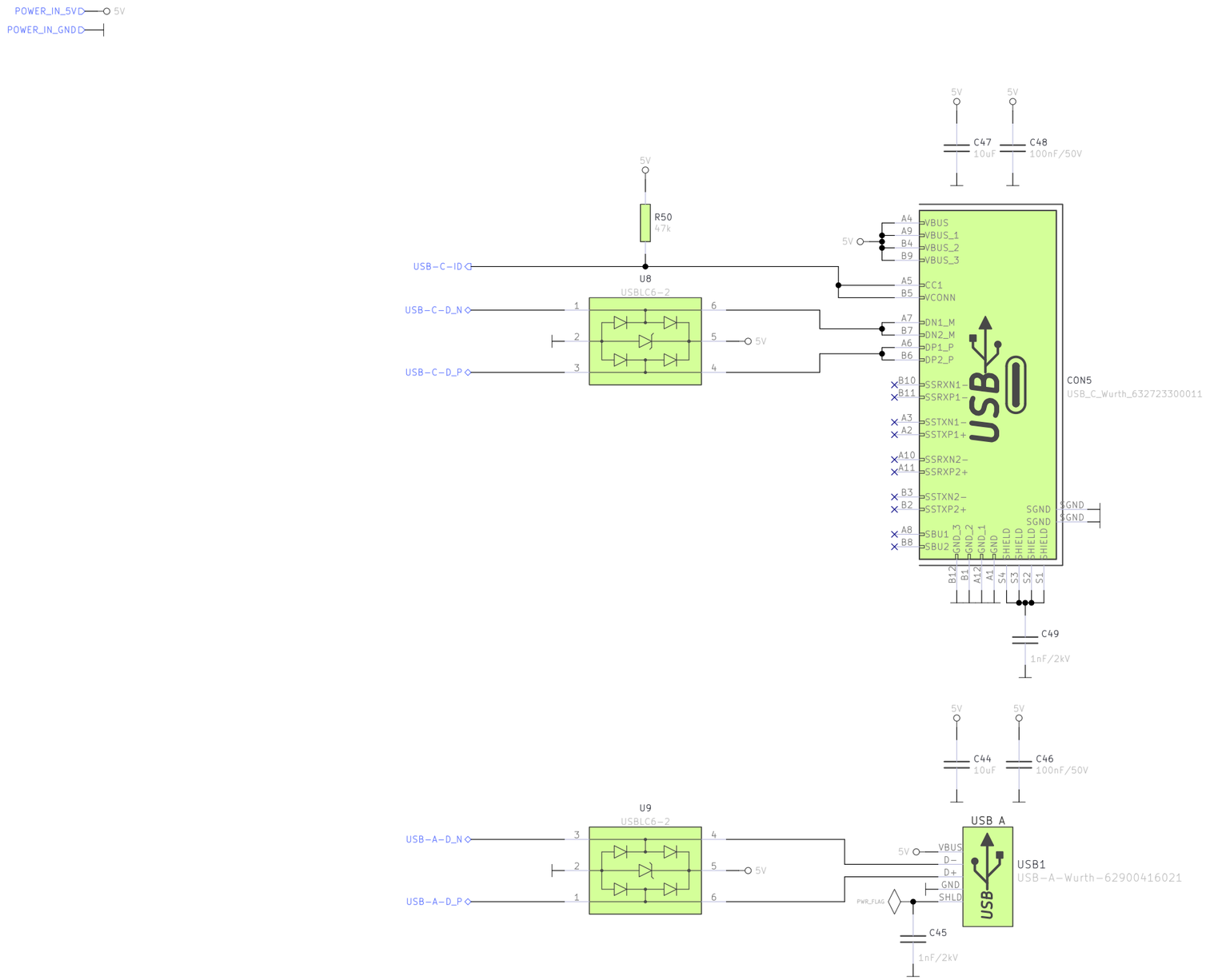


Embedded System Labs

Sheet: /STLink Module/
File: stlink.kicad_sch

Title: STLink Module

Size: A3	Date: 2020-12-20	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.0)		Id: 9/11

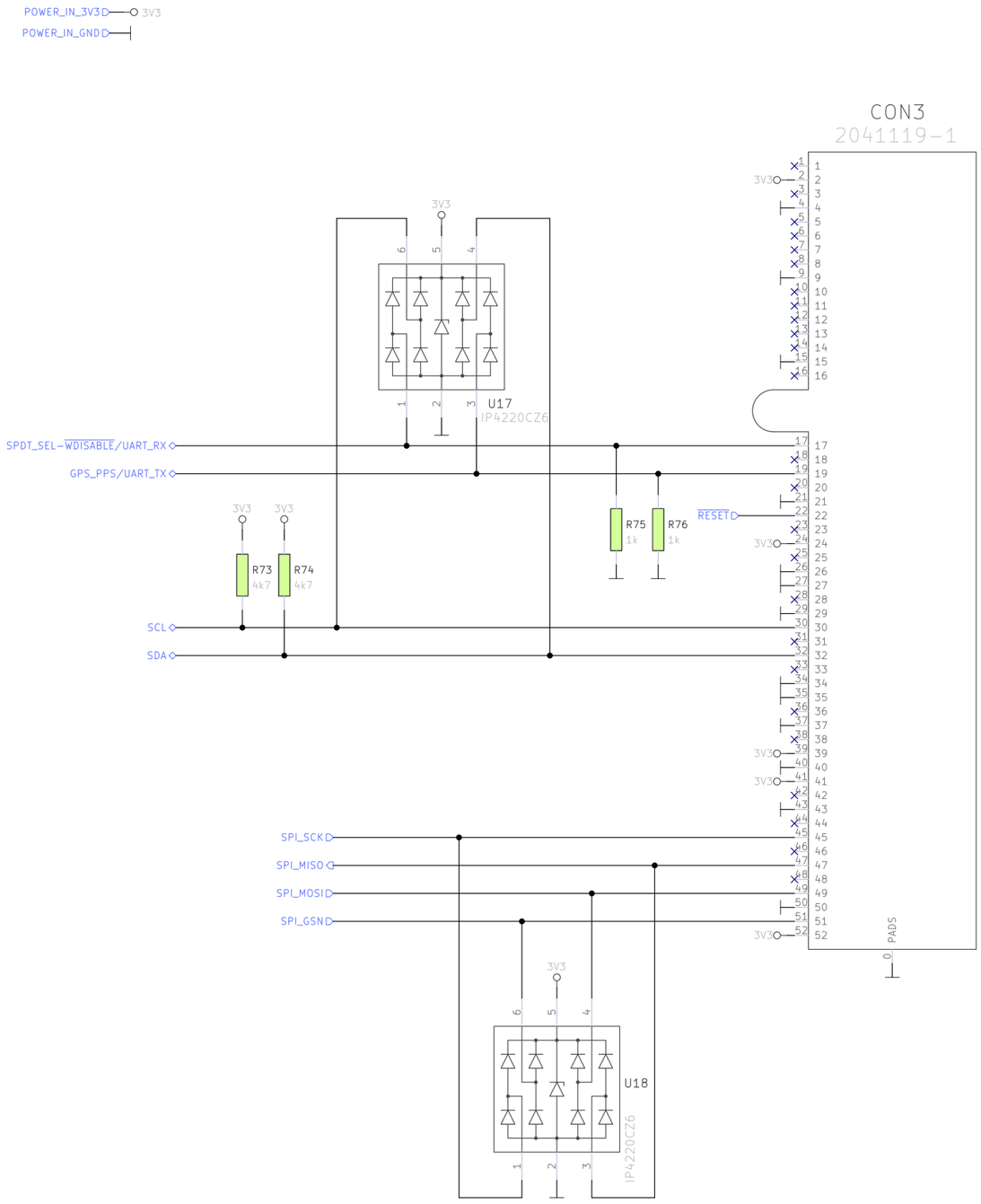


Embedded System Labs

Sheet: /USB Module/
File: usb.kicad_sch

Title: USB Section

Size: A3	Date: 2021-01-13	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.0)		Id: 10/11



Embedded System Labs		
Sheet: /MiniPci Module/		
File: minipci_module.kicad_sch		
Title: Minipci Module		
Size: A3	Date: 2021-01-10	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.0)		Id: 11/11