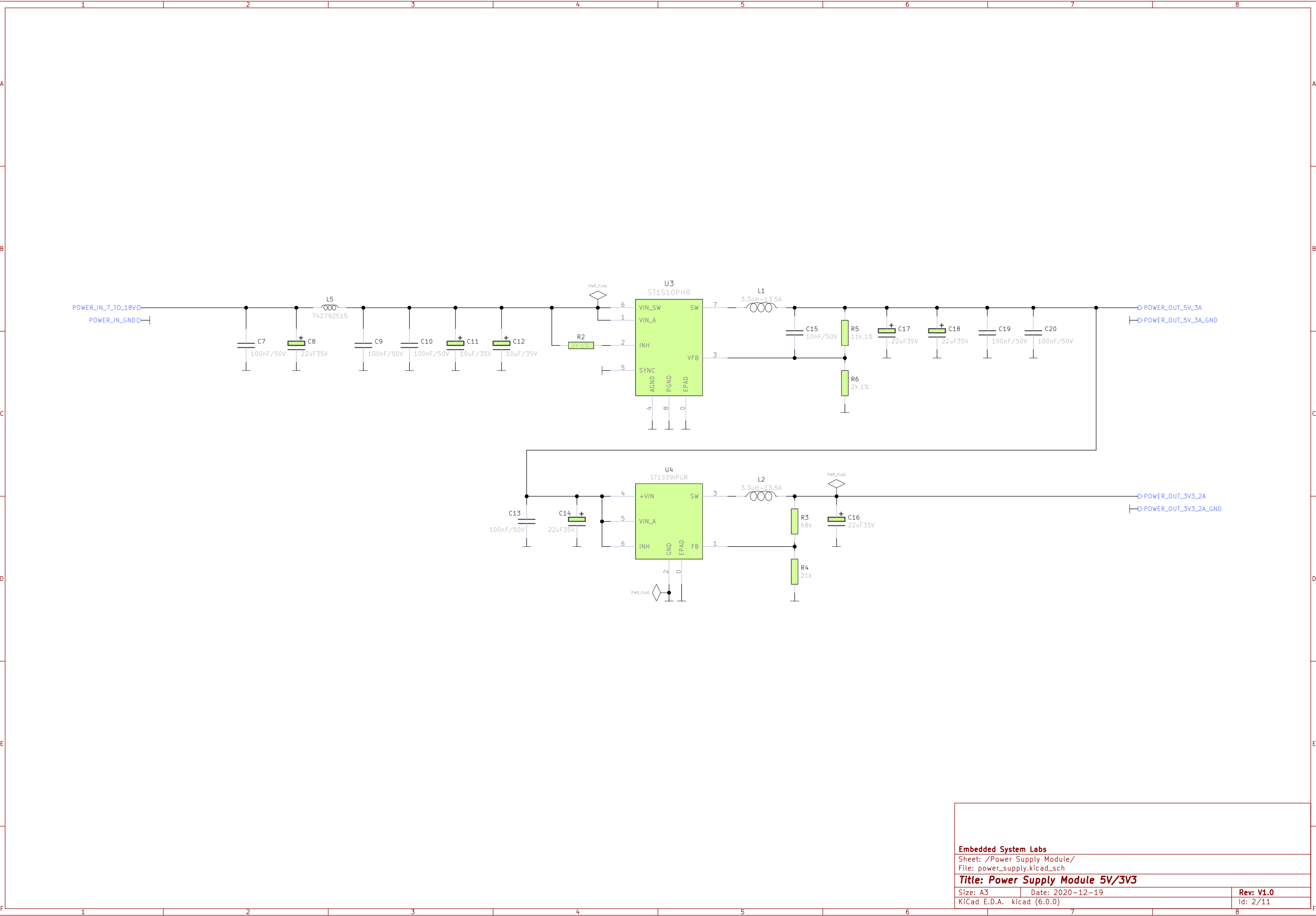


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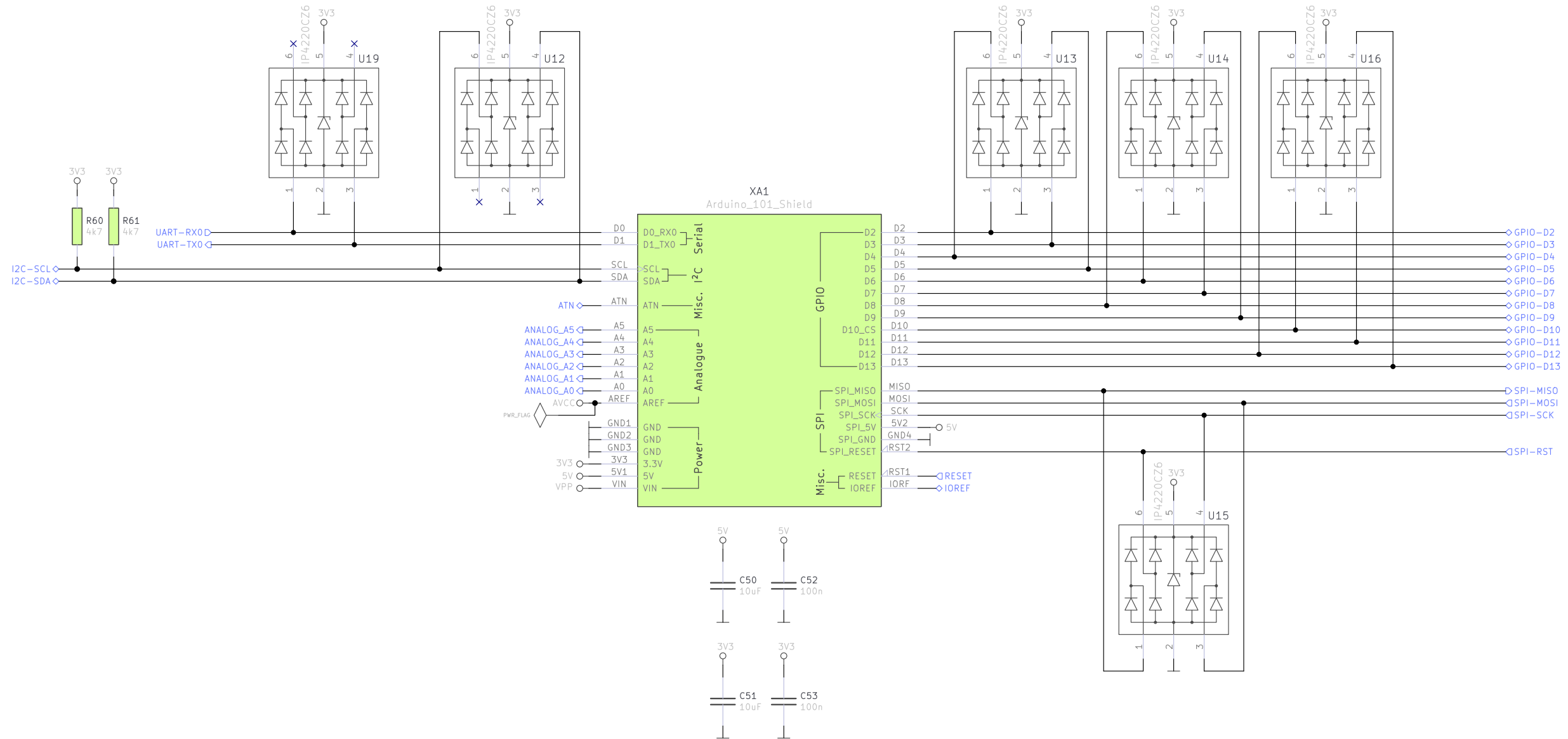


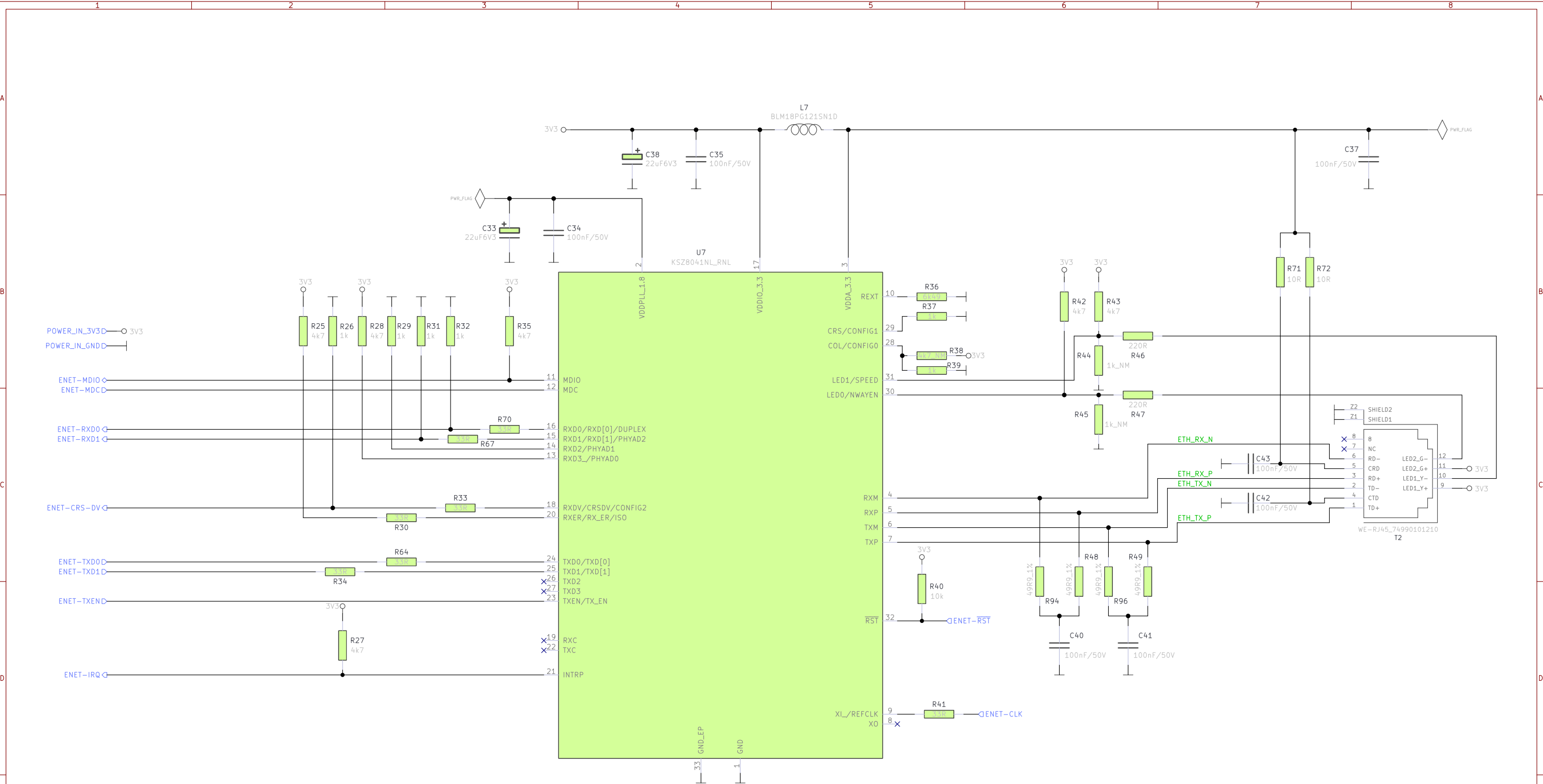
Embedded System Labs

Sheet: /Power Supply Module/
File: power_supply.kicad_sch

Title: Power Supply Module 5V/3V3

Size: A3	Date: 2020-12-19	Rev: V1.0
KiCad E.D.A. kicad (6.0.0)		Id: 2/11





Track width 4.75mil for all

MII and RMII Routing Guidelines

All connections on a PCB in MII and RMII routing are point-to-point connections. Although MII and RMII use relatively low data rates, the limiting parameter that determines whether a trace can act as a transmission line is the signal rise/fall time. Unless your board is very large or your signal switching speed is very fast, reflections at the end of each connection can be ignored. The recommended trace impedance in MII is 50 Ohms +/- 10%. Although the trace length between the PHY and MAC is generally short enough to ignore transmission line effects, you should pay attention to impedance when routing the signal and clock traces when the traces are electrically long. Since MII and RMII require clock signals between the PHY and MAC, best practices for routing clock signals should be used with longer traces. Generally, you should avoid the use of vias on traces carrying clock signals on board with impedance control as the trace impedance can be different between layers. However, as long as the impedance in each layer is carefully controlled to the right value, then the clock signals can certainly be routed through vias. This will prevent signal reflections on longer clock traces. For the above reasons, all MII/RMII signal traces should be routed as short as possible on a single layer, and traces should be routed in a straight path. If you must turn a corner with a signal trace, the trace should bend by no more than 45 degrees. Clock lines should also be shielded with GND lines to prevent crosstalk through capacitive coupling, especially when longer traces are necessary. Because the TX and RX data signals are triggered by the rising edge of the clock, communication in MII and RMII is synchronous. Thus, the data lines and the clock line between the MAC and PHY should be length matched. The allowed deviation in length matching depends on the rise/fall time for digital signals between these two elements, although it is generally recommended that any deviation be less than 10 mm as MII and RMII use TTL logic. Again, the allowed trace length mismatch depends on the rise/fall time of digital signals.

CONFIG[2:0]	Mode
000	MI
001	RMII
010	Reserved - not used
011	Reserved - not used
100	MI 100 Mbps Preamble Restore
101	Reserved - not used
110	Reserved - not used
111	Reserved - not used

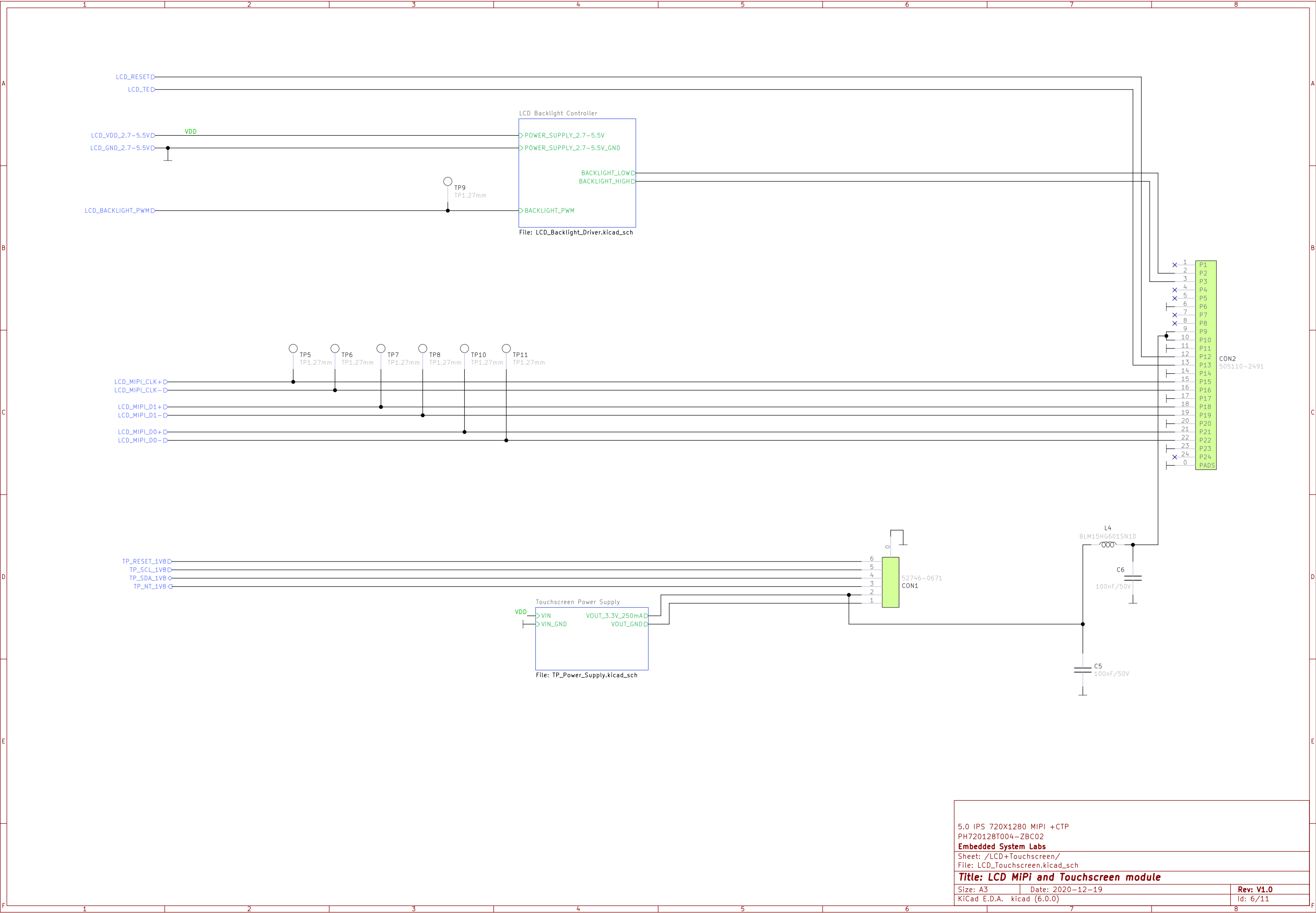
Embedded System Labs

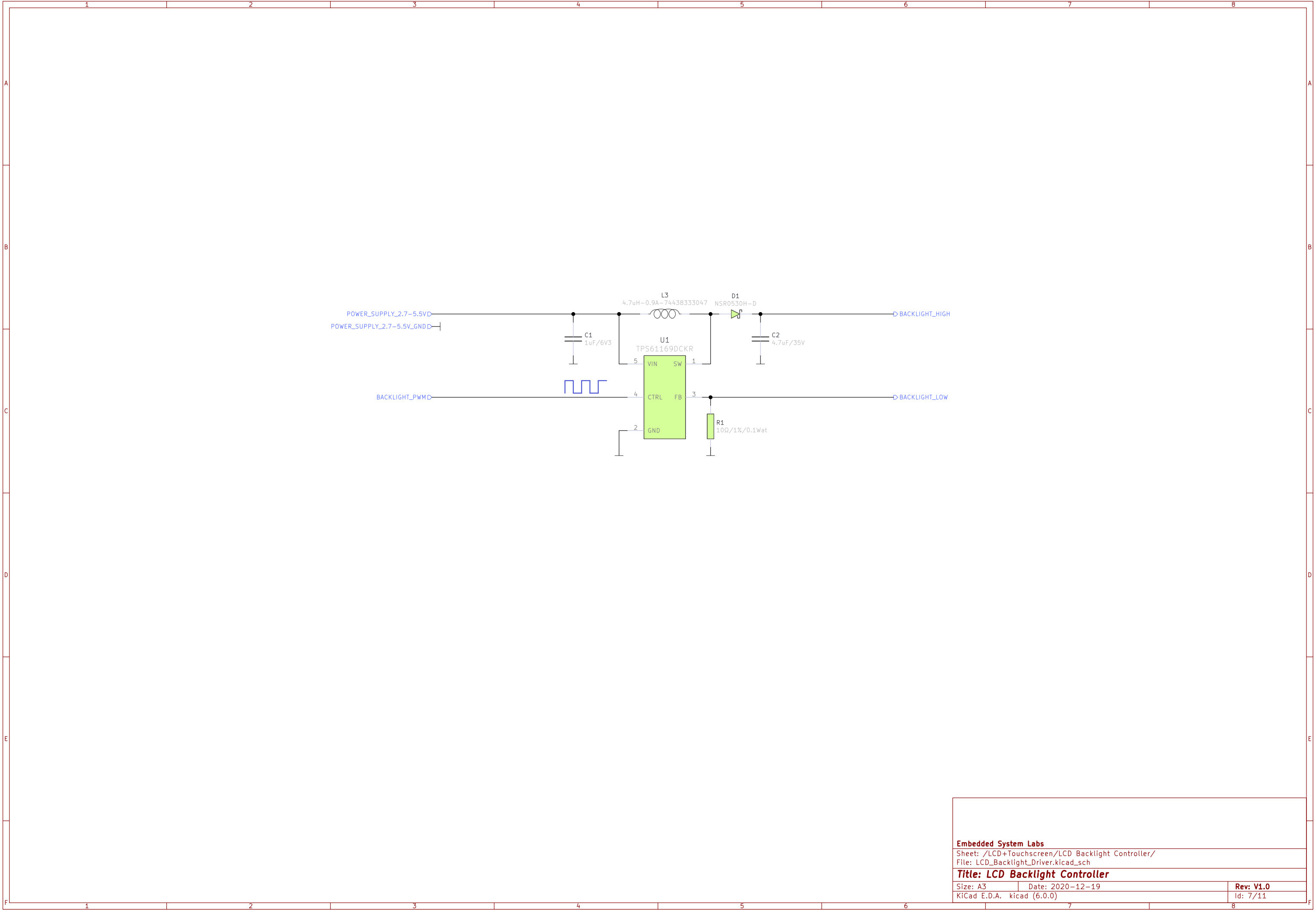
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File: ethernet.kicad_sch

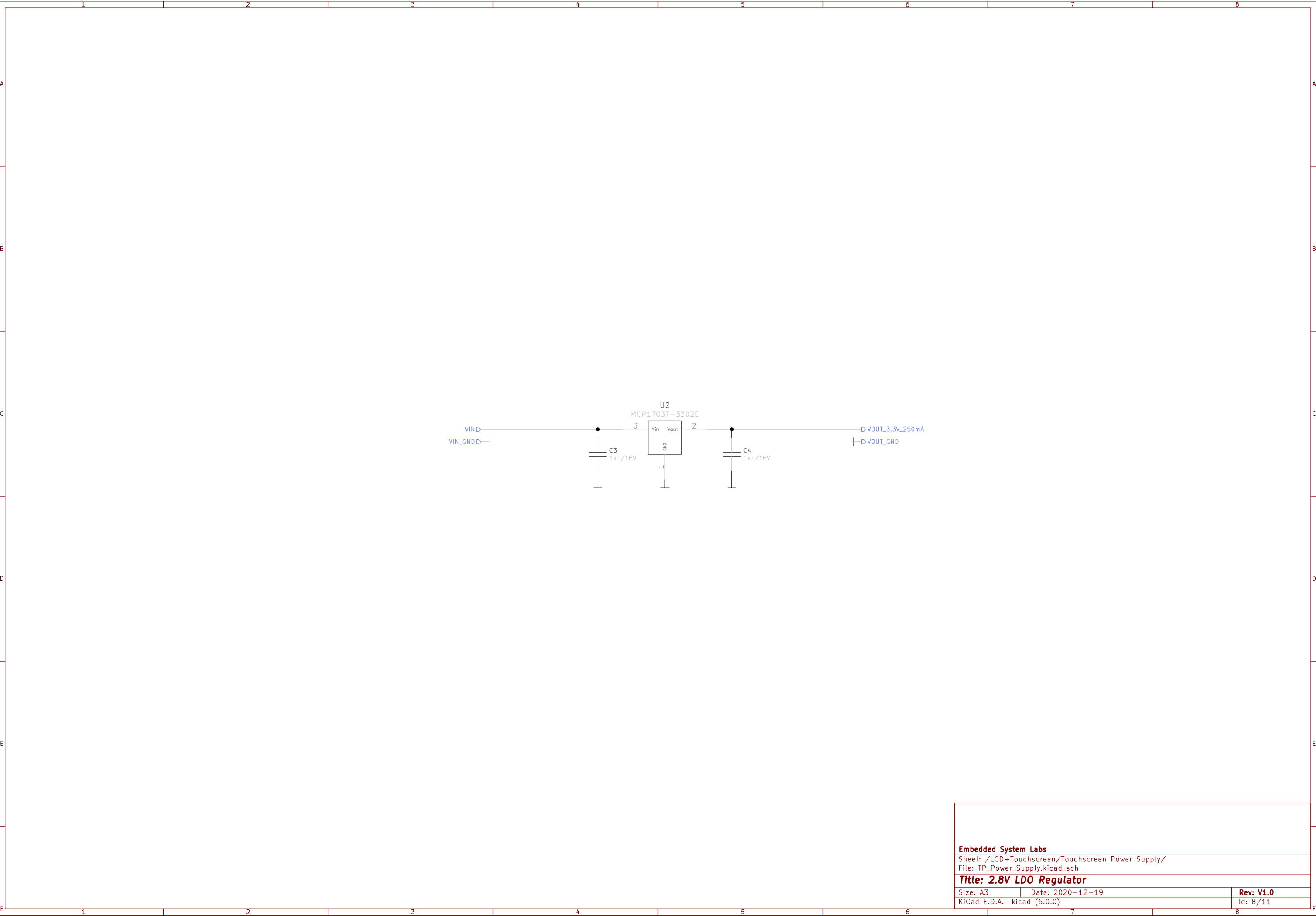
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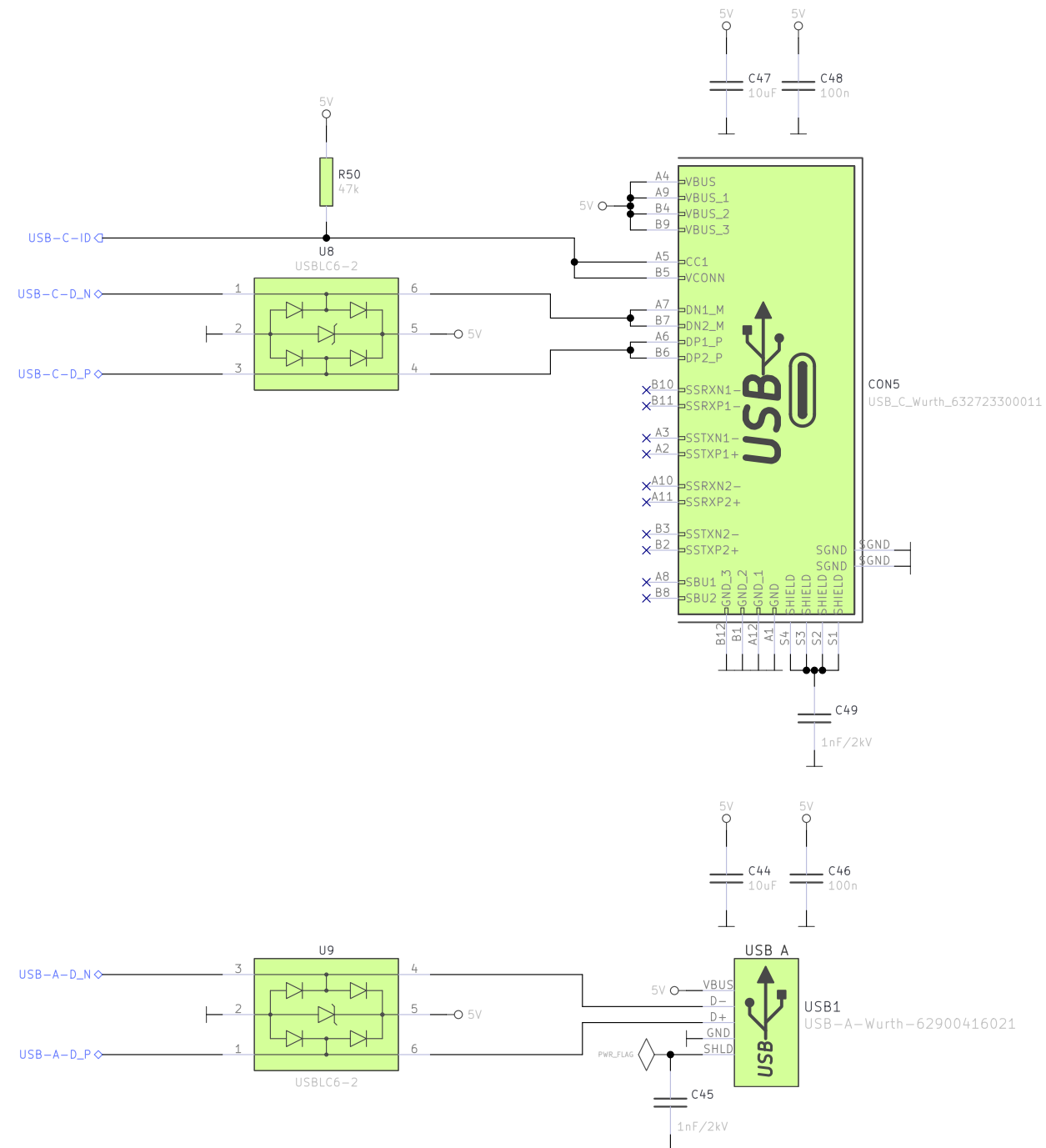
Size: A3	Date: 2021-01-13	Rev: V1.0
KiCad E.D.A. kicad (6.0.0)		Id: 4/11











POWER_IN_3V3 3V3
POWER_IN_GND

