HBM32G003

ARM -based 32-bit MCU, 64-KB Flash, timers,ADC,2.3-3.6V

- **Kernel and System**
  - The 32-bit ARM Cortex M0 processor has a
  - maximum operating frequency of 48MHz.
  - 24-bit system tick timer
  - Integrated nested vector interrupt controller (NVIC) provides Up to 32 interrupts
  - Programming via SWD interface
- **memory**
  - It has at least 64KB of built-in FLASH memory as program storage, 180KB of on-chip FLASH data
  - storage, and two RAM modules totaling 3KB: one 2KB for data storage and the other 1KB for cache. It
  - has cache functionality.
- **Clock, Reset and Power Management**
  - 2.3V~3.6V power supply voltage
  - Power-on/Power-off Reset (POR/PDR), Watchdog Reset, External Dedicated Pin Reset (EXTRST)
  - External 4MHz~32MHz high-frequency crystal oscillator
  - Internal 4MHz~48MHz high-frequency crystal oscillator
  - Built-in 32.768kHz low-frequency crystal oscillator
- **Low power consumption**
  - Standby mode
  - Sleep mode
  - Stop mode
- **SARADC**
  - The 9-channel 12-bit SAR ADC can
  - achieve a sampling rate of 2.4 MHz.
  - Used for power supply voltage and external signal sampling
- **GPIO**
  - Up to 16 I/O ports
  - It can be configured to the following modes: floating input, pull-up input, Pull-down input, push-pull output, open-drain output, analog I/O; flexible
  - interrupt configuration, configurable as level-triggered and side-triggered. Edge-triggered, level-triggered can be set to low level and high level. Flat, edge triggering can be set to rising edge, falling edge, and... bilateral
  - Each GPIO pin supports button wake-up functionality and is configurable. Wake-up on rising edge and wake-up on falling edge
- **Communication interface**
  - One SPI interface, configurable master/slave mode, programmable. Clock polarity and phase, main mode rate are configurable, most The high frequency is Fcpu/4, and the data transmission order is configurable. Independent read/write data registers, supporting ping-pong transfer.
  - 1 UART interface
  - 1 I2C interface Support main mode
- **timer**
  - Two 16-bit advanced timers, with clock division supporting 1-256, providing timing, counting, input capture, and periodic pulse output functions. One of them supports HALL. Function
  - One 32-bit independent watchdog timer
  - Three independent 16-bit basic PWM waveform generators, with a counting clock that supports frequency division from 1 to 256 and supports toggle point interrupts. and periodic overflow interrupt
  - Three independent 16-bit advanced PWM waveform generators, with a counting clock supporting frequency division from 1 to 256, dead time, complementary and braking functions, and rising edge counting or falling edge counting. Number, supports edge-aligned or center-symmetric waveform output, Supports initial level, count start level and output level Inverting is configurable and supports toggle point interrupt and cycle overflow. Interrupts and specific trigger point interrupts
- **environment**
  - Operating temperature: -40℃~85℃
  - Storage temperature: -50℃~150℃
  - Humidity level: MSL3
- **128The only one in the worldID (UUID)**
- **Development tools**
  - Keil
- **Packaging**
  - QFN20, TSSOP20, SOP16
- **Application Scope**
  - Consumer electronics, smart home products, motor drives, dimming lights, LCD display panels, and other products.

HBM32G003Data Manual

32Bit microcontroller

Version: 1.5

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Revision history

Version	date	author	Remark
1.2			Layout Reconstruction First Draft
1.3	2022/5/17	Sun Haojun	Add toSOP16Package pin diagram
1.4	2022/5/24	Sun Haojun	renewTS20Package Dimensions
1.5	2022/6/6	Sun Haojun	Updated foot position diagram

1.Introduction

1.1Overview

This product has a built-in feature.ARM Cortex M0The kernel can operate at a maximum frequency of up to48MHz,Flash 64K,2K RAMThis product includes 16roadIO,1indivual(9aisle)12positionADC,2indivual16A high-level timer with 36 bits, featuring input capture and periodic pulse output functions.1indivual32 positionIWDT,3The basic principle of road independencePWMWaveform generator3Independent High-Level RoadPWMWaveform generator, supporting dead time and complementary functions.1indivualSPI,1indivualIIC,1indivualUARTThis product supportsCLanguage development and debugging can be performed at [location].Keil MDKDevelopment is carried out using software.

The operating voltage of this product is:2.3V~3.6VOperating temperature is -40℃~85℃. Multiple power-saving operating modes ensure low-power application requirements. Currently available.QFN20,TSSOP20,SOP16The packaging is as follows, and different packaging forms will be added as needed in the future.

This product is suitable for the following applications: consumer electronics, smart home, motor drives, dimming lights, LCD display panels, etc.

2.Product Features Overview

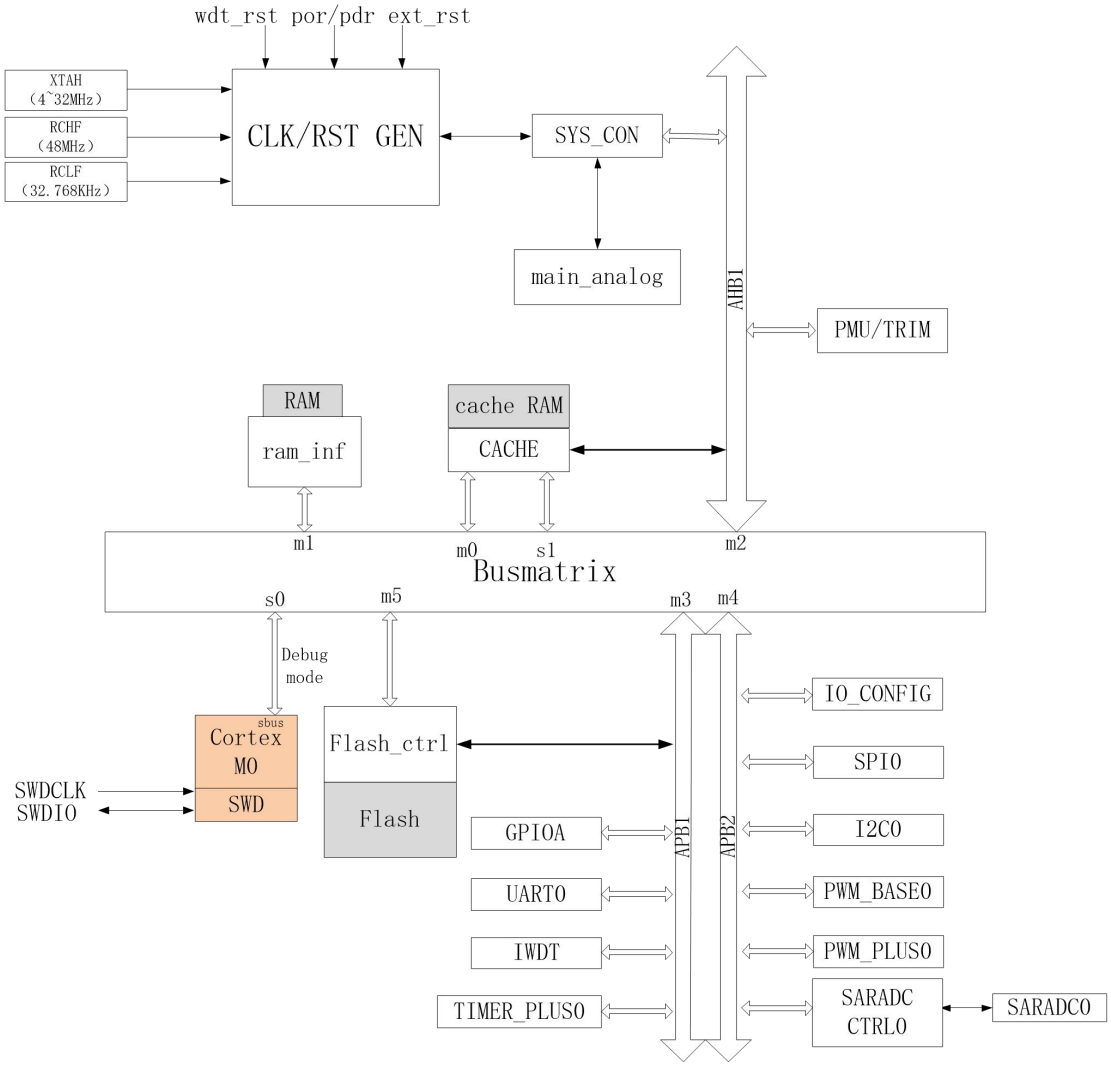
surface1 HBM32G003Resource List

Product Name / characteristic	HBM32G003QN20	HBM32G003TSP20	HBM32G003SP16
Voltage (V)	2.3V~3.6V		
FLASH (KB)	64		
RAM (KB)	2		
PIN	20		16
IO	16		12
EXTI_PIN	16		12
ADC_CH	9		8
TIMERPLUS	2		
PWMBASE	3		
PWMPLUS	3		
IWDT	1		
ADC	1		
UART	1		
SPI	1		
IIC	1		
CPU	ARM Cortex M0		
Temperature	- 45℃~85℃		
Package	QFN20	TSSOP20	SOP16

3.Product Features

3.1Chip structure block diagram

HBM32G003useARMofBUS MatrixThe structure, and the internal connections of each functional module are...AHB1,APB1, APB2The three buses are connected separately.AHB1Responsible for system clock,PMU,Cache. APB1Main connectionsGPIOA, UART,IWDT,TIMER_PLUS0.APB2Main connectionsIO_CONFIG,SPI,IIC,PWM_BASE, PWM_PLUS,SARADC.



picture1HBM32G003Structural diagram

3.2 ARM Cortex M0kernel

ARM Cortex M0forARMThe smallest and lowest power microprocessor in the embedded processor family. It boasts the lowest gate count, lowest power consumption, and outstanding performance.Cortex-M0for32Bit,3automated production lineRISCProcessor, its core andARM7Both are von Neumann (Von Neumann)The architecture adopts a design where instructions and data share the same bus.Cortex-M0The core uses a system memory address map, which is up to [number missing].4GBThe addressable memory space provides a simple and fixed mapping mechanism. This memory mapping mechanism provides a framework for program code,SRAMExternal memory and peripheral devices provide predefined dedicated addresses.Cortex-M0ReceivedARMMicrocontroller development kitKeil RealView MDKSupport, combined withARM RealViewCompilation tools and powerful, comprehensiveKeil uVision IDEandDebuggertool.

3.3Address space mapping

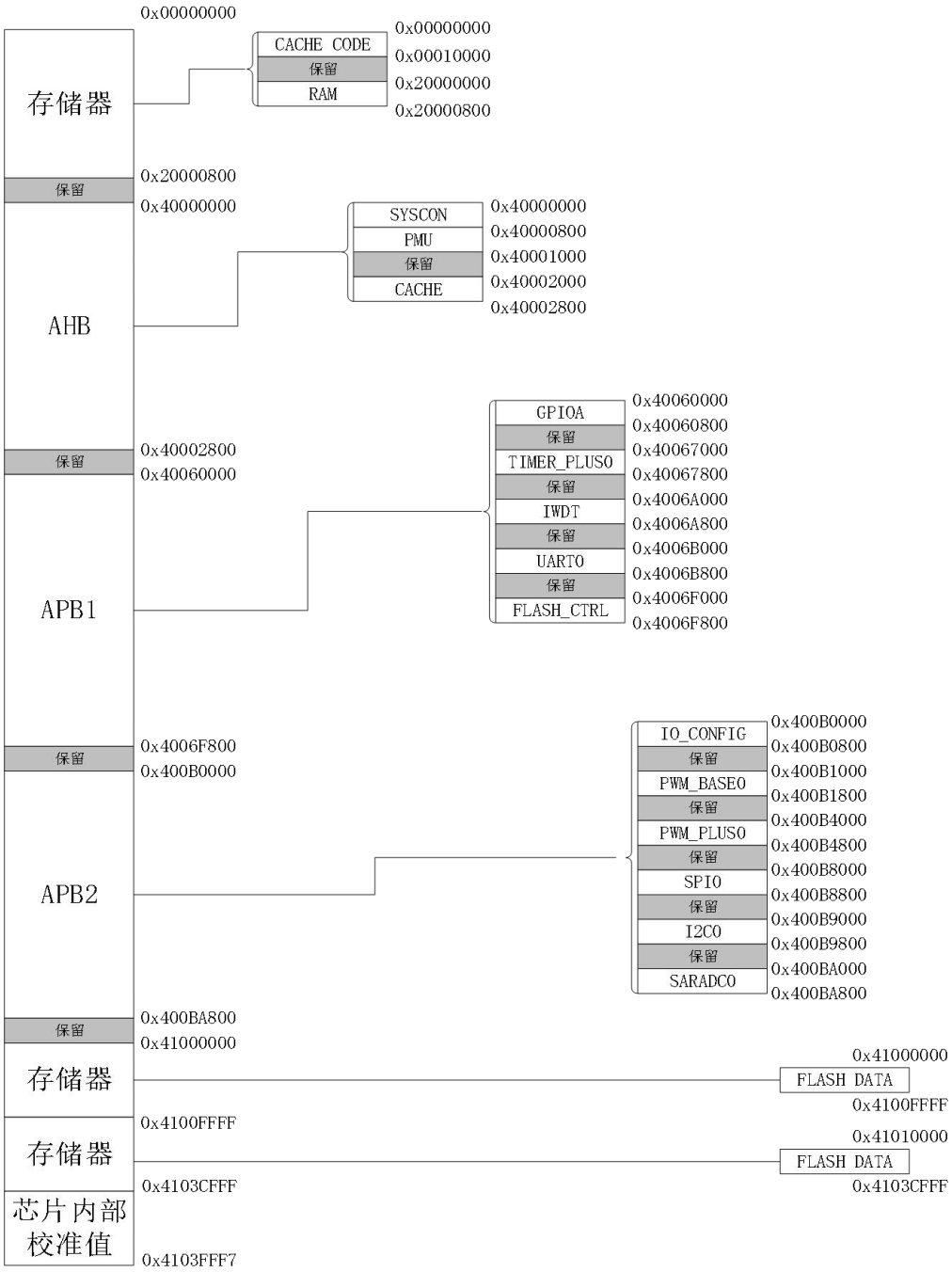
HBM32G003The controller is32A bit-wide general-purpose controller provides4GThe addressable space for bytes is shown in the table below. The specific register layout and operation instructions for each module are described in detail in later chapters. The addressable code space is as follows:64K. 64KIn addition to the programmable address space, there is also180KofFlashData storage space.

surface2 HBM32G003Address space mapping

bus	Start	Finish	Module
live Storage instrument	0x00000000	0x0000FFFF	CACHE CODE
	0x00010000	0x1FFFFFFF	reserve
	0x20000000	0x200007FF	RAM
	0x20000800	0x3FFFFFFF	reserve
AHB	0x40000000	0x400007FF	SYSCON
	0x40000800	0x40000FFF	PMU
	0x40001000	0x40001FFF	reserve
	0x40002000	0x400027FF	CACHE
	0x40002800	0x4005FFFF	reserve
APB1	0x40060000	0x400607FF	GPIOA
	0x40060800	0x40066FFF	reserve
	0x40067000	0x400677FF	TIMER_PLUS0
	0x40067800	0x40069FFF	reserve
	0x4006A000	0x4006A7FF	IWDT
	0x4006A800	0x4006AFFF	reserve
	0x4006B000	0x4006B7FF	UART0
	0x4006B800	0x4006EFFF	reserve
	0x4006F000	0x4006F7FF	FLASH_CTRL
	0x4006F800	0x400AFFFF	reserve

APB2	0x400B0000	0x400B07FF	IO_CONFIG
	0x400B0800	0x400B0FFF	reserve
	0x400B1000	0x400B17FF	PWM_BASE0
	0x400B1800	0x400B3FFF	reserve
	0x400B4000	0x400B47FF	PWM_PLUS0
	0x400B4800	0x400B7FFF	reserve
	0x400B8000	0x400B87FF	SPI0
	0x400B8800	0x400B8FFF	reserve
	0x400B9000	0x400B97FF	I2C0
	0x400B9800	0x400B9FFF	reserve
	0x400BA000	0x400BA7FF	SARADC0
	0x400BA800	0x4FFFFFFF	reserve
memory	0x41000000	0x4100FFFF	FLASH DATA
	0x41010000	0x4103CFFF	FLASH DATA
	0x4103D000	0x4103FFCB	reserve
	0x4103FFCC	0x4103FFCF	IN_Trim_ADC_OFFSET&K
	0x4103FFD4	0x4103FFD7	Trim_VREF_REALVOL
	0x4103FFD8	0x4103FFDB	Trim_RC_REALFREQ_DELTA
	0x4103FFDC	0x4103FFDF	Trim_ADC_OFF_K
	0x4103FFE0	0x4103FFE3	Trim_RC
	0x4103FFE4	0x4103FFE7	Trim_POW
	0x4103FFE8	0x4103FFF7	128-bit UUID

The memory address distribution diagram is shown below: mainly divided intoRAMareaAHBBus corresponding SYSCON,PMU, CACHE.APB1bus,APB2bus,FlashProgram storage areaFlashThe data storage area and the chip calibration data area are reserved areas.



picture2HBM32G003Structural diagram

surface3 HBM32G003 Register map

name	address	Bit width	type	Reset value	describe
CLK_SEL	0x40000000	32	R/W	0	Clock Selection Register
DIV_CLK_GATE	0x40000004	32	R/W	0	Frequency divider clock gate register
DEV_CLK_GATE	0x40000008	32	R/W	0	Peripheral clock gate register
CHIP_RST_ST	0x40000010	32	R/W	0	Chip Reset Status Register
RC_CON	0x40000100	32	R/W	0	RCOscillator Clock Control Register
XTAH_CON	0x40000104	32	R/W	0	Crystal clock control register
LPOW_MD	0x40000800	32	R/W	0x00	Low-power mode selection register
LPMD_WKEN	0x40000804	32	R/W	0x00	Low-power wake-up source enable register
LPMD_WKST	0x40000808	32	R/W	0x00	Low-power wake-up source status register
TRIM _POW	0x40000820	32	R/W	0x00	POWRelated simulation modulesTRIMregister
TRIM_RC	0x40000824	32	R/W	0x00	RCClock moduleTRIMregister
TRIM_LOCK	0x40000828	32	R/W	0x00	TRIMLock register
CACHE_CFG	0x40002000	32	R/W	1	CACHEConfiguration Register
PF_CTRL	0x40002004	32	R/W	0	Prefetch control register
GPIODATA	0x40060000	16	R/W	0	Data register
GPIODIR	0x40060004	16	R/W	0	Direction setting register
INTLVLTRG	0x40060008	16	R/W	0	Interrupt detection mode register
INTBE	0x4006000C	16	R/W	0	Trigger Mode Register
INTRISEEN	0x40060010	16	R/W	0	Interrupt event mode register
INTEN	0x40060014	16	R/W	0	Interrupt enable register
INTRAWSTAUS	0x40060018	16	R	0	Interrupt raw status register
INTSTAUS	0x4006001C	16	R	0	Interrupt Status Register
INTCLR	0x40060020	16	W	0	Clear register along interrupt trigger

TIMERPLUS_EN	0x40067000	32	R/W	0	TIMERPLUSEnable register
TIMERPLUS_DIV	0x40067004	32	R/W	0	TIMERPLUSCounting clock prescaler register
TIMERPLUS_CTR	0x40067008	32	R/W	0	TIMERPLUSConfiguration Register
TIMERPLUS_IE	0x40067010	32	R/W	0	TIMERPLUSInterrupt enable register
TIMERPLUS_IF	0x40067014	32	R/W	0	TIMERPLUSInterrupt Status Register
HIGH_PERIOD	0x40067020	32	R/W	0	TIMERPLUS HIGHTarget Configuration Register
HIGH_CNT	0x40067024	32	R	0	TIMERPLUS HIGHCurrent count register
HIGH_CVAL	0x40067028	32	R	0	TIMERPLUS HIGHCapture Value Register
LOW_PERIOD	0x40067030	32	R/W	0	TIMERPLUS LOWTarget Configuration Register
LOW_CNT	0x40067034	32	R	0	TIMERPLUS LOWCurrent count register
LOW_CVAL	0x40067038	32	R	0	TIMERPLUS HIGHCapture Value Register
HALL_VAL	0x40067040	32	R	0	HALLSignal raw value register
IWDTLOAD	0x4006A000	32	R/W	0	IWDTInitial value register
IWDTVALUE	0x4006A004	32	R	0	IWDTCurrent count register
IWDTCTRL	0x4006A008	32	R/W	0	IWDTControl Register
IWDTIF	0x4006A00C	32	R/W	0	IWDTInterrupt Status Register
IWDTFEED	0x4006A010	32	R/W	0	IWDTFeed the dog register
RBR	0x4006B000	32	R	0	Receive Data Register
THR	0x4006B000	32	W	0	Transmit Data Register
DLH	0x4006B004	32	R/W	0	High baud rate8Bit register
DLL	0x4006B000	32	R/W	0	low baud rate8Bit register
IER	0x4006B004	32	R/W	0	Interrupt enable register
CTRL	0x4006B00C	32	R/W	0	Data Control Register
MCR	0x4006B010	32	R/W	0	LOOPBACKEnable register

LSR	0x4006B014	32	R	0	Data Status Register
SPIF_CFG	0x4006F000	32	R/W	0	Configuration Register
SPIF_ADDR	0x4006F004	32	R/W	0	Address Register
SPIF_WDATA	0x4006F008	32	R/W	0	Write data register
SPIF_RDATA	0x4006F00C	32	R	0	Read data register
SPIF_START	0x4006F010	32	R/W	0	Startup Register
SPIF_ST	0x4006F014	32	R	0	Status Register
PORTA_SEL0	0x400B0000	32	R/W	0	PORTAFunction Selection Register0
PORTA_SEL1	0x400B0004	32	R/W	0	PORTAFunction Selection Register1
PORTA_IE	0x400B0100	32	R/W	0	PORTAInput enable register
PORTA_PU	0x400B0200	32	R/W	0	PORTAPull-up enable register
PORTA_PD	0x400B0300	32	R/W	0	PORTAPull-down enable register
PORTA_OD	0x400B0400	32	R/W	0	PORTAOpen-drain enable register
PORTA_WKE	0x400B0500	32	R/W	0	PORTAWake-up Enable Register
PORT_CFG	0x400B0600	32	R/W	0	PORTConfiguration Register
PWMBASE_EN	0x400B1000	32	R/W	0	PWMBASEEnable register
PWMBASE_DIV	0x400B1004	32	R/W	0	PWMBASEClock prescaler register
PWMBASE_CON	0x400B1008	32	R/W	0	PWMBASEOutput Configuration Register
PWMBASE_PERIOD	0x400B100C	32	R/W	0	PWMBASEPeriodic Configuration Register
PWMBASE_IE	0x400B1010	32	R/W	0	PWMBASEInterrupt enable register
PWMBASE_IF	0x400B1014	32	R/W	0	PWMBASEInterrupt Status Register
PWMBASE_CNT	0x400B1018	32	R/W	0	PWMBASECurrent count register
PWMBASE_CH0_COMP	0x400B1020	32	R/W	0	PWMBASEaisle0Flip point configuration register
PWMBASE_CH1_COMP	0x400B1030	32	R/W	0	PWMBASEaisle1Flip point configuration register

PWMBASE_CH2_COMP	0x400B1040	32	R/W	0	PWMBASEaisle2Flip point configuration register
PWMPLUS_CFG	0x400B4000	32	R/W	0	PWMPLUSConfiguration Register
PWMPLUS_GEN	0x400B4004	32	R/W	0	PWMPLUSChannel waveform generation register
PWMPLUS_CLKSRC	0x400B4008	32	R/W	0	PWMPLUSClock source and divider configuration register
PWMPLUS_BRAKE_CFG	0x400B400C	32	R/W	0	PWMPLUSBrake Configuration Register
PWMPLUS_MASK_LEV	0x400B4010	32	R/W	0	PWMPLUSForced output level selection register
PWMPLUS_PERIOD	0x400B401C	32	R/W	0	PWMPLUSCounter period value register
PWMPLUS_CH0_COMP	0x400B4020	32	R/W	0	PWMPLUSaisle0Flip point configuration register
PWMPLUS_CH1_COMP	0x400B4024	32	R/W	0	PWMPLUSaisle1Flip point configuration register
PWMPLUS_CH2_COMP	0x400B4028	32	R/W	0	PWMPLUSaisle2Flip point configuration register
PWMPLUS_CH0_DT	0x400B4030	32	R/W	0	PWMPLUSaisle0Dead Time Length Configuration Register
PWMPLUS_CH1_DT	0x400B4034	32	R/W	0	PWMPLUSaisle1Dead Time Length Configuration Register
PWMPLUS_CH2_DT	0x400B4038	32	R/W	0	PWMPLUSaisle2Dead Time Length Configuration Register
PWMPLUS_TRIG_COMP	0x400B4040	32	R/W	0	PWMPLUSInternal trigger compare value register
PWMPLUS_TRIG_CFG	0x400B4044	32	R/W	0	PWMPLUSInternal Trigger Configuration Register
PWMPLUS_IE	0x400B4060	32	R/W	0	PWMPLUSInterrupt enable register
PWMPLUS_IF	0x400B4064	32	R/W	0	PWMPLUSInterrupt Status Register
PWMPLUS_SWLOAD	0x400B4084	32	R/W	0	PWMPLUSConfigure registers software load registers
PWMPLUS_MASK_EN	0x400B4088	32	R/W	0	PWMPLUSDisable enable control register
PWMPLUS_CNT_ST	0x400B40e0	32	R/W	0	PWMPLUSCounter Status Register
PWMPLUS_BRAKE_ST	0x400B40e4	32	R/W	0	PWMPLUSBrake Status Register
SPICR	0x400B8000	32	R/W	0	SPIControl Register
SPIWDR	0x400B8004	32	R/W	0	SPIWrite data register
SPIRDR	0x400B8008	32	R	0	SPIRead data register

SPIIE	0x400B8010	32	RW	0	SPIInterrupt enable register
SPIIF	0x400B8014	32	R/W	0	SPIInterrupt Status Register
CLKDIV	0x400B9000	32	R/W	FFFFH	IICFrequency divider controller
CTRL	0x400B9004	32	R/W	0	Control Register
TXR	0x400B9008	32	R/W	0	Send register
RXR	0x400B900C	32	RW	0	Receive Register
CR	0x400B9010	32	R/W	0	Command Register
SR	0x400B9014	32	R/W	0	Status Register
ADC_CFG	0x400BA000	32	R/W	1	ADCConfiguration Register
ADC_START	0x400BA004	32	R/W	0	ADCStartup Register
ADC_IE	0x400BA008	32	R/W	0	ADCInterrupt enable register
ADC_IF	0x400BA00C	32	RW	0	ADCInterrupt Status Register
ADC_CH0_STAT	0x400BA010	32	R/W	0	ADCaisle0Status Register
ADC_CH0_DATA	0x400BA014	32	R/W	0	ADCaisle0Data register
ADC_CH1_STAT	0x400BA020	32	R/W	0	ADCaisle1Status Register
ADC_CH1_DATA	0x400BA024	32	R/W	0	ADCaisle1Data register
ADC_CH2_STAT	0x400BA030	32	R/W	0	ADCaisle2Status Register
ADC_CH2_DATA	0x400BA034	32	R/W	0	ADCaisle2Data register
ADC_CH3_STAT	0x400BA040	32	R/W	0	ADCaisle3Status Register
ADC_CH3_DATA	0x400BA044	32	R/W	0	ADCaisle3Data register
ADC_CH4_STAT	0x400BA050	32	R/W	0	ADCaisle4Status Register
ADC_CH4_DATA	0x400BA054	32	R/W	0	ADCaisle4Data register
ADC_CH5_STAT	0x400BA060	32	R/W	0	ADCaisle5Status Register
ADC_CH5_DATA	0x400BA064	32	R/W	0	ADCaisle5Data register

ADC_CH6_STAT	0x400BA070	32	R/W	0	ADCaisle6Status Register
ADC_CH6_DATA	0x400BA074	32	R/W	0	ADCaisle6Data register
ADC_CH7_STAT	0x400BA080	32	R/W	0	ADCaisle7Status Register
ADC_CH7_DATA	0x400BA084	32	R/W	0	ADCaisle7Data register
ADC_CH8_STAT	0x400BA090	32	R/W	0	ADCaisle8Status Register
ADC_CH8_DATA	0x400BA094	32	R/W	0	ADCaisle8Data register
ADC_FIFO_STAT	0x400BA0A0	32	R/W	0	ADC FIFOStatus Register
ADC_FIFO_DATA	0x400BA0A4	32	R/W	0	ADC FIFOData register
ADC_EXTTRIG_SEL	0x400BA0B0	32	R/W	0	External signal triggerADCSelect register
ADC_CTRL	0x400BA0E0	32	R/W	0	ADCControl Register
ADC_CALIB_OFFSET	0x400BA0F0	32	R/W	0	ADCcalibrationOFFSETregister
ADC_CALIB_KD	0x400BA0F4	32	R/W	0	ADCcalibrationKDregister

3.4Interrupt vector mapping

HBM32G003Totaltwenty threeThere are several interrupt vector entries, and the interrupt vector mapping is shown in the figure below:

surface4 HBM32G003Interrupt vector mapping

Interruption source	Peripheral interrupt	Introduction	Enter low power Consumption mode Can be turned on
0	UART0_IRQn	UART0Interruption	×
1	TIMERPLUS0_IRQn	TIMERPLUS0Interruption	×
2	PWMBASE0_IRQn	PWMBASE0Interruption	×
3	PWMPLUS0_IRQn	PWMPLUS0Interruption	×
4	IIC0_IRQn	IIC0Interruption	×
5	SARADC_IRQn	SARADCInterruption	×
6	SPI0_IRQn	SPI0Interruption	×
7	IWDT_IRQn	IWDTInterruption	×
8	GPIOA0_IRQn	GPIOA0Interruption	×
9	GPIOA1_IRQn	GPIOA1Interruption	×
10	GPIOA2_IRQn	GPIOA2Interruption	×
11	GPIOA3_IRQn	GPIOA3Interruption	×
12	GPIOA4_IRQn	GPIOA4Interruption	×
13	GPIOA5_IRQn	GPIOA5Interruption	×
14	GPIOA6_IRQn	GPIOA6Interruption	×
15	GPIOA7_IRQn	GPIOA7Interruption	×
16	GPIOA8_IRQn	GPIOA8Interruption	×
17	GPIOA9_IRQn	GPIOA9Interruption	×
18	GPIOA10_IRQn	GPIOA10Interruption	×
19	GPIOA11_IRQn	GPIOA11Interruption	×
20	GPIOA12_IRQn	GPIOA12Interruption	×
twenty one	GPIOA13_IRQn	GPIOA13Interruption	×
twenty two	GPIOA14_IRQn	GPIOA14Interruption	×
twenty three	GPIOA15_IRQn	GPIOA15Interruption	×

3.5Reset method

HBM32G003It supports three reset methods: power-on/power-down reset, external reset triggered by an external dedicated reset pin, and independent watchdog soft reset.

surface5 HBM32G003Reset method

serial number	Reset method
0	Power-on/Power-off reset (POR/PDR)
1	Watchdog reset
2	External dedicated reset (EXTRST)

3.6GeneralIOport

HBM32G003Maximum available16indivualGPIOEach port has an independent interrupt entry point, and the interrupt triggering condition is configurable, supporting both level-triggered and edge-triggered interrupts. Level-triggered interrupts support high and low levels, while edge-triggered interrupts support rising, falling, and double-edge triggering.IOAll support pull-up, pull-down, push-pull, and leak-opening functions.

3.7Clock source

HBM32G003It has two built-in clock sources, one of which is48MHzThe internal high-frequency oscillation, one of which is32.768kHzInternal low-frequency oscillation, while supporting1External clock source, capable of recognizing input4~32MHzCrystal oscillator. Each peripheral has an individual switch controlling the clock source. The system clock is selectable.RCHFOr a frequency-divided clock, where the frequency division factor is from...1arrive32The frequency divider clock source is as follows:RCHF,RCLF,XTAH.

surface6 HBM32G003Clock source

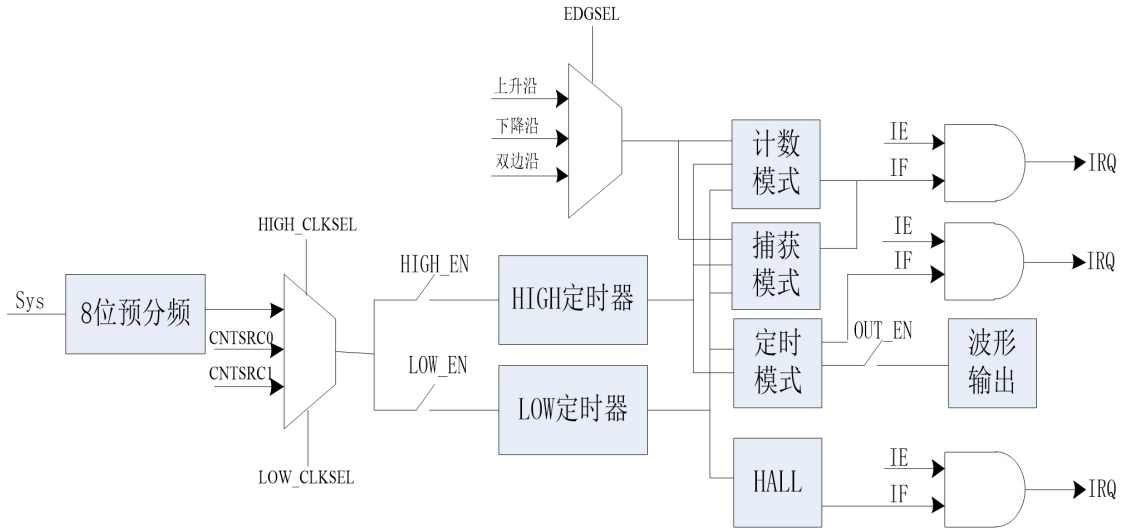
parameter	RCHF	RCLF	XTAH
clock frequency	48MHz	32.768kHz	4-32MHz

3.8timer

HBM32G003 Cortex™-M0The core provides atwenty fourThe chip also includes a bit system timer.2An independent16bit Advanced timers. The advanced timer module features timing, counting, and capture functions.HALLIt has functions such as periodic pulse output, and has a8Bit prescaler, supports interrupts2An independent16Bit timer (HIGHand LOWBefore use, the advanced timer module clock needs to be enabled.

surface7 HBM32G003timer

parameter	System Timer (SYSTICK)	Advanced Timer (TMERPLUS)	
		HIGH	LOW
Bit	24bit	16bit	
Clock source	HCLK	RCHF/RCLF/XTAH/CNT	
Frequency division	-	8bitOptional frequency division value	
Optional mode	-	Timer/Counter/Capture/HALL	



3.9Independent Watchdog

Independent watchdog timer (IWDTIt has interrupt functionality and has32Bit width of the counter. Generates a counter overflow reset signal; the reset signal enables configuration. Features include...32It features a bit-width counter with a flexible and wide-range configurable overflow cycle, interrupt functionality, and a dog-feeding function.

3.10Pulse Width Modulation Generator (PWM)PWM)

This chip supportsPWMBASEandPWMPLUStwoPWMModule.

PWMBASEModule provides3road(CH0,CH1,CH2Independent passage3indivual16-bit PWMIt can output different duty cycles.PWMWaveform. Prescaler function is supported.8bitPrescaler counter. Supports output level toggling, and supports interrupts upon reaching the toggle point and interrupts upon the end of the cycle.

PWMPLUSFor advancedPWMModule, supports3Each independent channel16-bit PWMChannel output (CH0/CH1/CH2)It can output different duty cycles.PWMWaveform.8bitPrescaler counter, supports on-chiptimerAlternatively, an external signal can be used as the counting clock. Each channel supports configurable dead time. The counter supports rising or falling counts, and is configurable in edge-aligned or center-symmetric mode. A braking function is supported, with configurable braking effective level. An internal specific trigger mechanism is supported, capable of outputting three pulse signals: cycle end, channel toggle point, and specific trigger point. Edge-aligned or center-symmetric waveforms can be generated. Fixed-period automatic loading or software loading of cycle value, channel toggle point value, and specific trigger point value is supported.

surface8 HBM32G003Pulse Width Modulation Generator

Function	PWMBASE	PWMPLUS
Number of channels	3	3
Complementary output	×	√
Prescaler	8bitOptional	8bitOptional
Number of digits	16-bit	16-bit
Dead Zone	×	√
brake	×	√
Initial level configuration	×	√
Output inversion	×	√
Additional internal trigger points	×	√

3.11 UARTUniversal Asynchronous Receiver

This chip has1Serial port, supports baud rate configuration, supports multiple interrupts, supports...breakFunctionality, support LOOPBACKFunctionality, supports standardsUARTThe protocol supports full-duplex mode, baud rate configuration, and more.5/6/7/8 Bit data format selection, configurable parity bits, odd parity, even parity, constant parity.0, often1,support1/2Stop bit selection, supports breakFunctionality, supportLOOPBACKFunctionality, supports multiple interrupts

surface9 HBM32G003 UART

Function	UART0
Break	√
LOOPBACK	√

3.12 SPIbus controller

This chip has1Synchronous serial interface (SPI)It supports master-slave mode, and the data transmission order is configurable. It supports both master and slave modes, programmable clock polarity and phase, configurable master mode speed, and a maximum frequency equal to the system clock.4 Frequency division, configurable data transmission order, transmission end interrupt flag, separate read data register and write data register.

3.13 IICcontroller

This chip has1roadIIC,support100kbit/sStandard mode and400kbit/sFast mode. Supports up to [number] [units].400kHz The speed and baud rate are configurable, and interrupts are supported. Slave mode is not currently supported.

3.14 12-Bit SARADCSuccessive approximation analog-to-digital converter

9aisle12-bit SARADCThe sampling rate can reach up to2.4MIt supports single-shot and continuous modes, and has a depth of 9of FIFOIt supports hardware averaging and can be configured as follows:1,2,4,8Next, calculate the average, and support...ADCThe clock is configurable, allowing you to select the system clock.1,2,4,8Frequency division and sampling setup time are configurable; it can be configured to use external clock sampling and supports...1,2,4,8,16,32,64,128indivualADCClock cycle setup time (at this time)ADCThe clock is configurable; the system clock can be selected.1,2,4,8(Frequency division), or can be configured for internal clock sampling, supports1,3, 5,7,9, 11,13,15indivualADCClock cycle setup time.

ADCThe conversion rate formula is as follows:ADCClock / (Setup Time +16) It has the function of interrupting data conversion completion.

FIFOHalf full interruption,FIFOFull interruption,FIFOOverflow interrupt,ADCThe reference voltage can be selected as either an internal reference or an external reference. Internal reference voltage1.4V,ADCCan collectVDDVoltage, select internal reference.1/3After pressure division, it enters the channel.8The collected data isdata,The voltage calculation formula is:VDD/(3*1.4) = data/4096.

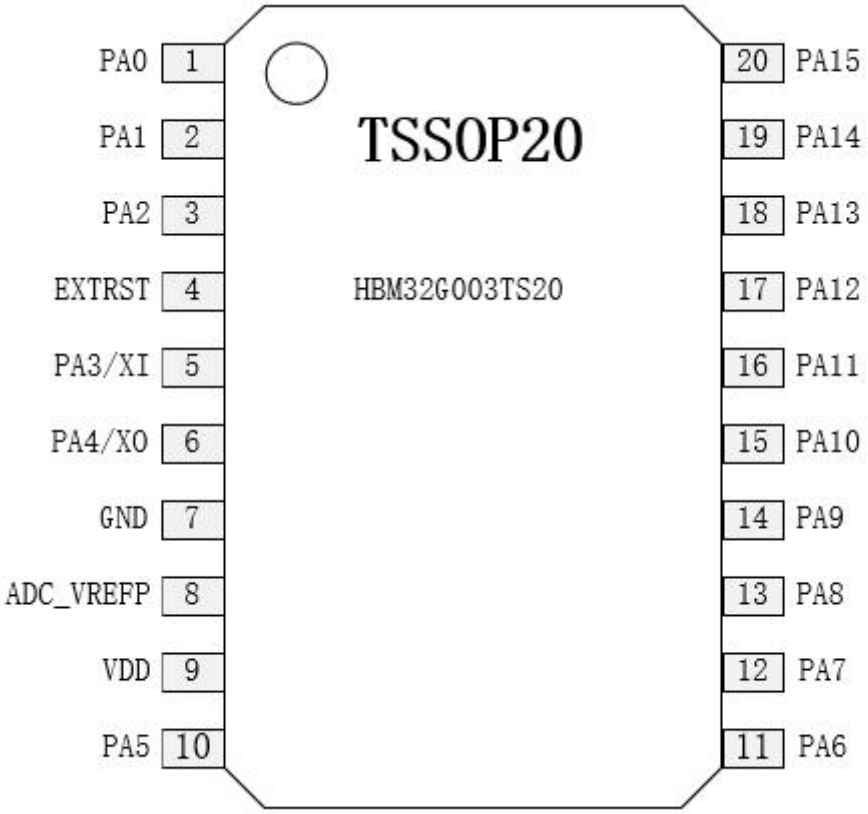
Output data calibration is supported and can be enabled or disabled during program initialization.KDandOFFSETcalibration.

3.15 UUIDonlyIDNumber

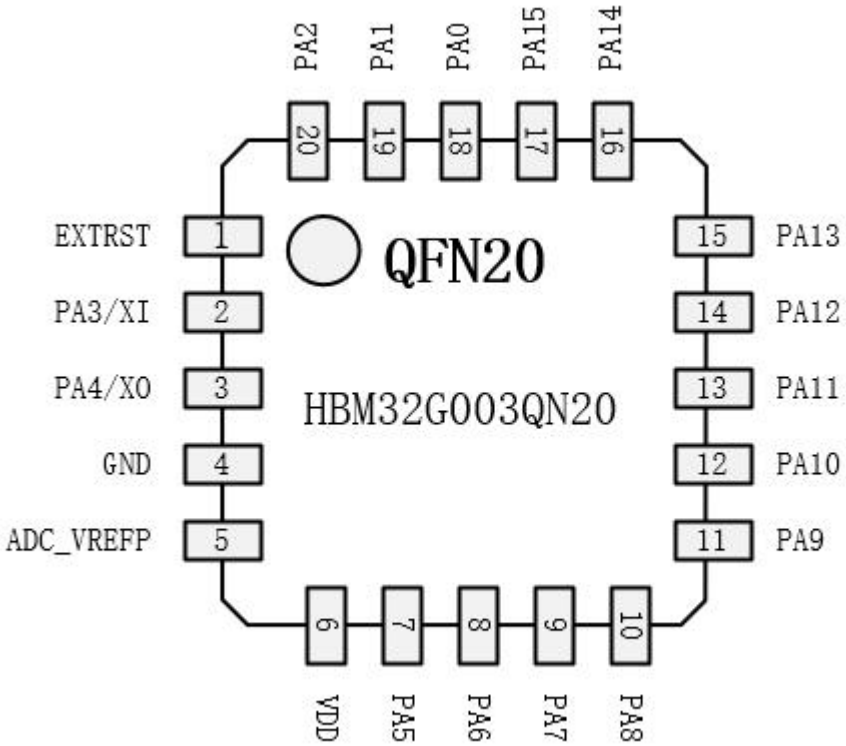
Each chip has a unique identifier when it leaves the factory.128Device identifier.IDaddress0x3FFE8~0x3FFF7.

4.Pin Definitions

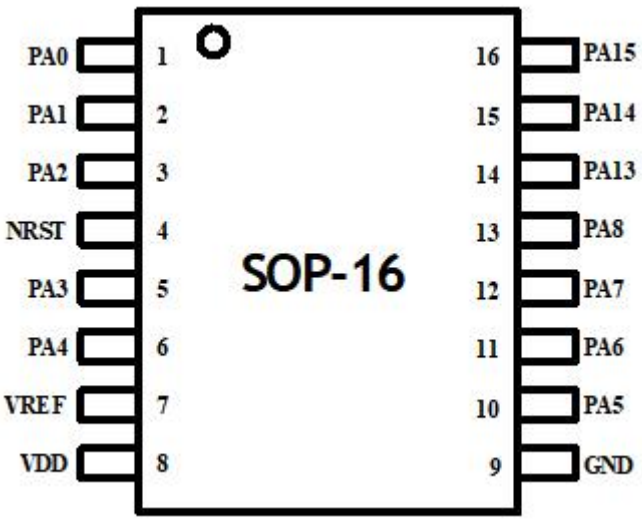
4.1Packaging



picture4.1 TSSOP20 (top view)



picture4.2 QFN20 (top view)



picture4.3 SOP16 (top view)

4.2Pin multiplexing function description

surface10 HBM32G003Pin Multiplexing Function Table

pin serial number TS20	pin serial number QN20	pin serial number SP16	pin definition	type	Reuse function	describe
9	6	8	VDD	S		2.3V~3.6VPower input pin
7	4	9	GND	S		power ground
4	1	4	RST	I/O		Hardware reset pin
8	5	7	VREF	I		ADCExternal reference voltage source
1	18	1	PA0	I/O	GPIO_PA0	PA0:numberGPIOFunctional pins
					SPI0_CLK	SPI0_CLK:SPI0clock pin
					TIMERP0_IN0	TIMERP0_IN0Advanced Timer0Input0pin
					TIMERP0_OUT0	TIMERP0_OUT0Advanced Timer0Output0pin
					PWMB0_CH0	PWMB0_CH0BasicPWM0passage0pin
					PWMP0_CH0N	PWMP0_CH0N:advancedPWM0passage0Npin
2	19	2	PA1	I/O	GPIO_PA1	PA1:numberGPIOFunctional pins
					SPI0_MOSI	SPI0_MOSI:SPI0host transmit pin
					UART0_TX	UART0_TXSerial port0transmit pin
					HALL_IN0	HALL_IN0Hall interface channel0pin
					PWMP0_CH1N	PWMP0_CH1N:advancedPWM0passage1Npin
					SARADC_CH1	SARADC_CH1:SARADCpassage1pin
3	20	3	PA2	I/O	GPIO_PA2	PA2:numberGPIOFunctional pins
					SPI0_MISO	SPI0_MISO:SPI0host receive pin
					UART0_RX	UART0_RXSerial port0Receive pin
					HALL_IN1	HALL_IN1Hall interface channel1pin
					PWMP0_CH2N	PWMP0_CH2N:advancedPWM0passage2Npin
					SARADC_CH0	SARADC_CH0:SARADCpassage0pin
5	2	5	PA3	I/O	GPIO_PA3	PA3:numberGPIOFunctional pins
					IIC0_SDA	IIC0_SDA:IIC0data pin
					PWMP0_CH0	PWMP0_CH0:advancedPWM0passage0pin
					XTAH_IN	XTAH_INInput pins of a high-frequency crystal oscillator
6	3	6	PA4	I/O	GPIO_PA4	PA4:numberGPIOFunctional pins
					IIC0_SCL	IIC0_SCL:IIC0clock pin
					PWMP0_CH1	PWMP0_CH1:advancedPWM0passage1pin
					XTAH_OUT	XTAH_OUT: Output pins of high-frequency crystal oscillators

10	7	10	PA5	I/O	GPIO_PA5	PA5:numberGPIOFunctional pins
					SPI0_SSN	SPI0_SSN:SPI0chip select pin
					TIMERP0_IN1	TIMERP0_IN1Advanced Timer0Input1pin
					TIMERP0_OUT1	TIMERP0_OUT1Advanced Timer0Output1pin
					PWMB0_CH1	PWMB0_CH1BasicPWM0passage1pin
					PWMP0_CH2	PWMP0_CH2:advancedPWM0passage2pin
					SARADC_CH7	SARADC_CH7:SARADCpassage7pin
11	8	11	PA6	I/O	GPIO_PA6	PA6:numberGPIOFunctional pins
					IIC0_SDA	IIC0_SDA:IIC0data pin
					BRAKE_IN0	BRAKE_IN0Brake input0aisle
					SARADC_CH6	SARADC_CH6:SARADCpassage6pin
12	9	12	PA7	I/O	GPIO_PA7	PA7:numberGPIOFunctional pins
					IIC0_SCL	IIC0_SCL:IIC0clock pin
					BRAKE_IN1	BRAKE_IN1Brake input1aisle
					HALL_IN2	HALL_IN2Hall interface channel2pin
					SARADC_CH5	SARADC_CH5:SARADCpassage5pin
13	10	13	PA8	I/O	GPIO_PA8	PA8:numberGPIOFunctional pins
					UART0_TX	UART0_TXSerial port0transmit pin
					TIMERP0_IN0	TIMERP0_IN0Advanced Timer0Input0pin
					TIMERP0_OUT0	TIMERP0_OUT0Advanced Timer0Output0pin
					PWMP0_CH2	PWMP0_CH2:advancedPWM0passage2pin
					PWMP0_CH0N	PWMP0_CH0N:advancedPWM0passage0Npin
14	11		PA9	I/O	GPIO_PA9	PA9:numberGPIOFunctional pins
					UART0_RX	UART0_RXSerial port0Receive pin
					TIMERP0_IN1	TIMERP0_IN1Advanced Timer0Input1pin
					TIMERP0_OUT1	TIMERP0_OUT1Advanced Timer0Output1pin
					PWMB0_CH2	PWMB0_CH2BasicPWM0passage2pin
					PWMP0_CH1N	PWMP0_CH1N:advancedPWM0passage1Npin
					SARADC_CH4	SARADC_CH4:SARADCpassage4pin
15	12		PA10	I/O	GPIO_PA10	PA10:numberGPIOFunctional pins
					SPI0_CLK	SPI0_CLK:SPI0clock pin
					TIMERP0_IN0	TIMERP0_IN0Advanced Timer0Input0pin
					TIMERP0_OUT0	TIMERP0_OUT0Advanced Timer0Output0pin
					PWMB0_CH0	PWMB0_CH0BasicPWM0passage0pin
					PWMP0_CH2N	PWMP0_CH2N:advancedPWM0passage2Npin
16	13		PA11	I/O	GPIO_PA11	PA11:numberGPIOFunctional pins
					SPI0_MOSI	SPI0_MOSI:SPI0host transmit pin
					TIMERP0_IN1	TIMERP0_IN1Advanced Timer0Input1pin
					TIMERP0_OUT1	TIMERP0_OUT1Advanced Timer0Output1pin
					PWMP0_CH0	PWMP0_CH0:advancedPWM0passage0pin
17	14		PA12	I/O	GPIO_PA12	PA12:numberGPIOFunctional pins

					SPI0_MISO	SPI0_MISO:SPI0host receive pin
					TIMERP0_IN0	TIMERP0_IN0Advanced Timer0Input0pin
					TIMERP0_OUT0	TIMERP0_OUT0Advanced Timer0Output0pin
					PWMP0_CH1	PWMP0_CH1:advancedPWM0passage1pin
18	15	14	PA13	I/O	GPIO_PA13	PA13:numberGPIOFunctional pins
					SWCLK	SWCLK:SWClock pin of the download port
					PWMP0_CH2	PWMP0_CH2:advancedPWM0passage2pin
19	16	15	PA14	I/O	GPIO_PA14	PA14:numberGPIOFunctional pins
					SWDIO	SWDIO:SWData pins of the download port
					TIMERP0_IN1	TIMERP0_IN1Advanced Timer0Input1pin
					TIMERP0_OUT1	TIMERP0_OUT1Advanced Timer0Output1pin
					PWMB0_CH1	PWMB0_CH1BasicPWM0passage1pin
					SARADC_CH3	SARADC_CH3:SARADCpassage3pin
20	17	16	PA15	I/O	GPIO_PA15	PA15:numberGPIOFunctional pins
					SPI0_SSN	SPI0_SSN:SPI0chip select pin
					TIMERP0_IN0	TIMERP0_IN0Advanced Timer0Input0pin
					TIMERP0_OUT0	TIMERP0_OUT0Advanced Timer0Output0pin
					PWMB0_CH2	PWMB0_CH2BasicPWM0passage2pin
					SARADC_CH2	SARADC_CH2:SARADCpassage2pin

4.3Pin multiplexing function

surface11HBM32G003Pin multiplexing function

TS20	QN20	SP16	pin name	SEL000	SEL001	SEL010	SEL011	SEL100	SEL101	SEL111
1	18	1	PA0	GPIOA0	SPI0_CLK	TIMERP0_IN0	TIMERP0_OUT0	PWMB0_CH0	PWMP0_CH0N	---
2	19	2	PA1	GPIOA1	SPI0_MOSI	UART0_TX	HALL_IN0	PWMP0_CH1N	---	SARADC_CH1
3	20	3	PA2	GPIOA2	SPI0_MISO	UART0_RX	HALL_IN1	PWMP0_CH2N	---	SARADC_CH0
5	2	5	PA3	GPIOA3	I2C0_SDA	PWMP0_CH0	---	---	---	XTAH_IN
6	3	6	PA4	GPIOA4	I2C0_SCL	PWMP0_CH1	---	---	---	XTAH_OUT
10	7	10	PA5	GPIOA5	SPI0_SSN	TIMERP0_IN1	TIMERP0_OUT1	PWMB0_CH1	PWMP0_CH2	SARADC_CH7
11	8	11	PA6	GPIOA6	I2C0_SDA	---	BREAK_IN0	---	---	SARADC_CH6
12	9	12	PA7	GPIOA7	I2C0_SCL	BREAK_IN1	HALL_IN2	---	---	SARADC_CH5
13	10	13	PA8	GPIOA8	UART0_TX	TIMERP0_IN0	TIMERP0_OUT0	PWMP0_CH2	PWMP0_CH0N	---
14	11		PA9	GPIOA9	UART0_RX	TIMERP0_IN1	TIMERP0_OUT1	PWMB0_CH2	PWMP0_CH1N	SARADC_CH4
15	12		PA10	GPIOA10	SPI0_CLK	TIMERP0_IN0	TIMERP0_OUT0	PWMB0_CH0	PWMP0_CH2N	---
16	13		PA11	GPIOA11	SPI0_MOSI	TIMERP0_IN1	TIMERP0_OUT1	PWMP0_CH0	---	---

17	14		PA12	GPIOA12	SPI0_MISO	TIMERP0_IN0	TIMERP0_OUT0	PWMP0_CH1	---	---
18	15	14	PA13	GPIOA13	SWCLK	PWMP0_CH2	---	---	---	---
19	16	15	PA14	GPIOA14	SWDIO	TIMERP0_IN1	TIMERP0_OUT1	PWMB0_CH1	---	SARADC_CH3
20	17	16	PA15	GPIOA15	SPI0_SSN	TIMERP0_IN0	TIMERP0_OUT0	PWMB0_CH2	---	SARADC_CH2

5.Electrical characteristics

This chapter describes the chip's electrical parameters, including operating voltage, operating temperature, power consumption, analog characteristics, and...IOCharacteristic parameters, etc.

5.1Test conditions

Unless otherwise specified, all voltages are in...3.3VBased on ambient temperature. Unless otherwise specified, the maximum and minimum parameters are based on ambient temperature.

SpendT_A=25 °C,V_{DD}=3.3VThe test was conducted below.

5.2Absolute maximum rating

5.2.1Voltage characteristics

surface12 Voltage characteristics

symbol	describe	Minimum value	Typical value	Maximum value	unit
V_{DD}-V_{SS}	External main power supply voltage	- 0.3		3.6	V
V_{IN}	Pin input voltage	VSS-0.3		3.6	V
-V_{DD}	Voltage difference between different power supply pins			50	mV
-VSS	Voltage difference between different ground pins			50	mV

5.2.2Current characteristics

surface13 Current characteristics

symbol	describe	Minimum value	Typical value	Maximum value	unit
I_{DD}	The total current flowing through the power line			120	*mA*
I_{OUT}	Output current on a single pin	- 30		30	*mA*
I_{IN}	Injected current on a single pin	- 5		5	*mA*
-I_{IN}	Total injected current on all pins	- 25		25	*mA*

5.2.3Temperature characteristics

surface14 Temperature characteristics

symbol	describe	Minimum value	Typical value	Maximum value	unit
T_{STG}	Storage temperature range	- 45		150	℃
T_J	Maximum junction temperature			125	℃

5.3Working conditions

5.3.1General working conditions

surface15 Common working conditions table

symbol	describe	Minimum value	Typical value	Maximum value	unit
V_{DD}	Standard operating voltage	2.4	3.3	3.6	V
F_{CLK}	System clock frequency			48	MHz
T_A	Operating temperature	- 40		85	℃

5.3.2Operating conditions for power on and power off

surface16 Operating conditions for power on and power off

symbol	describe	Minimum value	Typical value	Maximum value	unit
T_{VR}	VDDrate of increase	10		∞	uS/V
T_{VF}	VDDrate of descent	10		∞	uS/V

5.3.3Reset and power control module characteristics

surface17 Reset and power control module characteristics

symbol	describe	Minimum value	Typical value	Maximum value	unit
V_{POR}	Power-on reset threshold	2.45	2.5	2.58	V
V_{PDR}	Power-off reset threshold	2.35	2.4	2.47	V
V_{HYS}	PDRhysteresis	95	100	105	mV
T_{RST}	Reset duration		0.6		ms

5.3.4Supply current characteristics

surface18 Supply current characteristics

symbol	describe	condition	Minimum value	Typical value	Maximum value	unit
I_{DD}	Power supply current in operation mode	3.3V@48MHz Run in RAM All Peripherals clock OFF		3		*mA*
I_{DD}	Power supply current in operation mode	3.3V@24MHz Run in RAM All Peripherals clock OFF		1.5		*mA*

I_{DD}	Power supply current in operation mode	3.3V@12MHz Run in RAM All Peripherals clock OFF		950		-A
I_{DD}	Power supply current in operation mode	3.3V@32KHz Run in RAM All Peripherals clock OFF		250		-A
I_{DD}	Power supply current in operation mode	3.3V@48MHz All Peripherals clock ON		2.3		*mA*
I_{DD}	Power supply current in operation mode	3.3V@24MHz All Peripherals clock ON		1.3		*mA*
I_{DD}	Power supply current in operation mode	3.3V@12MHz All Peripherals clock ON		770		-A
I_{DD}	Power supply current in operation mode	3.3V@48MHz All Peripherals clock OFF		2.1		*mA*
I_{DD}	Power supply current in operation mode	3.3V@24MHz All Peripherals clock OFF		1.1		*mA*
I_{DD}	Power supply current in operation mode	3.3V@12MHz All Peripherals clock OFF		710		-A
I_{DD}	standbySupply current in mode	3.3V@48MHz	0.65	1	1.4	*mA*
I_{DD}	standbySupply current in mode	3.3V@48MHz All Peripherals clock ON		700		-A
I_{DD}	standbySupply current in mode	3.3V@24MHz All Peripherals clock ON		500		-A
I_{DD}	standbySupply current in mode	3.3V@12MHz All Peripherals clock ON		390		-A
I_{DD}	standbySupply current in mode	3.3V@48MHz All Peripherals clock OFF		510		-A
I_{DD}	standbySupply current in mode	3.3V@24MHz All Peripherals clock OFF		380		-A
I_{DD}	standbySupply current in mode	3.3V@12MHz All Peripherals clock OFF		330		-A
I_{DD}	sleepSupply current in mode	3.3V@48MHz	10.6	13	16.2	-A
I_{DD}	sleepSupply current in mode	3.3V@48MHz All Peripherals clock ON		64		-A
I_{DD}	sleepSupply current in mode	3.3V@24MHz All Peripherals clock ON		58		-A
I_{DD}	sleepSupply current in mode	3.3V@12MHz All Peripherals clock ON		55		-A

I_{DD}	sleepSupply current in mode	3.3V@48MHz All Peripherals clock OFF		51		-A
I_{DD}	sleepSupply current in mode	3.3V@24MHz All Peripherals clock OFF		47		-A
I_{DD}	sleepSupply current in mode	3.3V@12MHz All Peripherals clock OFF		40		-A
I_{DD}	stopSupply current in mode	3.3V@48MHz	0.64	0.8	0.95	-A
I_{DD}	stopSupply current in mode	3.3V@48MHz All Peripherals clock OFF		25		-A
I_{DD}	stopSupply current in mode	3.3V@24MHz All Peripherals clock OFF		25		-A
I_{DD}	stopSupply current in mode	3.3V@12MHz All Peripherals clock OFF		25		-A

Note: All bandsAll Peripherals clockThe conditional current is measured after connecting the basic peripherals.

5.3.5Clock source characteristics

surface19 Clock source characteristics

symbol	describe	condition	Minimum value	Typical value	Maximum value	unit
HSI	Internal high-frequency clock frequency	VDD=3.3V - 40℃~85℃	4	48	48	MHz
ACC	HSIOscillator accuracy	VDD = 2.3V~3.6V - 40℃~85℃	- 0.8		0.8	%
DC	Internal crystal oscillator duty cycle	VDD=3.3V	45	50	55	%
T_{SU}	HSIOscillator start-up time	VDD=3.3V F_{MCLK}=48MHz		10		-S
I_{DD}	HSIOscillator power consumption	VDD=3.3V F_{MCLK}=48MHz	70	105	150	-A
LSI	Internal low-frequency clock frequency	VDD=3.3V - 40℃~85℃	32.276	32.768	33.26 kHz	
ACC	LSIOscillator accuracy	VDD=3.3V	- 1.5		1.5	%
I_{DD}	LSIOscillator power consumption	VDD=3.3V	0.3	0.5	1	-A
HSE	External high-frequency clock frequency		4	8	32	MHz
DC	External crystal oscillator duty cycle	VDD=3.3V	40	50	60	%
T_{SU}	HSEOscillator start-up time	VDD=3.3V F=16MHz	3	6	8	*mS*

5.3.6 EMCcharacteristic

surface20 EMCcharacteristic

symbol	describe	condition	Maximum value	unit
ESD(HBM)	Electrostatic discharge human body model	TA = 25◦C, conform toJEDEC JS-001-2017	4000	V
ESD(CDM)	Model of electrostatic discharge charging equipment	TA = 25◦C, conform toJEDEC JS-002-2014	500	V
LatchUp	Static latch class	TA = 25◦C, conform toJEDEC78D	100	*mA*

5.3.7 IOPort characteristics

surfacetwenty one IOPort characteristics

symbol	describe	Minimum value	Typical value	Maximum value	unit
V_{IL}((delayed gate)	Input low level voltage			0.3VDD	V
V_{IH}((delayed gate)	Input high level voltage	0.7VDD			V
V_{HYS}((delayed gate)	IOSchmitt trigger voltage hysteresis		1.3		V
V_{IL}((Delayed opening)	Input low level voltage			0.15VDD	V
V_{IH}((Delayed opening)	Input high level voltage	0.85VDD			V
V_{HYS}((Delayed opening)	IOSchmitt trigger voltage hysteresis		2.2		V
I_{IH}	Input leakage current	- 1		1	-A
I_{IL}	Input leakage current	- 1		1	-A
R_{PU}	If the pull-up equivalent resistance		30/40/150		K-
R_{PD}	If the equivalent resistance is pulled down		40		K-
V_{OL}	Output low level voltage			0.35	V
V_{OH}	Output high level voltage	VDD-0.35			V

5.3.8Memory characteristics

surfacetwenty two Memory characteristics

symbol	describe	Minimum value	Typical value	Maximum value	unit
T_P	Page programming time		2	3	*mS*
T_E	Page erase time		1.7	2	*mS*
T_E	Sector erase time		1.7	2	*mS*
I_{DPD}	Low power mode current		0.6	1.5	-A
N_{END}	Erasing/writing count	100000			Second-rate
T_{RET}	Data retention period	20			Year

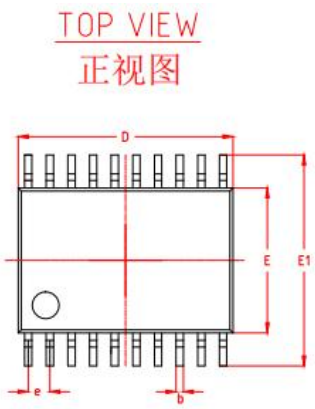
5.3.9 ADCcharacteristic

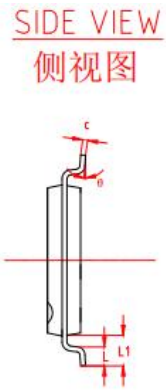
surfacetwenty three ADCcharacteristic

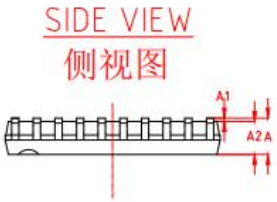
symbol	describe	Minimum value	Typical value	Maximum value	unit
EX_{VREF-}	External reference voltage			VDD	V
IN_{VREF-}	Internal reference voltage	1.386	1.4	1.414	V
F_{CLK}	ADCclock frequency			48	MHz
F_S	Sampling rate			2.4	MHz
V_{AIN}	Conversion voltage range	0		VREF+	V
R_{AIN}	External input impedance	1.2		1050	K-
T_S	Sampling time	0.1		16	-S
T_V	Total conversion time	1		16.9	-S
E_T	Comprehensive error	- 16		16	LSB
E_O	Offset error	- 10		10	LSB
E_G	Gain error	- 10		10	LSB
E_D	Differential linearity error	- 4		4	LSB
E_L	Integral linearity error	- 8		8	LSB

6.Package size

6.1 TSSOP20Package size

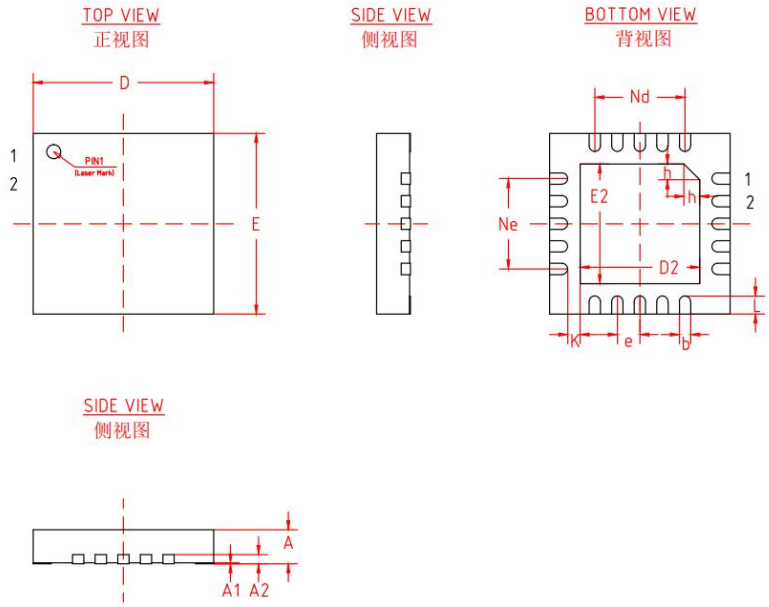






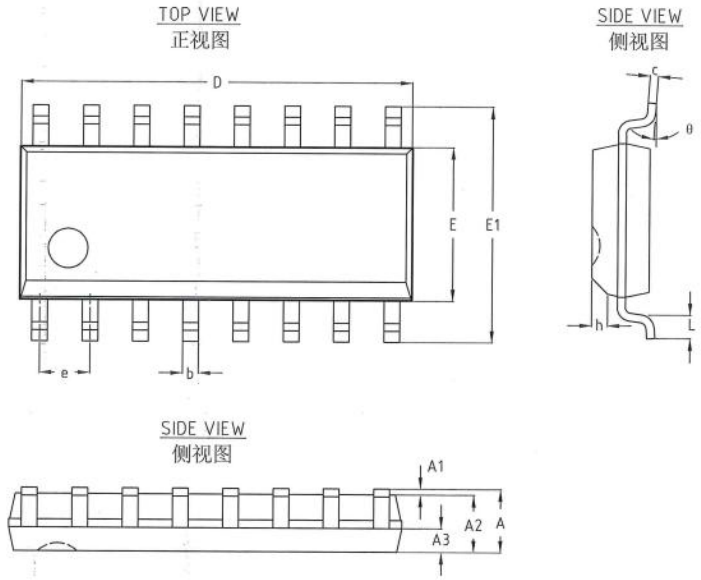
机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	6.50	6.60
E	4.30	4.40	4.50
E1	6.25	6.40	6.55
e	0.65 BSC		
L1	1.00REF		
L	0.45	0.60	0.75
θ	0°	-	8°

6.2 QFN20Package size



机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	0.70	0.75	0.80
A1	–	0.02	0.05
A2	0.203 REF		
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.55	2.65	2.75
E	3.90	4.00	4.10
E2	2.55	2.65	2.75
e	0.50 BSC		
K	0.225	0.275	0.325
L	0.30	0.40	0.50
h	0.30	0.35	0.40
Ne	2.00 BSC		
Nd	2.00 BSC		

6.3 SOP16Package size



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.10	–	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.35	–	0.50
c	0.19	–	0.25
D	9.80	10.00	10.20
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	–	0.50
L	0.40	–	0.80
θ	0°	–	8°