Steps for all experiment

Expt 1 : Schematic of nmos transistor

schematic

Steps:

1. Open electric vlsi
2. Click on file then New library name it with your name and expt (no space)
3. Click on cell write your name with expt (no space) and select schematic
4. Then select nmos 4 port transistor port and ground
5. Click on nmos and ctrl + I
6. A window appears and select width = 10 click ok
7. Click on nmos and click on Tools and then simulation(spice)
8. In that select spice model then spice model text appears click on it and ctrl+i
9. Then write “NMOS” (NO small letters and this “”)
10. Connect substrate and ground by wire
11. First left click on the substrate end and then right click anywhere for the wire to connect
12. To add g,d,s selec the end of the nmos
13. Like for gate select the gate end terminal then click on export tab then create new export then write g and ok similarly for d and s.
14. To write the code, click on Misc. in that select spice code and then click on the screen
15. A text appears on that click it and ctrl+I a window appears and click on multi-line
16. Then write the code
17. Then click on tools and then click on simulation(spice) and click on write spice deck.
18. Lt spice windows appears then right clickon the black screen select add trace in that select Id[Mnmos] and graph appears.

Layout

1. Open electric vlsi
2. Click on file then New library name it with your name and expt (no space)
3. Click on cell write your name with expt (no space) and select layout.
4. Select nmos rotate clockwise 90 from edit
5. Ctrl+I and change width to 10
6. Select 2 n act one put on the left and other on right, change both n act y-size to 10 by ctrl+i.
7. Connect the to nmos and then drag and place it at 3.5 spacing
8. Select p well below nmos and then ctrl+i, x-size = 25
9. Connect left n act with p well
10. Drag close to nmos till spacing 3.5
11. Select metal-1 polysilicon and connect to the pink part.
12. Select the metal click on export in that create export and name it as g similarly for s, d and gnd.
13. To write the code, click on Misc. in that select spice code and then click on the screen
14. A text appears on that click it and ctrl+I a window appears and click on multi-line
15. Then write the code
16. Then click on tools and then click on simulation(spice) and click on write spice deck.
17. Lt spice windows appears then right clickon the black screen select add trace in that select Is[Mnmos] and graph appears.

Code:

```
vs s 0 DC 0
vg g 0 DC 0
vd d 0 DC 0
vw w 0 DC 0
.dc vd 0 5 1m vg 0 5 1
.include C:\electric\C5_models.txt
```

Expt2: schematic on cmos inverter

1. Open electric vlsi
2. Click on file then New library name it with your name and expt (no space)
3. Click on cell write your name with expt (no space) and select schematic
4. Select pmos transistor node
5. Click on pmos and ctrl + I
6. A window appears and select width = 10 click ok
7. Click on pmos and click on Tools and then simulation(spice)
8. In that select spice model then spice model text appears click on it and ctrl+i
9. Then write “PMOS” (NO small letters and this “”)

10. Select Nmos transistor node
11. Click on Nmos and ctrl + I
12. A window appears and select width = 10 click ok
13. Click on Nmos and click on Tools and then simulation(spice)
14. In that select spice model then spice model text appears click on it and ctrl+i
15. Then write “NMOS” (NO small letters and this “”)
16. Select ground and connect it to nmos
17. Select power and connect to pmos
18. Select off page and connect the arrow side to common gate of nmos and pmos
19. Select another off page and connect the common wire to back of offpage
20. Then click on offpage and click on export and create export and write in, similarly for another one and write out
21. To write the code, click on Misc. in that select spice code and then click on the screen
22. A text appears on that click it and ctrl+I a window appears and click on multi-line
23. Then write the code
24. Then click on tools and then click on simulation(spice) and click on write spice deck.
25. Lt spice windows appears then right clickon the black screen select add plot .
26. On the first plot click on it then right click and add trace v[in].
27. On the second plot click on it then right click and add trace v[out].
28. Then in view on ltspice click on spice error log

Code:

```
vdd vdd 0 DC 5
vin in 0 DC pwl 10n 0 20n 5 50n 5 60n 0
cload out 0 250fF
.measure tran tf trig v(out) val=4.5 fall=1 td=8ns targ v(out) val=0.5 fall=1
.measure tran tr trig v(out) val=0.5 rise=1 td=50ns targ v(out) val=4.5 rise=1
.tran 0 100ns
.include C:\electric \C5_models.txt
```

Expt 3 : Layout of CMOS inverter

1. Open electric vlsi
2. Click on file then New library name it with your name and expt (no space)
3. Click on cell write your name with expt (no space) and select layout.
4. Select nmos rotate clockwise 90 from edit
5. Ctrl+I and change width to 10
6. Select 2 n act one put on the left and other on right, change both n act y-size to 10 by ctrl+i.
7. Connect the to nmos and then drag and place it at 3.5 spacing
8. Select p well below nmos and then ctrl+i, x-size = 25
9. Connect left n act with p well
10. Drag close to nmos till spacing 3.5
11. Select pmos rotate clockwise 90 from edit
12. Ctrl+I and change width to 10
13. Select 2 p act one put on the left and other on right, change both p act y-size to 10 by ctrl+i.
14. Connect the to pmos and then drag and place it at 3.5 spacing
15. Select n well above pmos and then ctrl+i, x-size = 25
16. Connect left p act with p well
17. Drag close to pmos till spacing 3.5
18. Then connect the pink part together with metal act and export and give it name as 'in '
19. Connect together right side acts and export and give it name as "out"
20. Export pwell and nwell as give name as "gnd" and "vdd"
18. To write the code, click on Misc. in that select spice code and then click on the screen
19. A text appears on that click it and ctrl+I a window appears and click on multi-line
20. Then write the code
21. Then click on tools and then click on simulation(spice) and click on write spice deck.
22. Lt spice windows appears then right clickon the black screen select add plot .
23. On the first plot click on it then right click and add trace v[in].
24. On the second plot click on it then right click and add trace v[out].
25. Then in view on ltspice click on spice error log.

Code:

```
vdd vdd 0 DC 5
vin in 0 DC pwl 10n 0 20n 5 50n 5 60n 0
cload out 0 250fF
.measure tran tf trig v(out) val=4.5 fall=1 td=8ns targ v(out) val=0.5 fall=1
.measure tran tr trig v(out) val=0.5 rise=1 td=50ns targ v(out) val=4.5 rise=1
.tran 0 100ns
.include C:\electric \C5_models.txt
```

Expt 4 : schematic of nand gate

1. Open electric vlsi
2. Click on file then New library name it with your name and expt (no space)
3. Click on cell write your name with expt (no space) and select schematic
4. Select 2 pmos transistor node
5. Click on pmos and ctrl + I
6. A window appears and select width = 10 click ok
7. Click on pmos and click on Tools and then simulation(spice)
8. In that select spice model then spice model text appears click on it and ctrl+i
9. Then write “PMOS” (NO small letters and this “”)
10. Then connect pmos parallely
11. Similarly for nmos and connect in series
12. Select ground and connect it to nmos
13. Select power and connect to pmos
14. Select off page and connect the arrow side to common gate of nmos and pmos
15. Select another off page and connect the common output to back of offpage
16. Using export give name to arrow off pages
17. To write the code, click on Misc. in that select spice code and then click on the screen
18. A text appears on that click it and ctrl+I a window appears and click on multi-line
19. Then write the code
20. Then click on tools and then click on simulation(spice) and click on write spice deck.
21. Lt spice windows appears then right click on the black screen select add plot .
22. On the first plot click on it then right click and add trace v[in].
23. On the second plot click on it then right click and add trace v[out].
24. Then in view on ltspice click on spice error log

Code:

```
vdd vdd 0 DC 5
va A 0 DC pwl 10n 0 20n 5 50n 5 60n 0 90n 0 100n 5 130n 5 140n 0 170n 0 180n 5
vb B 0 DC pwl 10n 0 20n 5 100n 5 110n 0n
.measure tran tf trig v(Y) val = 4.5 fall=1 td=4ns targ v(Y) val = 0.5 fall=1
.measure tran tr trig v(Y) val = 0.5 rise= 1 td=4ns targ v(Y) val = 4.5 rise=1
.tran 200n
.include C:\electric \C5_models.txt
```

Expt 5 : LAYOUT of NOR gate

21. Open electric vlsi
22. Click on file then New library name it with your name and expt (no space)
23. Click on cell write your name with expt (no space) and select layout.
24. Select 2 nmos rotate clockwise 90 from edit
25. Ctrl+I and change width to 10
26. Select 3 n act one put on the left, center and other on right, change both n act y-size to 10 by ctrl+i.
27. Connect the to 2 nmos and then drag and place it at 3.5 spacing
28. Select p well below nmos and then ctrl+i, x-size = 30
29. Connect left and right n act with p well
30. Drag close to nmos till spacing 3.5
31. Select 2 pmos rotate clockwise 90 from edit
32. Ctrl+I and change width to 10
33. Select 2 p act one put on the left and other on right, change both p act y-size to 10 by ctrl+i.
34. NOTE: NO 3rd P ACT . DIRECTLY CONNECT PMOS
35. Connect the to pmos and then drag and place it at 3.5 spacing
36. Select n well above pmos and then ctrl+i, x-size = 30
37. Connect left p act with p well
38. Drag close to pmos till spacing 3.5
39. Then common connect pink part(gate) and do necessary connection
40. Give name to offpages by create export and give name A ,B, AND Y
41. To write the code, click on Misc. in that select spice code and then click on the screen
42. A text appears on that click it and ctrl+I a window appears and click on multi-line
43. Then write the code
44. Then click on tools and then click on simulation(spice) and click on write spice deck.
45. Lt spice windows appears then right clickon the black screen select add plot .
46. On the first plot click on it then right click and add trace v[A].
47. On the second plot click on it then right click and add trace v[B].
48. On the third plot click on it then right click and add trace v[Y].
49. Then in view on ltspice click on spice error log.

Code:

```
vdd vdd 0 DC 5
va A 0 DC pwl 10n 0 20n 5 50n 5 60n 0 90n 0 100n 5 130n 5 140n 0 170n 0 180n 5
vb B 0 DC pwl 10n 0 20n 5 100n 5 110n 0
.measure tran tf trig v(Y) val=4.5 fall=1 td=4ns targ v(Y) val=0.5 fall=1
.measure tran tf trig v(Y) val=0.5 rise=1 td=4ns targ v(Y) val=4.5 rise=1
.tran 200n
.include C:\electric \C5_models.txt
```