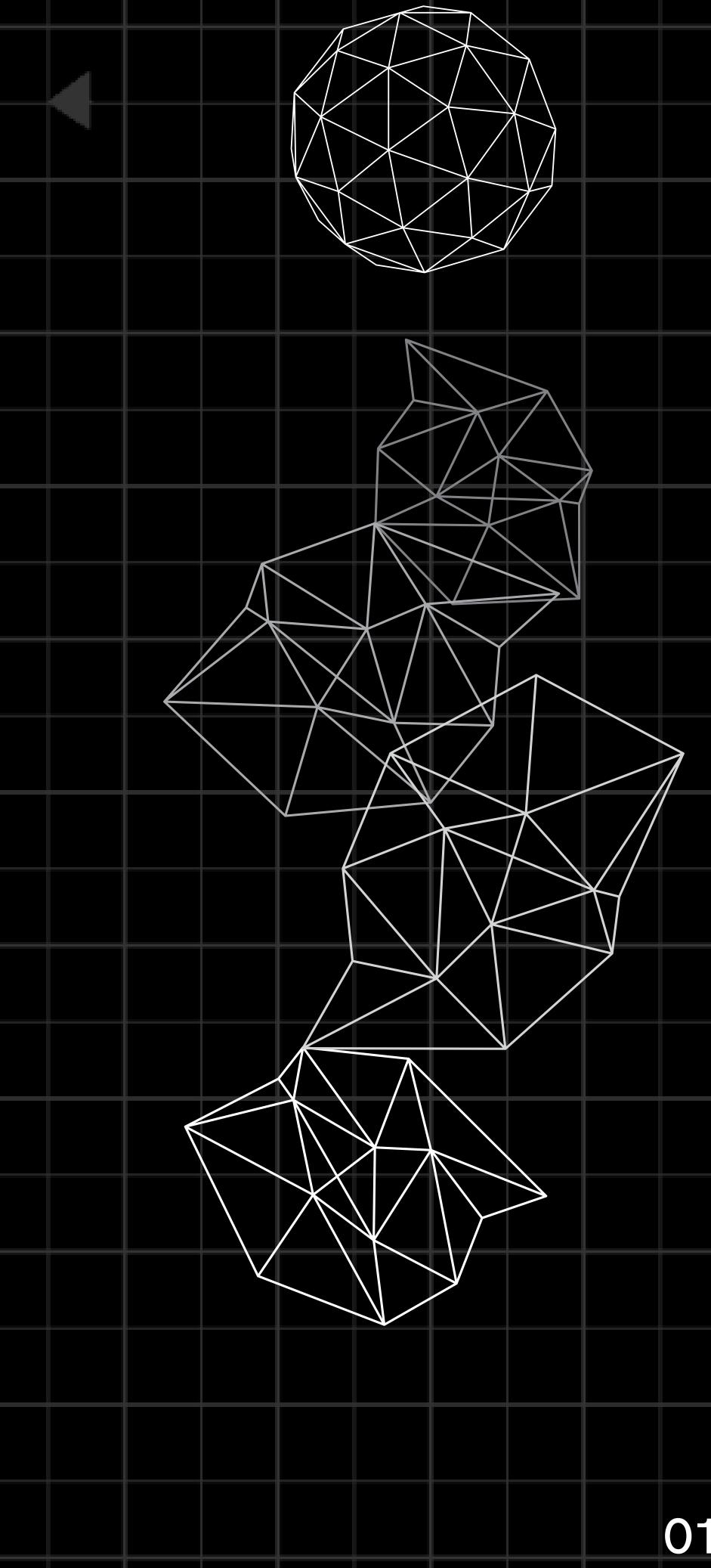


Performance Evaluation of FIR Filter After Implementation on Different FPGA and SOC and Its Utilization in Communication and Network

Varad Patil	120A2036
Pranali Salvi	221A2064
Sashank Singh	221A2067
Ajaz Shaikh	221A2068
Shreyash Wankhede	221A2069

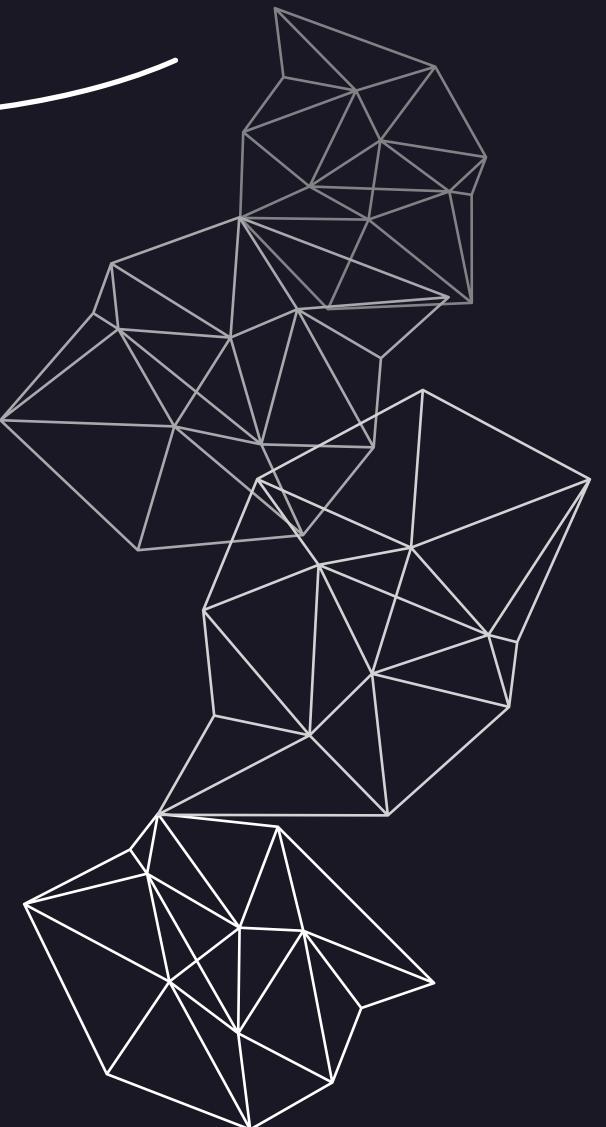
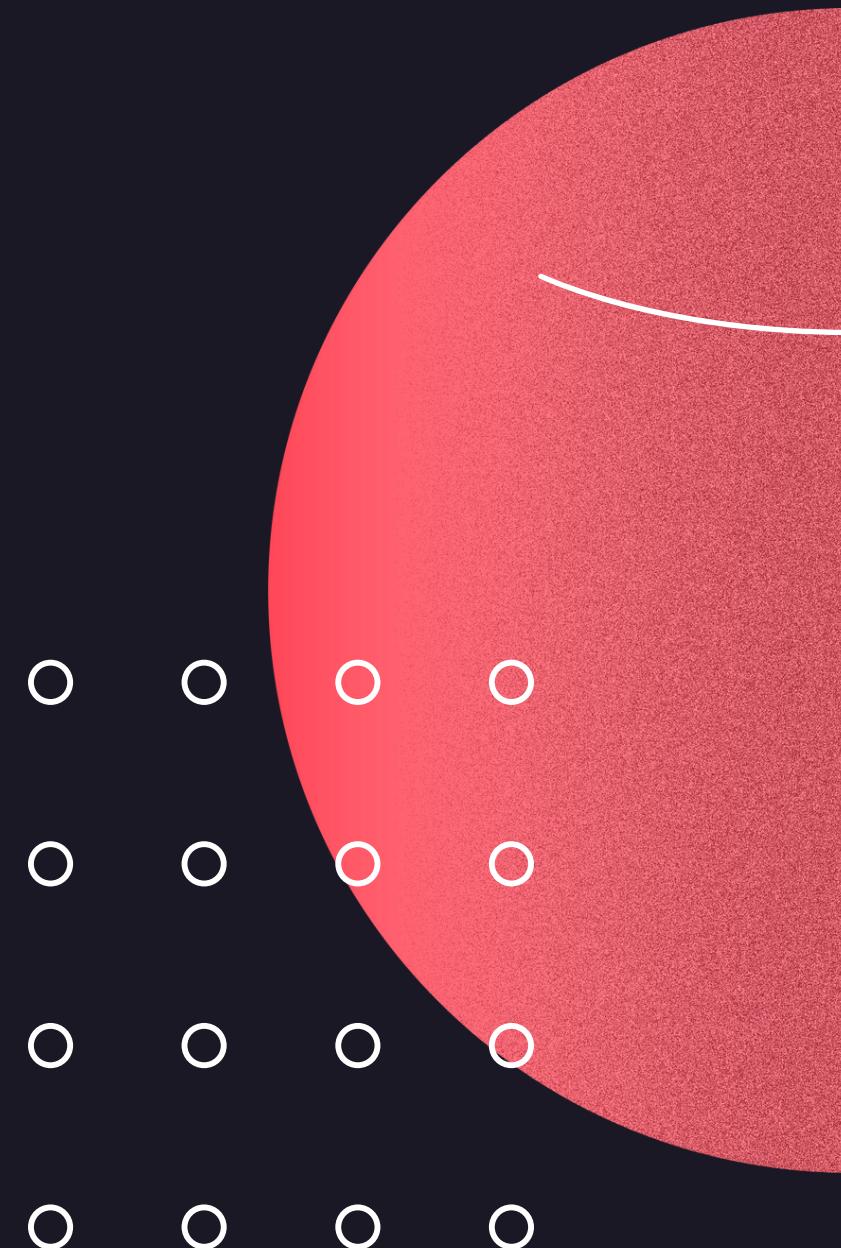


Introduction

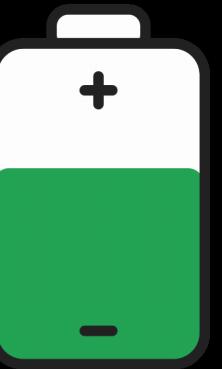
- Ultrascale FPGA is ideal for packet processing in 100G networking and heterogeneous wireless infrastructure.
- Three different FPGAs: Artix-7, Zynq, Kintex-7 and Ultrascale performance of our FIR Filter design. FPGA and SoCs offer high performance and low capabilities (capacity and performance) of FPGAs increased dramatically. So, the current architecture of FPGA and SOC are almost similar to Xilinx 7 series FPGAs comprising three new FPGA families In our research, we are using: two 28 nm 7 Series FPGAs, one SOC, and one 20 nm ultra scale FPGA
- Artix-7 and Kintex-7 are two 7 series FPGA families are specially optimized for best price performance. Kintex UltraScale FPGA was made using 20 nm process technology in comparison with the other three devices made using 28 nm Ultrascale FPGA is considered as the best device for packet processing in 100G networking and wireless communication.



Literature Survey

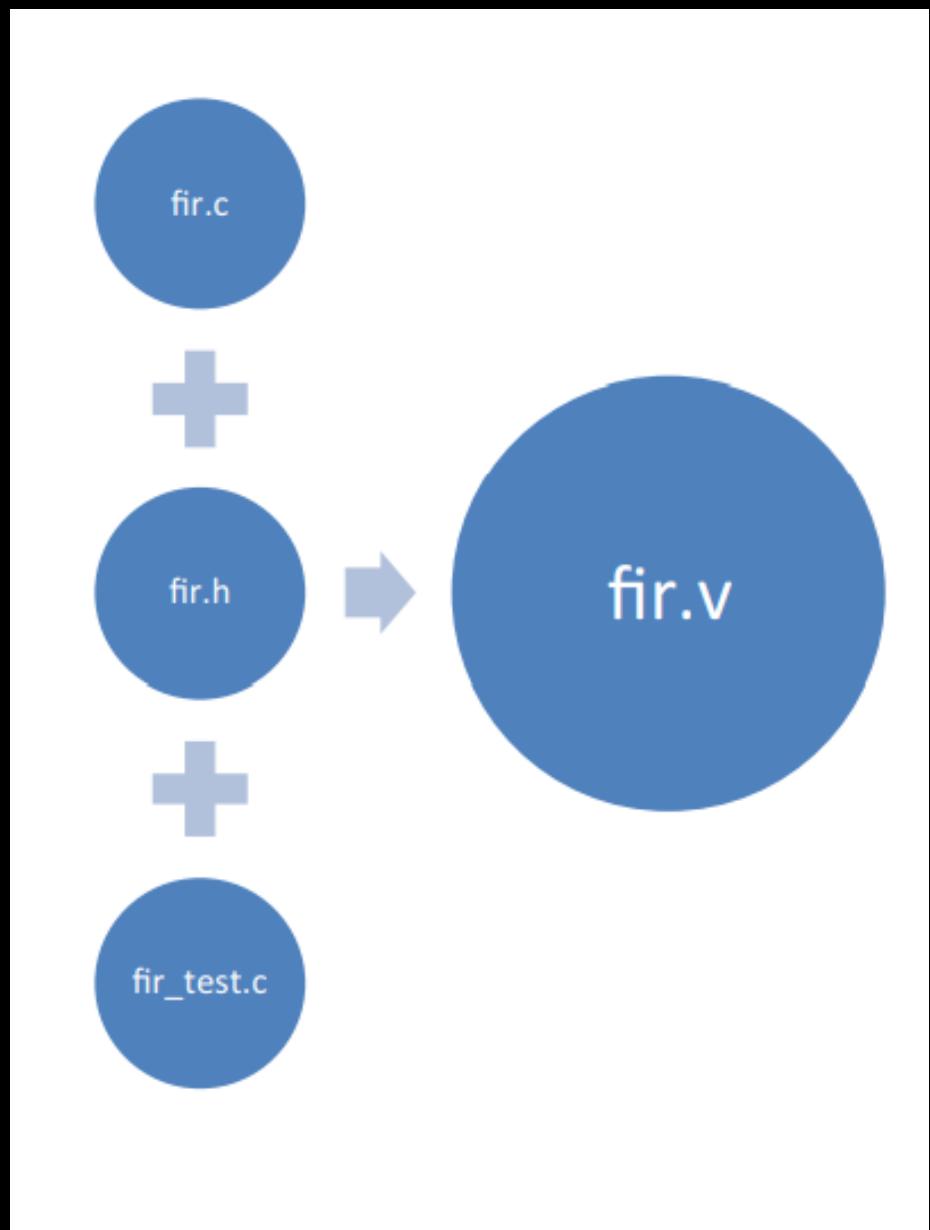


- Rezaee, A. (2015). Using coevolutionary genetic algorithms for estimation of blind fir channel. *Wireless Personal Communications*, 83(1), 191–201.
- Kannan, G., Garg, M., Merchant, S. N., et al. (2008). MPOE based prefiltering and MRT beamforming with matched filter receiver for DS-CDMA systems. *Wireless Personal Communications*
- Mosavi, M. R., Moghaddasi, M. S., & Rezaei, M. J. (2016). A new method for continuous wave interference mitigation in single-frequency GPS receivers. *Wireless Personal Communications*



POWER ANALYSIS OF GENERATED HDL CODE OF COMMUNICATION SPECIFIC FIR FILTER

- The Vivado HLS 2016.1 tool receive benchmark C code provided by Xilinx and synthesize that C code and measure latency, delay and interval for four different architecture.
- Then we export synthesized design into RTL that save in form of HDL either Verilog or VHDL.
- The benchmark code fir.c is translated to fir.v (Verilog Code)



Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 14.634 W
Junction Temperature: 61.2 °C
Thermal Margin: 23.8 °C (9.3 W)
Effective ΔJA: 2.5 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: [Low](#)

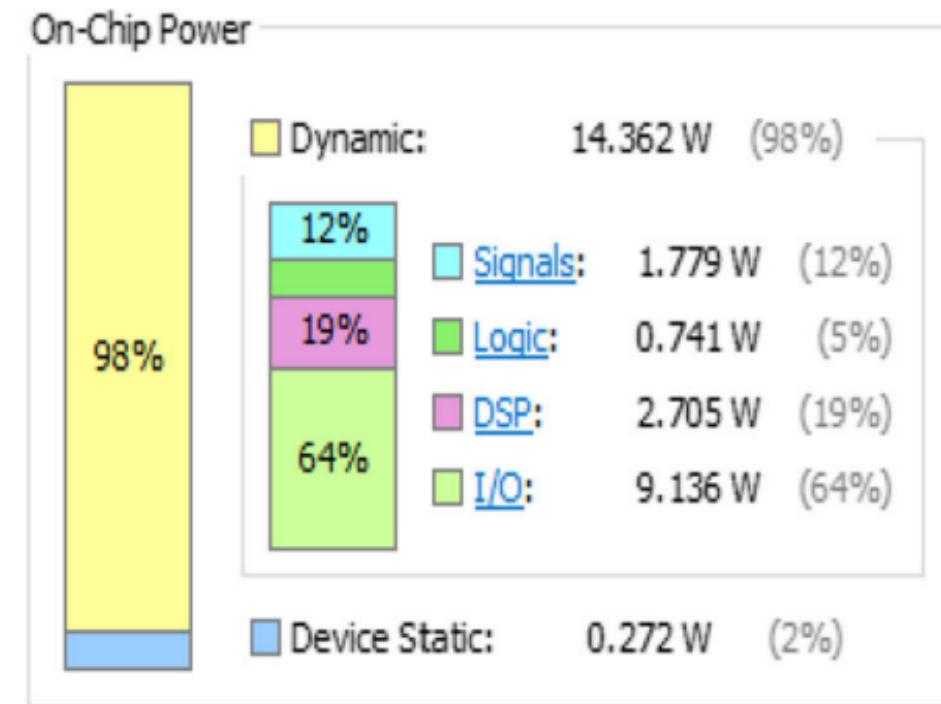


Fig. 3 Power analysis of FIR filter on Kintex-7 FPGA

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 15.143 W
Junction Temperature: 64.2 °C
Thermal Margin: 20.8 °C (7.8 W)
Effective ΔJA: 2.6 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: [Low](#)

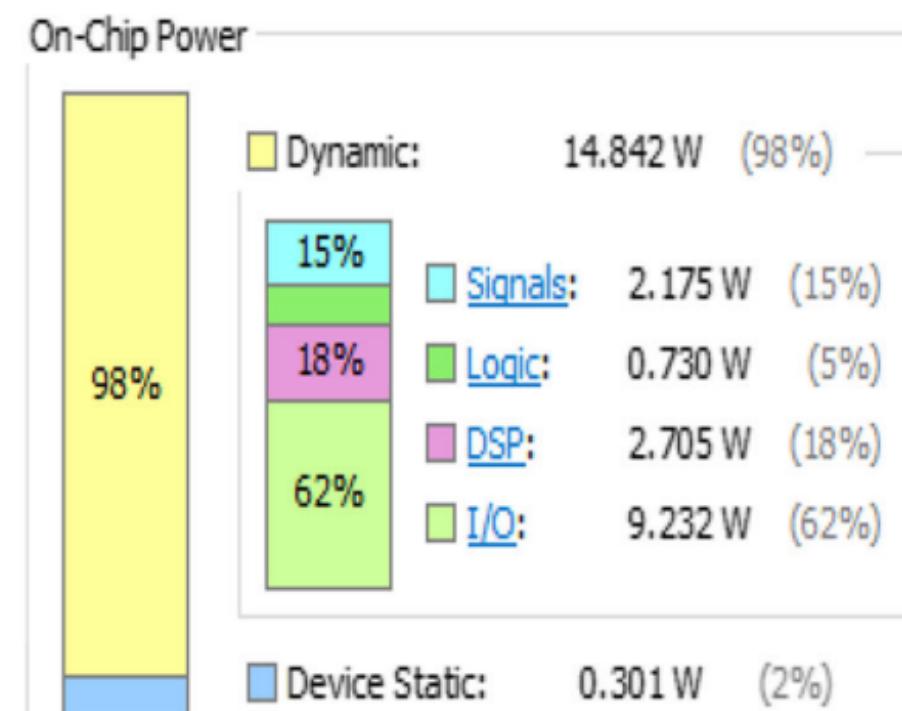


Fig. 4 Power analysis of FIR filter on Zynq 7000 all programmable SOC

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 14.697 W
Junction Temperature: 92.6 °C
Thermal Margin: 7.4 °C (1.6 W)
Effective ΔJA: 4.6 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: [Low](#)

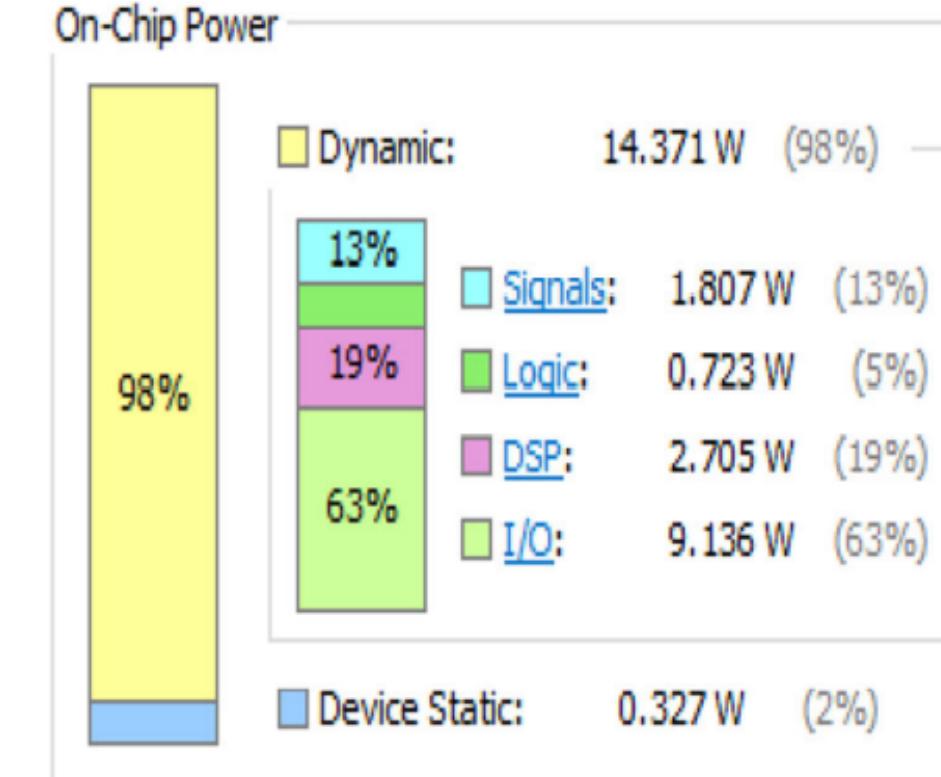


Fig. 5 Power analysis of FIR filter on Artix-7 FPGA

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 12.51 W
Junction Temperature: 52.2 °C
Thermal Margin: 47.8 °C (20.7 W)
Effective ΔJA: 2.2 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: [Low](#)

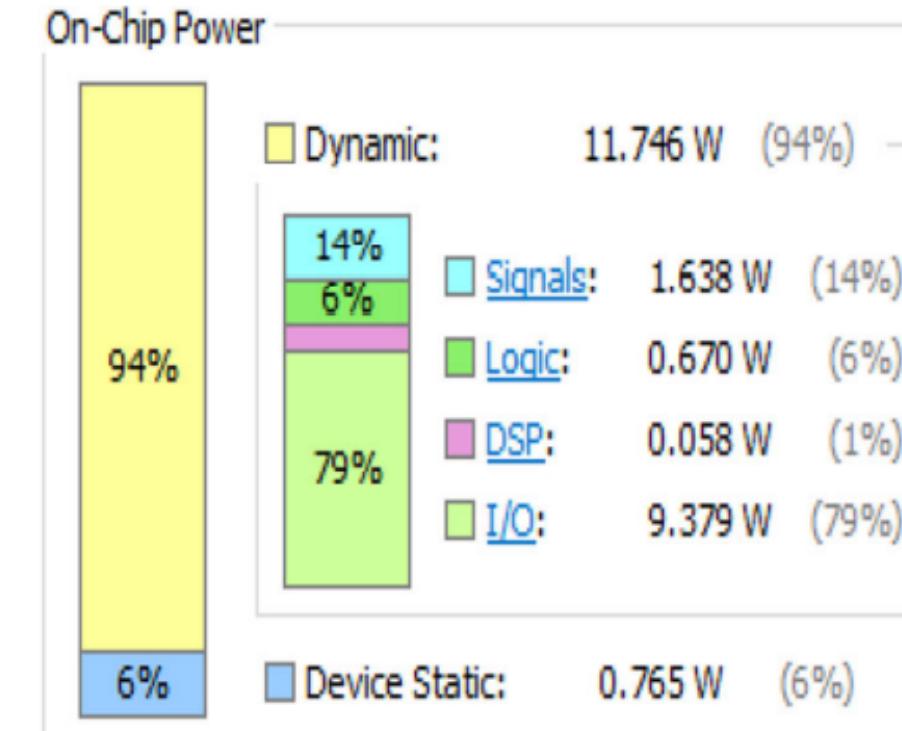


Fig. 6 Power analysis of FIR filter on Kintex ultrascale FPGA

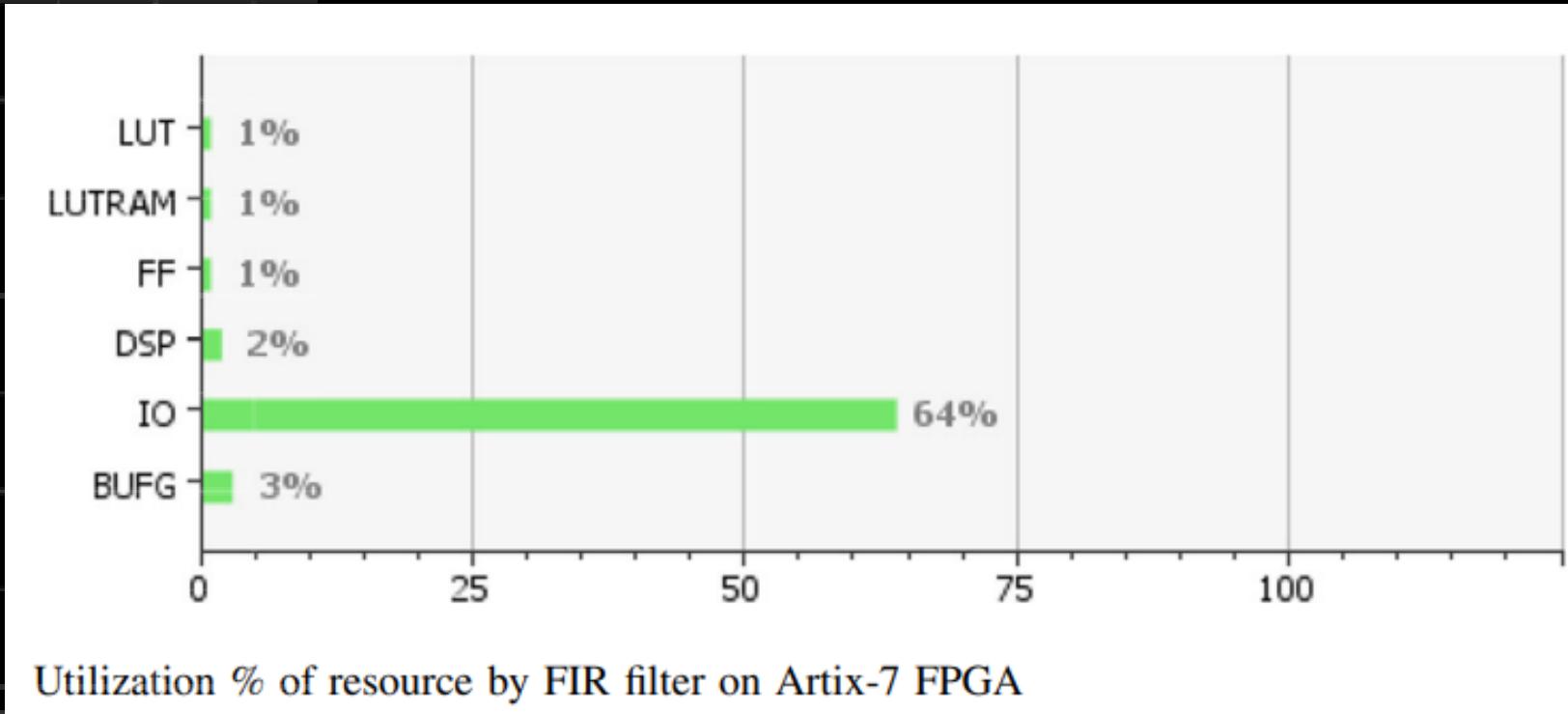


PERFORMANCE ANALYSIS OF C CODE OF COMMUNICATION SPECIFIC FIR FILTER ON 3 DIFFERENT FPGA FAMILIES AND I SOC

- Performance Analysis of Communication Specific FIR Filter on Artix-7 FPGA

Table 4 Resource utilization by FIR filter on Artix-7 FPGA

Artix-7	BRAM_18 K	DSP48E	FF	LUT
Available	210	180	94,400	47,200
Utilization	0	4	246	161



Resource	Utilization	Available	Utilization %
LUT	193	47,200	0.41
LUTRAM	32	19,000	0.17
FF	102	94,400	0.11
DSP	3	180	1.67
IO	108	170	63.53
BUFG	1	32	3.13



- Performance Analysis of Communication Specific FIR Filter on Zynq 7000 All Programmable SOC

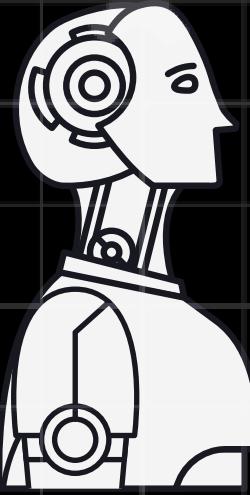
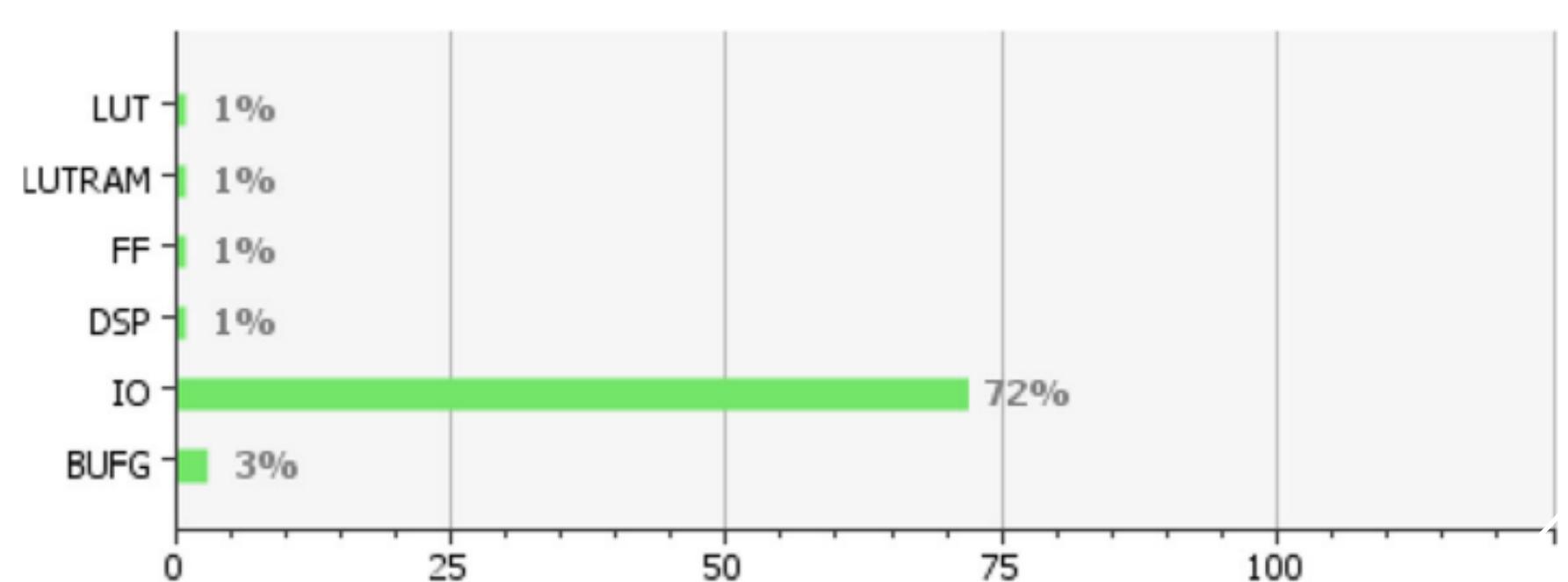


Table 6 Resource utilization by FIR filter on Zynq 7000 all programmable SOC

Zynq	BRAM_18K	DSP48E	FF	LUT
Available	530	400	157,200	78,600
Utilization	0	4	243	159

Resource	Utilization	Available	Utilization %
LUT	193	78,600	0.25
LUTRAM	32	26,600	0.12
FF	102	157,200	0.06
DSP	3	400	0.75
IO	108	150	72.00
BUFG	1	32	3.13



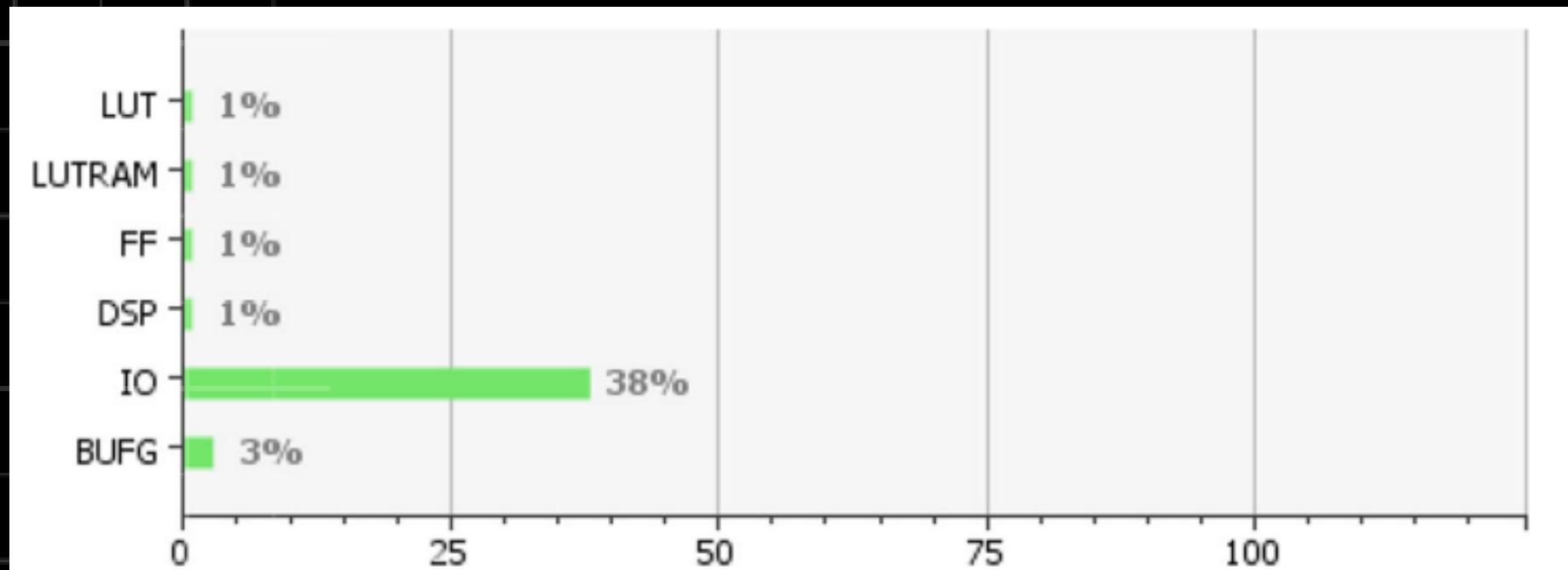


- Performance Analysis of Communication Specific FIR Filter on Kintex-7 FPGA



Table 8 Resource utilization by FIR filter on Kintex-7 FPGA

Kintex-7	BRAM_18 K	DSP48E	FF	LUT
Available	650	600	202,800	101,400
Utilization	0	4	180	159



Resource	Utilization	Available	Utilization %
LUT	193	101,400	0.19
LUTRAM	32	35,000	0.09
FF	102	202,800	0.05
DSP	3	600	0.50
IO	108	285	37.89
BUFG	1	32	3.13



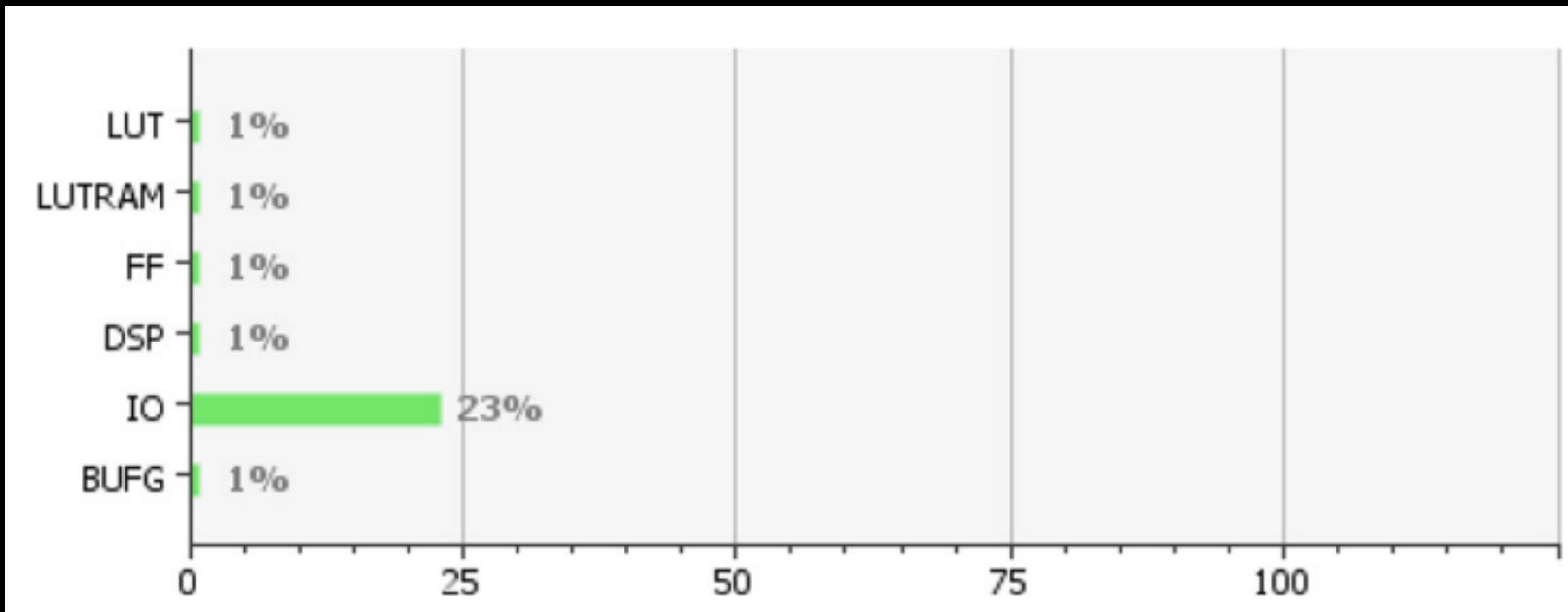


- Performance Analysis of Communication Specific FIR Filter on Kintex Ultrascale FPGA

Table 10 Resource utilization by FIR filter on Kintex ultrascale FPGA

Kintex ultrascale	BRAM_18K	DSP48E	FF	LUT
Available	1080	1700	406,256	203,128
Utilization	0	4	241	156

Resource	Utilization	Available	Utilization %
LUT	177	203,128	0.09
LUTRAM	16	112,800	0.01
FF	102	406,256	0.03
DSP	3	1700	0.18
IO	108	468	23.08
BUFG	1	560	0.18

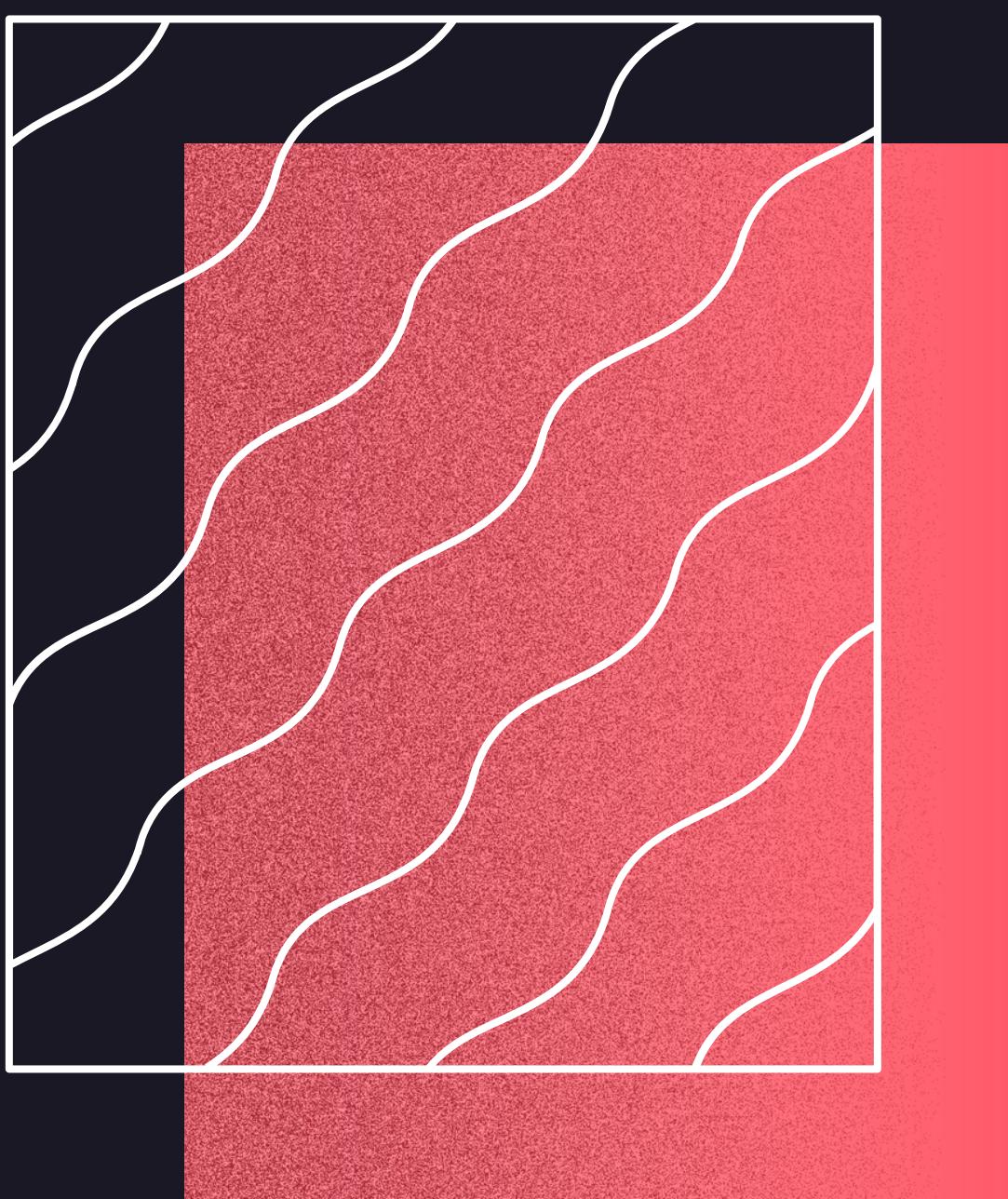




ANALYSIS OF DELAY, LATENCY AND INTERVAL OF 3 FPGA AND 1 SOC

Table 12 Comparison of delay, latency and interval of 3 FPGA and 1 SOC

FPGA	Worst case delay	Latency	Interval
Artix-7	8.11	111	112
Zynq	8.48	78	79
Kintex-7	8.43	78	79
Kintex ultrascale	8.27	56	57



FUTURE SCOPE

- In future, we can use 16 nm process technology based FPGA for implementation of communication specific design
- In future, we can apply various energy efficient techniques like capacitance scaling, thermal scaling, voltage scaling, and use energy efficient IO standards in order to develop the most energy efficient design

Conclusion

WE CONCLUDE THAT ZYNQ 7000 ALL PROGRAMMABLE SOC IS POWER HUNGRY ARCHITECTURE AND KINTEX ULTRASCALE ARCHITECTURE IS THE MOST ENERGY EFFICIENT ARCHITECTURE. ULTRASCALE FPGA IS ALSO IDEAL FOR PACKET PROCESSING IN 100G NETWORKING AND HETEROGENEOUS WIRELESS INFRASTRUCTURE. THEREFORE, WE CONCLUDE THAT ULTRA SCALE FPGA IS THE BEST ARCHITECTURE FOR ENERGY EFFICIENT IMPLEMENTATION OF ANY COMMUNICATION DESIGN ON FPGA. THERE IS 47.74% REDUCTION IN LATENCY WHEN WE MIGRATE OUR DESIGN FROM 28 NM PROCESS TECHNOLOGY BASED SEVEN SERIES ARCHITECTURE TO 20 NM PROCESS TECHNOLOGY BASED ULTRASCALE ARCHITECTURE. /

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- REZAEE, A. (2015). USING COEVOLUTIONARY GENETIC ALGORITHMS FOR ESTIMATION OF BLIND FIR CHANNEL. WIRELESS PERSONAL COMMUNICATIONS, 83(1), 191–201.
- KANNAN, G., GARG, M., MERCHANT, S. N., ET AL. (2008). MPOE BASED PREFILTERING AND MRT BEAMFORMING WITH MATCHED FILTER RECEIVER FOR DS-CDMA SYSTEMS.
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