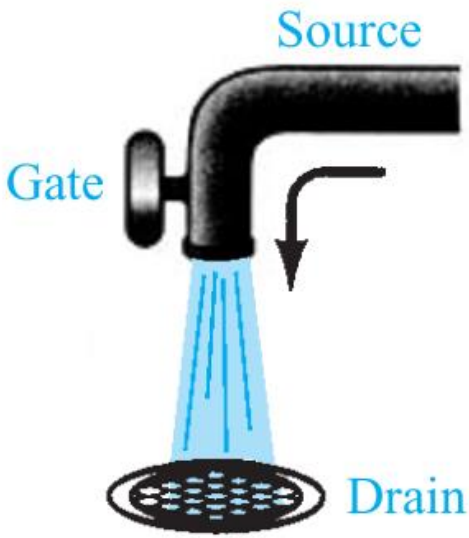
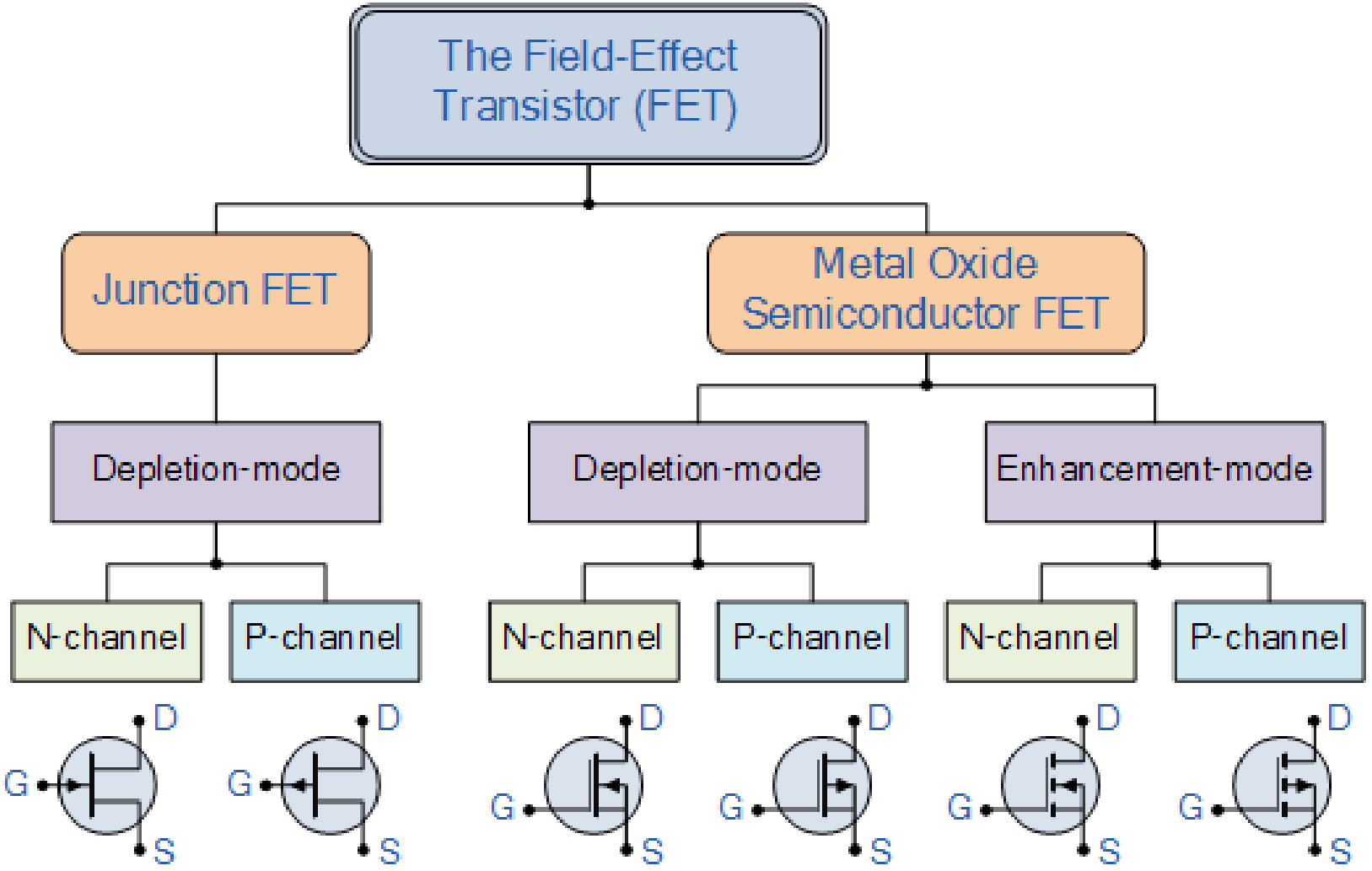
CO2015

Field Effect Transistor

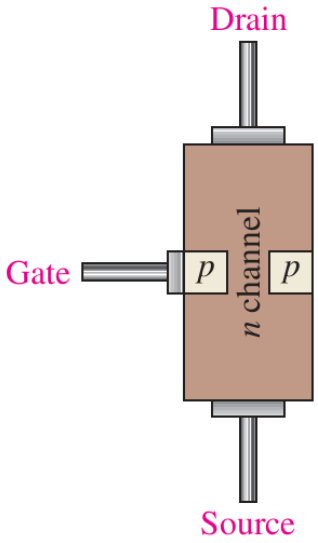


DCE
Dept. of Computer Engineering

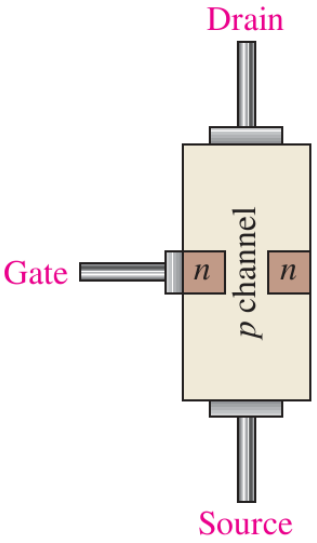
Field-Effect Transistor (FET)



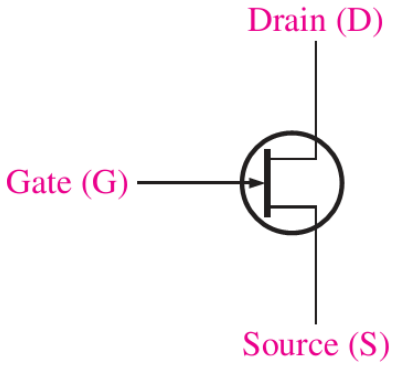
JFET



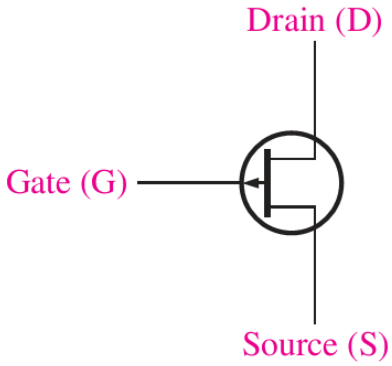
(a) *n* channel



(b) *p* channel



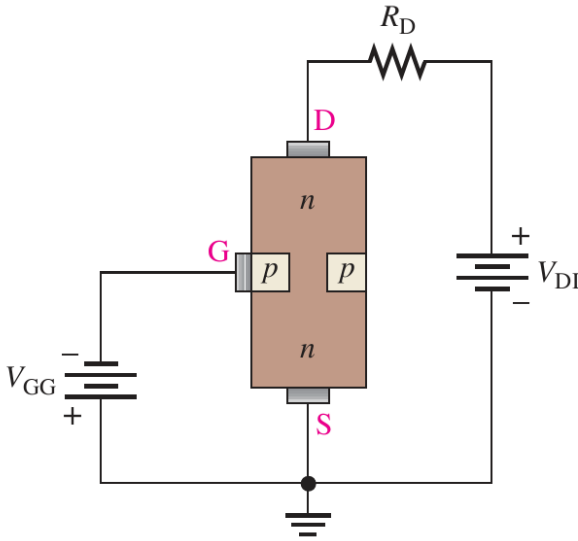
n channel



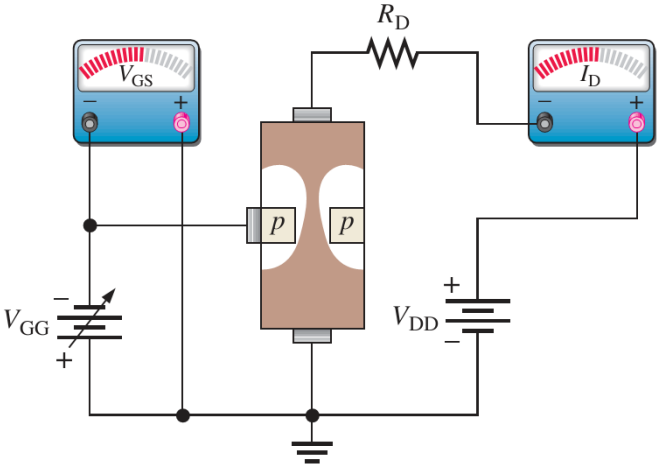
p channel

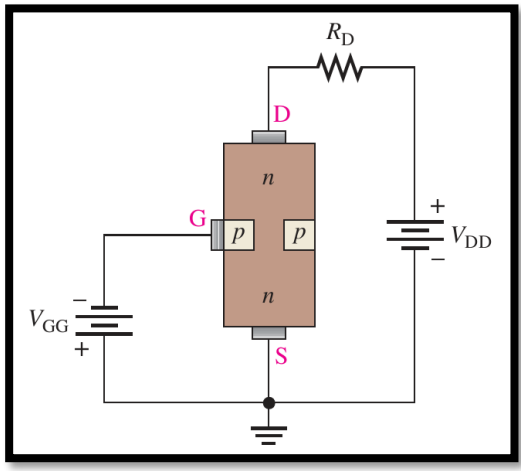
JFET Operations

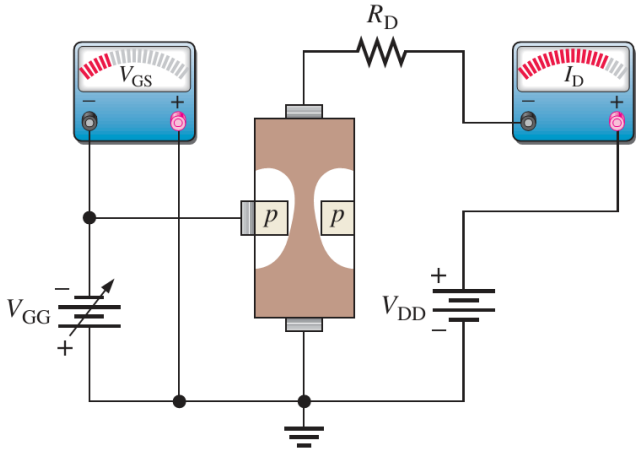
- G and S always in reversed-bias:
  - V_{GS} is negative: Depletion area is increased → Resistance between D and S is increased
  - V_{GS} is increased (to Zero): Depletion area is decreased → Resistance between D and S is decreased
- G and S is in forward-bias:
  - JFET likes a **resistor**

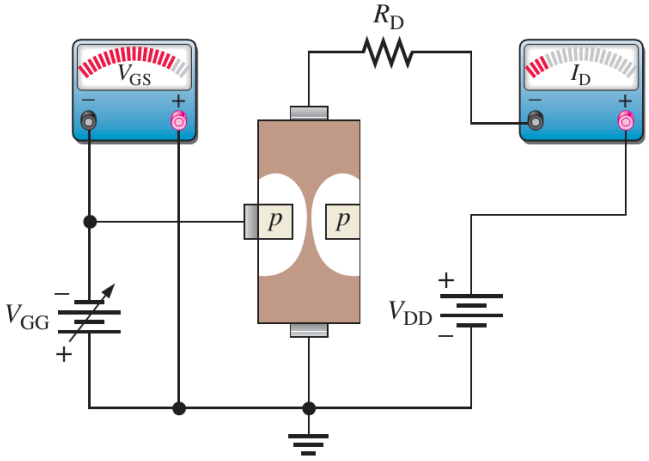


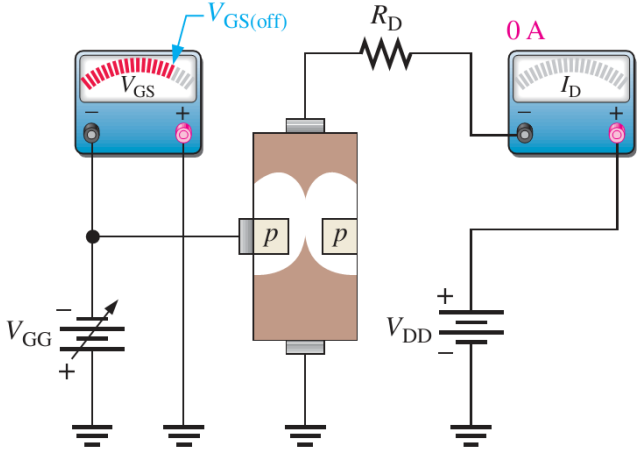
JFET Operations











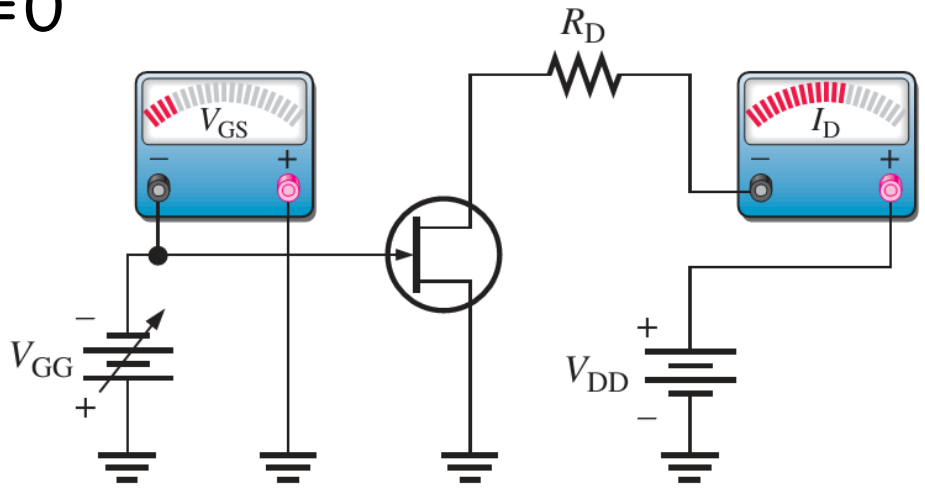
JFET Characteristics

- JFET n-channel has three operation modes when $V_{DS} > 0$

A. $V_{GS} = 0$, JFET is in saturation, I_D=Max

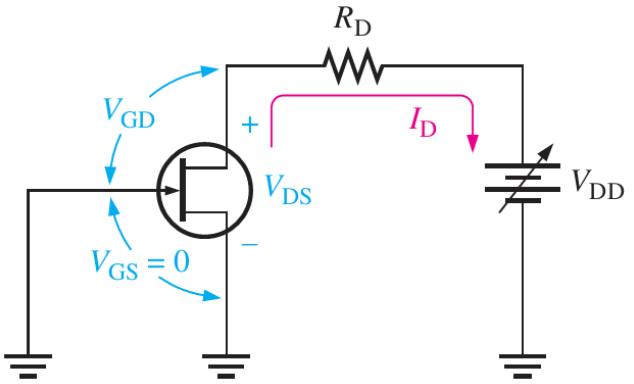
B. $V_{GS} < 0$, JFET is in linear status, $I_D \downarrow$

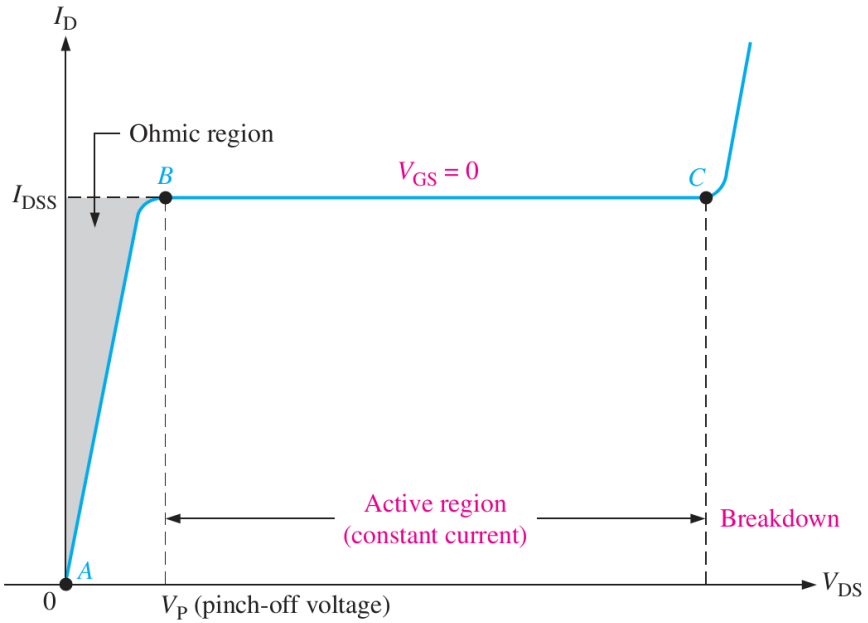
C. $V_{GS} = -V_{off}$, JFET is OFF, $I_D = 0$

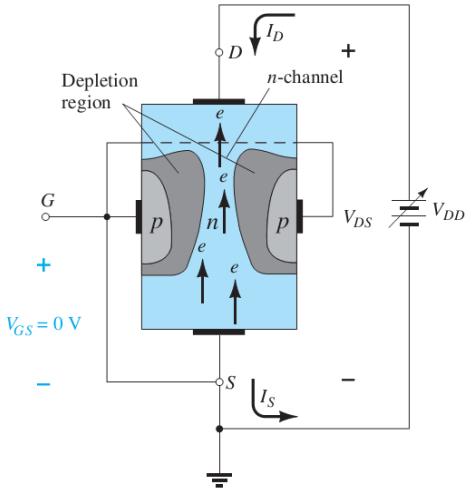


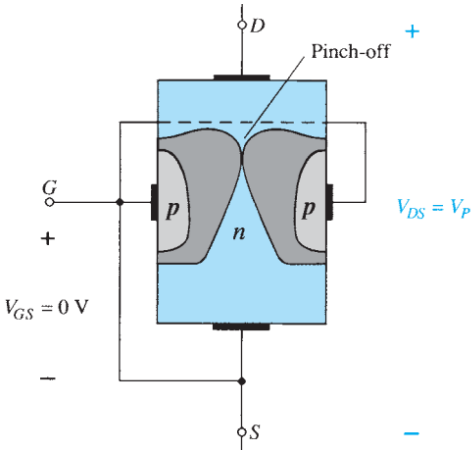
JFET Saturation Mode

- V_{GS} = 0V, V_{DD} is increased slowly
  - **Linear region** A-B: $V_{DS} = RI_D$
  - **Saturation region** B-C: I_D is constant
  - **Pinch off region** due to the increase of depletion area.

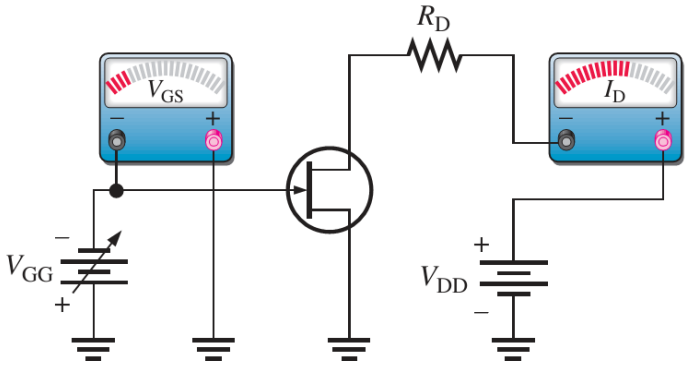


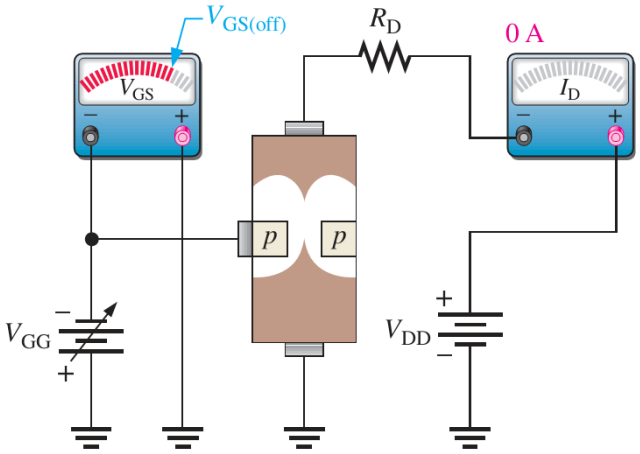


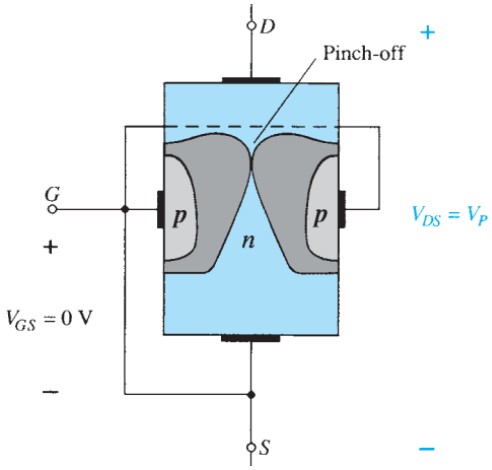




Cut-off State

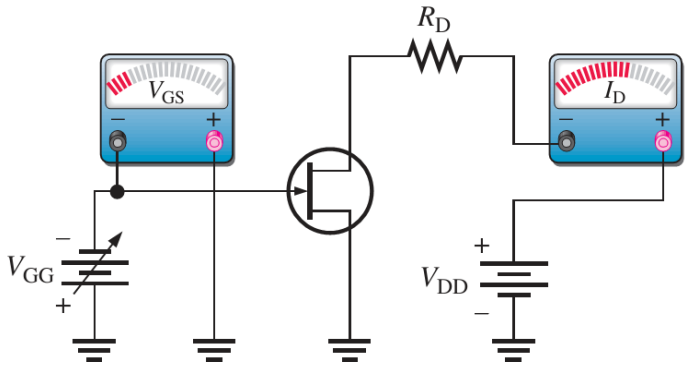


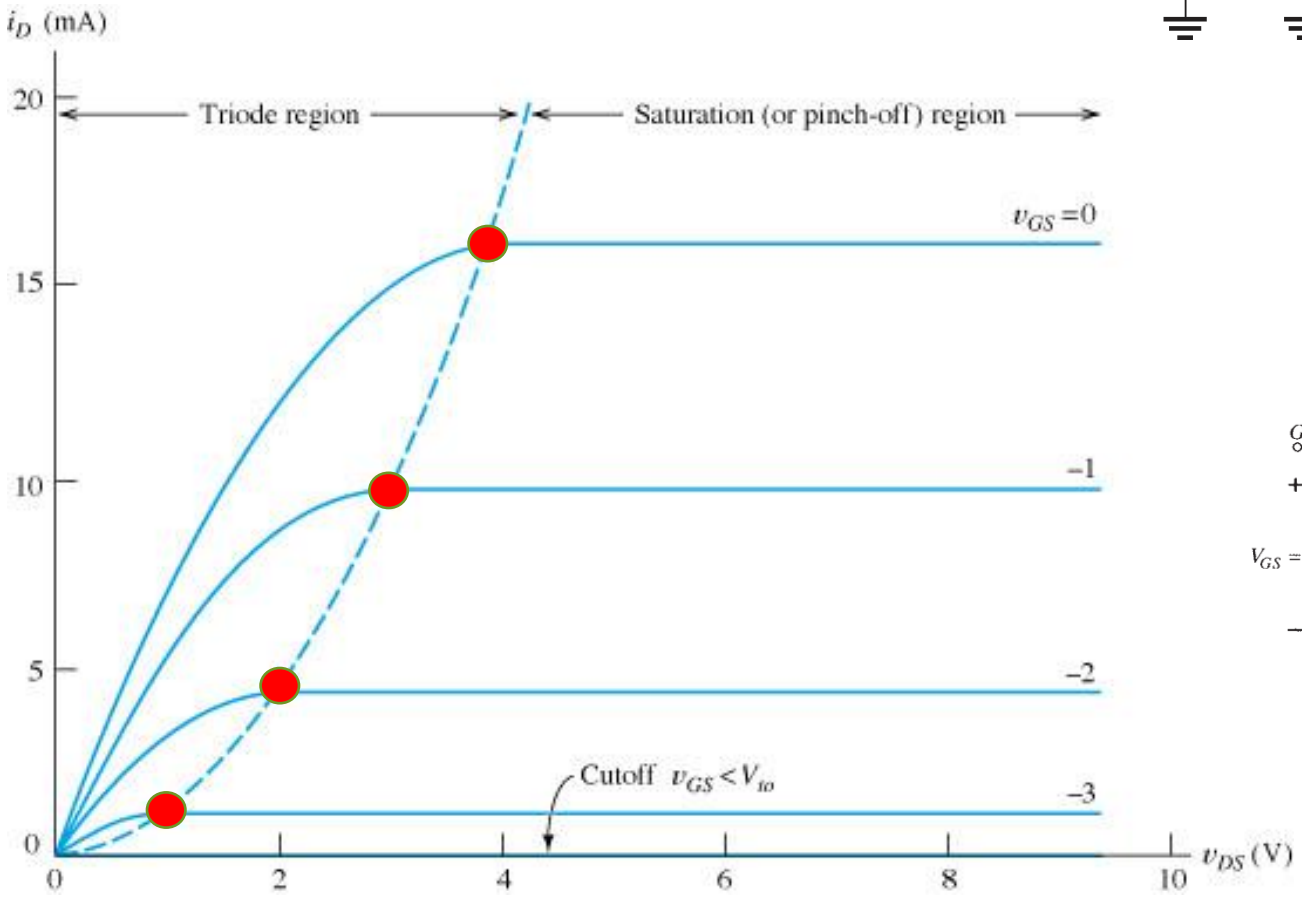


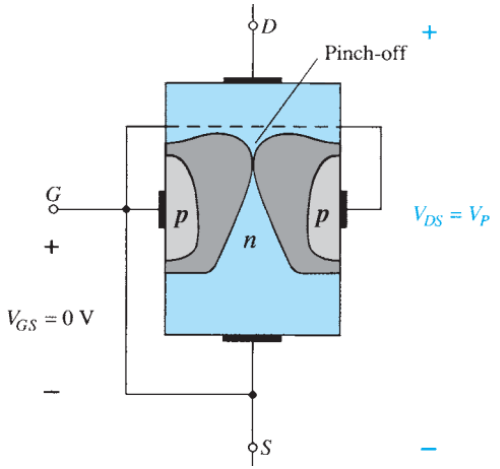


- Reversed-bias: $0 < V_{GS} < V_{GS(off)}$
  - Depletion area is increased → closer to Pinch-off state

JFET Characteristic



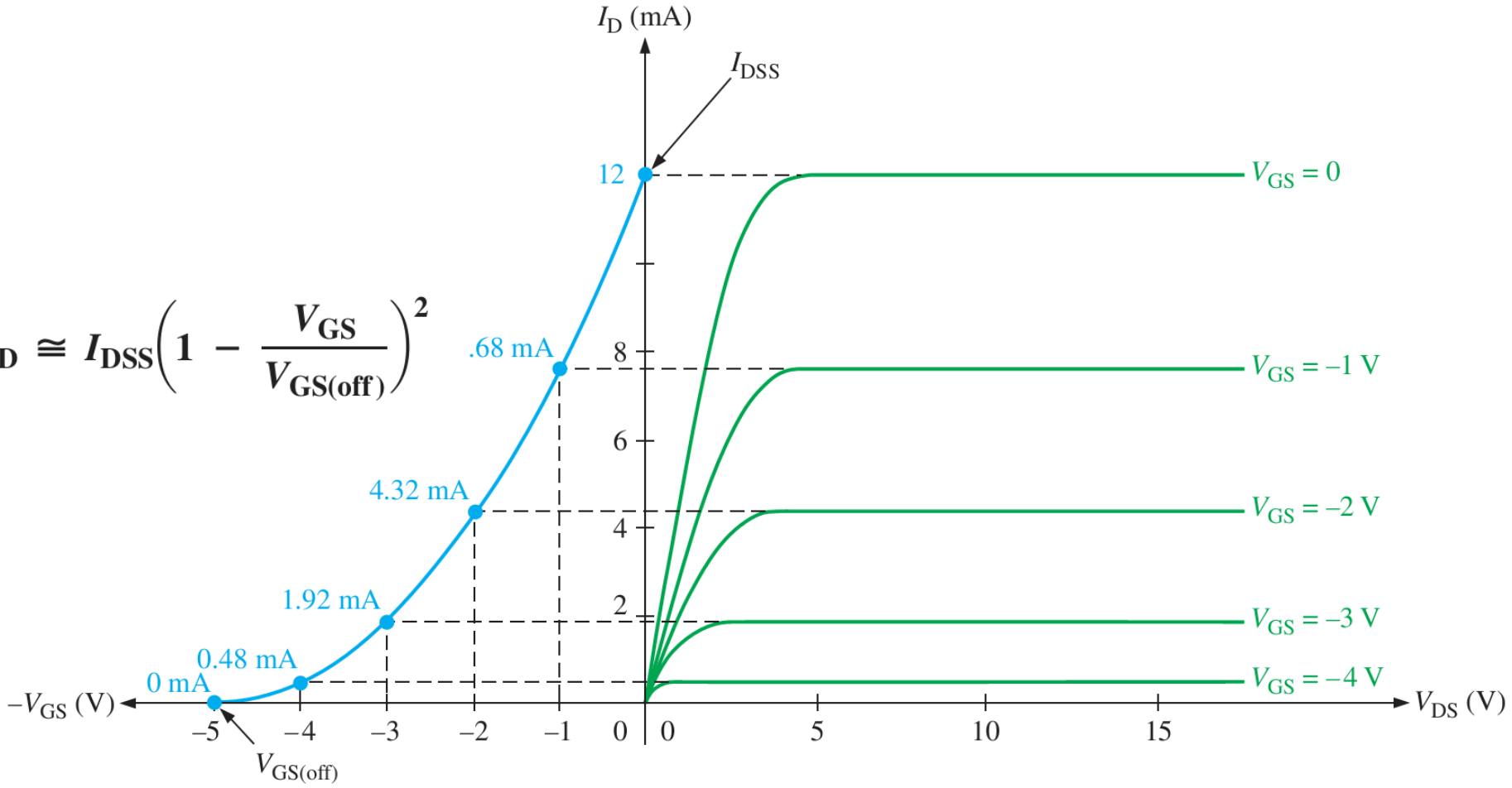




JFET Transfer Curve

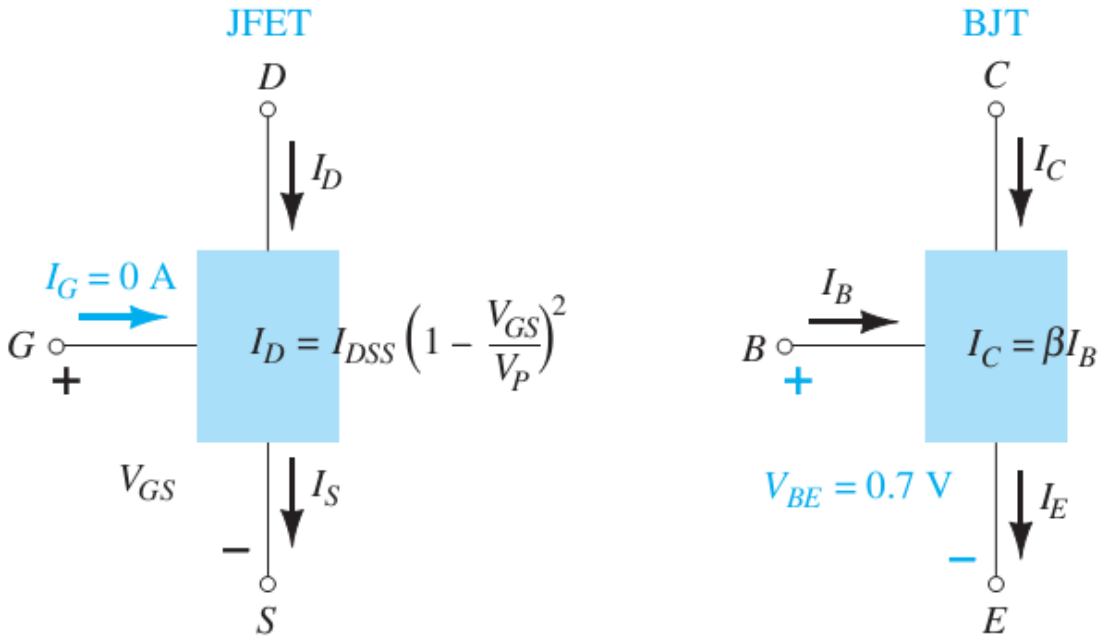
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$



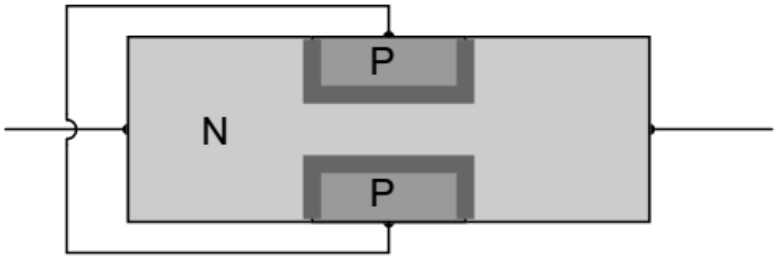
JFET vs. BJT

JFET		BJT
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0\ \text{A}$	$\Leftrightarrow$	$V_{BE} \cong 0.7\ \text{V}$

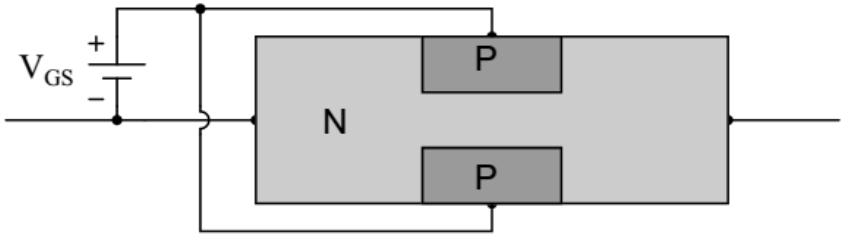


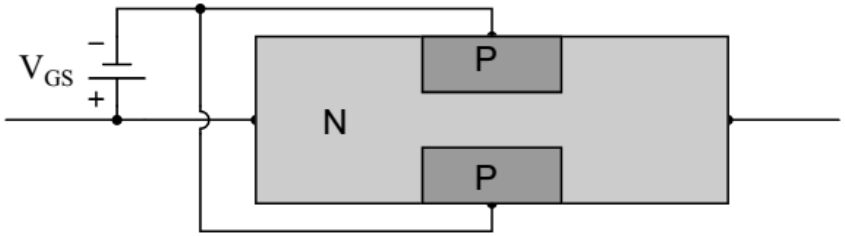
Example

- JFET normal state

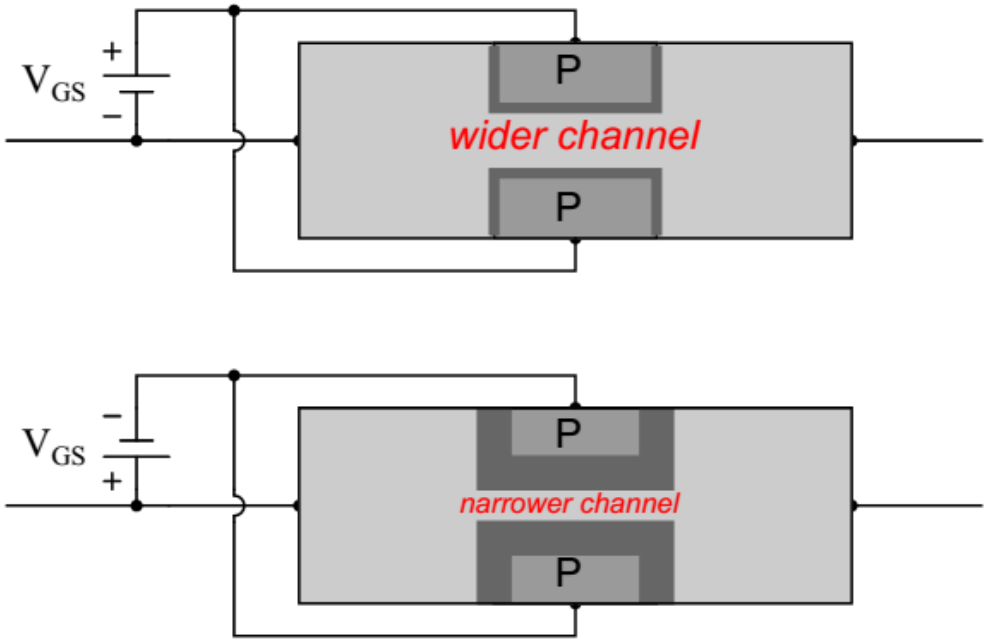


- Determine depletion area in follows:



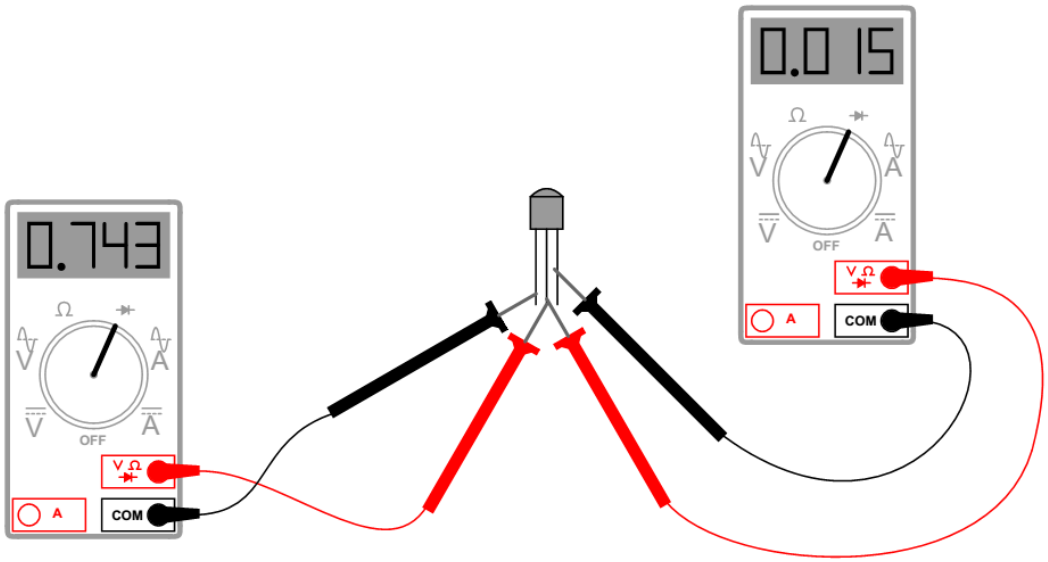


Answer



- First figure: Forward-bias → depletion area is wider
- Second figure: Inverse-bias → depletion area is narrower

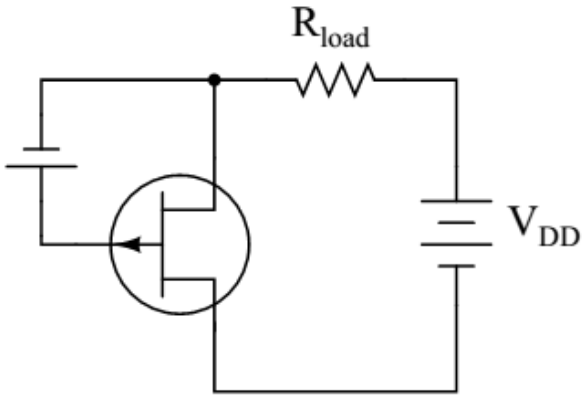
Example

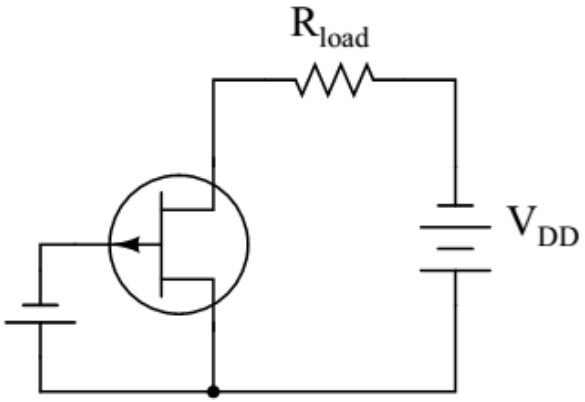


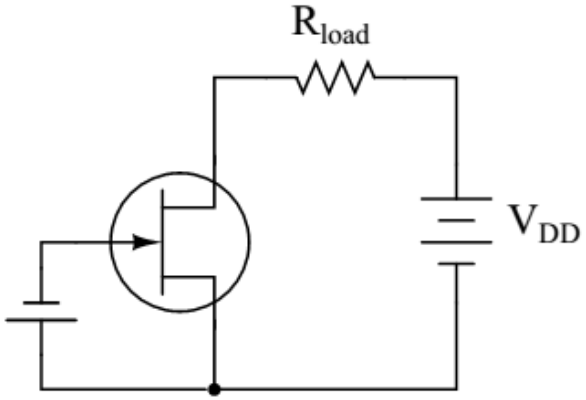
- Determine JFET pins

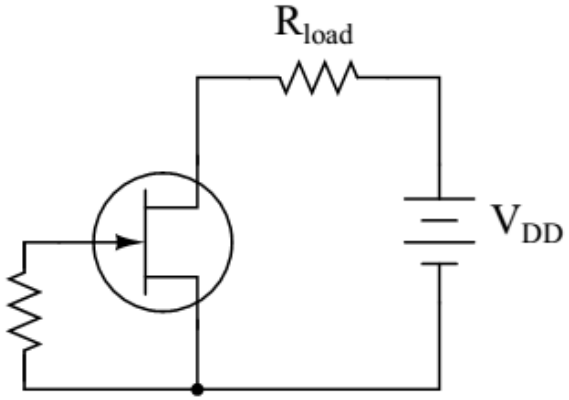
Example

- Determine the correct type (p-channel or n-channel) of the following JFETs and its state (ON or OFF)

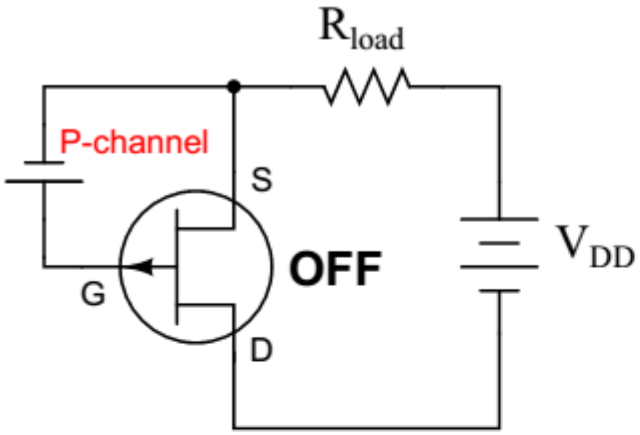


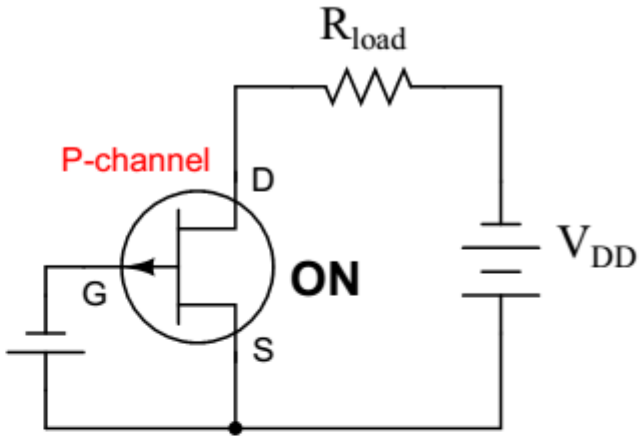


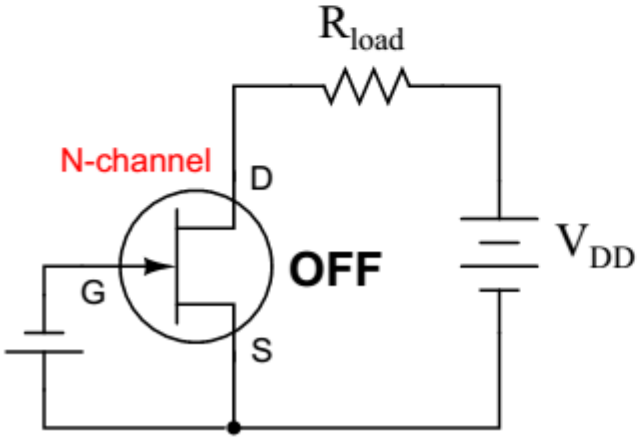


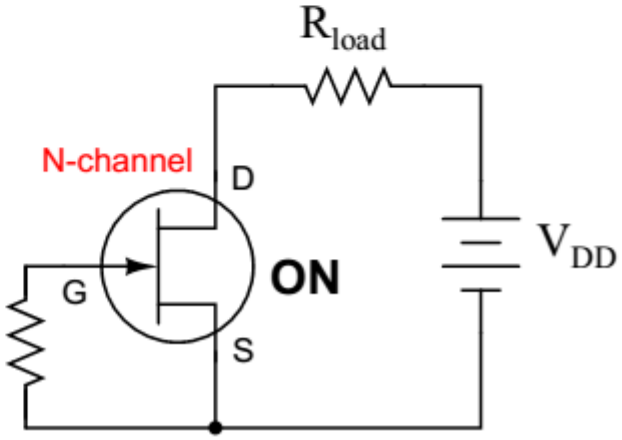


Answer


R_{load}
P-channel
S
G
D
OFF
V_{DD}

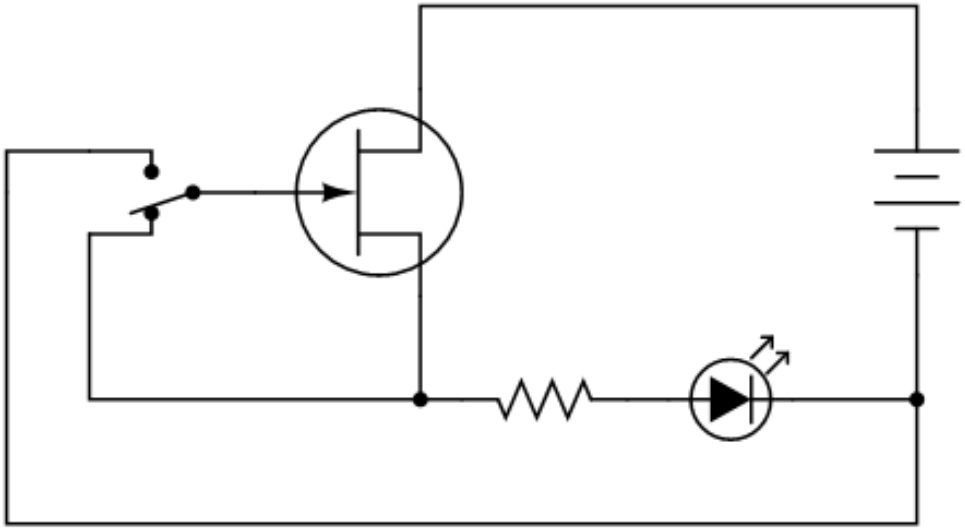

R_{load}
P-channel
D
G
S
ON
V_{DD}


R_{load}
N-channel
D
G
S
OFF
V_{DD}


R_{load}
N-channel
D
G
S
ON
V_{DD}

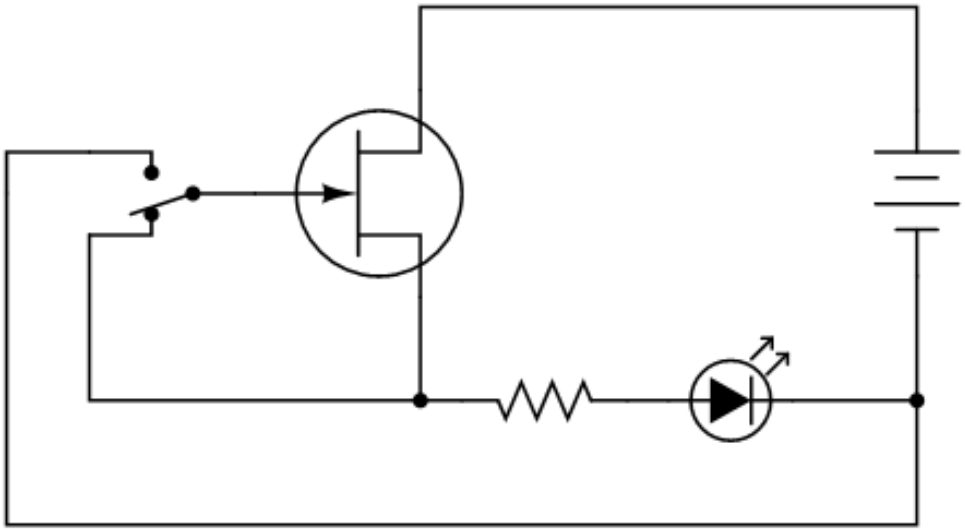
Example

- Determine the LED status (ON or OFF) regarding each position of switch.

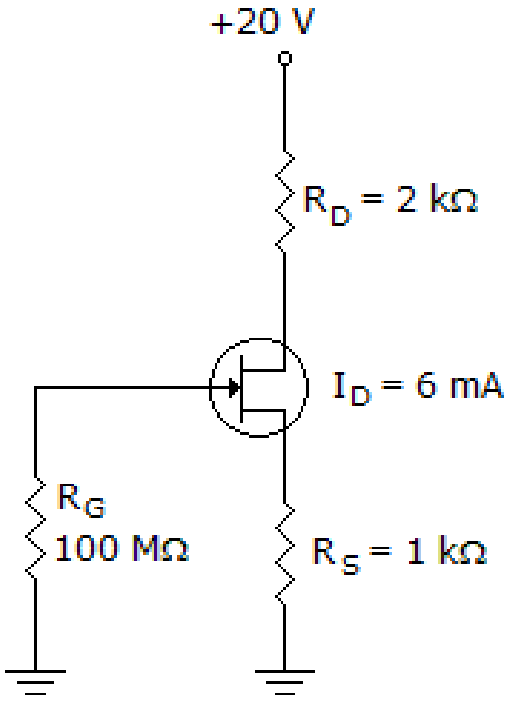


Answer

- ON State: $V_{GS} = 0V$ (Saturation mode)
- Next: OFF state: Inversed-bias with very negative V_{GS}



Example



- Determine V_{DS}
- Determine V_S

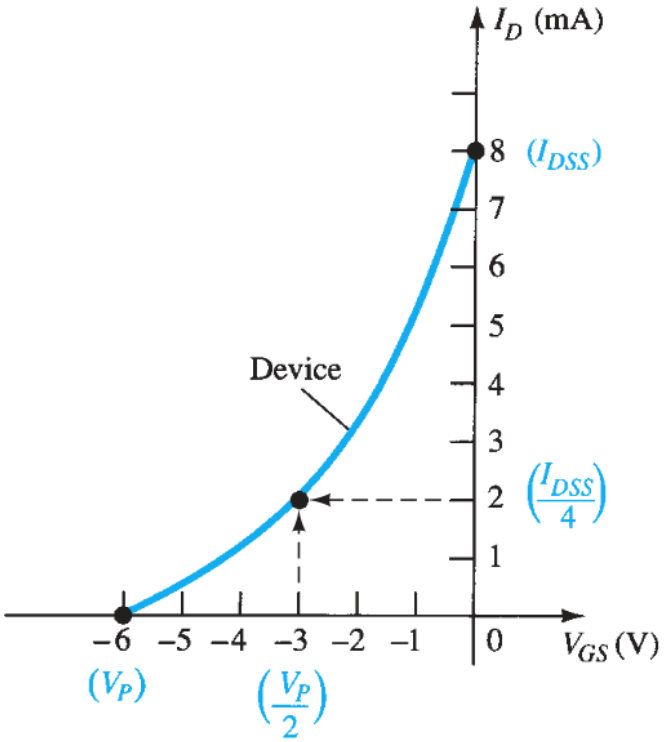
Answer

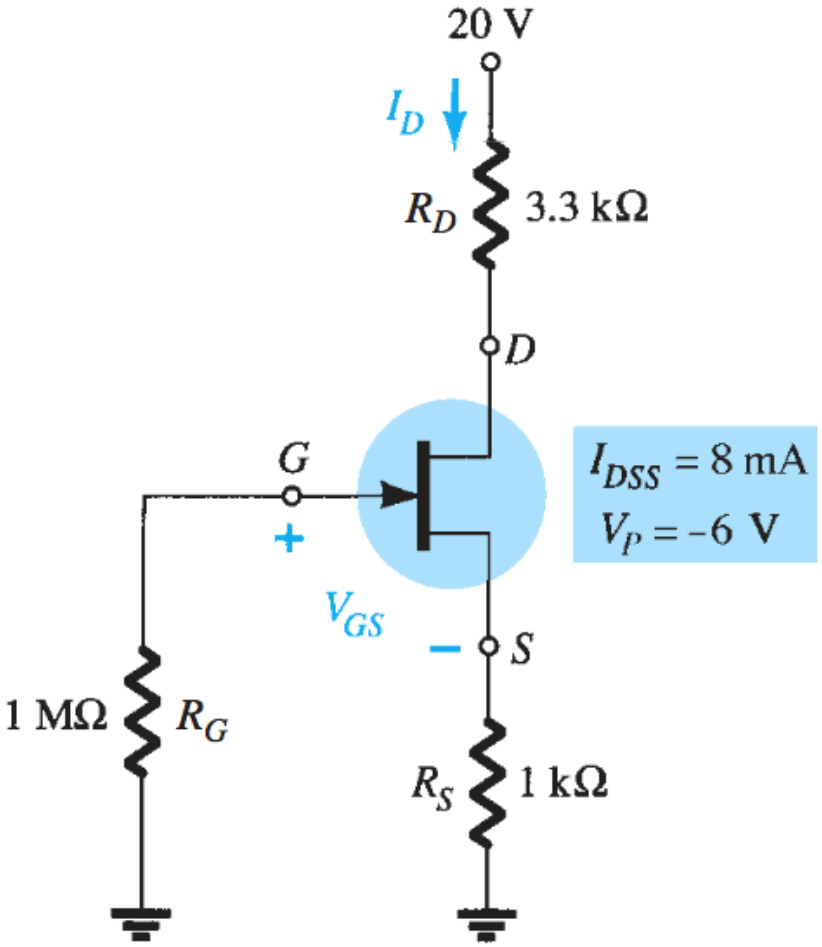
- $V_{DS} = V_{DD} - I_D R_D - I_S R_S$

Exercise

- Determine

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

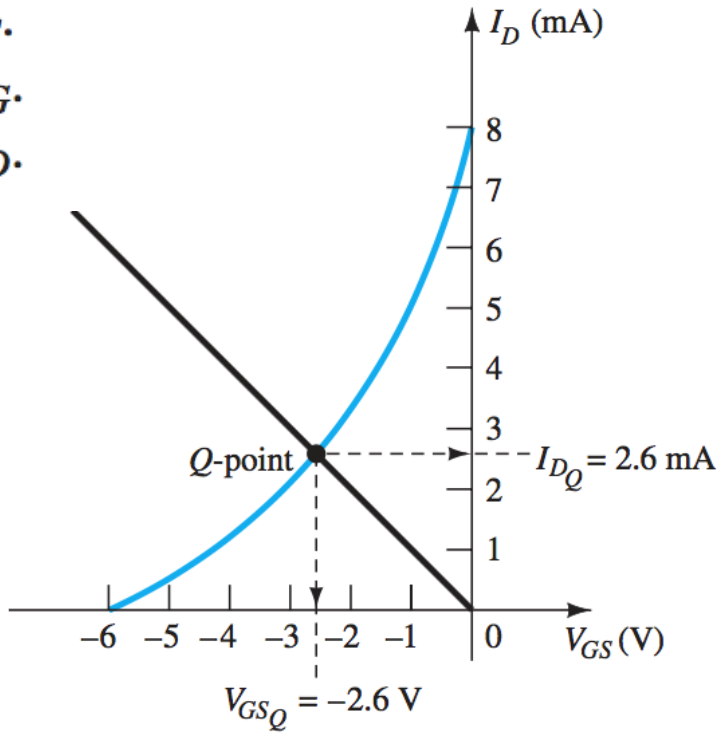


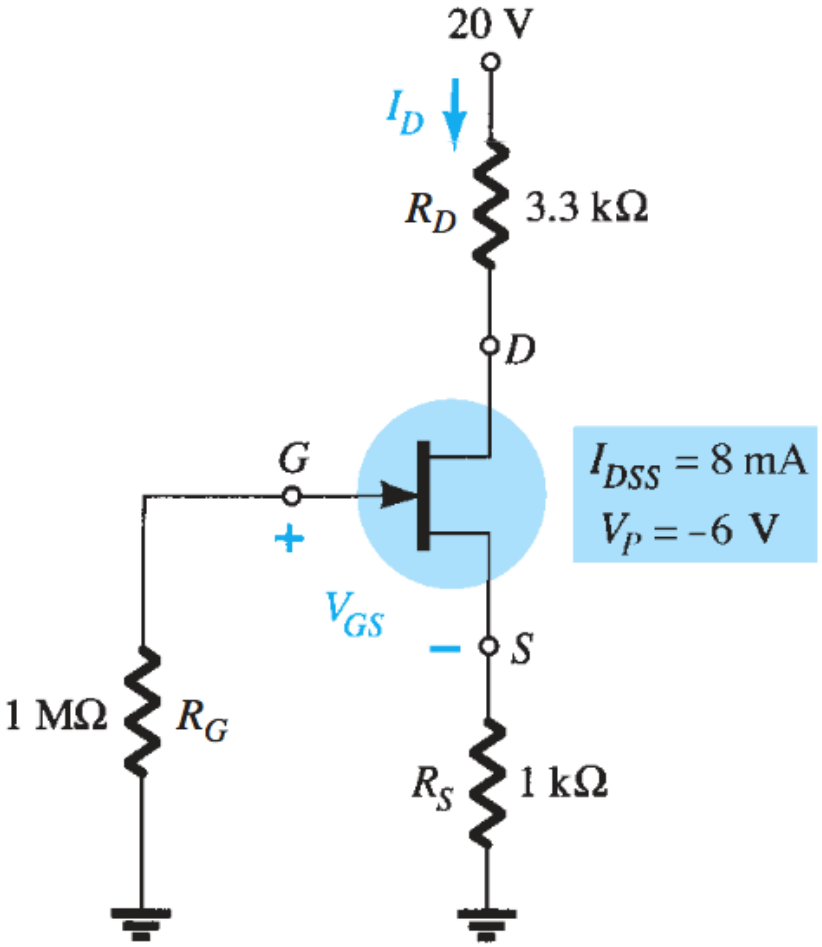


Exercise

- Determine

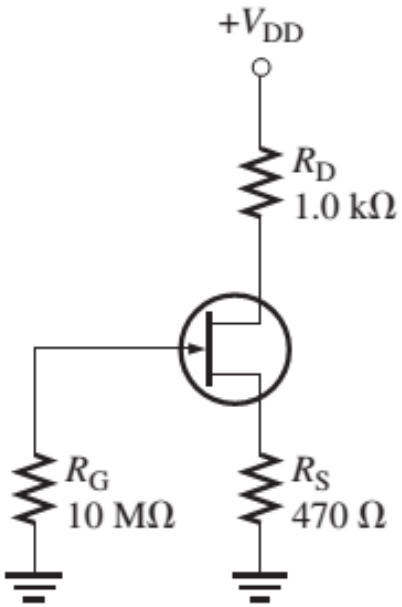
a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

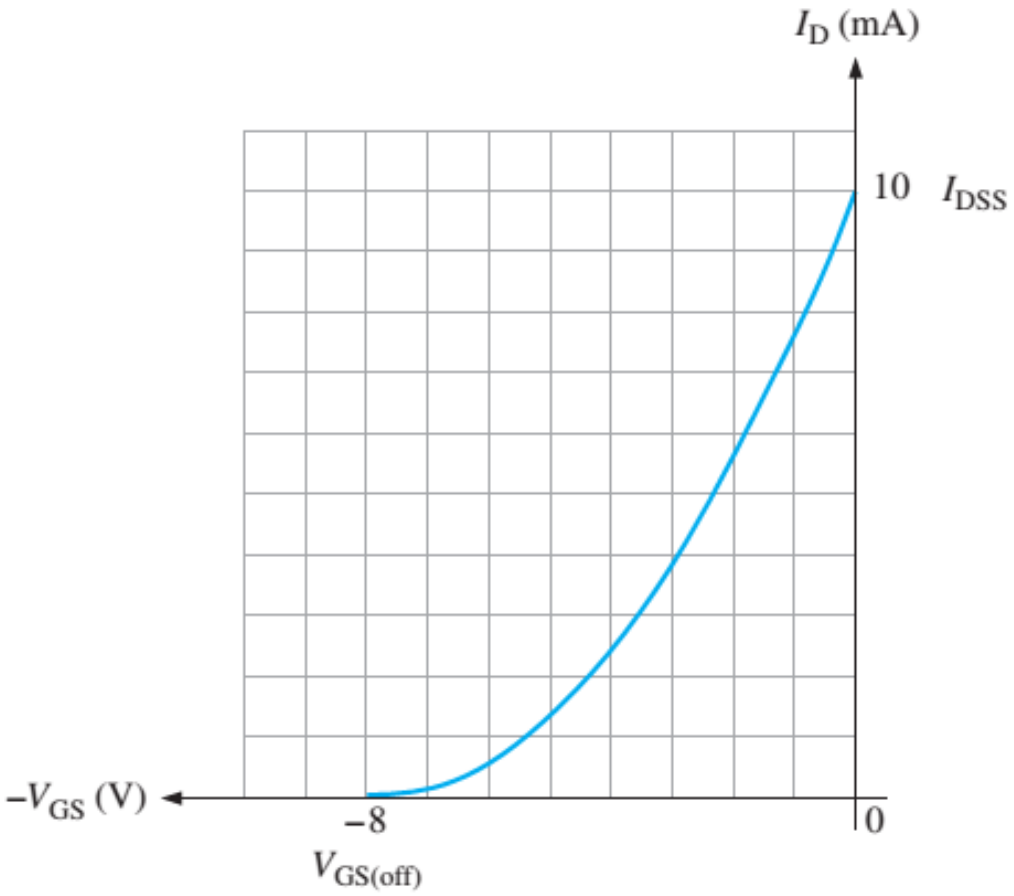




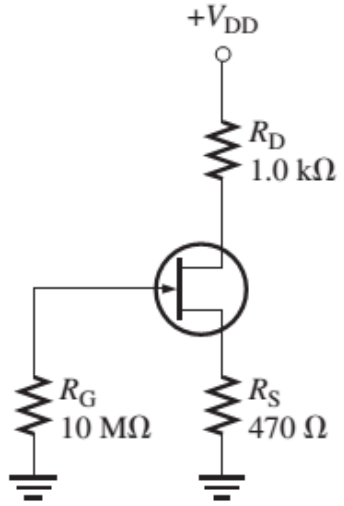
Example

- Determine V_{GS} and I_D





Answer



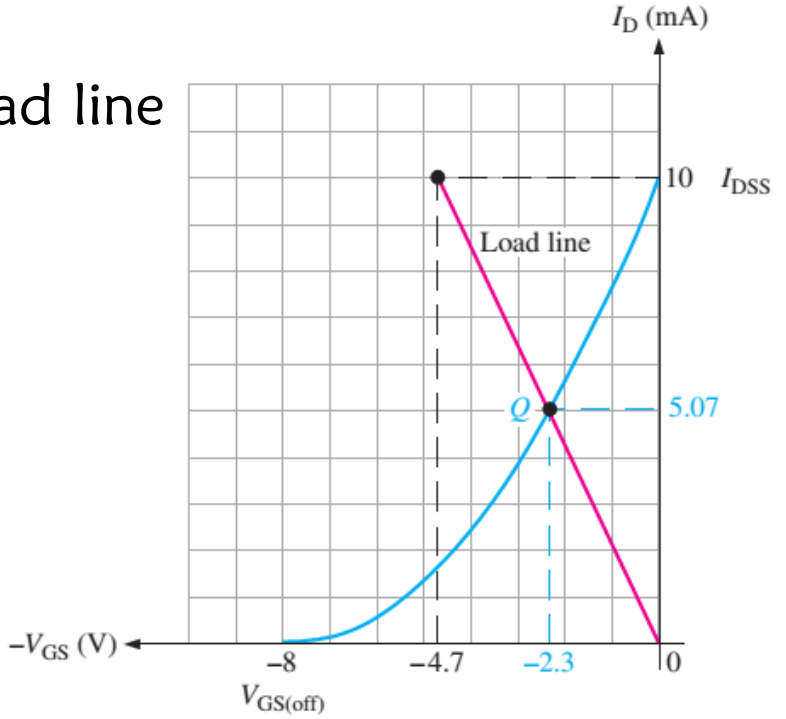
- Determine the Load line
  - $I_D = 0$

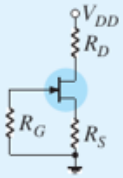
$$V_{GS} = -I_D R_S = (0)(470\ \Omega) = 0\ \text{V}$$

  - $I_D = I_{DSS}$

$$V_{GS} = -I_D R_S = -(10\ \text{mA})(470\ \Omega) = -4.7\ \text{V}$$

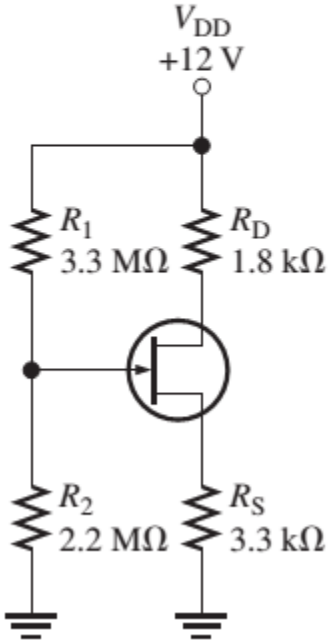
  - Q is the intersection point of the load line & transfer curve.
    - I_D = 5.07 mA
    - V_{GS} = -2.3V

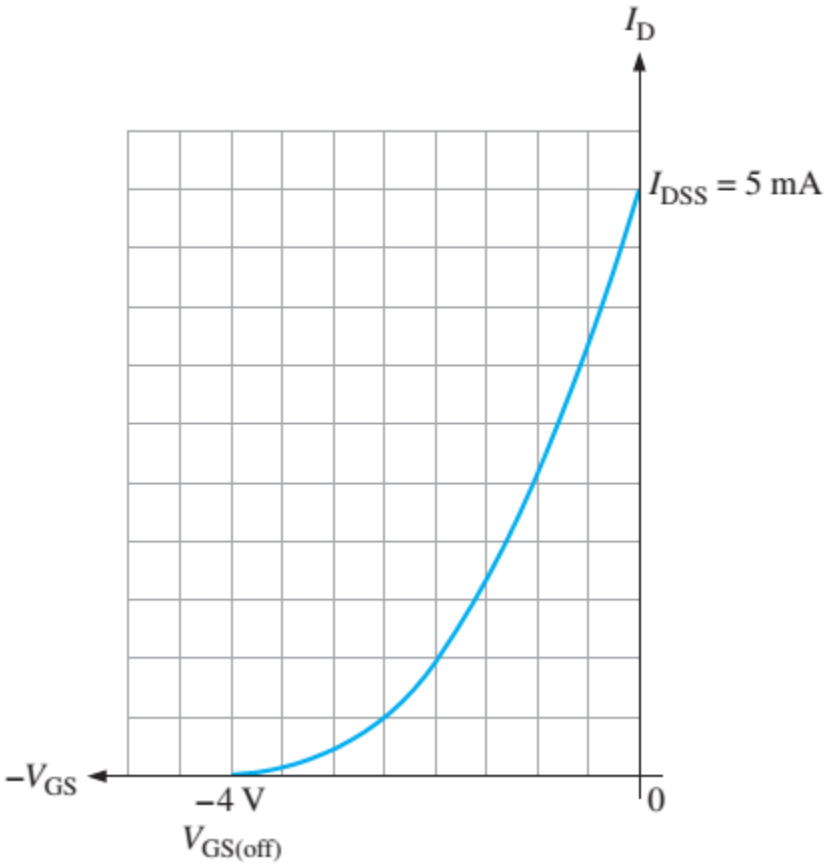


JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$

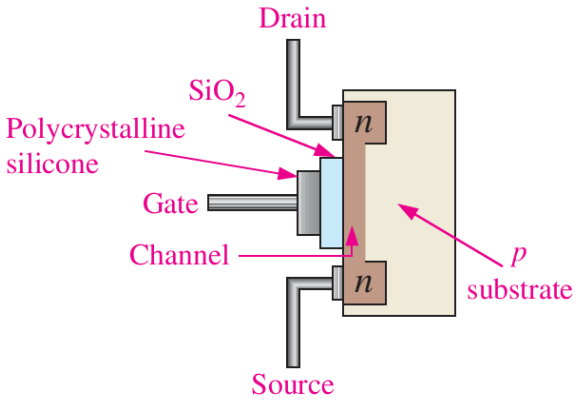
Home Work

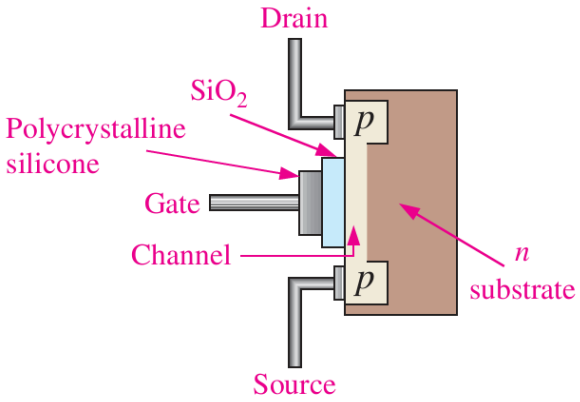
- Determine V_{GS} and V_{DS} for the given JFET, where
  - I_{DSS} = 5mA and $V_{GS(off)}$ = -4V

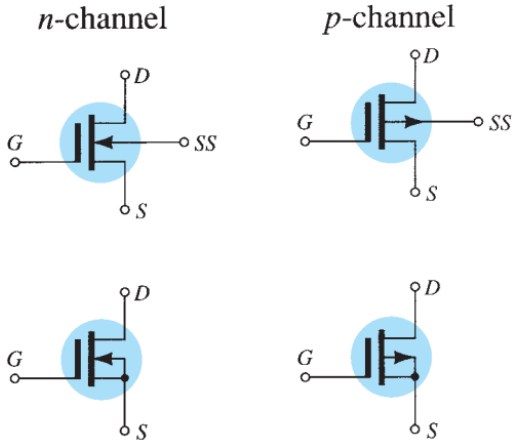


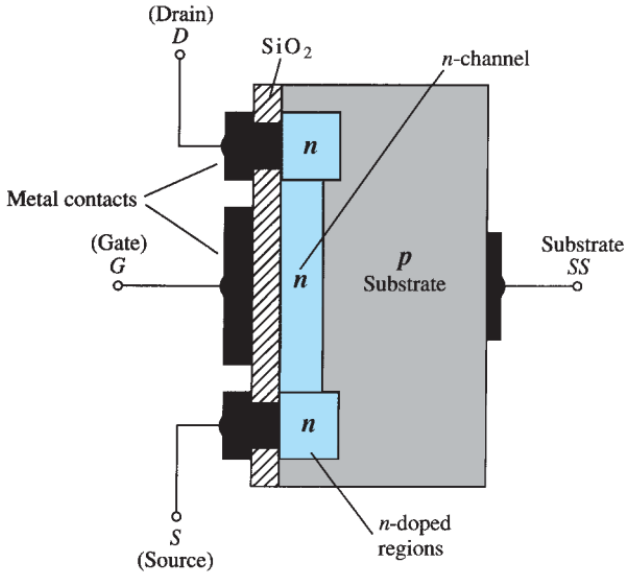


D-MOSFET

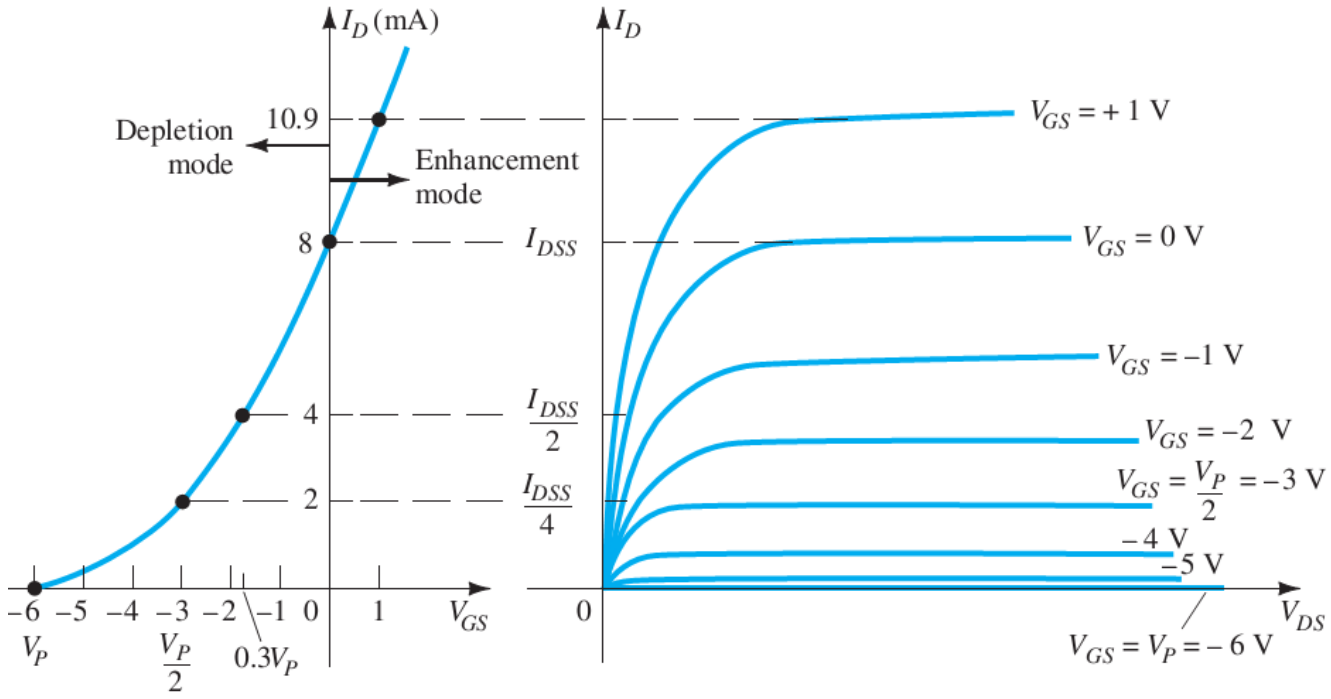

Drain
SiO_2
Polycrystalline silicone
Gate
Channel
n
n
p substrate
Source

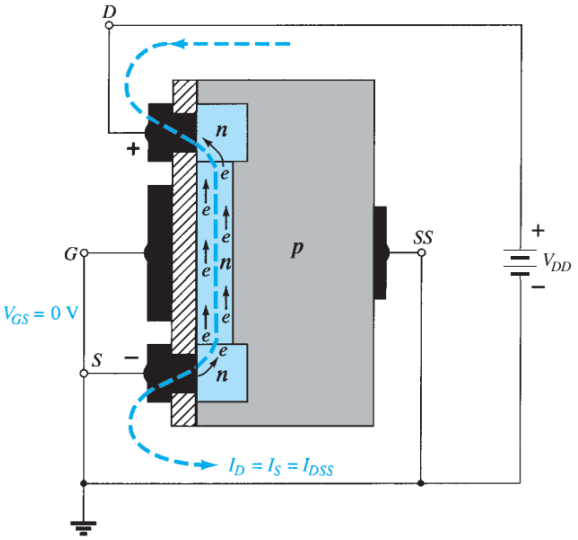

Drain
SiO_2
Polycrystalline silicone
Gate
Channel
p
p
n substrate
Source

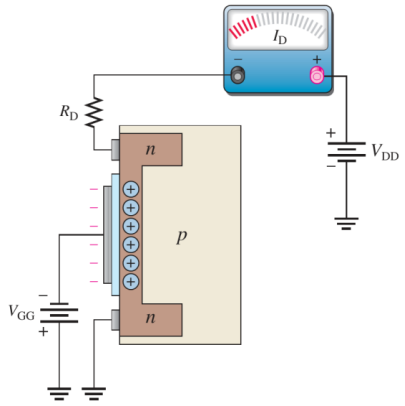

n-channel
p-channel
D
G
SS
S

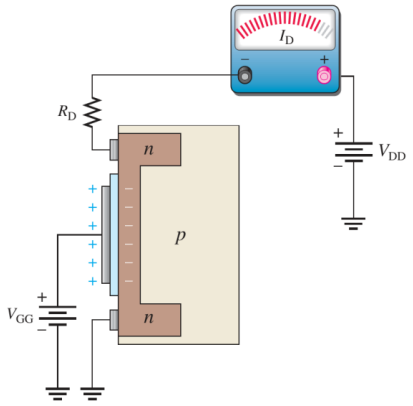

(Drain)
D
SiO_2
n-channel
Metal contacts
(Gate)
G
n
n
p
Substrate
Substrate
SS
n
S
(Source)
n-doped regions

D-MOSFET Operations (N type)



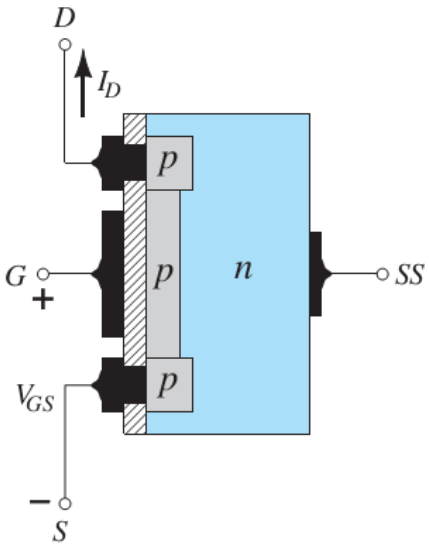


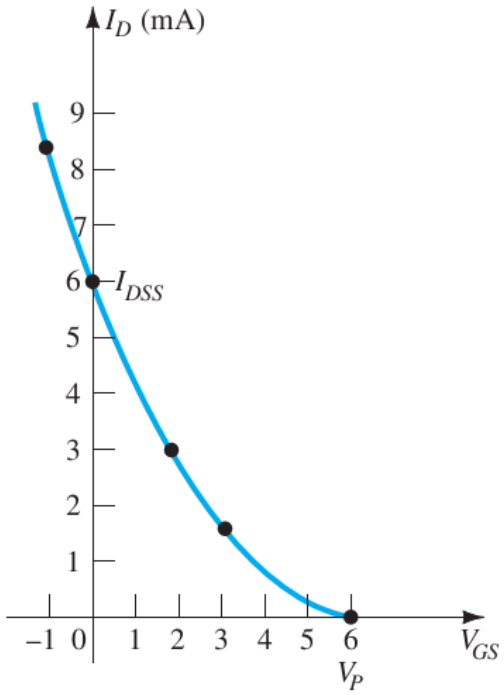


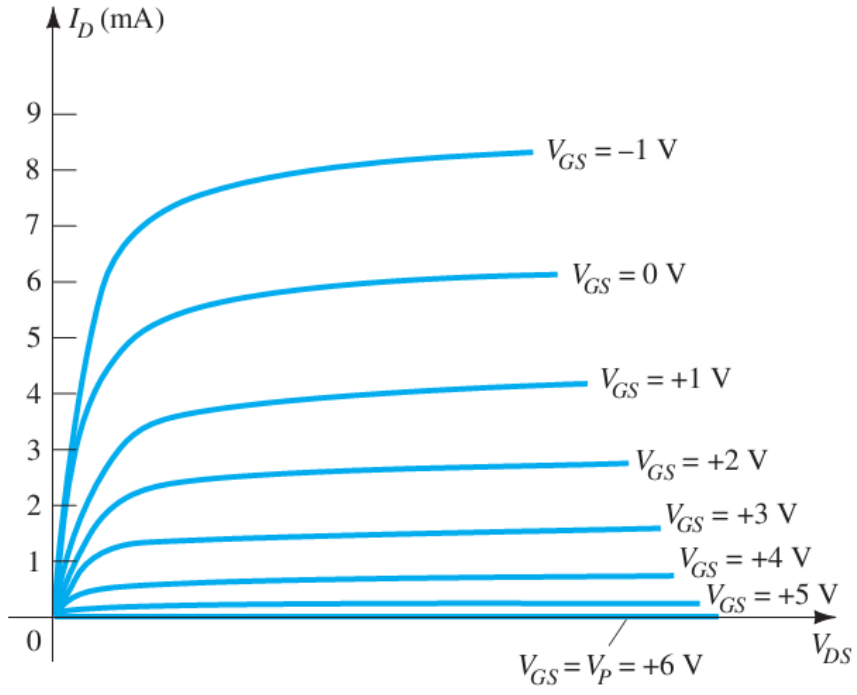


D-MOSFET Operations (P type)

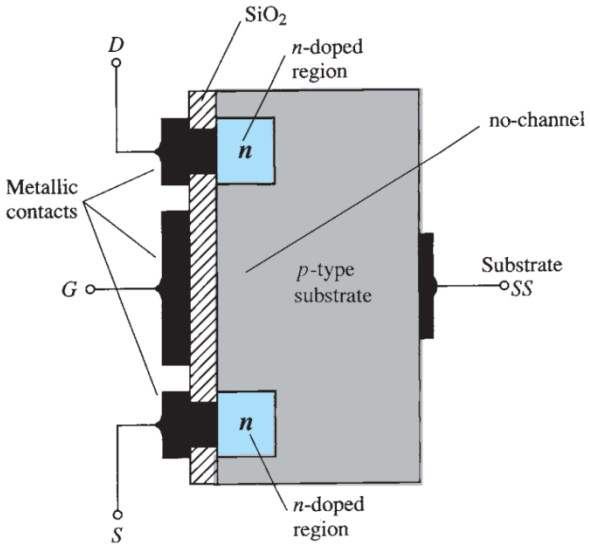
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

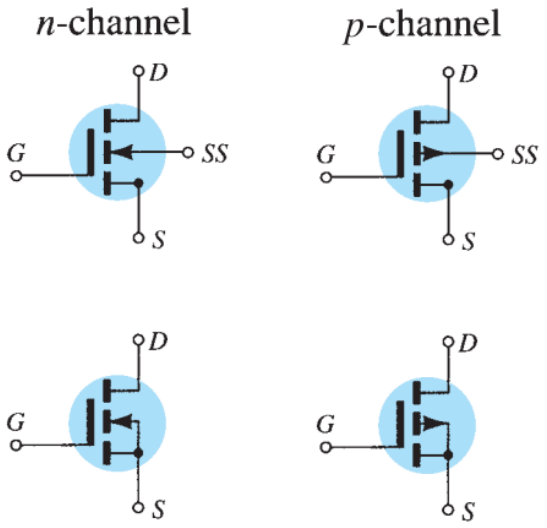


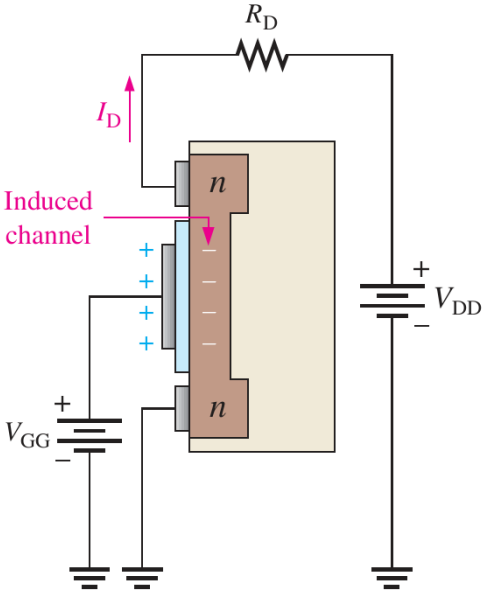


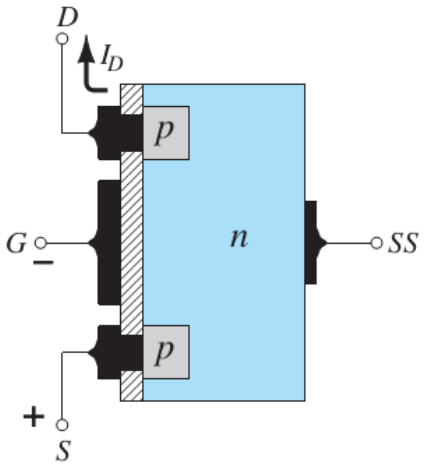


E-MOSFET

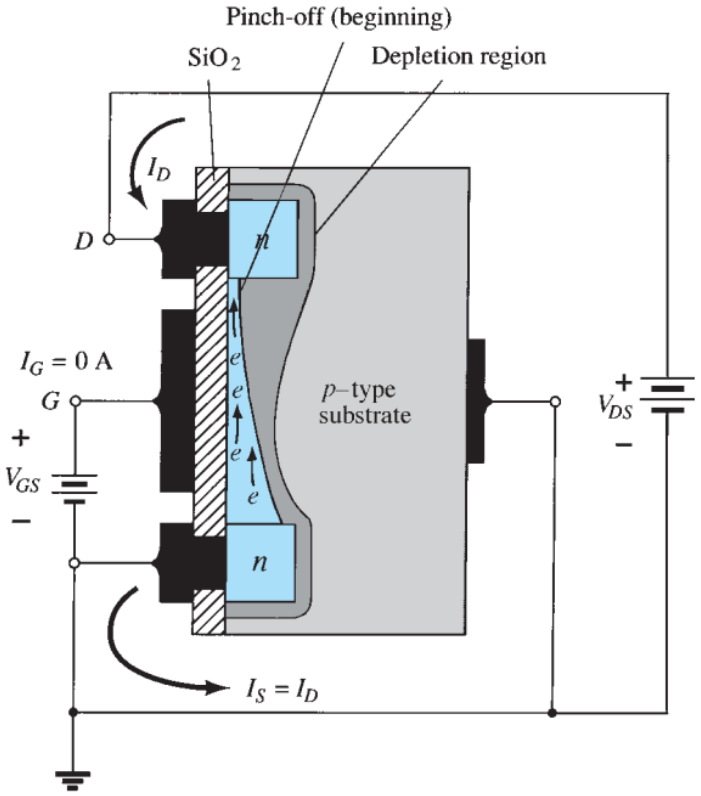

SiO2
D
n-doped region
no-channel
Metallic contacts
G
p-type substrate
Substrate
SS
n
n
S
n-doped region

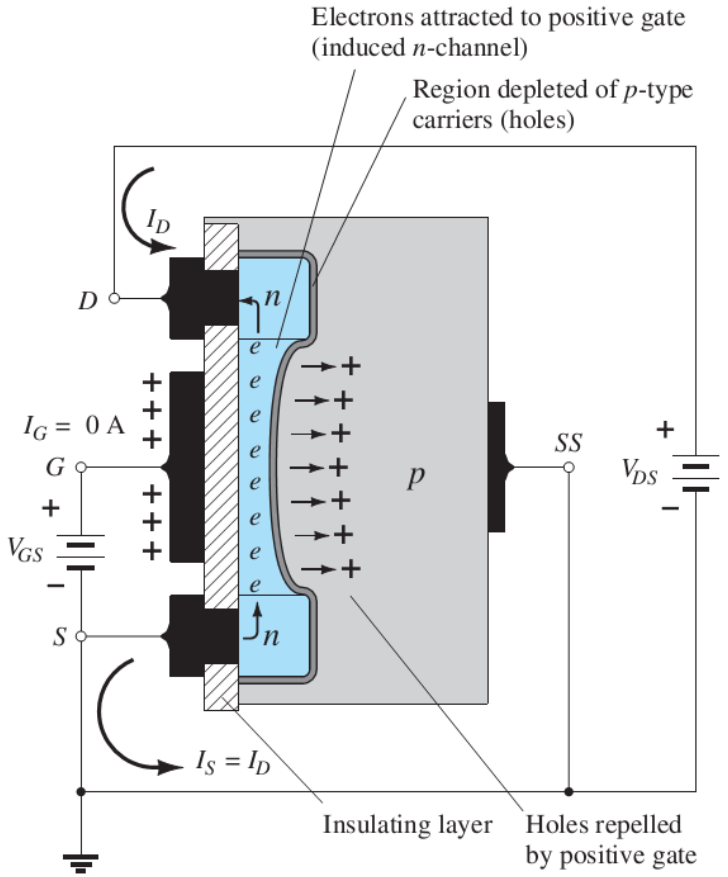

n-channel
p-channel
D
G
SS
S


RD
ID
Induced channel
n
n
VDD
VGG


D
ID
p
G
n
SS
p
S

E-MOSFET Operations





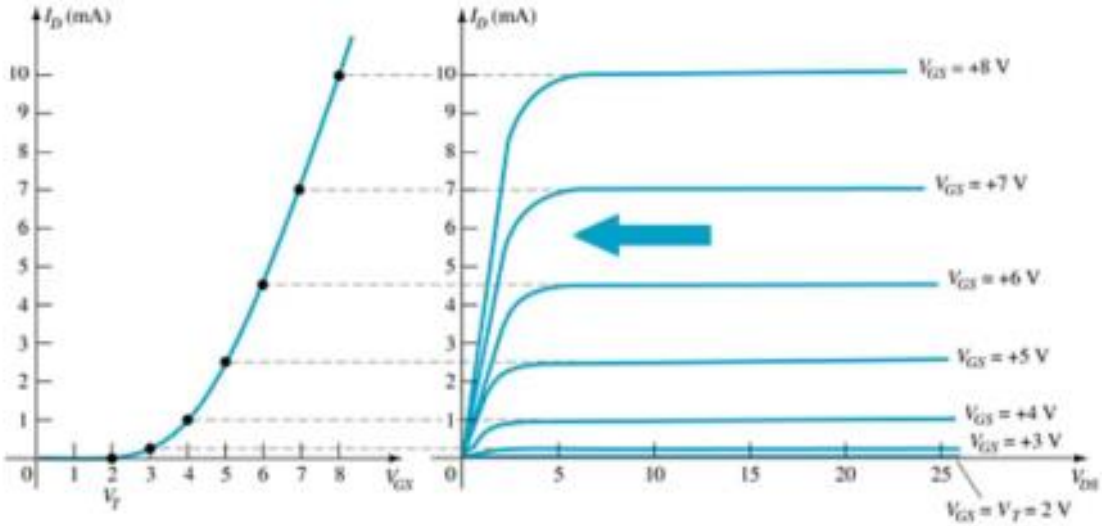
E-MOSFET Transfer Curve

To determine I_D given V_{GS}:

$$I_D = k(V_{GS} - V_T)^2$$

Where:

V_T = threshold voltage or voltage at which the MOSFET turns on



***k*, a constant, can be determined by using values at a specific point and the formula:**

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

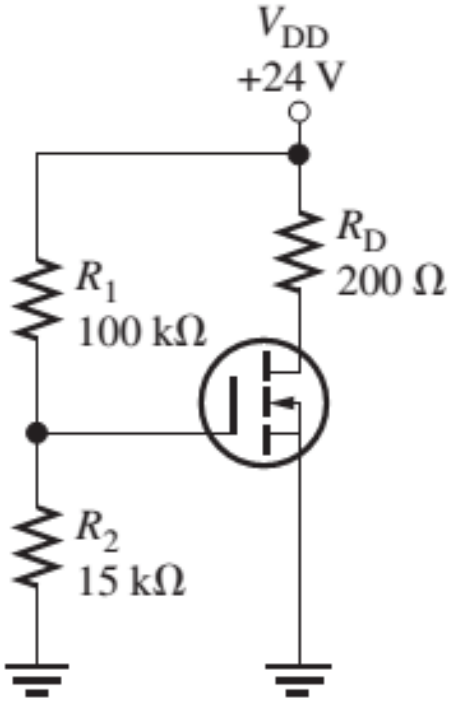
V_{DSsat} can be calculated by:

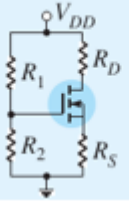
$$V_{Dsat} = V_{GS} - V_T$$

Example

- Determine k, I_D, V_{GS} and V_{DS} for given E-MOSFET where
  - $V_{GS(on)} = 4V$ and $I_{D(on)} = 200mA$
  - $V_{GS(th)} = 2V$ $(=V_T)$

- Hint:



Enhancement type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$

To determine I_D given V_{GS}:

$$I_D = k(V_{GS} - V_T)^2$$

***k*, a constant, can be determined by using values at a specific point and the formula:**

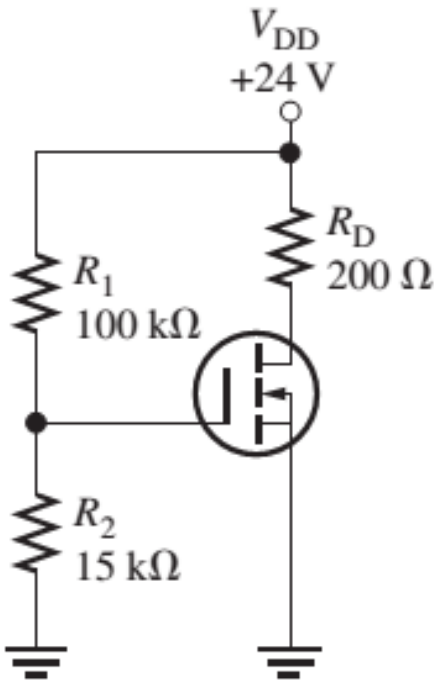
$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

Answer

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{200\text{ mA}}{(4\text{ V} - 2\text{ V})^2} = \frac{200\text{ mA}}{4\text{ V}^2} = 50\text{ mA/V}^2$$

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{15\text{ k}\Omega}{115\text{ k}\Omega}\right)24\text{ V} = \mathbf{3.13\text{ V}}$$

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (50\text{ mA/V}^2)(3.13\text{ V} - 2\text{ V})^2$$
$$= (50\text{ mA/V}^2)(1.13\text{ V})^2 = 63.8\text{ mA}$$

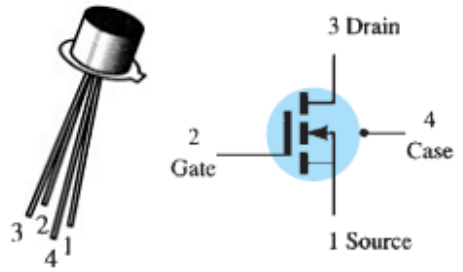


$$V_{DS} = V_{DD} - I_D R_D = 24\text{ V} - (63.8\text{ mA})(200\ \Omega) = \mathbf{11.2\text{ V}}$$

E-MOSFET Datasheet

2N4351

MOSFET SWITCHING



N-CHANNEL – ENHANCEMENT

MAXIMUM RATINGS

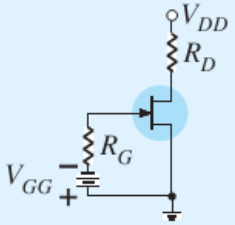
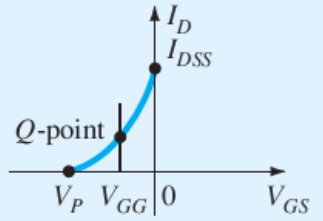
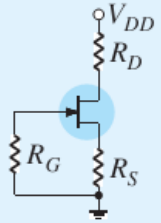
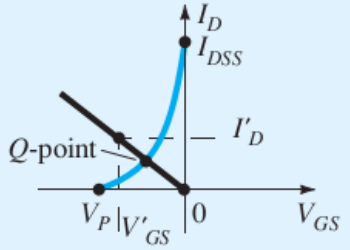
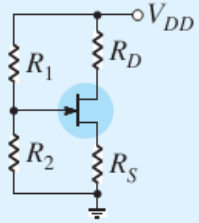
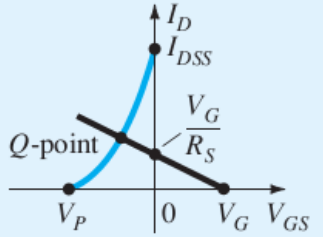
Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

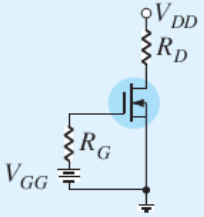
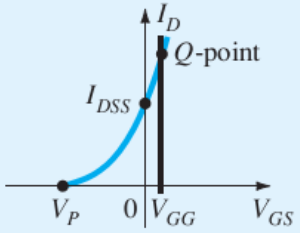
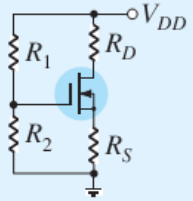
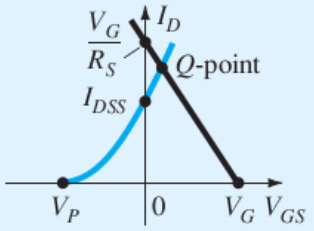
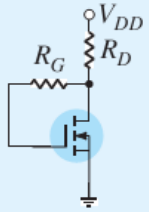
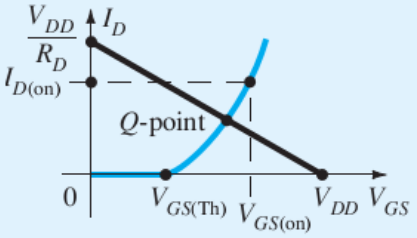
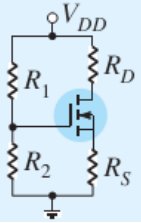
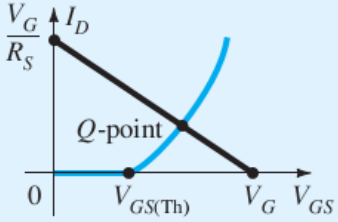
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($I_D = 10\ \mu A$, $V_{GS} = 0$)	$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$) $T_A = 25°C$ $T_A = 150°C$	I_{DSS}	– –	10 10	nAdc μAdc
Gate Reverse Current ($V_{GS} = \pm 15$ Vdc, $V_{DS} = 0$)	I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 10\ \mu A$)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage ($I_D = 2.0$ mA, $V_{GS} = 10$V)	$V_{DS(on)}$	–	1.0	V
On-State Drain Current ($V_{GS} = 10$ V, $V_{DS} = 10$ V)	$I_{D(on)}$	3.0	–	mAdc

JFET Bias

JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	

MOSFET Bias

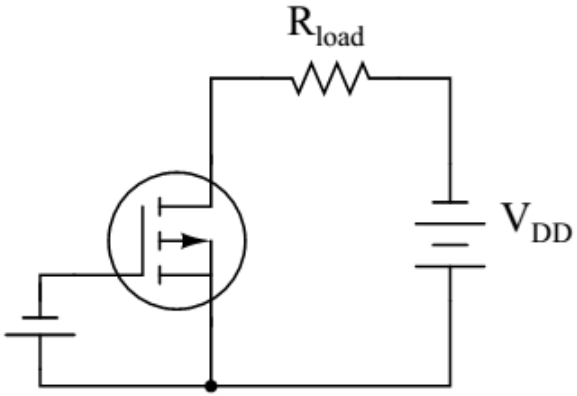
Depletion-type MOSFET Fixed-bias (and MESFETs)		$V_{GS_Q} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration (and MESFETs)		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

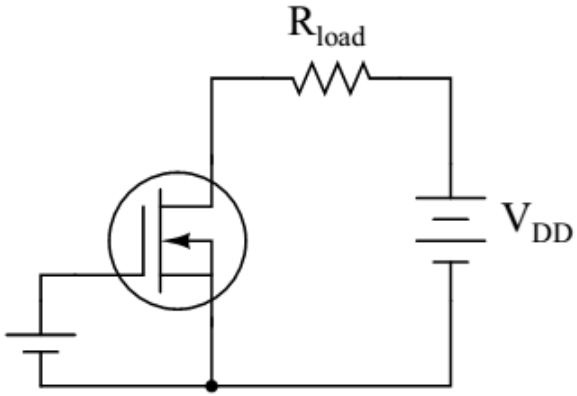
MOSFET Operation Status

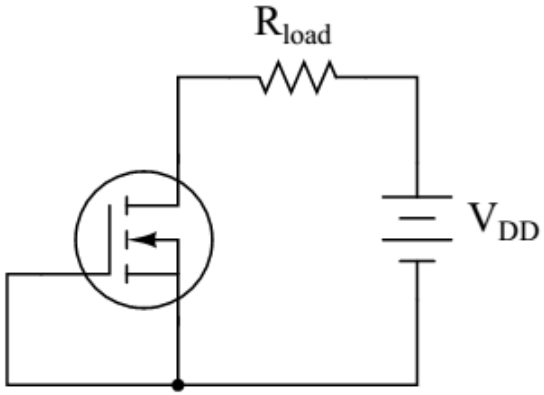
MOSFET type	$V_{GS} > 0$	$V_{GS} = 0$	$V_{GS} < 0$
N-Channel D-MOSFET	ON	ON	OFF
N-Channel E-MOSFET	ON	OFF	OFF
P-Channel D-MOSFET	OFF	ON	ON
P-Channel E-MOSFET	OFF	OFF	ON

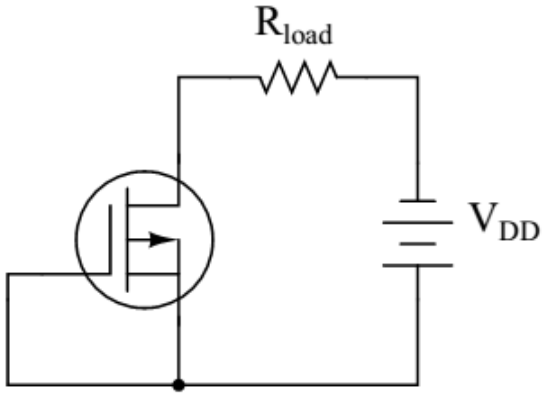
Example

- Determine the correct type (p-channel or n-channel, D-type or E-type) of the following MOSFETs

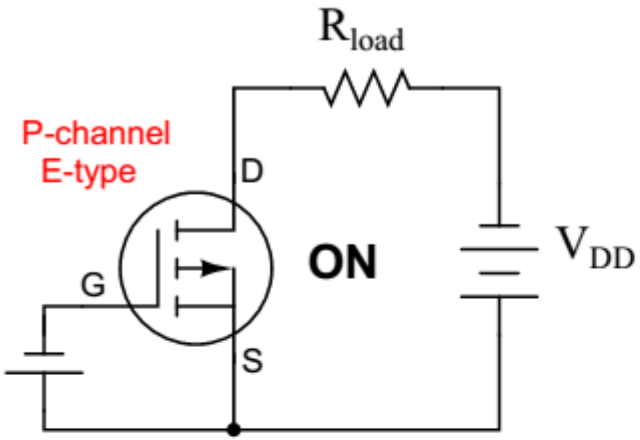


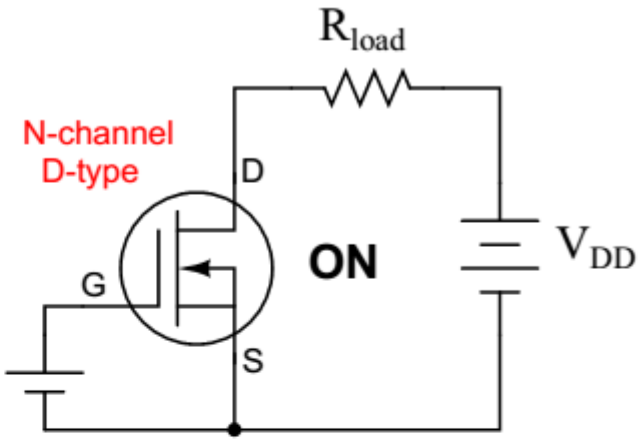


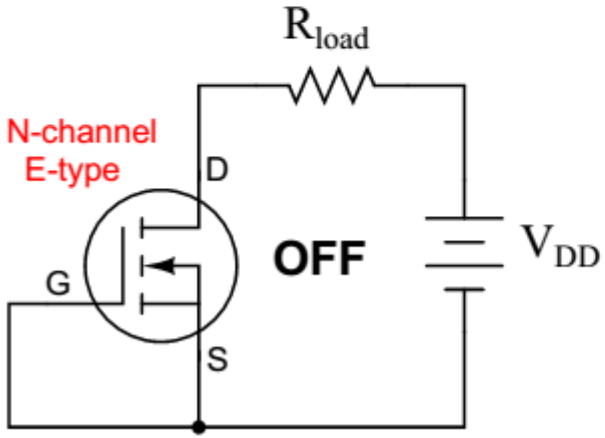


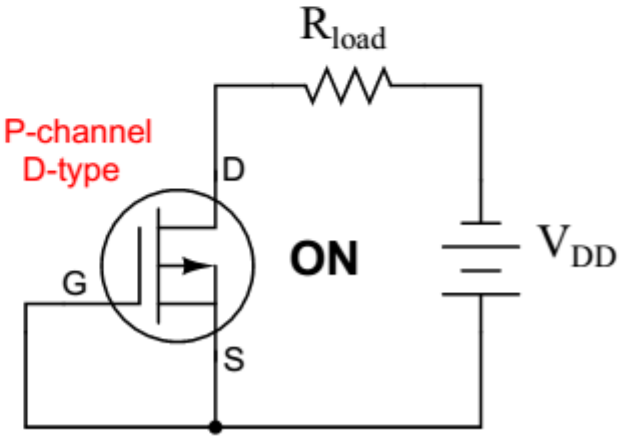


Answer


R_{load}
P-channel
E-type
D
G
S
ON
V_{DD}


R_{load}
N-channel
D-type
D
G
S
ON
V_{DD}


R_{load}
N-channel
E-type
D
G
S
OFF
V_{DD}


R_{load}
P-channel
D-type
D
G
S
ON
V_{DD}

Reference