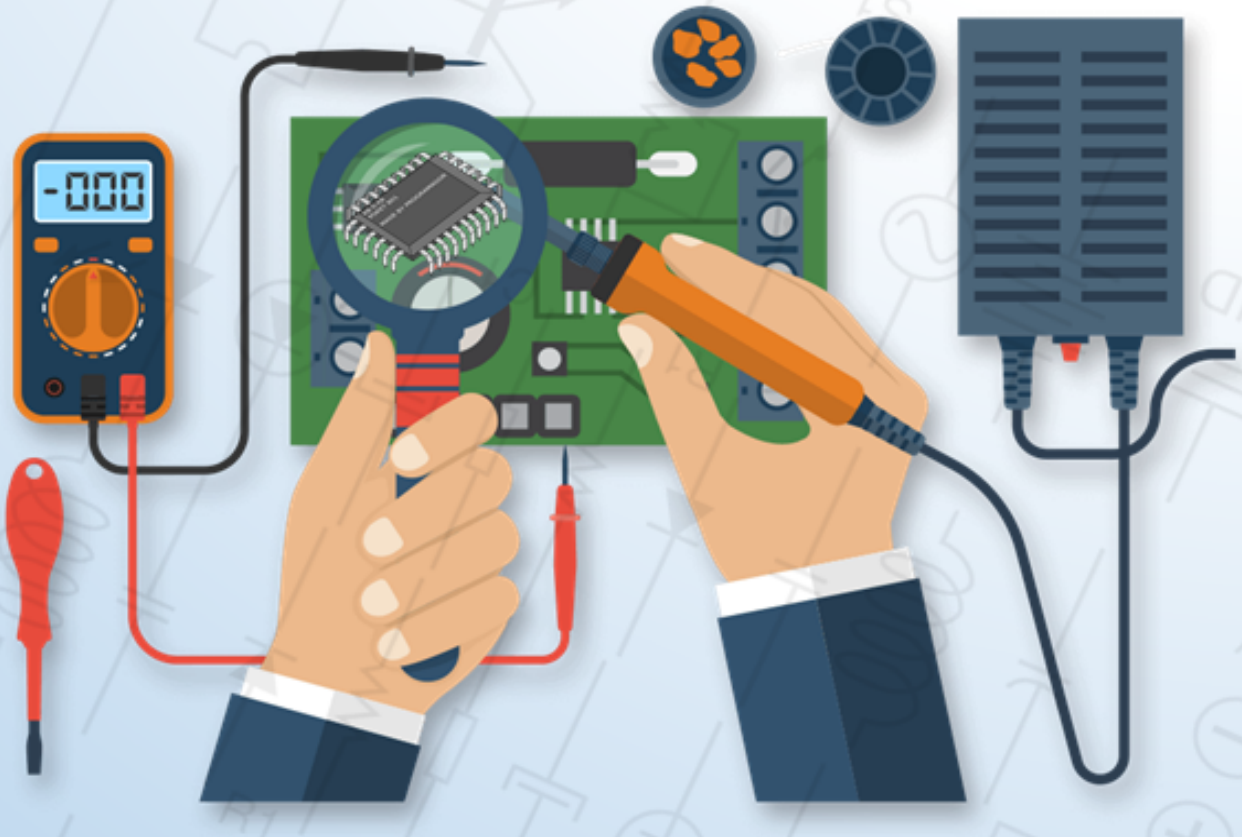
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
COMPUTER ENGINEERING

Electronic Device Component



Dr. Le Trong Nhan

Contents

CHAPTER 1

Bipolar Junction Transistor

1 Introduction

In the diode tutorials we saw that simple diodes are made up from two pieces of semiconductor material to form a simple pn-junction and we also learnt about their properties and characteristics.

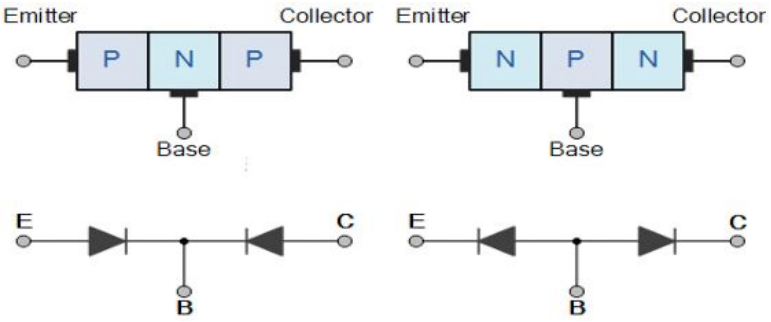


Figure 1.1: *Bipolar transistor construction*

If two individual signal diodes are joined together back-to-back, this will form a two PN-junctions connected together in series which would share a common Positive, (P) or Negative, (N) terminal. The fusion of these two diodes produces a three layer, two junction, three terminal device forming the basis of a Bipolar Junction Transistor (BJT), which is shown in the figure above.

Considering the symbol of the transistor in the schematic, the direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

The transistor is ability to change between these two states enables it to have two basic functions: “switching” (digital electronics) or “amplification” (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- Active region: The transistor operates as an amplifier and $I_C = \beta I_B$
- Saturation: The transistor is “Fully-ON” operating as a switch and $I_C = I_{Sat}$
- Cut-off: The transistor is “Fully-OFF” operating as a switch and $I_C = 0$

2 BJT simulation circuit

Implement the following circuit in PSPICE. The new component used is **QBreakN NPN**, which can be found in the Favorites list. The default transistor gain is $\beta = 100$, and the saturated voltage $V_{CE(Sat)} = 0.65V$

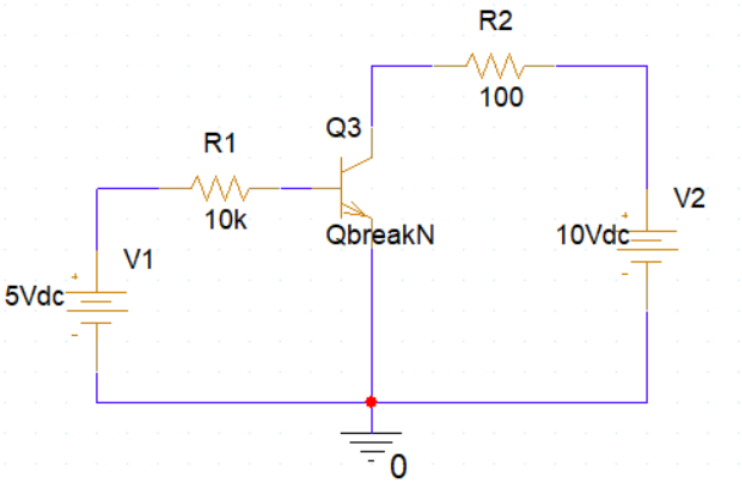


Figure 1.2: Simple connection with transistor

For a bias point simulation profile, the following results are expected:

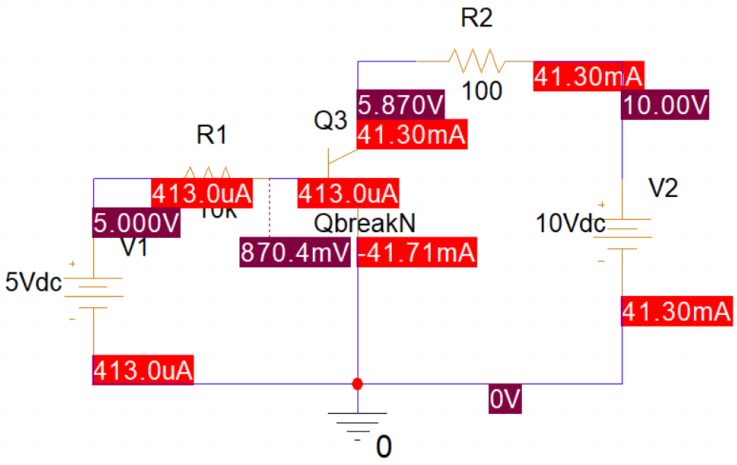


Figure 1.3: Bias profile simulation results

It is assumed that $V_{BE} = 0.7V$, the simulation results in PSPice are explained as follows:

- According to the Ohm Low, $I_B = (V_{BB} - V_{BE})/R1$ = (5V - 0.7V)/10k = 0.43mA
- It is assumed that the transistor is in linear (or active) mode, $I_C = \beta * I_B$ = 43mA
- Finally, in order to confirm the assumption above, $V_{CE} = V_{CC} - I_C * R2$ = 10V - 43mA * 100Ohm = 5.7V

Since $V_{CE} > V_{CE(Sat)}$, the transistor is working in the linear mode, to confirm our assumption. Moreover, the theory calculation is very close to the PSpice simulations.

3 Exercise and Report

3.1 BJT in Saturation Mode

Change the value of **R1 to 1k** and run the simulation again. Capture the simulation results and explain the values of I_B, I_C, V_{CE}. The default transistor gain is $\beta = 100$, and the saturated voltage $V_{CE(Sat)} = 0.65V$ and $V_{BE} = 0.7V$.
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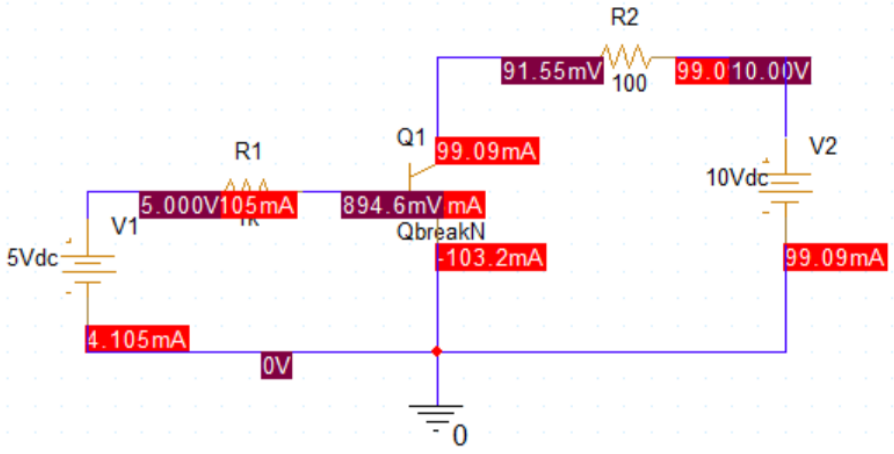

Figure 1.4: Change the value of R1 to 1k.

The results in PSpice are explained as follows:

- According to the Ohm Low, $I_B = \dfrac{V1 - V_{BE}}{1k} = 4.3(mA)$.
- It is assumed that the transistor is in linear (or active) mode, $I_C = \beta * I_B = 0.43$ (mA).
- Finally, in order to confirm the assumption above, $V_{CE} = V_{CC} - I_C * R2 = -33$ (V).

Since $V_{CE} < 0$, our assumption is not correct. The transistor stays in saturation mode. Therefore, I_C is determined as follows:

$I_{C(Sat)} = (V_{CC} - V_{CE(Sat)})/R2 = 93.5$ (mA).

3.2 DC Sweep Simulation

The schematic in the first exersice with **R1 = 1k** is re-used in this exercise. However, a DC-Sweep simulation mode is performed with V1 is varied from 0V to 5V (0.1V for the step), as follows:

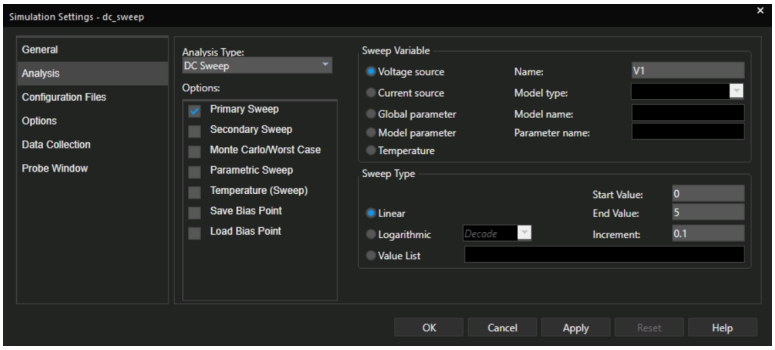

Figure 1.5: *DC-Sweep profile for simulation*

Run the simulation and trace for the current I_C according to the value of V1. Capture your screen and plot it in the report. Please increase the width of the curve.
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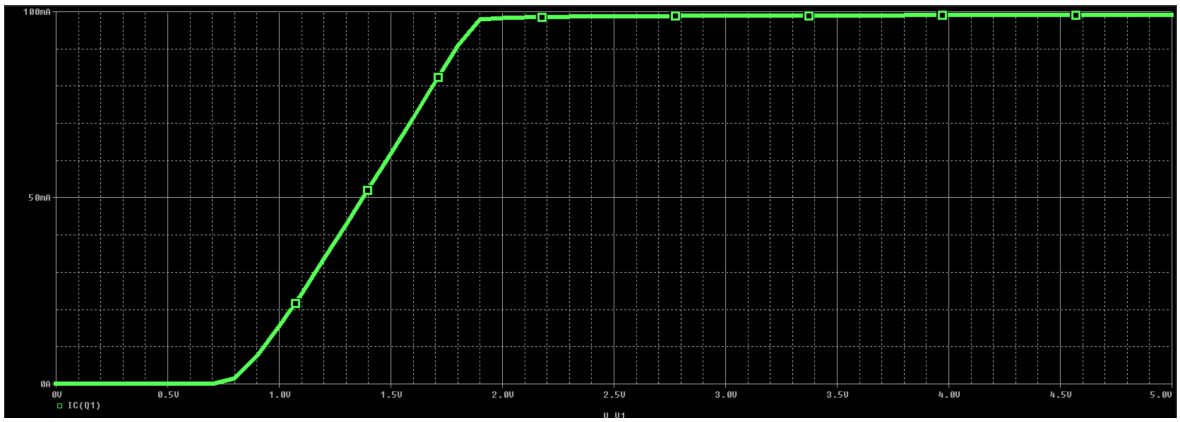

Figure 1.6: Simulation.

When the transistor becomes saturation, the value of V1 is 1.9 (v).
At this value, the value of I_B is 983µ$A(A)$.
And the value of $I_{C(Sat)}$ is 98.3mA.

3.3 BJT used as a Switch

For a given BJT circuit, determine R1 and R2 to have I_C saturated at 50mA. In this saturation mode, $V_{CE(Sat)}$ is 30mV. Assume that V_{BE} = 0.7V and the current gain β = 100.

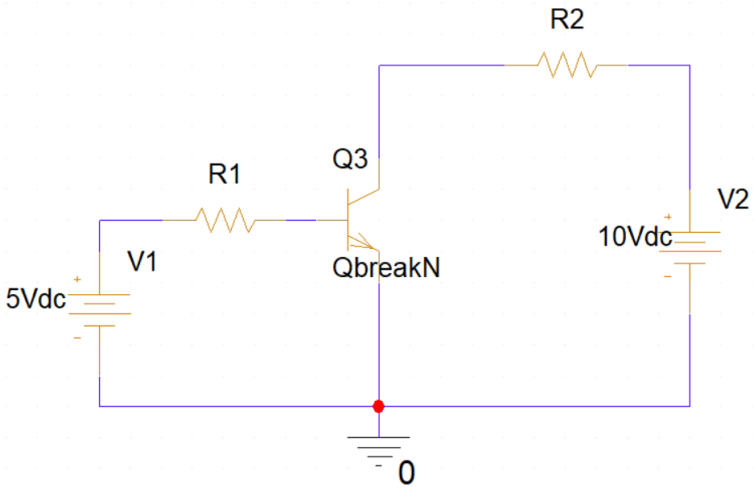

Figure 1.7: *BJT used as switch in saturation mode*

Present your solution to determine R1 and R2. Perform the simulation in PSpice to confirm the results. Capture the screen in PSpice and present in the report.
Solution:

$$R2 = \frac{V_{CC} - V_{CE(sat)}}{I_{C(Sat)}} = \frac{10 - 30 \cdot 10^{-3}}{50 \cdot 10^{-3}} = 199.4\Omega.$$

$$I_B = \frac{I_C}{\beta} = \frac{50 \cdot 10^{-3}}{100} = 0.5mA.$$

$$R1 = \frac{V_{BB} - V_{BE}}{I_B} = \frac{5 - 0.7}{0.5 \cdot 10^{-3}} = 8.6k\Omega.$$

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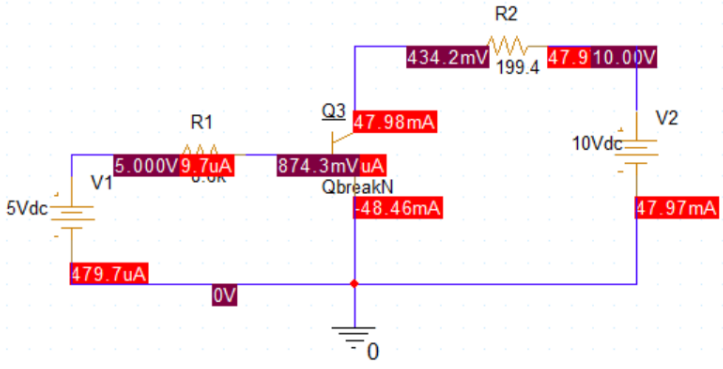

Figure 1.8: Result.

3.4 Drive a device with an NPN BJT

This exercise has a $5V$ logic output (the V_{ter} in Figure 1.9) that can source up to $10mA$ of current without a severe voltage drop and stand a maximum current of $20mA$. If the logic terminal sources a current larger than $20mA$, it would be damaged. Or, if it sources a current larger than $10mA$, the V_{ter} voltage will drop to less than $4V$. We should avoid this drop in many cases. However, this logic terminal has to be used to drive an electrical component with an equivalent internal resistance of 5 ohms (the LOAD in Figure 1.9) and requires a current of at least $300mA$ and not exceeding $500mA$ to function normally. Given that we have an NPN transistor with the current gain β equals 100, the maximum I_C current is $400mA$, and the barrier potential at the BE junction is $V_{BE} = 0.7V$, select a resistor available in the market to replace the resistor R_B revealed in Figure 1.9. to make the circuit function well. After that, perform a simulation to double-check your selection.

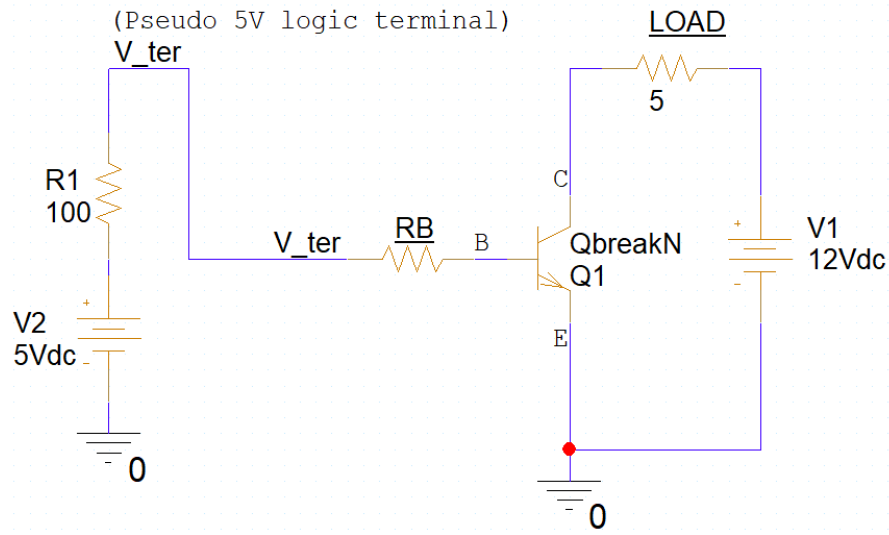

Figure 1.9: Select a resistor available in the market for R_B

3.4.1 Theory calculations

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the limits of the LOAD and the npn transistor, we have:

$$300mA \text{ (Minimum of Load)} < I_C < 400mA \text{ (Maximum of transistor)}$$

$$3mA \text{ (Minimum of Load)} < I_B < 4mA \text{ (Maximum of transistor)} \left(I_B = \frac{I_C}{\beta} \right)$$

With $I_B(min) = 3mA$, we have: $R_B(max) = \dfrac{V_{ter} - V_{R1} - V_{BE}}{I_B} = \dfrac{5 - 3 \cdot 10^{-3} \cdot 100 - 0.7}{3 \cdot 10^{-3}} =$ 1333.3333Ω

With $I_B(max) = 4mA$, we have: $R_B(min) = \dfrac{V_{ter} - V_{R1} - V_{BE}}{I_B} = \dfrac{5 - 4 \cdot 10^{-3} \cdot 100 - 0.7}{5 \cdot 10^{-3}} =$ 975Ω

So: 975Ω < R_B < 1333.3333Ω.R_B selected: 1$k\Omega$.

When $R_B = 1k\Omega$
$I_B = \frac{V_2 - V_{BE}}{R_1 + R_2} = \frac{5 - 0.7}{100 + 10^3} = 3.91mA.$

3.4.2 Simulation

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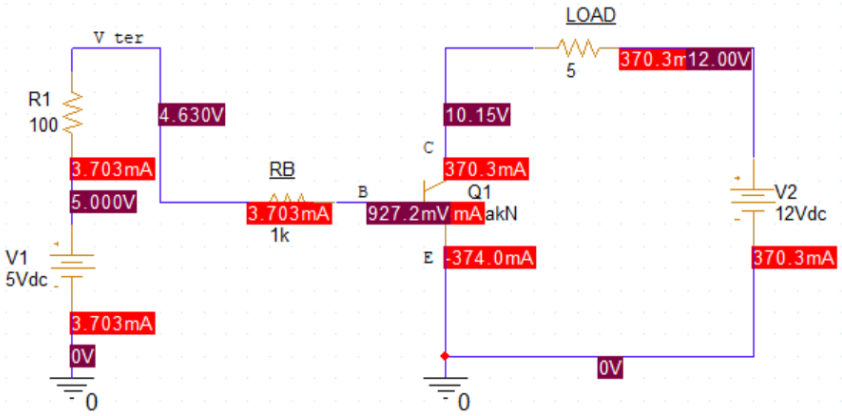

Figure 1.10: R_B equal 1k Ω.

3.4.3 Compare

		Theory			PSpice		
	R_B	V_{BE}	I_B	I_C	V_{BE}	I_B	I_C
$R_B(min)$	975Ω	0.7V	4mA	400A	927.8mV	3.788mA	378.8mA
$R_B(max)$	1333.3333Ω	0.7V	3mA	300mA	920.4mV	2.846mA	284.6mA
$R_B(selected)$	1$k\Omega$	0.7V	3.91mA	391mA	927.2mV	3.703mA	370.3mA

3.5 Simple bias configuration

The circuit given in Figure 1.11 is known as a simple kind of NPN bias configuration. First, students simulate the circuit with two values of RC, respectively 10 Ohms and 1k Ohms. Then, give your statement on the change of the current I_E and explain the phenomena.

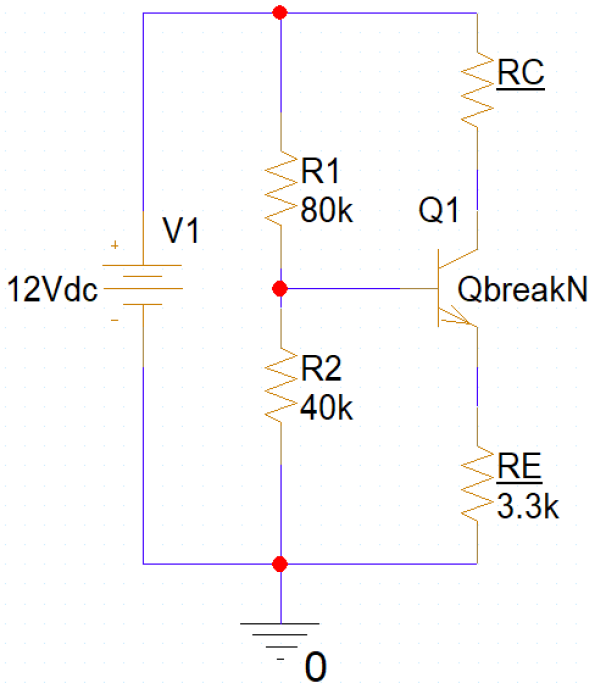

Figure 1.11: Simple bias configuration

3.5.1 Simulation

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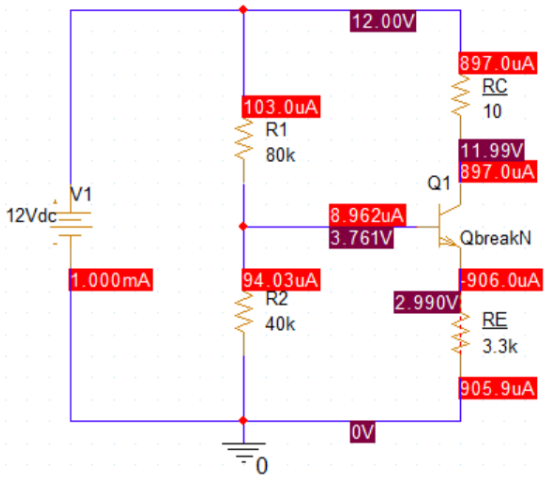
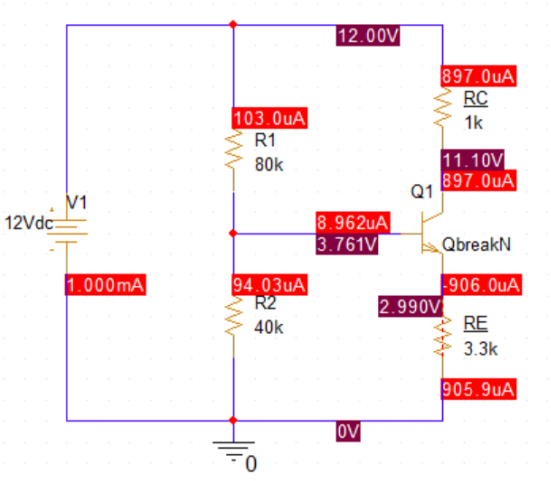
Step 1: Simulate the circuit with R_C = 10 Ohms.



Step 2: Simulate the circuit with R_C = 1k Ohms.



3.5.2 Circuit analysis

Conduct some theoretical calculation to explain for the phenomena you have observed from the simulation.

We have: $R_{Th} = R_1 // R_2 = \dfrac{80 \cdot 10^3 \cdot 40 \cdot 10^3}{(80+40) \cdot 10^3} = \dfrac{80}{3} k\Omega$

$$V_{Th} = V_B = \frac{R_2 \cdot V_{CC}}{R_1 + R_2} = \frac{40 \cdot 12}{80+40} = 4V$$

Applying Kirchhoff's voltage for Base-Emitter Loop, we have: $V_{Th} - I_B \cdot R_{Th} - V_{BE} - I_E \cdot R_E = 0$

$$\longrightarrow I_E = \frac{V_{Th} - V_{BE}}{\dfrac{R_{Th}}{\beta+1} + R_E} = \frac{4 - 0.7}{(\dfrac{\dfrac{80}{3}}{100+1} + 3.3) \cdot 10^3} = 925.9\mu A \left(\text{Substituting } I_B = \frac{I_E}{\beta+1}, \beta = 100 \right)$$

The change in current I_E is due to the difference of V_{BE} in Pspice(0.77) and in theory(0.7), but it's not significant .

3.6 PNP Circuit

Figure 1.12 shows a very typical PNP transistor circuit. Calculate I_B, I_E, and I_C then simulate the circuit to double-check your calculation. Assume the current gain β = 100.

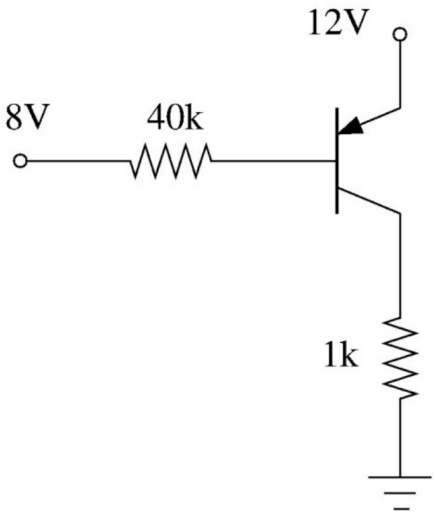


Figure 1.12: A PNP Circuit

3.6.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

$V_{EB} = 0.7V$

$$I_B = \frac{V_{EE} - V_{BB} - V_{EB}}{R_B} = \frac{12 - 8 - 0.7}{40 \cdot 10^3} = 82.5\mu A$$

$$I_C = \beta \cdot I_B = 100 \cdot 82.5 = 8.25mA$$

$$I_E = I_B + I_C = 82.5 \cdot 10^{-6} + 8.25 \cdot 10^{-3} = 8.3325mA$$

3.6.2 Simulation

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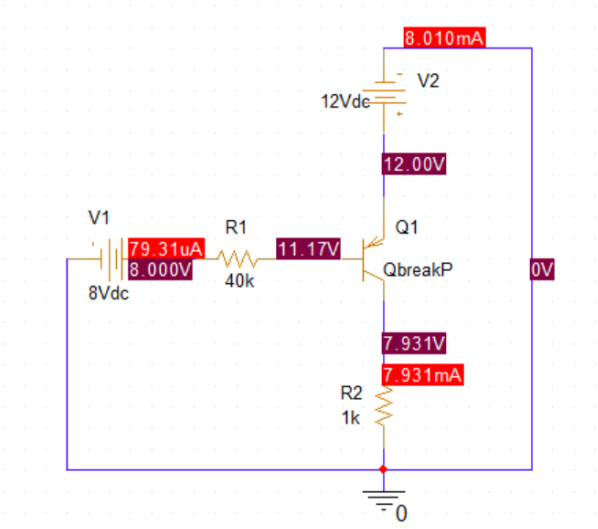

3.6.3 Comparison

I_B (In theory) = 82.5 µA and I_B (simulation) = 79.31 µA

I_C (In theory) = 8.25 mA and I_C (simulation) = 7.931 mA

I_E (In theory) = 8.3325 mA and I_E (simulation) = 8.01 mA

3.7 Circuit with NPN and PNP bipolar junction transistors

Give the circuit in Figure 1.13. Calculate the Voltage at all nodes and the current in all branches. Assume the current gain of both transistors is the same at $\beta = 100$. Then perform a simulation and compare the result with the theoretical calculation.

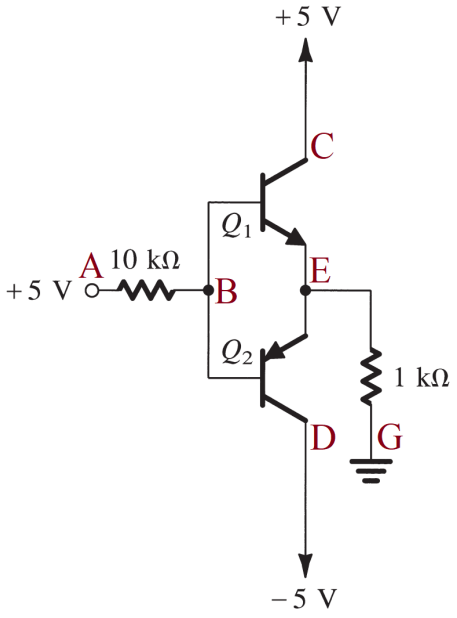

Figure 1.13: Circuit with NPN and PNP bipolar junction transistors

3.7.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

We have $V_E < V_B$, therefore the transistor Q_2 is close

According to the KVL, we have the following equation:

$$I_{BE} \text{ (hereinafter called } I_B) = \frac{V_A - V_{BE}}{R_B + (\beta + 1) \cdot R_E} \quad (1)$$

Solve (1) we have $I_B = \frac{5 - 0.7}{(10 + (100 + 1) \cdot 1) \cdot 10^3} = 38.74 \mu A$

$I_C = \beta \cdot I_B = 100 \cdot 0.0387 = 3.8739 mA$

$I_{EG} = I_B + I_C = (3.8739 + 0.0387) \cdot 10^{-3} = 3.9126mA$

$V_E = I_{EG} \cdot R_E = 3.9126 \cdot 1 = 3.9126V$

$V_B = V_E + V_{BE} = 3.9126 + 0.7 = 4.6126V$

3.7.2 Simulation

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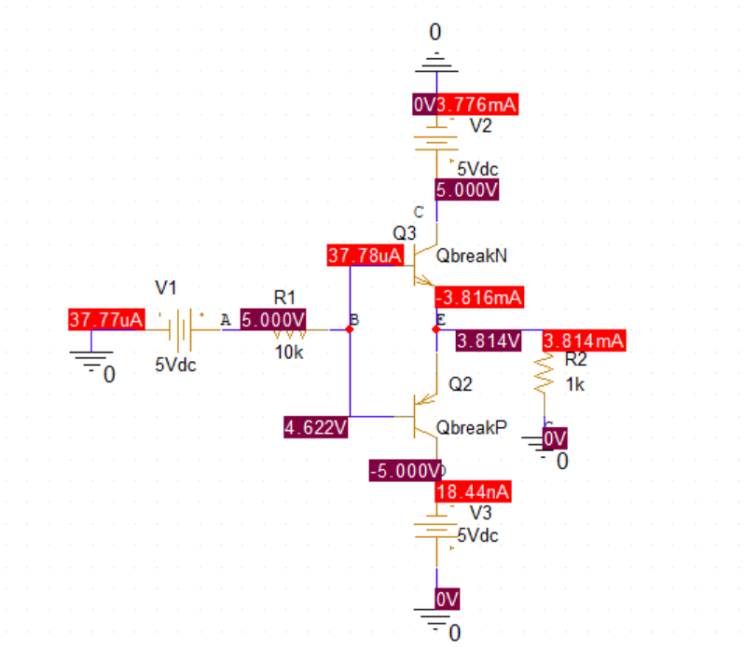

3.7.3 Comparison

I_B (In theory) = 38.74 µA, I_B (simulation) = 37.76 µA

I_C (In theory) = 3.874 mA, I_C (simulation) = 3.776 mA

I_{EG} (In theory) = 3.913 mA, I_{EG} (simulation) = 3.814 mA

V_E (In theory) = 3.913 V, V_E (simulation) = 3.814 V

V_B (In theory) = 4.613 V, V_B (simulation) = 4.622 V

3.8 NPN Circuit with E resistance

In Figure 1.14, calculate all the values of I_B, I_C, I_E, V_E, and V_C. Assume the voltage drop V_{BE} = 0.7V and the current gain coefficient of the transistor is β = 100. Then, perform a simulation to double-check your theoretical calculations.

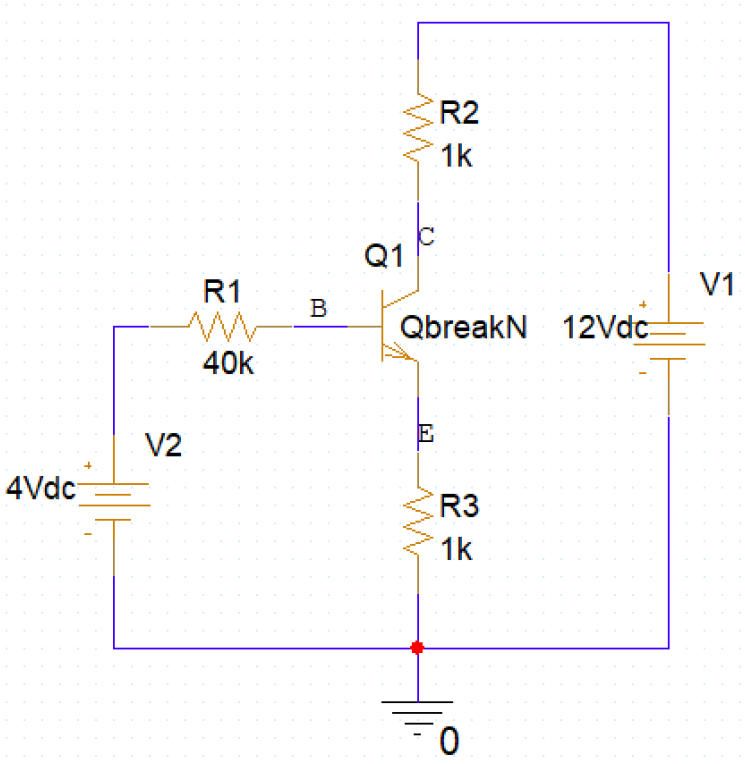

Figure 1.14: NPN Circuit with E resistance

3.8.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the Kirchhoff's voltage law, we have the following equation:

$V_2 - I_B \cdot R_1 - V_{BE} - I_E \cdot R_3 = 0$

$\Longleftrightarrow V_2 - I_B \cdot R_1 - V_{BE} - (\beta+1) \cdot I_B \cdot R_3 = 0$ (Because $I_E = (\beta+1) \cdot I_B$) (1)

Solve (1), we have $I_B = \dfrac{V_2 - V_{BE}}{R_1 + (\beta+1) \cdot R_3} = \dfrac{4 - 0.7}{(40 + (100+1) \cdot 1) \cdot 10^3} = \dfrac{11}{470} mA = 0.0234 mA$

$I_C = \beta \cdot I_B = 100 \cdot \dfrac{11}{470} = \dfrac{110}{47} mA = 2.3404 mA$

$I_E = I_C + I_B = (\dfrac{11}{470} + \dfrac{110}{47}) \cdot 10^{-3} = \dfrac{1111}{470} mA = 2.3638 mA$

$V_E = I_E \cdot R_3 = \dfrac{1111}{470} \cdot 1 = \dfrac{1111}{470} V = 2.3638 V$

$V_C = V_1 - I_C \cdot R_2 = 12 - \dfrac{110}{47} \cdot 1 = \dfrac{454}{47} V = 9.6596 V$

3.8.2 Simulation

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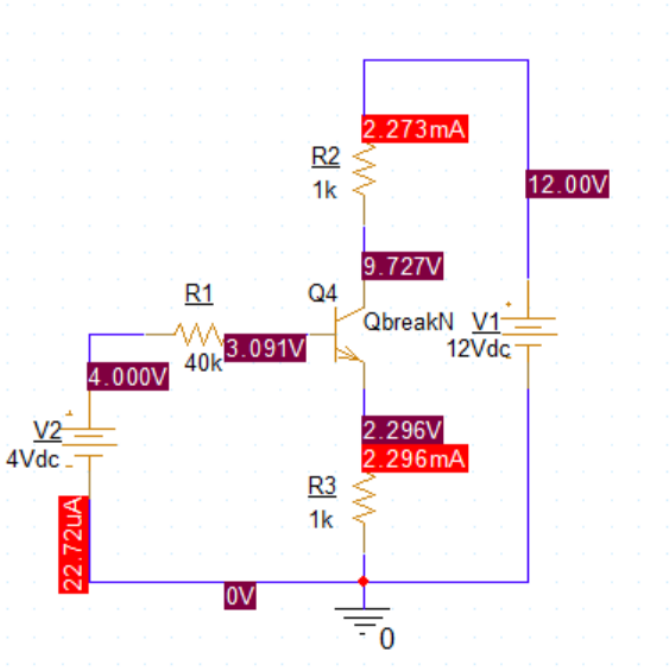

Figure 1.15: Caption

3.9 Darlington circuit

The circuit given in Figure 1.16 is known as a darlington circuit. Calculate I_{BE}, I_{AC}, I_{AL}, and the overall current gain $\frac{I_{AL}}{I_{BE}}$. After that, simulate the circuit to double-check your theoretical calculations. Assume both transistors have the same current gain coefficient $\beta = 100$.

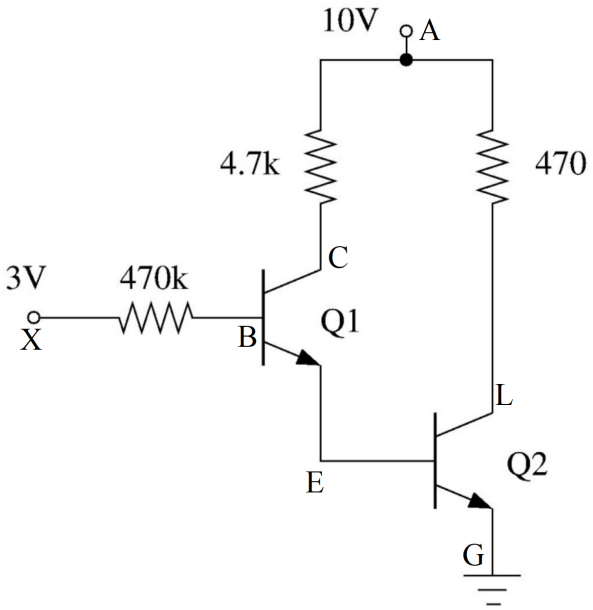

Figure 1.16: Darlington circuit

3.9.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

$$I_{BE} = \frac{3-0.7-0.7}{470} = \frac{4}{1175} mA = 3.404 \mu A$$

$$I_{AC} = \beta \cdot I_{BE} = 100 \cdot \frac{4}{1175} = \frac{16}{47} mA = 340.4 \mu A$$

We have:

- $I_{AL} = \beta \cdot (I_{BE} + I_{AC}) = 100 \cdot (\frac{4}{1175} + \frac{16}{47}) \cdot 10^{-3} = \frac{202}{5875} A$

- $U_{LG} = VA - I_{AL} \cdot R_{AL} = 10 - \frac{202}{5875} \cdot 470 = -6.16V$

- Because $U_{LG} < 0 \longrightarrow Q_2$ saturates

$$I_{AL(Sat)} = \frac{V_{AL}}{R_{AL}} = \frac{10}{470} = \frac{1000}{47} mA$$

$$\frac{I_{AL(Sat)}}{I_{BE}} = \frac{\frac{1000}{47}}{\frac{4}{1175}} = 6250$$

3.9.2 Simulation

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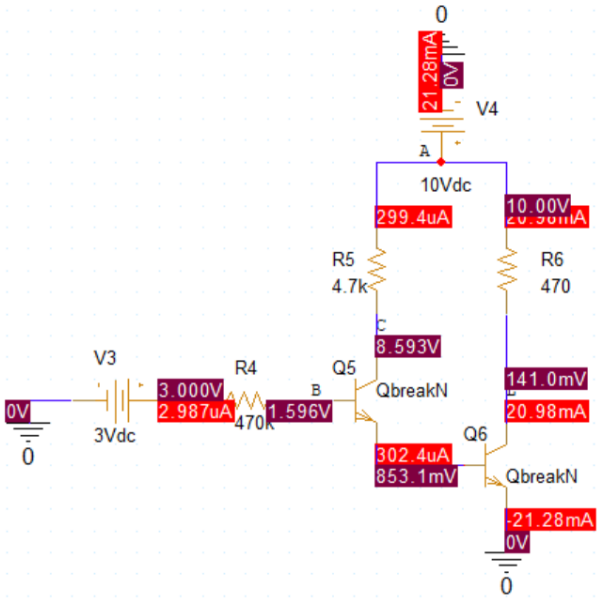


3.10 Common base

Figure 1.17 shows a bias techniques named common base bias. Calculate the values of I_E, I_B, I_C, and V_{CE}. Then simulate the circuit to double-check your theoretical calculations. Assume the current gain coefficient $\beta = 100$.

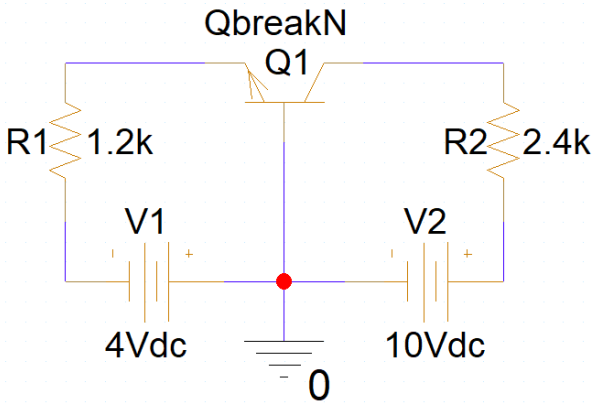


Figure 1.17: Common base

3.10.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the Kirchhoff's voltage law for Base-Emitter Loop, we have:

$$-V_1 + I_E \cdot R_1 + V_{BE} = 0$$

$$I_E = \frac{V_1 - V_{BE}}{R_1} = \frac{4 - 0.7}{1.2 \cdot 10^3} = 2.75mA$$

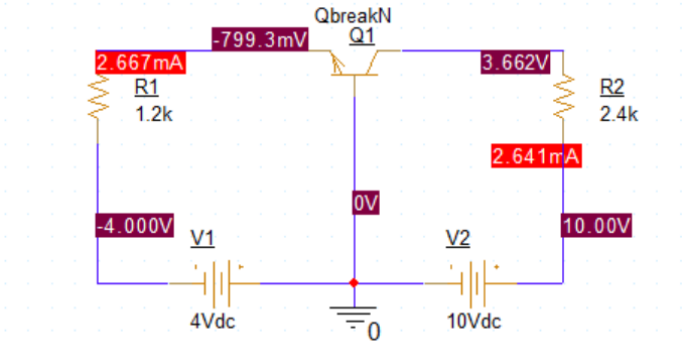
$$I_B = \frac{I_E}{\beta + 1} = \frac{2.75 \cdot 10^{-3}}{100 + 1} = \frac{11}{404} mA = 27.23\mu A$$

$$I_C = \beta \cdot I_B = 100 \cdot \frac{11}{404} mA = 2.7228mA$$

$$V_{CE} = V_1 + V_2 - I_E \cdot R_1 - I_C \cdot R_2 = 4 + 10 - 2.75 \cdot 1.2 - 2.7228 \cdot 2.4 = 4.1648V$$

3.10.2 Simulation

Your image goes here



3.11 Current mirror

The circuit shown in Figure 1.18 is known as a current mirror circuit. First, students do some theoretical calculations to get an understanding of it. After that, perform a simulation to double-check its principles and your analysis. Assume that the two transistors Q1 and Q2, are the same type and the current gain $\beta = 100$.

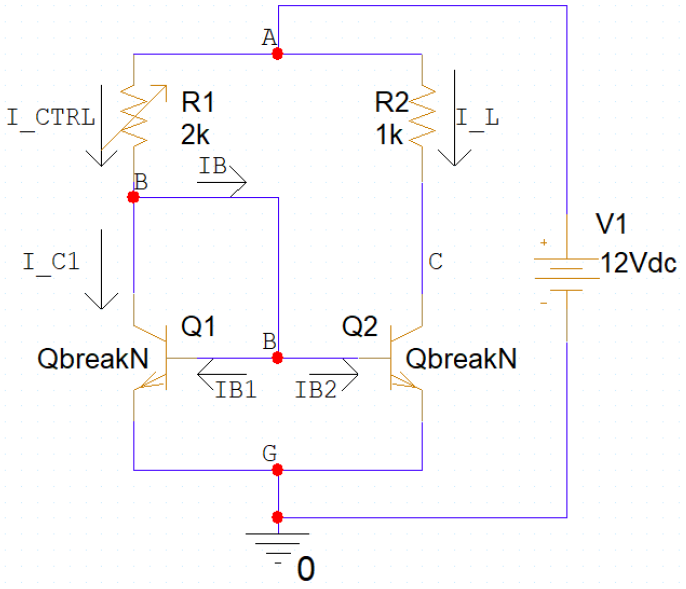


Figure 1.18: Current mirror circuit example

3.11.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the KVL, KCL, BJT Theory we have:

$$I_{CTRL} = \frac{V_1 - 0.7}{R_1} = \frac{12 - 0.7}{2 \cdot 10^3} = 5.65mA$$

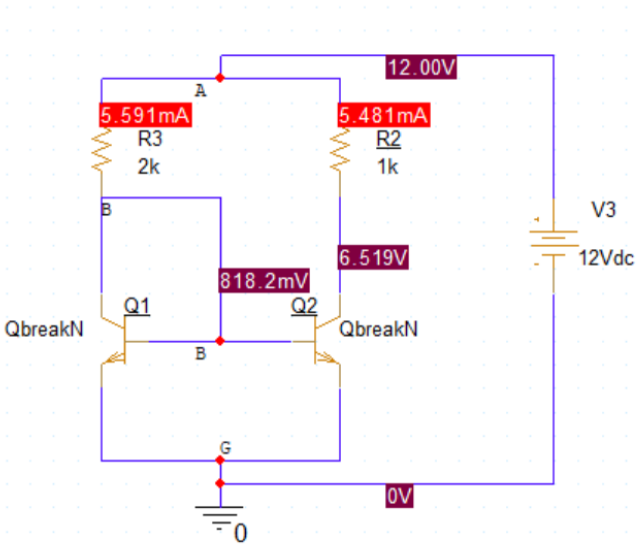
Because Q_1 and Q_2 transistors are the same type, so $I_{B1} = I_{B2}$, $V_{BE1} = V_{BE2}$ and $I_B = I_{B1} + I_{B2} = 2 \cdot I_{B1}$ and $I_{control} \approx I_{C1} = \beta \cdot I_{B1}$

$$\Longrightarrow I_{B2} = I_{B1} = \frac{I_{control}}{\beta} = 56.5\mu A$$

$$I_L = \beta \cdot I_{B_2} = 100 \cdot 56.5 \cdot 10^{-6} = 5.65mA$$

3.11.2 Simulation

Your image goes here



Why is the circuit in Figure 1.18 called circuit mirror?
The current mirror is a dc network in which the current through a load is controlled by a current at another point in the network. That is, if the controlling current is raised or lowered the current through the load will change to the same level.The effectiveness of the design is dependent on the fact that the two transistors employed have identical characteristics. For instance, if I L should try to increase for whatever reason, the base current of Q2 will also increase due to the relationship $I_{B2} = I_{C2}/B_2 = I_L/B_2$. We find that an increase in I_{B2} will cause voltage V_{BE2} to increase also. Because the base of Q2 is connected directly to the collector of Q1, the voltage V_{CE1} will increase also. This action causes the voltage across the control resistor R to decrease, causing IR to drop. But if IR drops, the base current I B will drop, causing both I_{B1} and I_{B2} to drop also. A drop in I_{B2} will cause the collector current and therefore the load current to drop also. The result, therefore, is a sensitivity to unwanted changes that the network will make every effort to correct.

Now, replace the resistor R_1 with a 100-Ohms one. Next, calculate all the values again. Then, finally, simulate the new circuit and explain the phenomena you've observed.

$$I_{CTRL} = \frac{V_1 - 0.7}{R_1} = \frac{12 - 0.7}{100} = 113mA$$

$$I_{C_1} \approx I_{CTRL} = 113mA$$

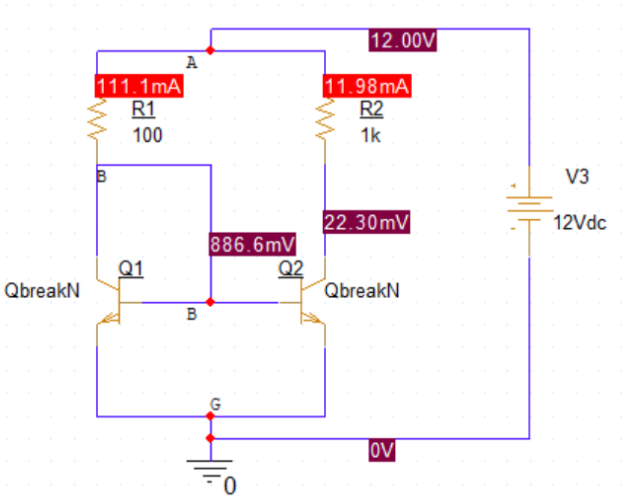
$$I_{B_1} = I_{B_2} = \frac{I_{C1}}{\beta} = 1.13mA$$

$I_{C2} = I_L = \beta \cdot I_{B2} = 113mA > I_{C2(Sat)} = 12mA$ (is not satisfied).

$\Longrightarrow$ Transistor Q2 is saturated, so $I_{C2} = I_{C2(Sat)} = 12mA$.

$I_L = I_{C2(Sat)} = 12mA$.

The 2nd simulation result goes here:



What is the phenomena?

The BJT Q2 saturates so $I_L \neq I_{CTRL}$, then there is not the current mirror.

Explain:

We assume that Q2 does not saturate, $I_L \approx I_{CTRL} = 113mA$, so $V_2 = I_L \cdot R_2 = 113 \cdot 1 \cdot 10^3 = 113V$.

$V_{CE} = V_1 - V_2 = 12 - 113 = -101V < 0$

So in this case, Q2 saturates.

The current through R2 is calculated by $\frac{V_1}{R_2}$.

3.12 BJT's logic gate application

Figure 1.19 describes a straightforward NOT gate theoretical implementation using an NPN bipolar junction transistor. In the circuit, the NPN junction transistor operates in the saturation mode.

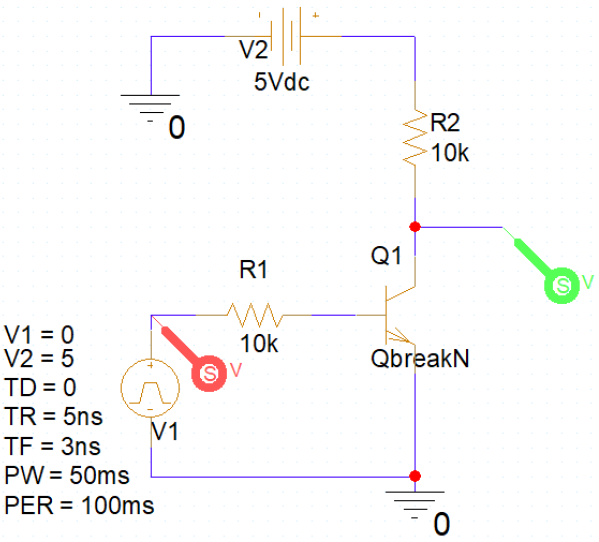


Figure 1.19: NPN theoretical NOT gate

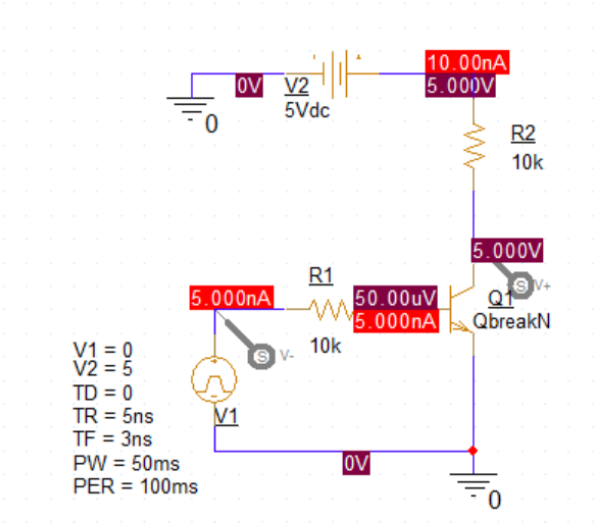
V1 = 0 When the source is off, the voltage would be 0V.
V2 = 5 When the source is on, the voltage would be 5V.
TD = 0 Delay time. This exercise assumes that there is no delay.
TR = 5ns The rise time of the pulse (from off to on stage).
TF = 3ns The fall time of the pulse (from on to off stage).
PW = 50ms Pulse width: The time in which the source keeps on.
PER = 100ms The period of the signal.

Tips:

To get the Voltage Pulse Source component in the PSpice for TI, go to ***Place -> Pspice Compoment... -> Source -> Voltage Sources -> Pulse.***

3.12.1 Simulation

Your image goes here



But, wait! How large is the maximum current this NOT gate can source? Of course, it cannot exceed 5V/10kOhm. How tiny it is! So, what if we want to use it to drive an LED? Just put an additional 220 Ohm resistor in parallel with the existing 10k one. And in this case, the 10k resistor is quite useless. Therefore, in many cases, people let the collector pin of the transistor open. This design is called open-collector output, as shown in Figure 1.20.

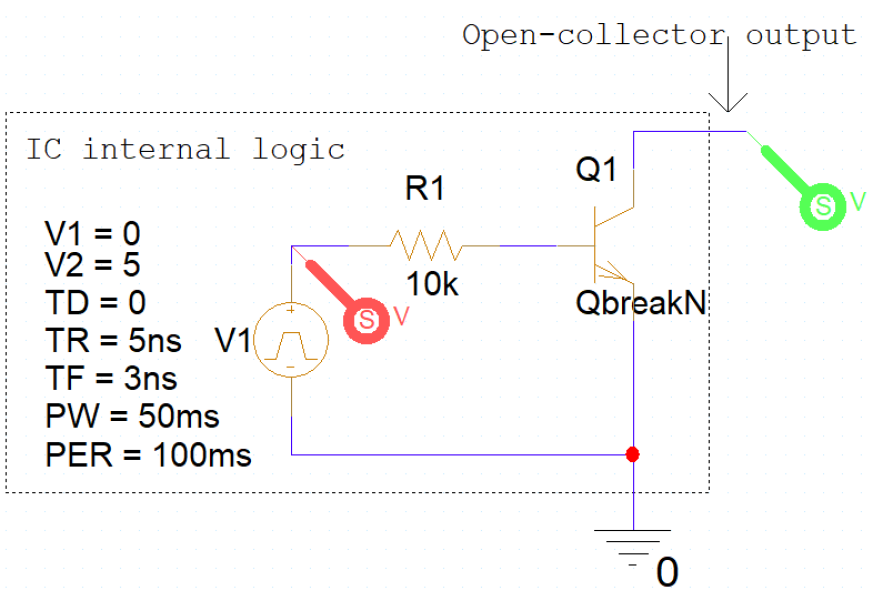


Figure 1.20: Open-collector output example

But, with this design, the input of another IC can't read the voltage of this output. Because without a pull-up resistor, the voltage V_C is floating. To read this voltage, the users have to pull it up using a resistor. There advantage here is to let the users choose the value of the pull-up resistor as their desire.

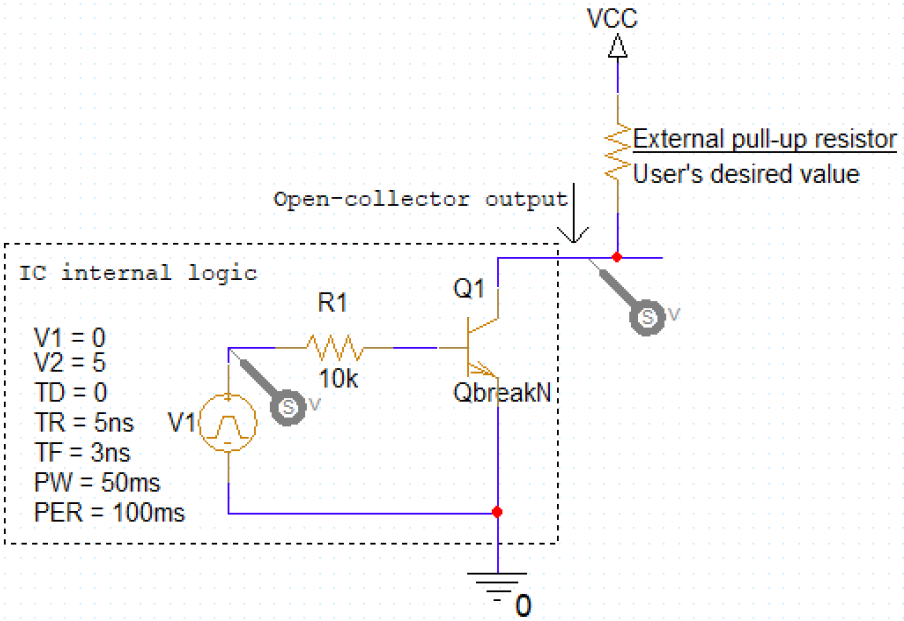


Figure 1.21: External pull-up resistor whose value selected by the users

By the side, the open-collector design manner gives an exciting way of the use of these outputs, as shown in Figure 1.22. The open-collector wired output is at the LOW level if one of the elements is LOW and is HIGH only when all the elements output HIGH.

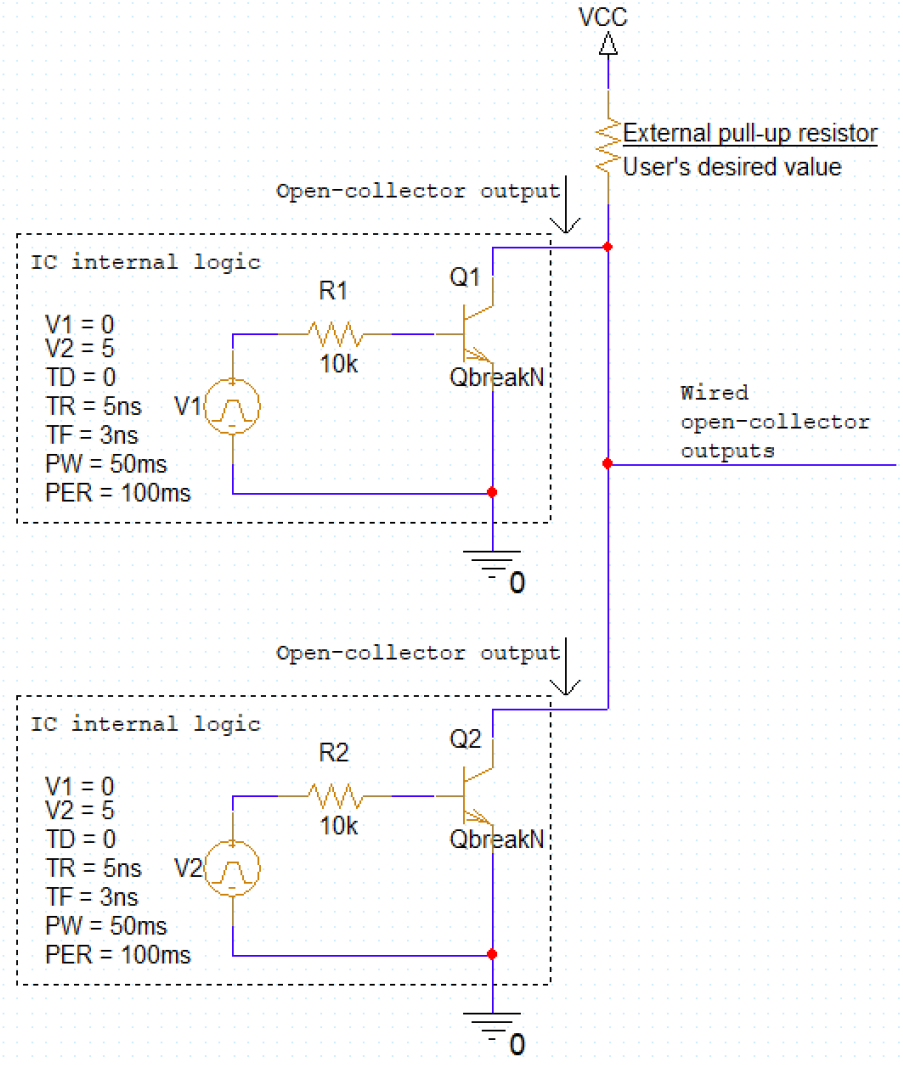


Figure 1.22: Wired open-collector outputs

3.13 Opto

The element OK_1 in Figure 1.23 is an optocoupler, which includes a light-emitting diode (LED) and a photodiode. The photodiode's conductivity depends on the intensity of the light emitted by the LED, and of course, depends on the current intensity through the LED. When the voltage across the LED is lower than its barrier potential, the Opto is cut-off. When there is current through the LED, the Opto is in the transfer mode. Like the current gain β of a BJT, the Opto also has the current transfer ratio (CTR). Assume the LED has its own barrier potential $V_F = 1.7$V, and the Opto has the CTR = 2. Calculate the voltage V_{OUT} when the switch is closed. Finally, give your idea about what we may use an Opto for, and how to use it?

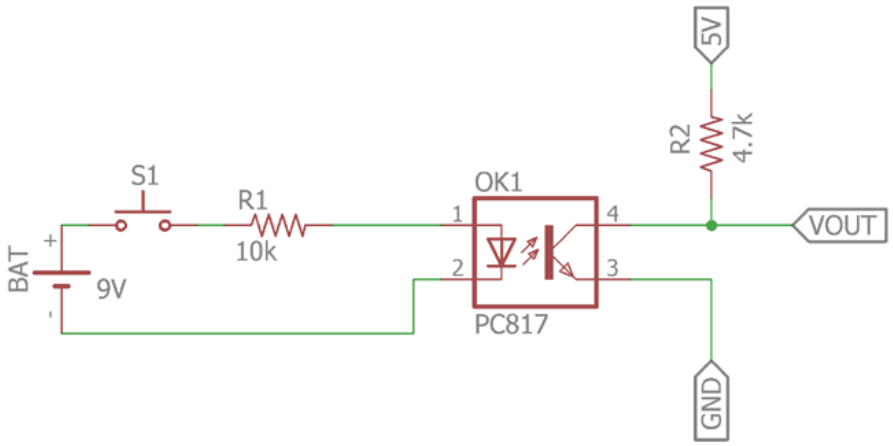


Figure 1.23: Voltage isolation with opto

$$I_F = I_{R_1} = \frac{BAT - V_F}{R_1} = \frac{9 - 1.7}{10 \cdot 10^3} = 0.73mA$$

$$I_{R_2} = CTR \cdot I_{R_1} = 2 \cdot 0.73 \cdot 10^{-3} = 1.46mA$$

$$V_{OUT} = 5 - I_{R_2} \cdot R_2 = 5 - 1.46 \cdot 4.7 = -1.862V < 0 \longrightarrow V_{OUT} = 0$$

My current idea is to use an opto to control the circuit to connect 2 audunos together to perform more tasks. The opto collector, also known as Ic, will be connected to 1 auduno and 1 auduno emittor.