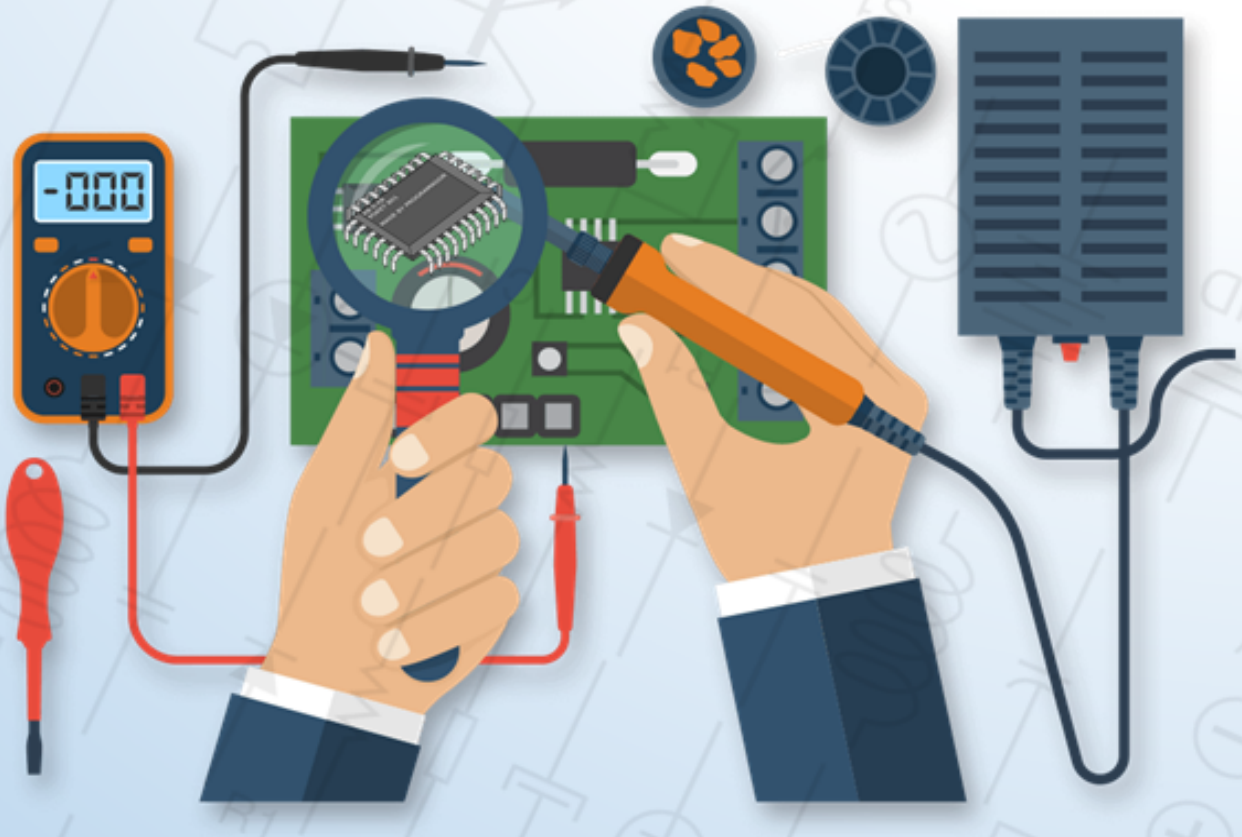
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
COMPUTER ENGINEERING

Electronic Device Component



Dr. Le Trong Nhan

Contents

CHAPTER 1

Bipolar Junction Transistor

1 Introduction

In the diode tutorials we saw that simple diodes are made up from two pieces of semiconductor material to form a simple pn-junction and we also learnt about their properties and characteristics.

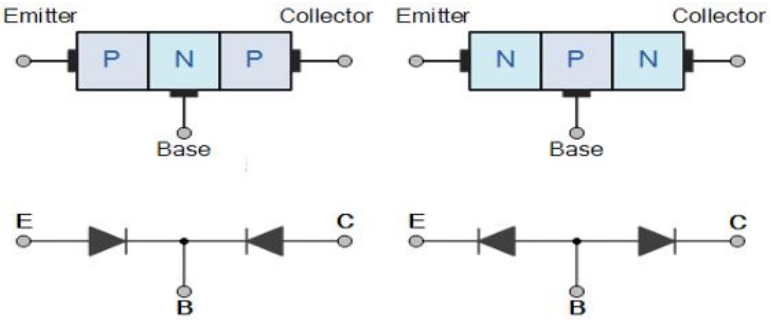


Figure 1.1: *Bipolar transistor construction*

If two individual signal diodes are joined together back-to-back, this will form a two PN-junctions connected together in series which would share a common Positive, (P) or Negative, (N) terminal. The fusion of these two diodes produces a three layer, two junction, three terminal device forming the basis of a Bipolar Junction Transistor (BJT), which is shown in the figure above.

Considering the symbol of the transistor in the schematic, the direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

The transistor is ability to change between these two states enables it to have two basic functions: “switching” (digital electronics) or “amplification” (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- Active region: The transistor operates as an amplifier and $I_C = \beta I_B$
- Saturation: The transistor is “Fully-ON” operating as a switch and $I_C = I_{Sat}$
- Cut-off: The transistor is “Fully-OFF” operating as a switch and $I_C = 0$

2 BJT simulation circuit

Implement the following circuit in PSPICE. The new component used is **QBreakN NPN**, which can be found in the Favorites list. The default transistor gain is $\beta = 100$, and the saturated voltage $V_{CE(Sat)} = 0.65V$

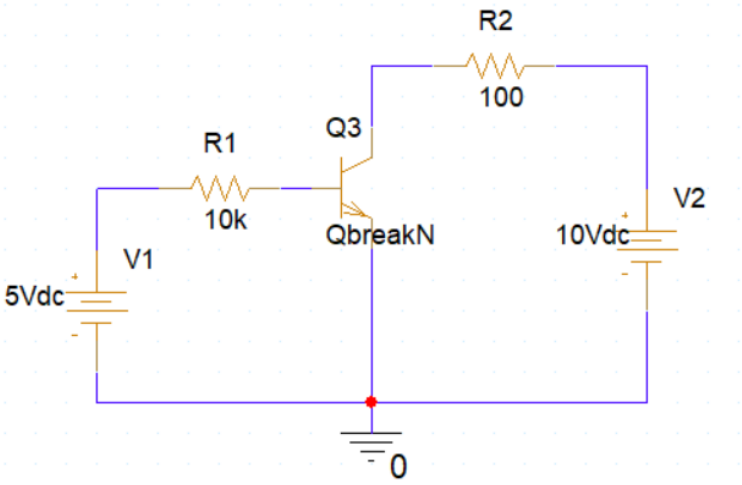


Figure 1.2: Simple connection with transistor

For a bias point simulation profile, the following results are expected:

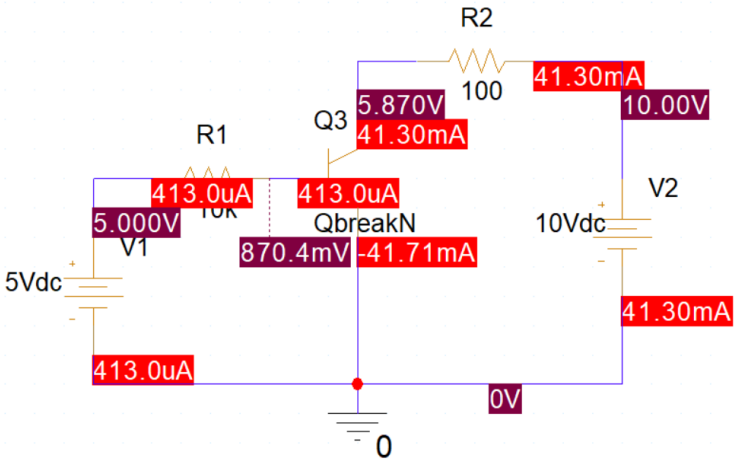


Figure 1.3: Bias profile simulation results

It is assumed that $V_{BE} = 0.7V$, the simulation results in PSPice are explained as follows:

- According to the Ohm's Law, $I_B = (V_{BB} - V_{BE})/R1$ = (5V - 0.7V)/10k = 0.43mA
- It is assumed that the transistor is in linear (or active) mode, $I_C = \beta * I_B$ = 43mA
- Finally, in order to confirm the assumption above, $V_{CE} = V_{CC} - I_C * R2$ = 10V - 43mA * 100Ohm = 5.7V

Since $V_{CE} > V_{CE(Sat)}$, the transistor is working in the linear mode, to confirm our assumption. Moreover, the theory calculation is very close to the PSpice simulations.

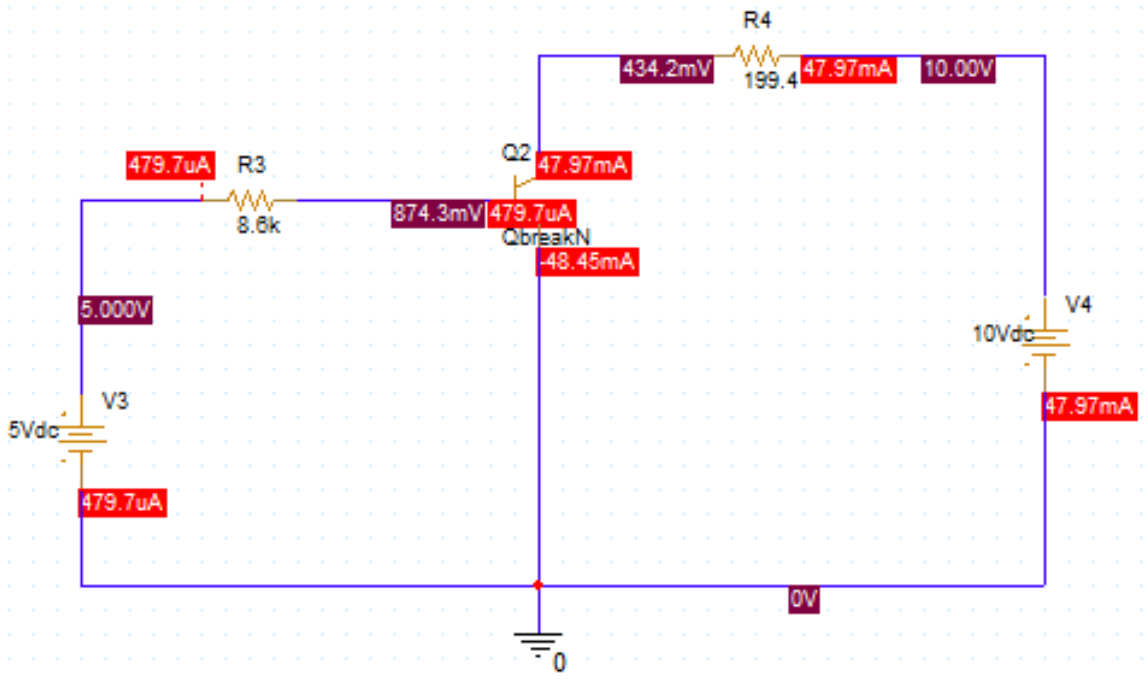


Figure 1.4: Enter Caption

3 Exercise and Report

3.1 BJT in Saturation Mode

Change the value of **R1 to 1k** and run the simulation again. Capture the simulation results and explain the values of I_B, I_C, V_{CE}. The default transistor gain is $\beta = 100$, and the saturated voltage $V_{CE(Sat)} = 0.65V$ and $V_{BE} = 0.7V$.
Your image goes here:
The results in PSpice are explained as follows:

- According to the Ohm's Law, $I_B = \frac{V_1 - V_{BE}}{R_1} = 4.3(mA)$
- It is assumed that the transistor is in linear (or active) mode, $I_C = \beta * I_B = 100 * 4.3 = 0.43(mA)$
- Finally, in order to confirm the assumption above, $V_{CE} = V_{CC} - I_C * R2 = -33(V)$

Since $V_{CE} < 0$, our assumption is not correct. The transistor stays in saturation mode. Therefore, I_C is determined as follows:

$I_C = (V_{CC} - V_{CE(Sat)})/R2 = 93.5(mA)$

3.2 DC Sweep Simulation

The schematic in the first exersice with **R1 = 1k** is re-used in this exercise. However, a DC-Sweep simulation mode is performed with V1 is varied from 0V to 5V (0.1V for the step), as follows:

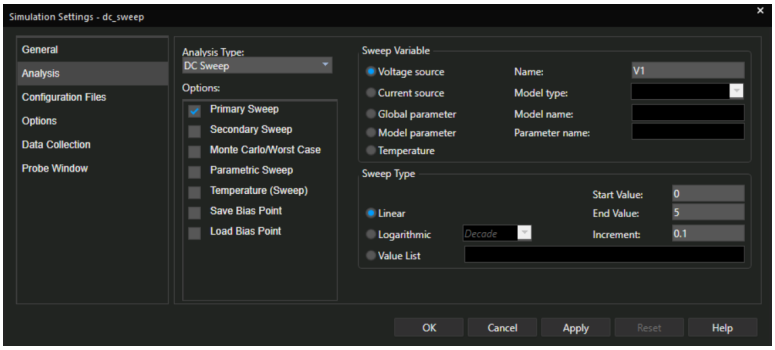


Figure 1.5: DC-Sweep profile for simulation

Run the simulation and trace for the current I_C according to the value of V1. Capture your screen and plot it in the report. Please increase the width of the curve.
Your image goes here:
6cm
When the transistor becomes saturation, the value of V1 is 1.9 (V)
At this value, the value of I_B is 978.89(μA)
And the value of $I_{C(Sat)}$ is 97.889 (mA)

3.3 BJT used as a Switch

For a given BJT circuit, determine R1 and R2 to have IC saturated at 50mA. In this saturation mode, $V_{CE(Sat)}$ is 30mV. Assume that V_{BE} = 0.7V and the current gain β = 100.

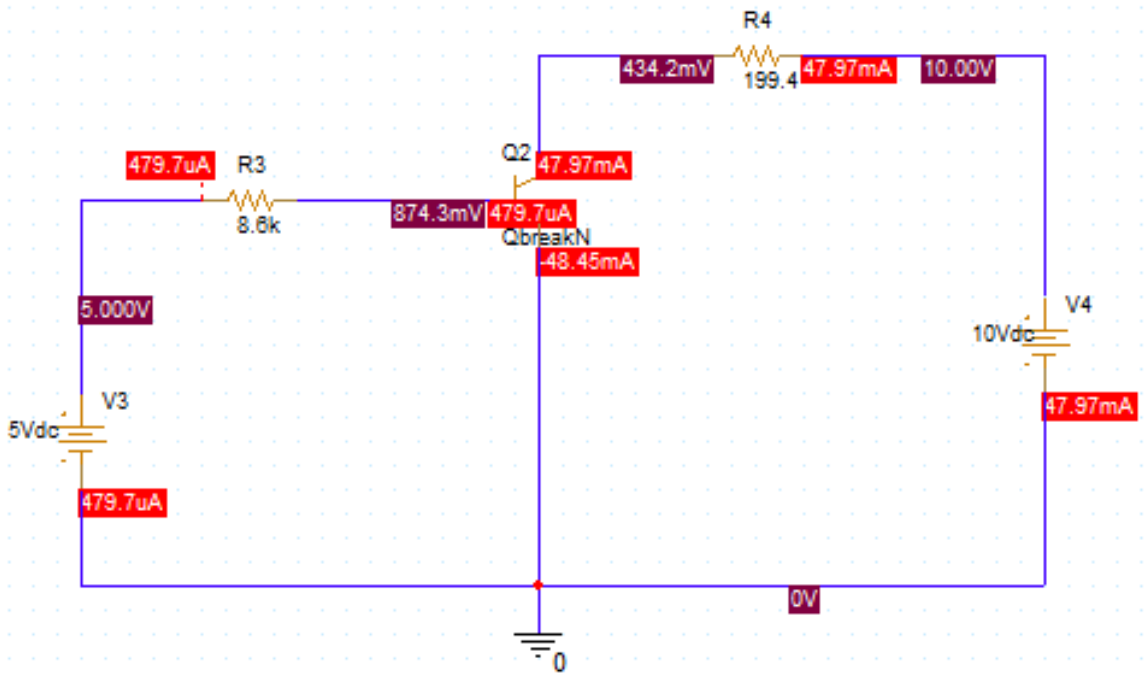


Figure 1.6: Enter Caption

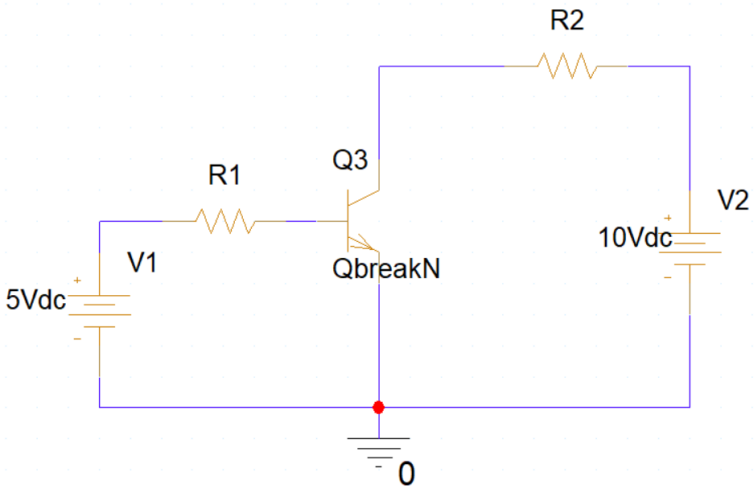


Figure 1.7: *BJT used as switch in saturation mode*

Present your solution to determine R1 and R2. Perform the simulation in PSpice to confirm the results. Capture the screen in PSpice and present in the report.
Solution
$R_2 = \frac{V_{CC} - V_{CE(sat)}}{I_C(sat)} = \frac{10-30*10^{-3}}{50*10^{-3}} = 199.4(\Omega)$

$I_B = \frac{I_C}{\beta} = \frac{50*10^{-3}}{100} = 0.5(mA)$

$R_1 = \frac{V_{BB} - V_{BE}}{I_B} = \frac{5-0.7}{0.5*10^{-3}} = 8.6(k\Omega)$

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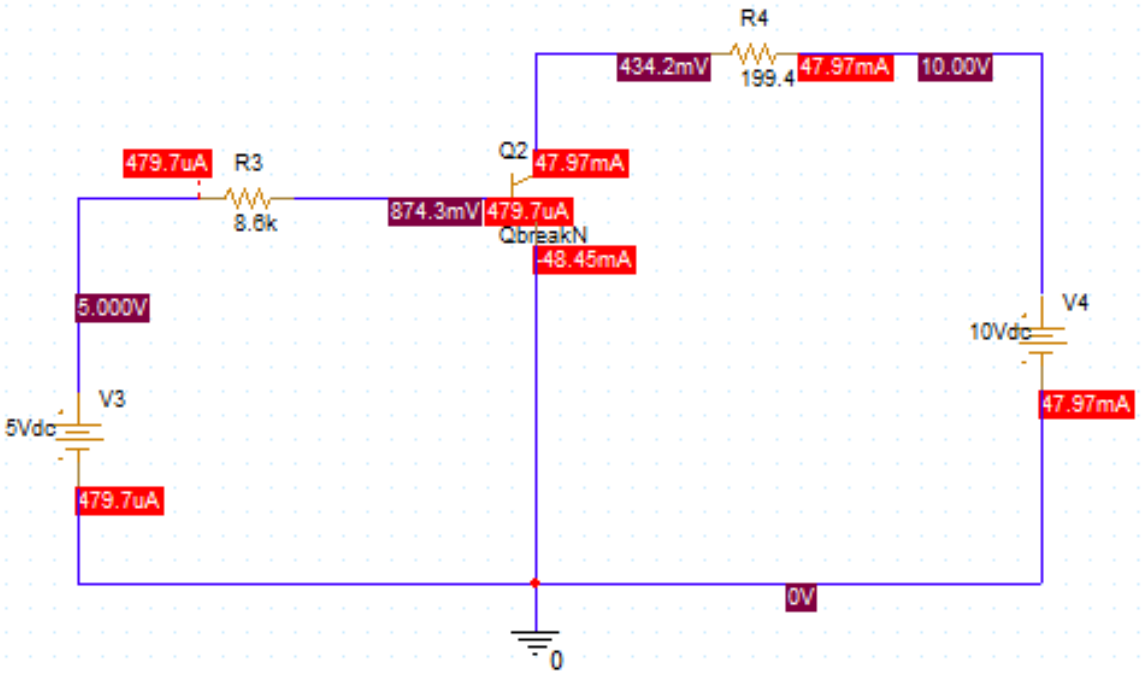

Figure 1.8: Enter Caption

3.4 Drive a device with an NPN BJT

This exercise has a $5V$ logic output (the V_{ter} in Figure 1.9) that can source up to $10mA$ of current without a severe voltage drop and stand a maximum current of $20mA$. If the logic terminal sources a current larger than $20mA$, it would be damaged. Or, if it sources a current larger than $10mA$, the V_{ter} voltage will drop to less than $4V$. We should avoid this drop in many cases. However, this logic terminal has to be used to drive an electrical component with an equivalent internal resistance of 5 ohms (the LOAD in Figure 1.9) and requires a current of at least $300mA$ and not exceeding $500mA$ to function normally. Given that we have an NPN transistor with the current gain β equals 100, the maximum I_C current is $400mA$, and the barrier potential at the BE junction is $V_{BE} = 0.7V$, select a resistor available in the market to replace the resistor R_B revealed in Figure 1.9. to make the circuit function well. After that, perform a simulation to double-check your selection.

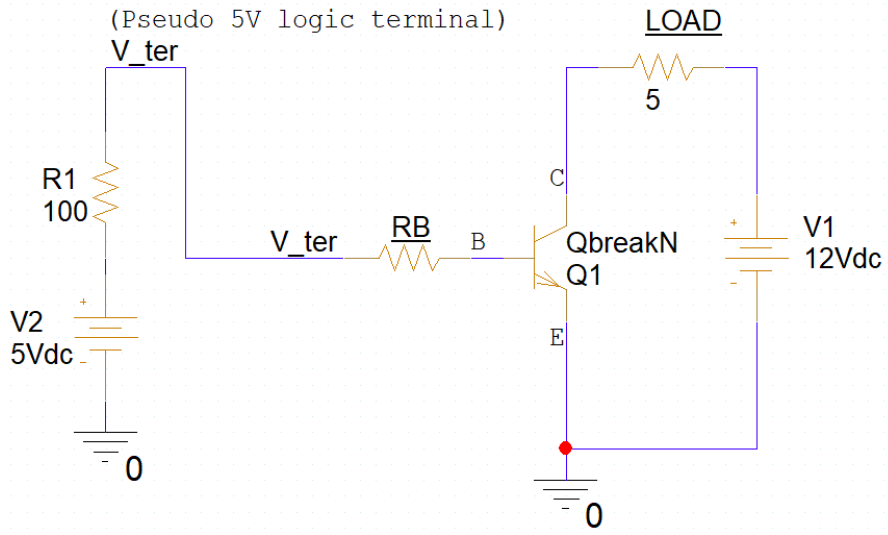

Figure 1.9: Select a resistor available in the market for R_B

3.4.1 Theory calculations

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the limits of the LOAD and the transistor, we have:

$$300\text{mA (min)} < I_C < 400\text{mA(max)}$$

$$3\text{mA (min)} < I_B < 4\text{mA(max)}$$

With $I_B(min)$ =3mA we have:

$$R_B(max) = \frac{V_{ter} - V_{BE} - V_{R1}}{I_B} = \frac{5 - 0.7 - 0.003 \cdot 100}{0.003} = 1333.33\Omega$$

With $I_B(max)$ =4mA we have:

$$R_B(min) = \frac{V_{ter} - V_{BE} - V_{R1}}{I_B} = \frac{5 - 0.7 - 0.004 \cdot 100}{0.004} = 975\Omega$$

So:

$$975\ \Omega\text{(min)} < R_B < 1333.33\ \Omega\text{(max)}$$

R_B selected: 1200 Ω

3.4.2 Simulation

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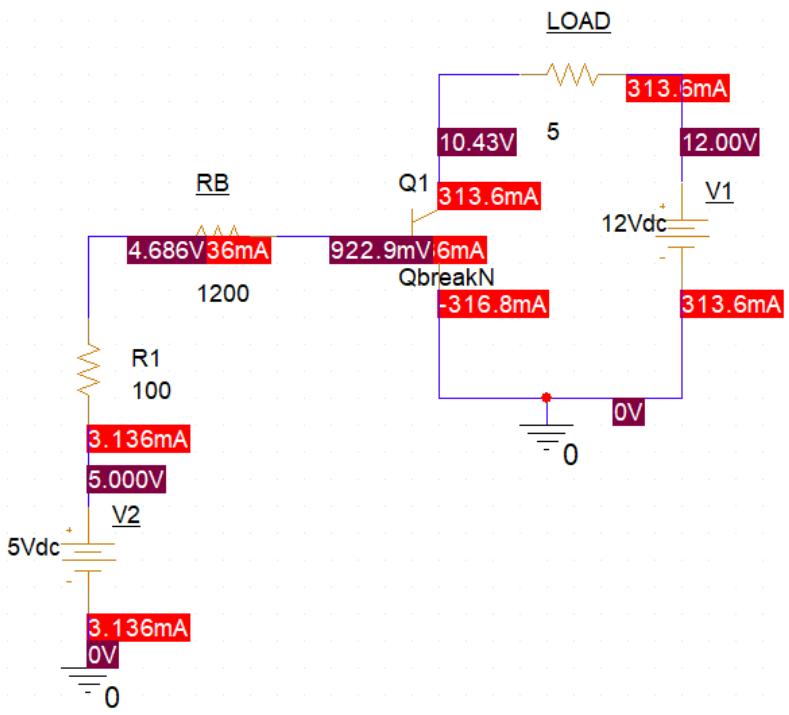

3.4.3 Compare

		Theory			PSpice		
	R_B	V_{BE}	I_B	I_C	V_{BE}	I_B	I_C
$R_B(min)$	975Ω	0.7V	4mA	300mA	927.8mV	3.788mA	378.8mA
$R_B(max)$	1333.33Ω	0.7V	3mA	400mA	920.4mV	2.846mA	284.6mA
$R_B(selected)$	1200Ω	0.7V	3.3mA	330mA	922.9mV	3.136mA	313.6mA

3.5 Simple bias configuration

The circuit given in Figure 1.10 is known as a simple kind of NPN bias configuration. First, students simulate the circuit with two values of RC, respectively 10 Ohms and 1k Ohms. Then, give your statement on the change of the current I_E and explain the phenomena.

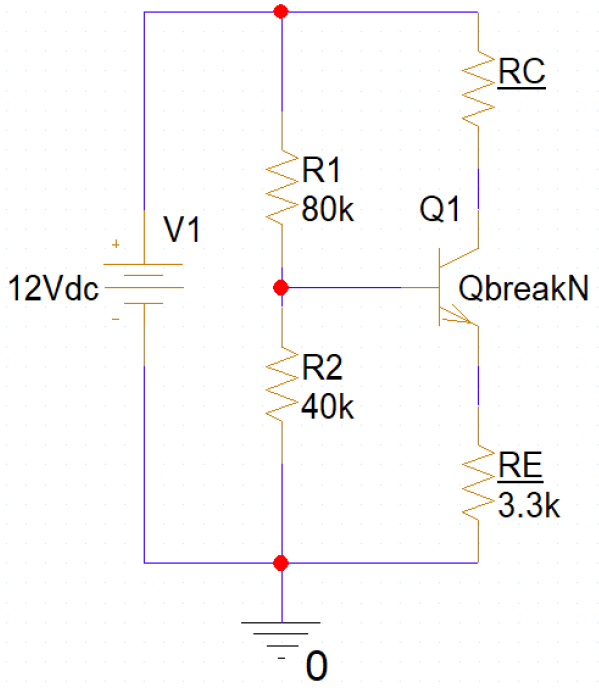

Figure 1.10: Simple bias configuration

3.5.1 Simulation

Your images go here (2 images)
Step 1: Simulate the circuit with R_C = 10 Ohms.

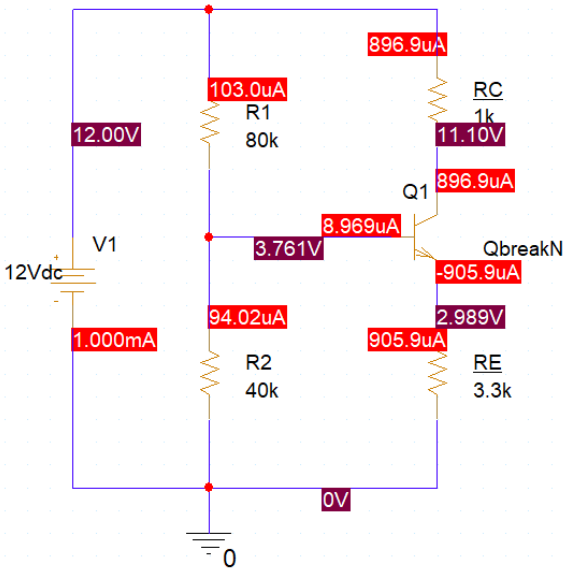

Figure 1.11: Enable Bias Current Display

Step 2: Simulate the circuit with R_C = 1k Ohms.

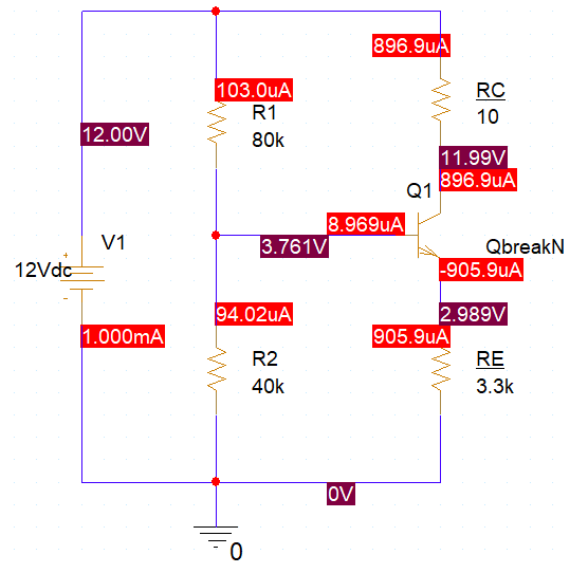

Figure 1.12: Enable Bias Current Display

3.5.2 Circuit analysis

Conduct some theoretical calculation to explain for the phenomena you have observed from the simulation.

- We have (R_1 // R_2):

$$R_{TH} = \frac{R_1 * R_2}{R_1 + R_2} = \frac{80*10^3*40*10^3}{(80+40)*10^3} = \frac{80}{3} k\Omega$$
$$V_{TH} = V_B = \frac{R_2}{R_1+R_2} * V_{CC} = \frac{40*10^3}{(80+40)*10^3} * 12 = 4V$$

- Applying Kirchhoff's voltage for Base-Emitter Loop, we have:

$$V_{TH} - I_B * R_{TH} - V_{BE} - I_E * R_E = 0$$
$$==> I_E = \frac{V_{TH}-V_{BE}}{R_E + \frac{R_{TH}}{\beta_{DC}}} = \frac{4-0.7}{(3.3+\frac{\frac{80}{3}}{100})*10^3} = 925.234 * 10^{-6} A$$

- The change in current I_E is due to the difference of V_{BE} in Pspice (0.77) and in theory (0.7), but it's not significant.

3.6 PNP Circuit

Figure 1.13 shows a very typical PNP transistor circuit. Calculate I_B, I_E, and I_C then simulate the circuit to double-check your calculation. Assume the current gain β = 100.

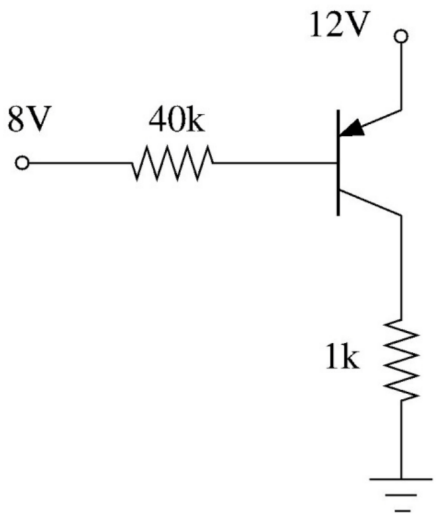

Figure 1.13: A PNP Circuit

3.6.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

V_{EB} = 0.7V

$$I_B = \frac{V_{EE} - V_{BB} - V_{BE}}{R_B} = \frac{12-8-0.7}{40000} = 82.5\mu A$$

$$I_C = \beta \cdot I_B = 100 \cdot 82.5\mu A = 8.25mA$$

$$I_E = I_C + I_B = 82.5\mu A + 8.25mA = 8.3325mA$$

3.6.2 Simulation

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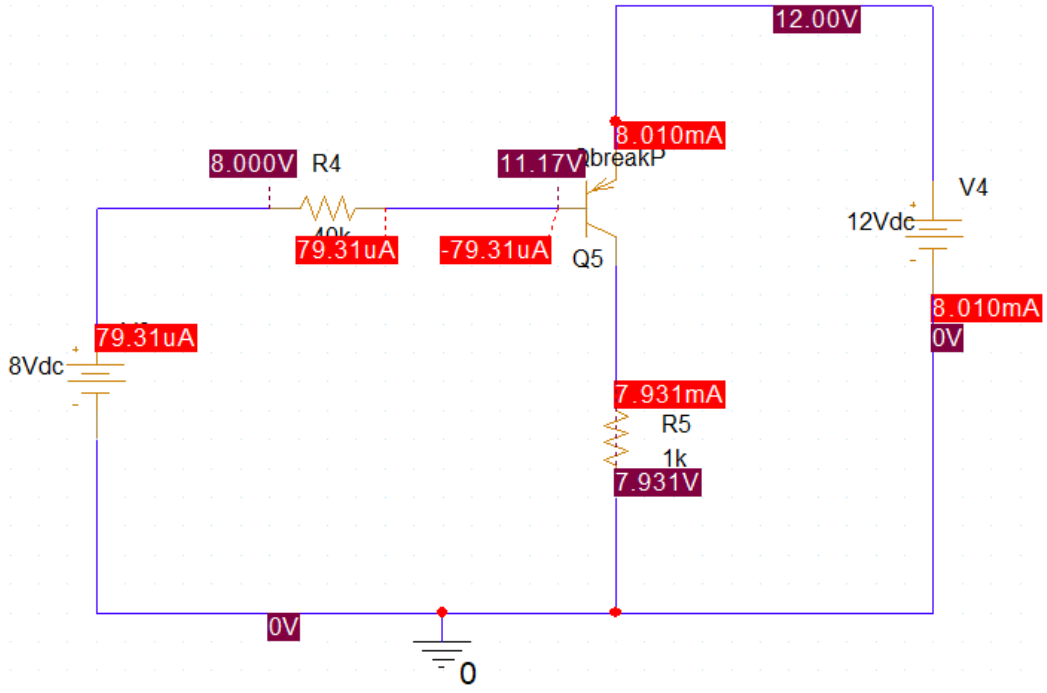


3.6.3 Comparison

I_B (In theory) = 82.5μA I_B (simulation) = 79.31μA

I_C (In theory) = 8.25mA I_C (simulation) = 7.931mA

I_E (In theory) = 8.3325mA I_E (simulation) = 8.010mA

3.7 Circuit with NPN and PNP bipolar junction transistors

Give the circuit in Figure 1.14. Calculate the Voltage at all nodes and the current in all branches. Assume the current gain of both transistors is the same at β = 100. Then perform a simulation and compare the result with the theoretical calculation.

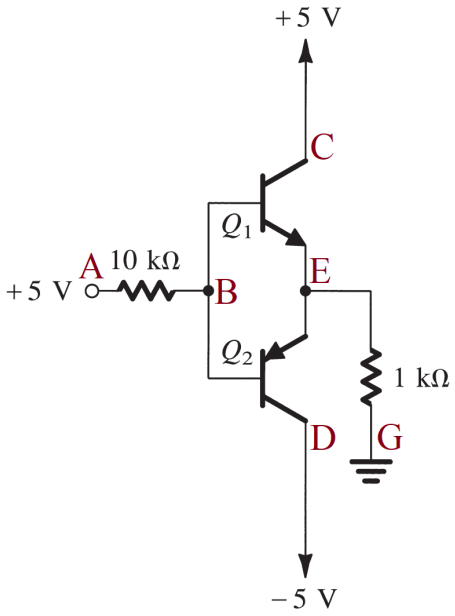


Figure 1.14: Circuit with NPN and PNP bipolar junction transistors

3.7.1 Theoretical calculation

Notes:

Explanations, formulas, and equations are expected rather than only results. We have V_E < V_B, therefore the transistor Q_2 is close.
According to the KVL, we have the following equation:
I_{BE} (hereinafter called I_B) = $\frac{V_A - V_{BE}}{R_B + (\beta+1) * R_E}$ (1)

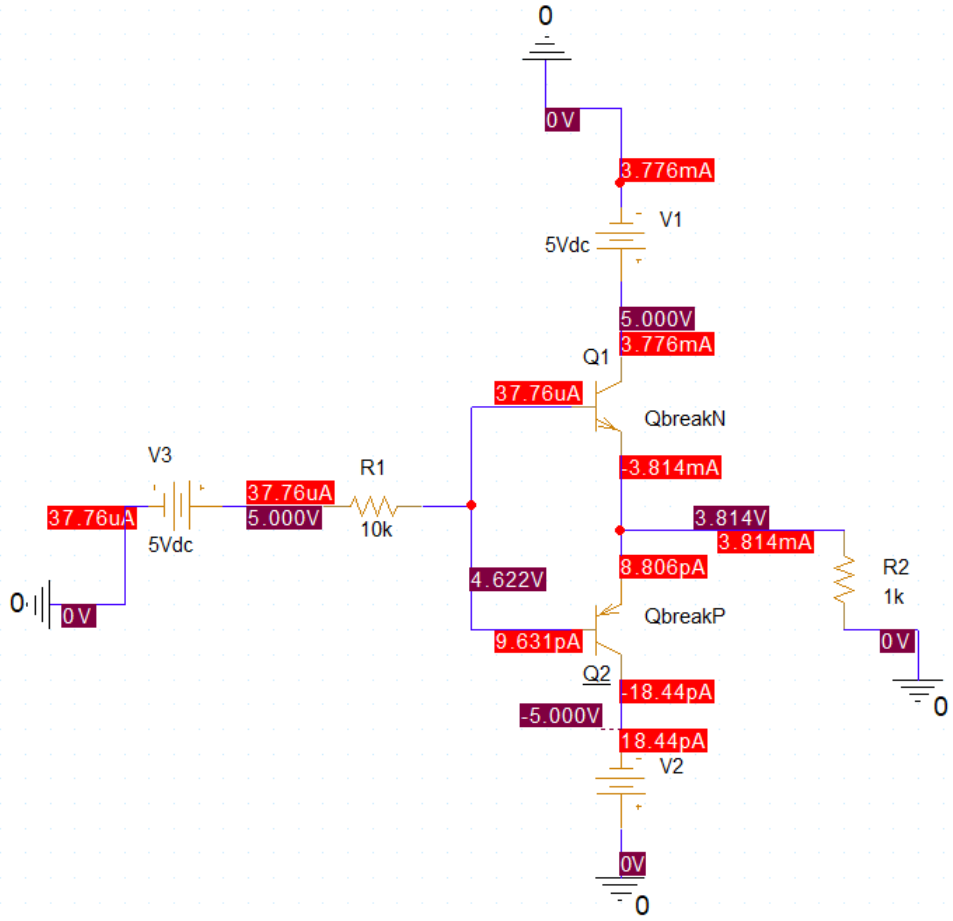
Solve (1) we have $I_B = \frac{5-0.7}{10*10^3+(100+1)*1*10^3} = 38.74 * 10^{-6} A$

$I_C = \beta * I_B = 100 * 38.74 * 10^{-6} = 3.874mA$
$I_{EG} = I_B + I_C = 38.74 * 10^{-6} + 3.874 * 10^{-3} = 3.9126mA$
$V_E = I_{EG} * R_E = 3.9127 * 1 = 3.9126V$

$$V_B = V_E + V_{BE} = 3.9126 + 0.7 = 4.6126V$$

3.7.2 Simulation

Your image goes here



3.7.3 Comparison

I_B (In theory) = 38.74μA, I_B (simulation) = 37,6μA

I_C (In theory) = 3.874mA, I_C (simulation) = 3,775mA

I_{EG} (In theory) = 3.9126mA, I_{EG} (simulation) = 3.814mA

V_E (In theory) = 3.9126V, V_E (simulation) = 3.814V

V_B (In theory) = 4.6126V, V_B (simulation) = 4.622V

3.8 NPN Circuit with E resistance

In Figure 1.15, calculate all the values of I_B, I_C, I_E, V_E, and V_C. Assume the voltage drop V_{BE} = 0.7V and the current gain coefficient of the transistor is β = 100. Then, perform a

simulation to double-check your theoretical calculations.

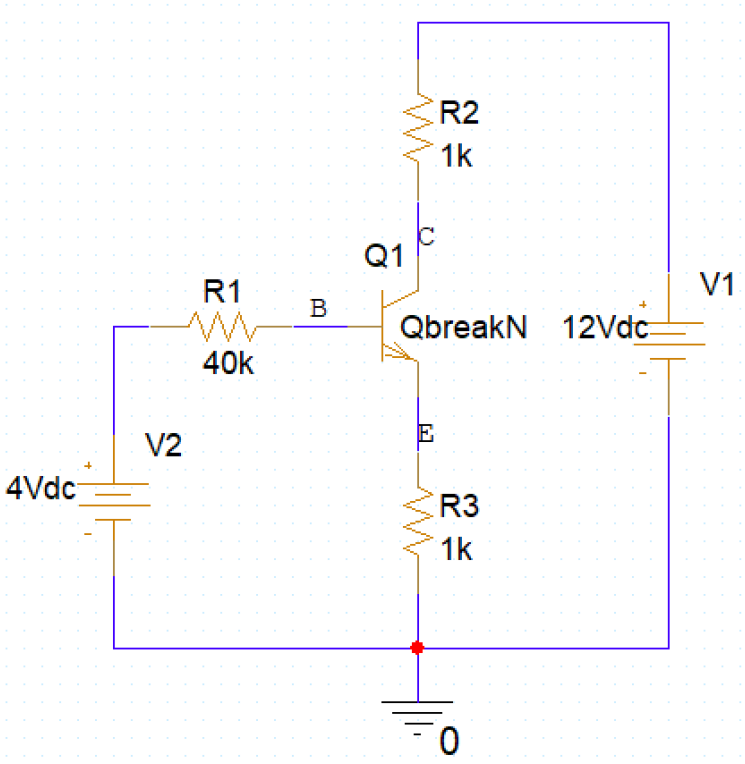


Figure 1.15: NPN Circuit with E resistance

3.8.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the Kirchhoff's voltage law, we have the following equation:

$V_B - I_B \cdot R_1 - V_{BC} - I_E \cdot R_3 = 0$ and $\beta = \frac{I_C}{I_B} \iff I_E = I_C + I_B = \beta \cdot I_B + I_B = (\beta + 1) \cdot I_B$

$\iff V_B - I_B \cdot R_1 - V_{BC} - (\beta + 1) \cdot I_B \cdot R_3 = 0$ (1)

Solve (1), we have $I_B = \frac{V_B - V_{BC}}{R_1 + (\beta+1) \cdot R_3} = \frac{4-0.7}{40000+(100+1)\cdot 1000} = 23.4 \mu A$

$I_C = \beta \cdot I_B = 100 \cdot 23.4 \mu A = 2.34 mA$

$I_E = I_B + I_C = 23.4 \cdot 10^{-6} + 2.34 \cdot 10^{-3} = 2.634 mA$

$V_E = I_E \cdot R_3 = 2.364 \cdot 10^{-3} \cdot 1000 = 2.364 V$

$V_C = V_{CC} - I_C \cdot R_2 = 12 - 2.34 \cdot 10^{-3} \cdot 1000 = 9.66 V$

3.8.2 Simulation

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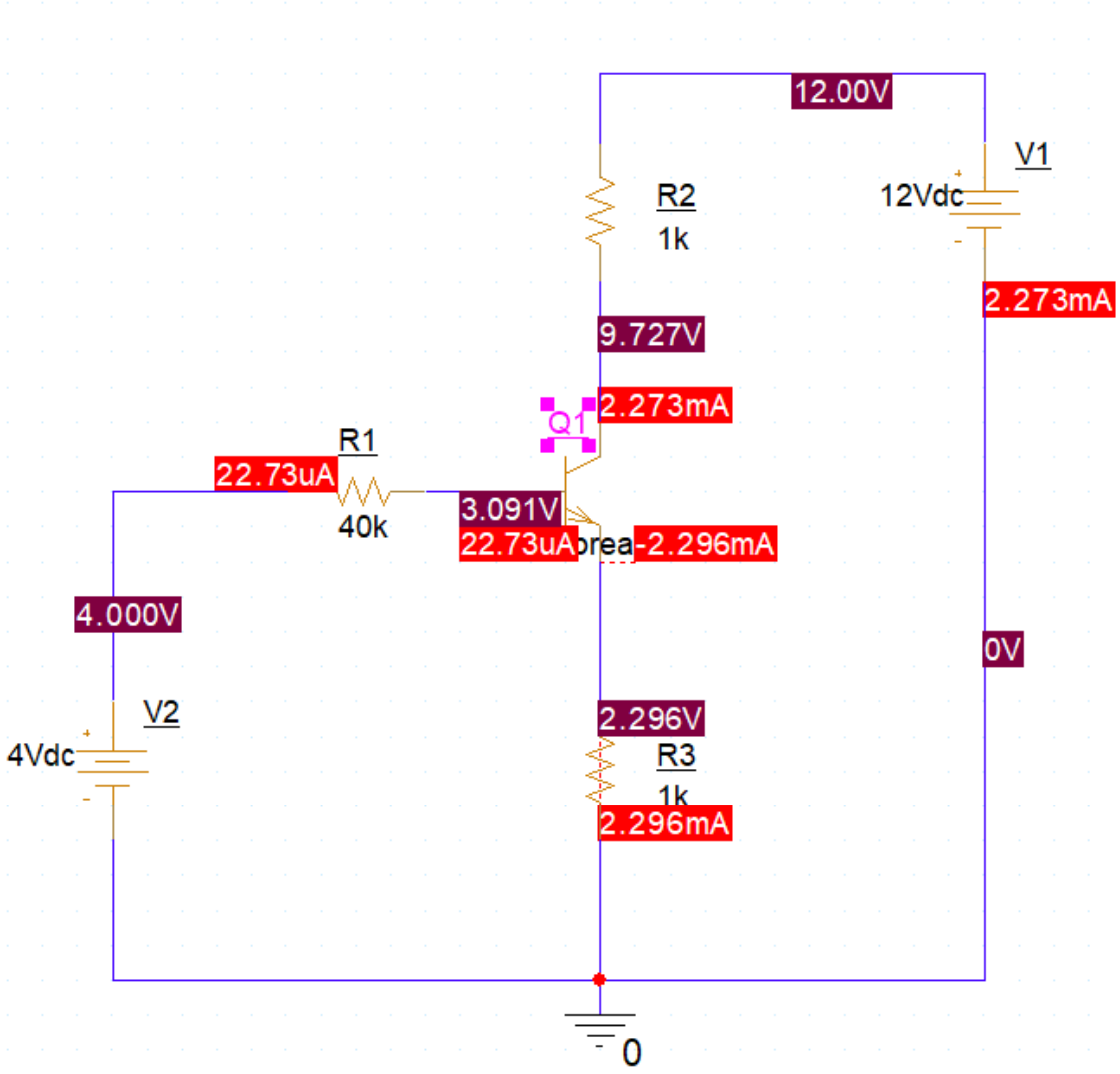

3.9 Darlington circuit

The circuit given in Figure 1.16 is known as a darlington circuit. Calculate I_{BE}, I_{AC}, I_{AL}, and the overall current gain $\frac{I_{AL}}{I_{BE}}$. After that, simulate the circuit to double-check your theoretical calculations. Assume both transistors have the same current gain coefficient $\beta = 100$.

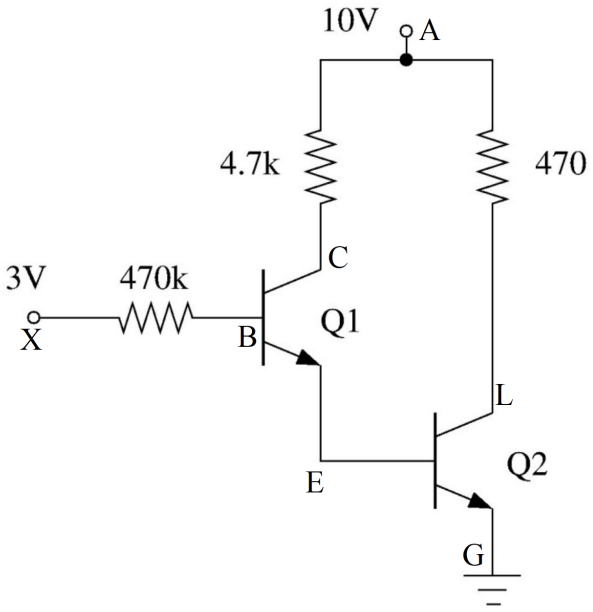

Figure 1.16: Darlington circuit

3.9.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

$I_{BE} = \frac{3-0.7-0.7}{470} = \frac{4}{1175}(mA) = 3.404(\mu A)$
$I_{AC} = \beta \times I_{BE} = 100 \times \frac{4}{1175} = \frac{16}{47}(mA) = 340.4(\mu A)$
$I_{AL} = \beta \times (I_{BE} + I_{AC}) = 100 \times (\frac{4}{1175} + \frac{16}{47}) \times 10^{-3} = \frac{202}{5875}(A)$
$U_{LG} = V_A - I_{AL} \times R_{AL} = 10 - \frac{202}{5875} \times 470 = -6.16(V)$ As $U_{LG} < 0 => Q_2$ saturated
$I_{AL} = \frac{V_{AL}}{R_{AL}} = \frac{10}{470} = \frac{1000}{47}(mA)$
$\frac{I_{AL}}{I_{BE}} = \frac{\frac{1000}{47}}{\frac{4}{1175}} = 6250$

3.9.2 Simulation

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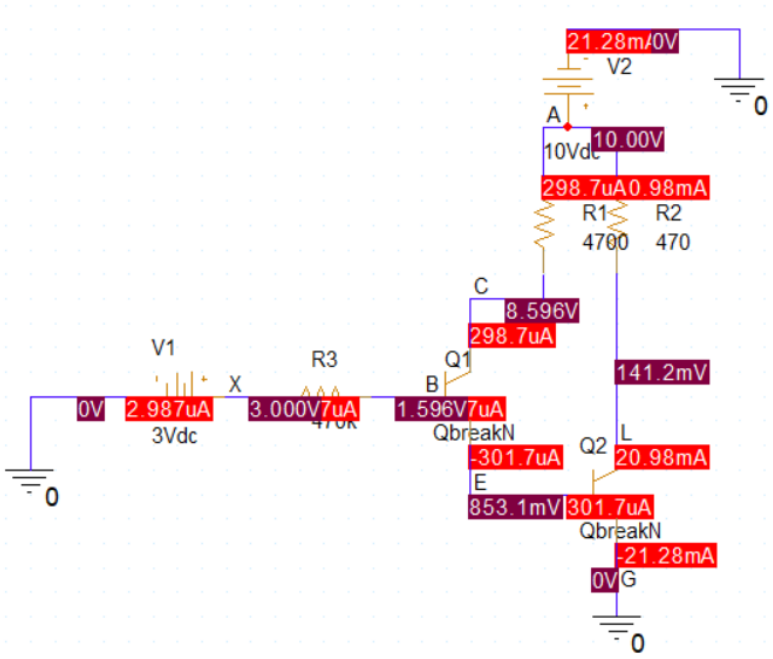


3.10 Common base

Figure 1.17 shows a bias techniques named common base bias. Calculate the values of I_E, I_B, I_C, and V_{CE}. Then simulate the circuit to double-check your theoretical calculations. Assume the current gain coefficient β = 100.

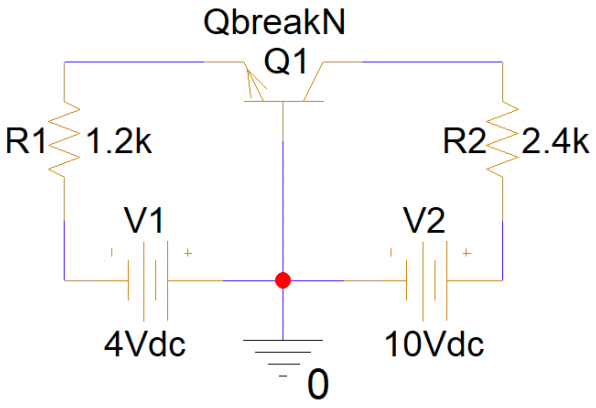


Figure 1.17: Common base

3.10.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the Kirchhoff's voltage law for Base-Emitter Loop, we have:

$-V_1 + I_E \times R_1 + V_{BE} = 0$ $I_E = \frac{V_1 - V_{BE}}{R_1} = \frac{4-0.7}{1.2\times10^3} = 2.75(mA)$

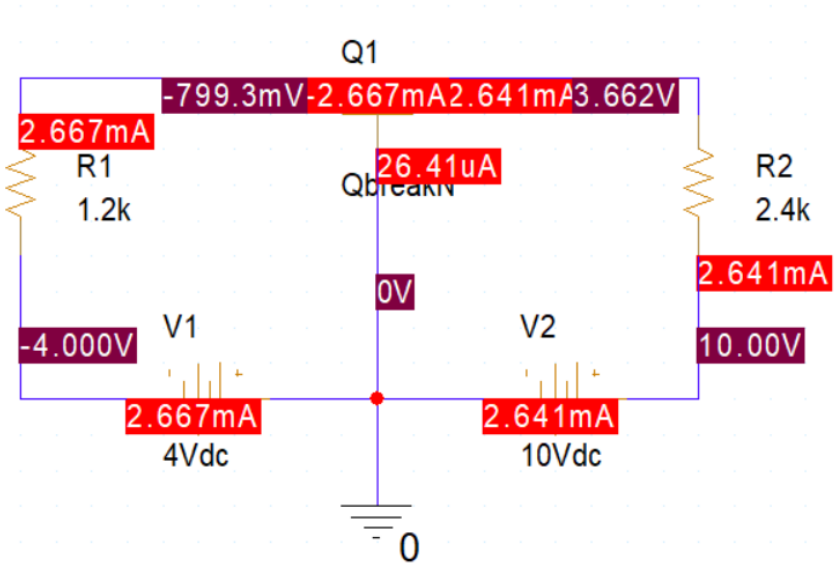
$I_B = \frac{I_E}{\beta+1} = \frac{2.75\times10^{-3}}{100+1} = \frac{11}{404}(mA) = 27.23(\mu A)$

$I_C = \beta \times I_B = 100 \times \frac{11}{404}(mA) = 2.7228(mA)$

$V_{CE} = V_1 + V_2 - I_E \times R_1 - I_C \times R_2 = 4 + 10 - 2.75 \times 1.2 - 2.7228 \times 2.4 = 4.1648(V)$

3.10.2 Simulation

Your image goes here



3.11 Current mirror

The circuit shown in Figure 1.18 is known as a current mirror circuit. First, students do some theoretical calculations to get an understanding of it. After that, perform a simulation to double-check its principles and your analysis. Assume that the two transistors Q1 and Q2, are the same type and the current gain $\beta = 100$.

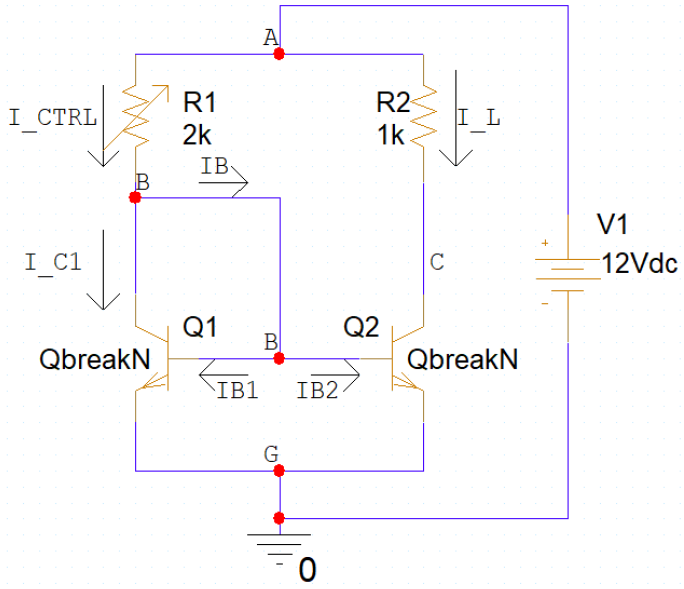


Figure 1.18: Current mirror circuit example

3.11.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the ..... we have:

I_{CTRL} = ...

I_{C_1} = ...

$I_{B_1} = I_{B_2}$ = ...

I_L = ...

3.11.2 Simulation

Your image goes here

Why is the circuit in Figure 1.18 called circuit mirror? .....

.....

Now, replace the resistor R_1 with a 100-Ohms one. Next, calculate all the values again. Then, finally, simulate the new circuit and explain the phenomena you've observed.

I_{CTRL} = ...

I_{C_1} = ...

$I_{B_1} = I_{B_2}$ = ...

I_L = ...

The 2nd simulation result goes here:

What is the phenomena?

.....

Explain:

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3.12 BJT's logic gate application

Figure 1.19 describes a straightforward NOT gate theoretical implementation using an NPN bipolar junction transistor. In the circuit, the NPN junction transistor operates in the saturation mode.

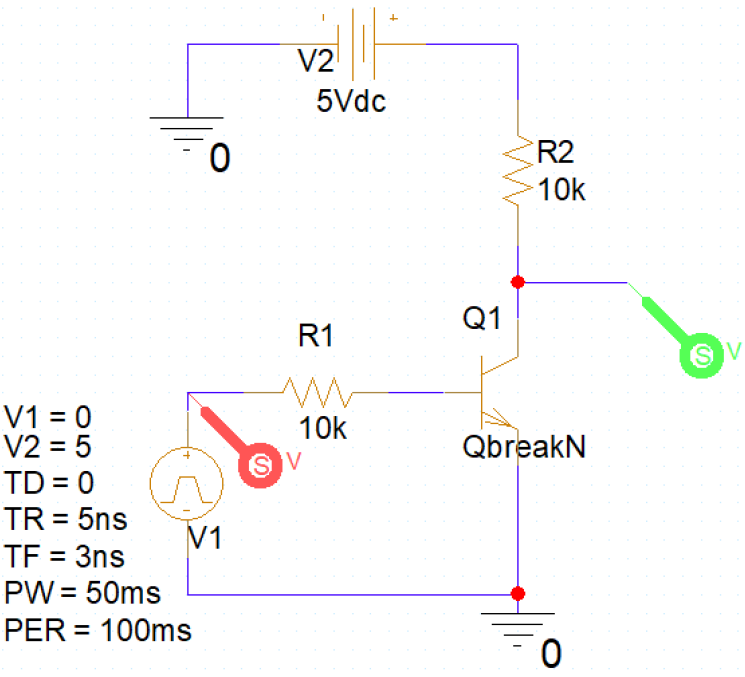

Figure 1.19: NPN theoretical NOT gate

V1 = 0 When the source is off, the voltage would be 0V.
V2 = 5 When the source is on, the voltage would be 5V.
TD = 0 Delay time. This exercise assumes that there is no delay.
TR = 5ns The rise time of the pulse (from off to on stage).
TF = 3ns The fall time of the pulse (from on to off stage).
PW = 50ms Pulse width: The time in which the source keeps on.
PER = 100ms The period of the signal.

Tips:

To get the Voltage Pulse Source component in the PSpice for TI, go to ***Place -> Pspice Compoment... -> Source -> Voltage Sources -> Pulse.***

3.12.1 Simulation

Your image goes here

But, wait! How large is the maximum current this NOT gate can source? Of course, it cannot exceed 5V/10kOhm. How tiny it is! So, what if we want to use it to drive an LED? Just put an additional 220 Ohm resistor in parallel with the existing 10k one. And in this case, the 10k resistor is quite useless. Therefore, in many cases, people let the collector pin of the transistor open. This design is called open-collector output, as shown in Figure 1.20.

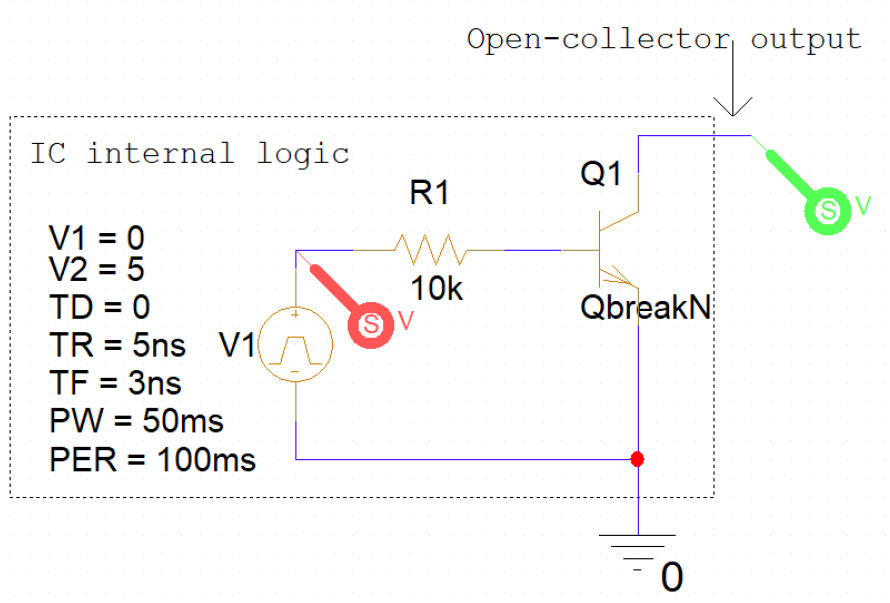

Figure 1.20: Open-collector output example

But, with this design, the input of another IC can't read the voltage of this output. Because without a pull-up resistor, the voltage V_C is floating. To read this voltage, the users have to pull it up using a resistor. There advantage here is to let the users choose the value of the pull-up resistor as their desire.

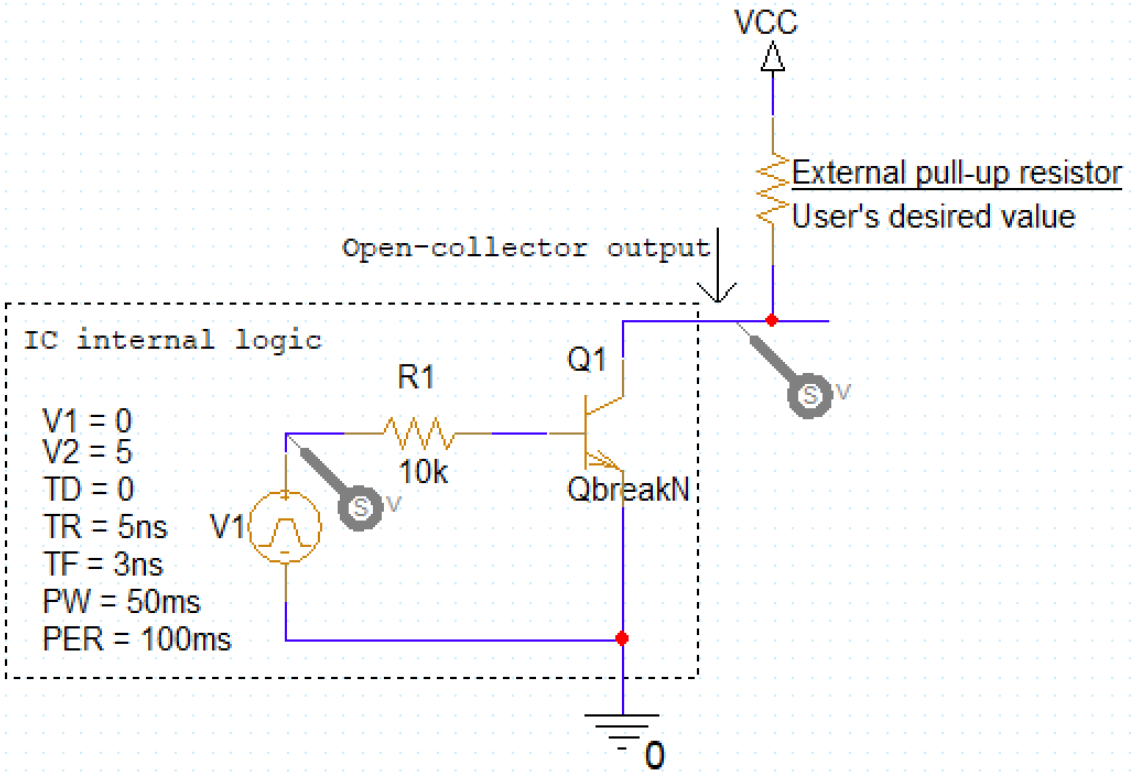

Figure 1.21: External pull-up resistor whose value selected by the users

By the side, the open-collector design manner gives an exciting way of the use of these outputs, as shown in Figure 1.22. The open-collector wired output is at the LOW level if one of the elements is LOW and is HIGH only when all the elements output HIGH.

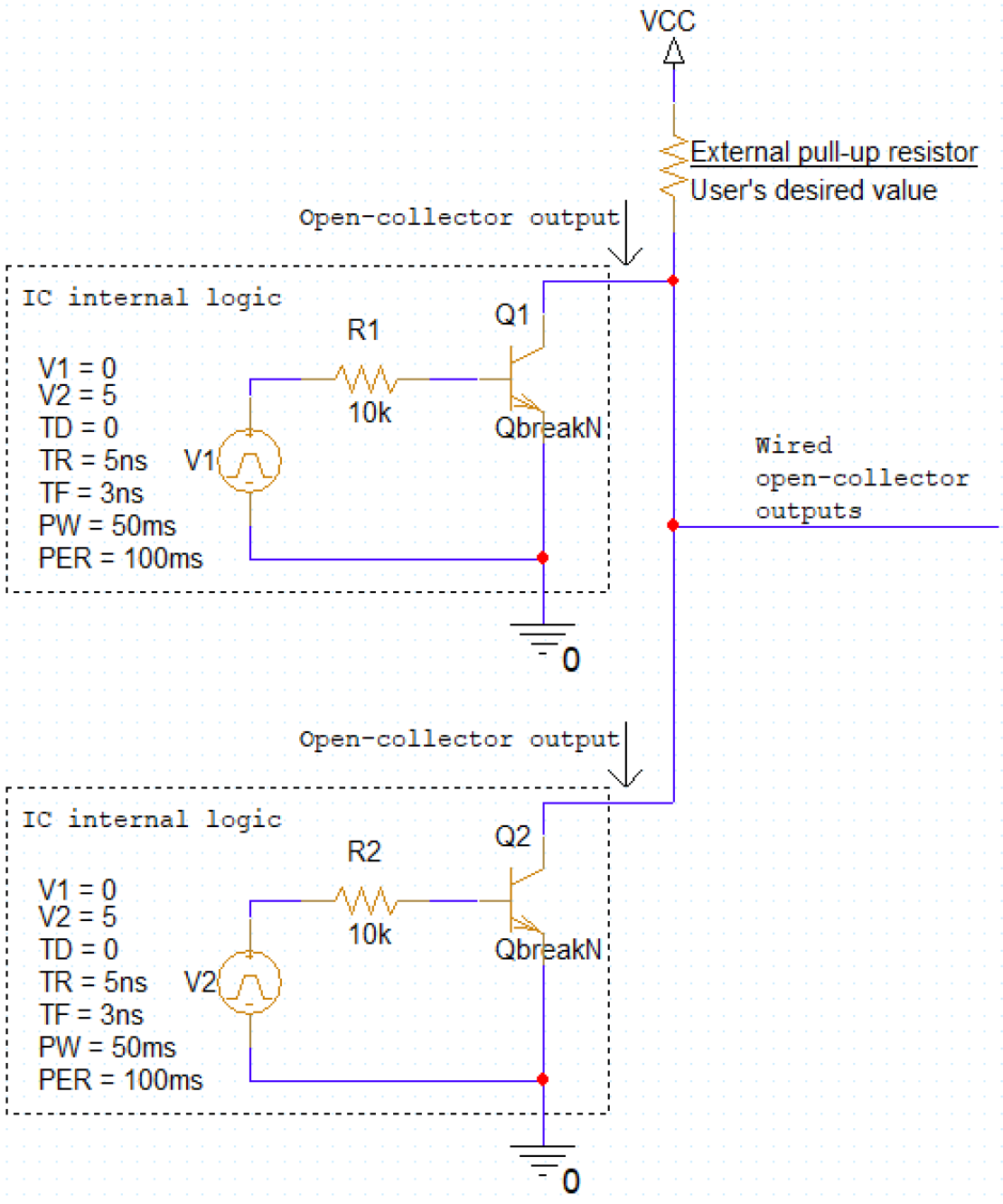

Figure 1.22: Wired open-collector outputs

3.13 Opto

The element OK_1 in Figure 1.23 is an optocoupler, which includes a light-emitting diode (LED) and a photodiode. The photodiode's conductivity depends on the intensity of the light emitted by the LED, and of course, depends on the current intensity through the LED. When the voltage across the LED is lower than its barrier potential, the Opto is cut-off. When there is current through the LED, the Opto is in the transfer mode. Like the current gain β of a BJT, the Opto also has the current transfer ratio (CTR). Assume the LED has its own barrier potential V_F = 1.7V, and the Opto has the CTR = 2. Calculate the voltage V_{OUT} when the switch is closed. Finally, give your idea about what we may use an Opto for, and how to use it?

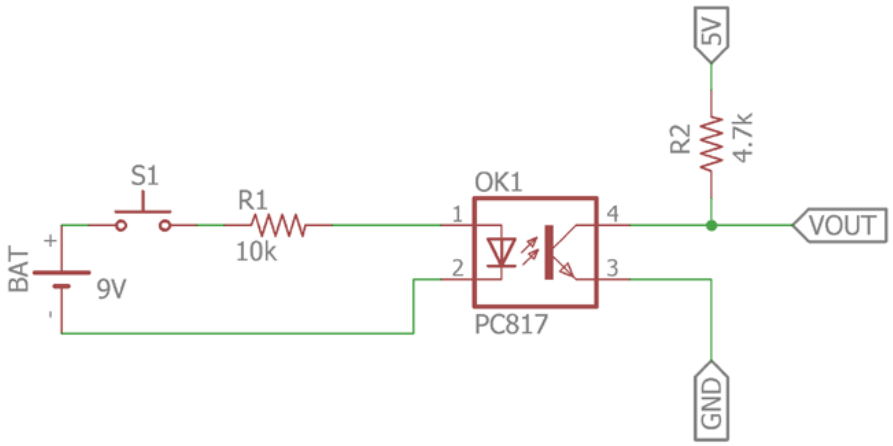

Figure 1.23: Voltage isolation with opto

$I_F = I_{R_1} =$ .....

$I_{R_2} =$ .....

$V_{OUT} =$ .....

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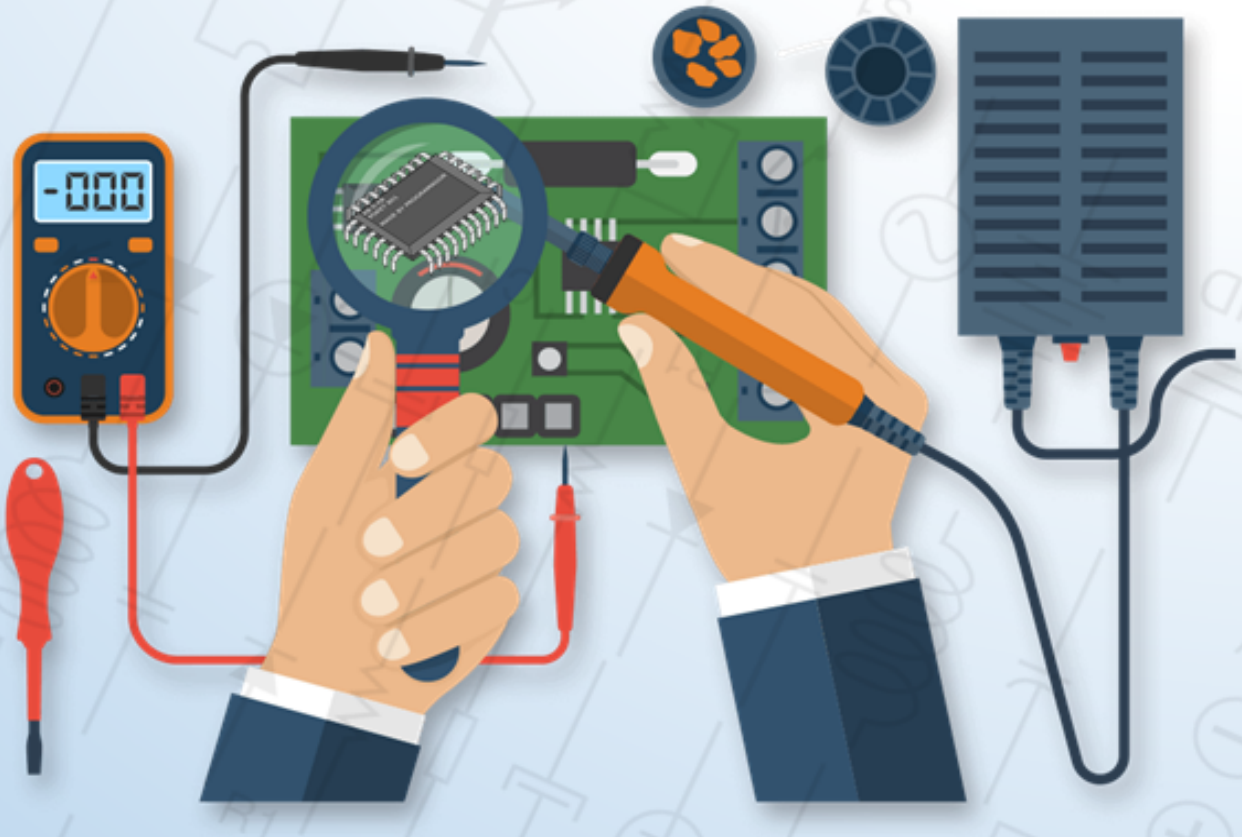
COMPUTER ENGINEERING

Electronic Device Component



Dr. Le Trong Nhan

Contents

CHAPTER 1

Circuit Design with Altium Designer

1 Introduction

Altium Designer is an electronic design automation software package for printed circuit board (PCB), FPGA and embedded software design, and associated library and release management automation. A Printed Circuit Board (PCB) mechanically supports and electrically connects electric components using conductive tracks, pads and other features etched from copper sheets laminated onto a non-conductive substrate.

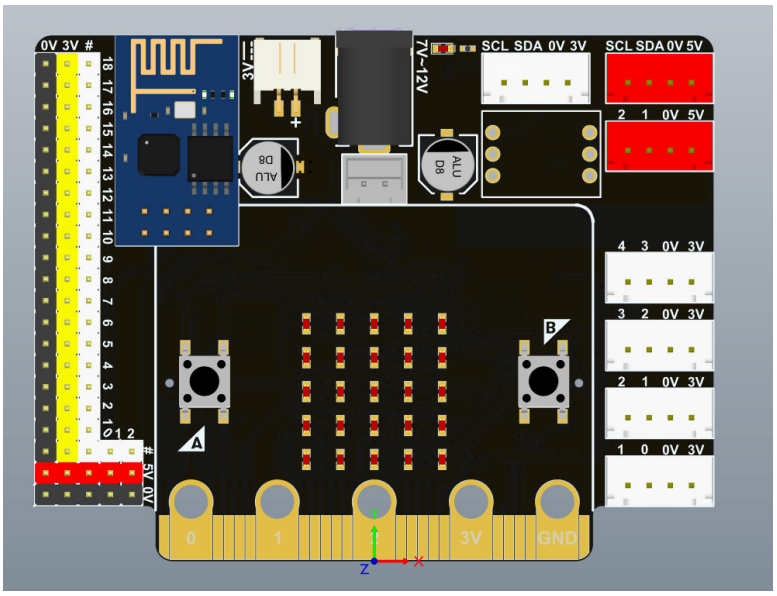


Figure 1.1: *PCB circuit in Altium Designer*

In this lab, two different voltage regular circuits are designed in Altium, based on IC 7805 and LM2596. **The manuals are provided by videos**.

2 Voltage Regulator using 7805

Voltage regulator like IC7805 belongs to the 78xx series ICs. In the 78xx series, xx represents the fixed output voltage value and 7805 is a fixed linear voltage regulator. Batteries provide a voltage of 1.2V, 3.7V, 9V, and 12V. This voltage is good for the circuits which voltage requirements are in that range. The regulated power supply in this regulator is +5V DC.

The 7805 voltage regulator is a three-terminal voltage regulator IC. In various applications, a 7805 voltage regulator with a fixed output voltage is used. The availability of this is through various packages like SOT-223, TO-263, TO-220, and TO-3. Among this, TO-220 is the most used one. The pin diagram of 7805 voltage regulator IC and its description are explained bellow:

- **Pin1 - Input**: This is an input pin and the voltage range should be between 7V to 35V. an unregulated voltage is applied to this input pin for regulation. The pin will receive its maximum efficiency at 7.2V input.
- **Pin 2 - Ground**: Pin2 is the ground pin, it means the ground is connected to this pin. Input and output are common to it.

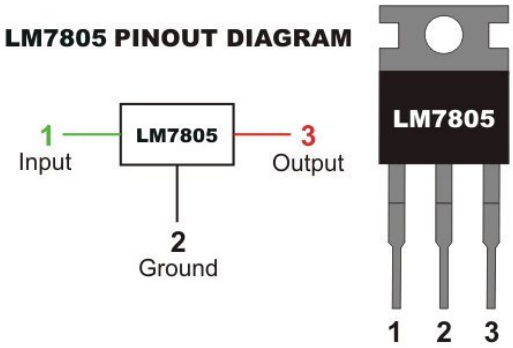


Figure 1.2: LM7805 Pin Out

- **Pin 3 - Output**: Pin3 is the output pin, where the regulated output is taken by this pin. It is about 5V(4.8V to 5.2V)

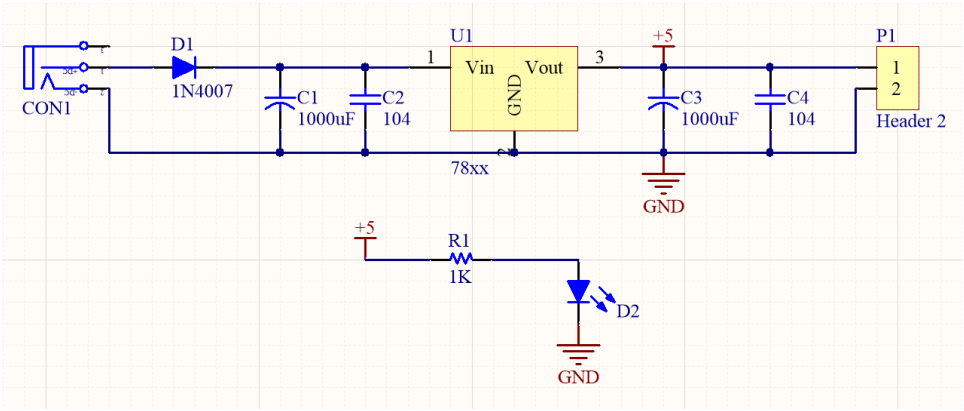


Figure 1.3: Voltage regulator using 78xx schematic in Altium Designer

The basic circuit of 7805 is very simple. It just needs two capacitors if the input is unregulated DC voltage, even the two capacitors used are also not mandatory. This 7805 circuit is capable of upholding fixed output voltage even if some changes take place in input voltage.

The manual for this circuit is posted at the link bellow:

https://www.youtube.com/watch?v=mSEBrma5MNM

2.1 Schematic design

Students are proposed to capture the schematic design in Altium Designer and place the image in this part.

Some hot keys are normally used in the schematic is the space bar, X(horizontal mirror), Y (vertial mirror) and Ctrl + W (place a wire).

Your image goes here

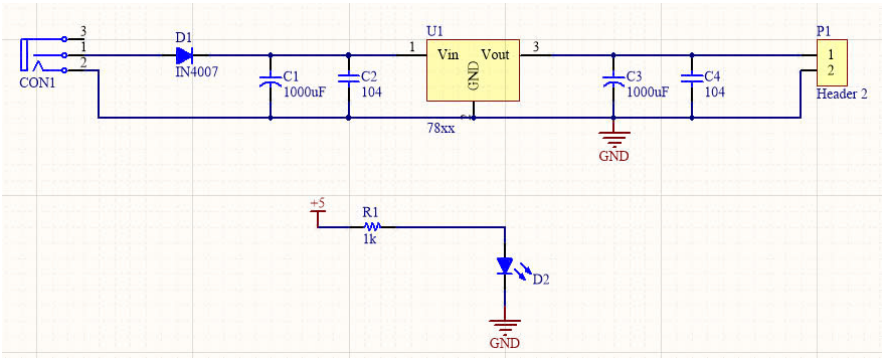


Figure 1.4: Voltage regulator using 7805 schematic in Altium Designer

2.2 PCB layout

Similarly to the schematic, some snap shorts of for the TOP, BOTTOM layers are required in this report. Moreover, several 3D images of your schematic are also required.

A manual video can be found at:

https://www.youtube.com/watch?v=PW_QQpoODDk

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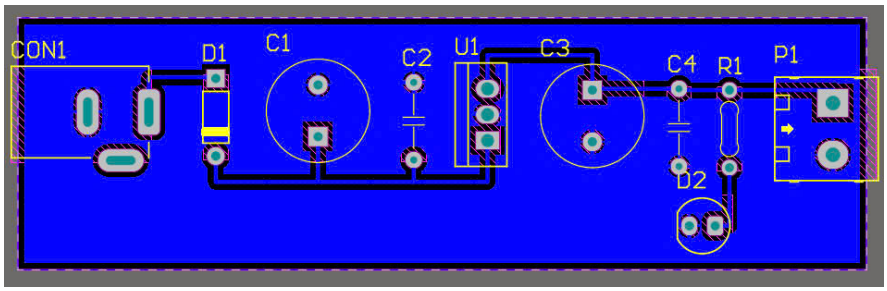

Figure 1.5: Voltage regulator using 7805 bottom layer in Altium Designer

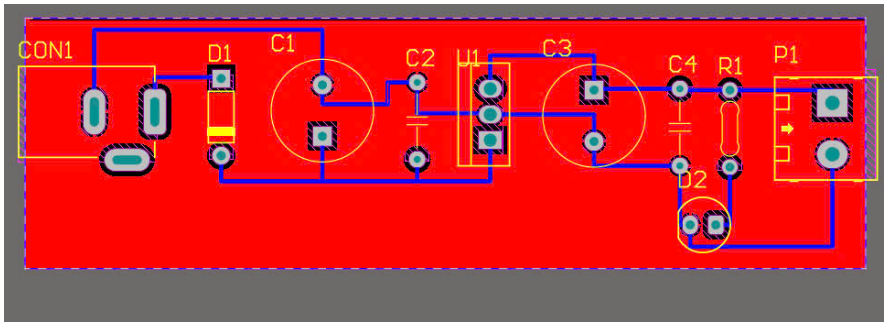

Figure 1.6: Voltage regulator using 7805 top layer in Altium Designer

3 Volatage Regulator using LM2596

LM2596 is a voltage regulator mainly used to step down the voltage or to drive load under 3A. It is also known as DC-to-DC power converter or buck converter which is used to step

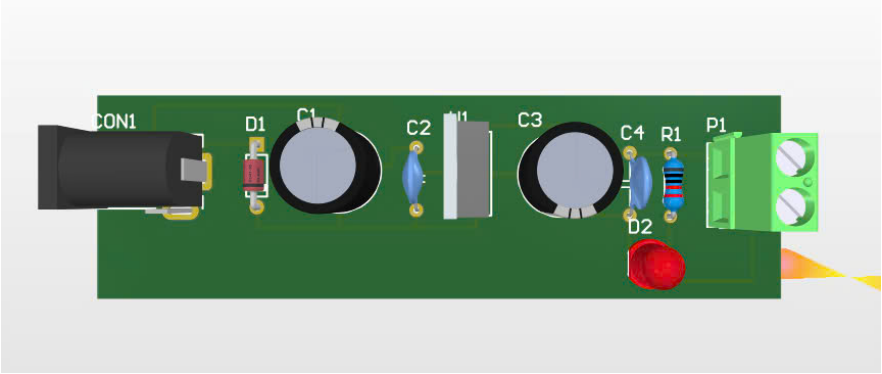

Figure 1.7: *Voltage regulator using 7805 3D image in Altium Designer*

down the voltage from its input supply to the output load. The current goes up during this voltage step down process.

LM2596 comes with a remarkable load and line regulation. It is available in both versions: fixed output voltage version with 3.3V, 5V, 12V, and customized output version where you can choose the output as per your requirement. This regulator is incorporated with a fixed-frequency oscillator and an internal frequency compensation method.

The typical connection for LM2596 is proposed by Texas Instrument (TI), as following:

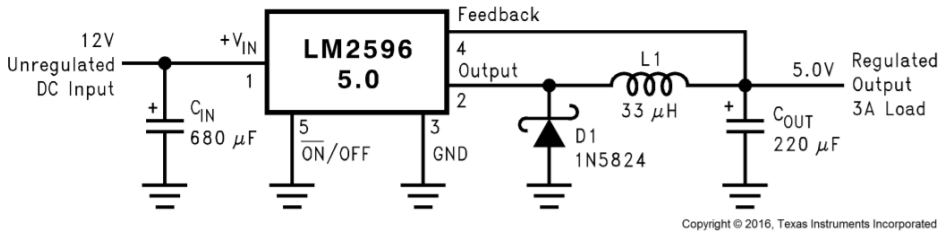

Figure 1.8: *Typical connection for LM2596*

This circuit is simulated in PSpice in previous lab, and is implemented in Altium Design in this lab. The introduction of this circuit is presented in the video bellow:

https://www.youtube.com/watch?v=57Ra92p3C0k

3.1 Schematic design

Students are proposed to capture the schematic design in Altium Designer and place the image in this part.

Some hot keys are normally used in the schematic is the space bar, X(horizontal mirror), Y (vertial mirror) and Ctrl + W (place a wire).

The manual is posted in this link:

https://www.youtube.com/watch?v=DGiHsGWPyYw

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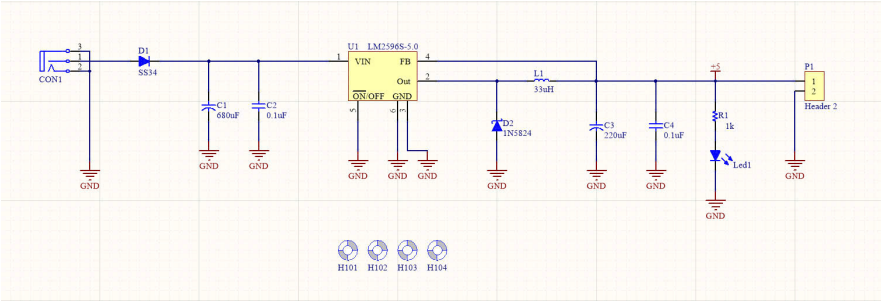

Figure 1.9: Voltage regulator using LM2596 schematic in Altium Designer

3.2 PCB layout

Similarly to the schematic, some snap shorts of for the TOP, BOTTOM layers are required in this report. Moreover, several 3D images of your schematic are also required.

The manual is posted in this link:

https://www.youtube.com/watch?v=WXszMiTSGPo

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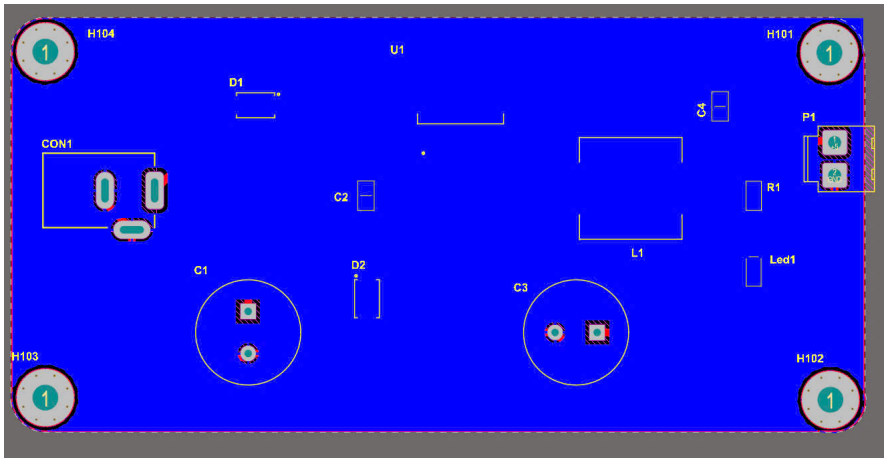

Figure 1.10: Voltage regulator using LM2596 bottom layer image in Altium Designer

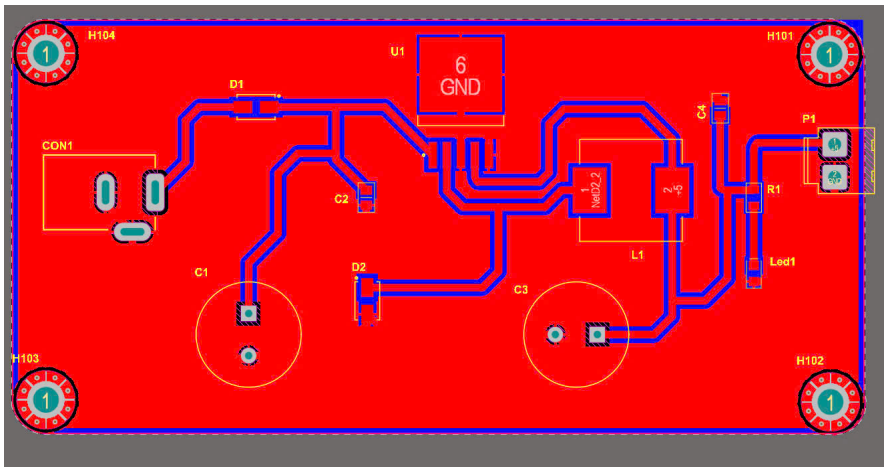

Figure 1.11: Voltage regulator using LM2596 top layer in Altium Designer

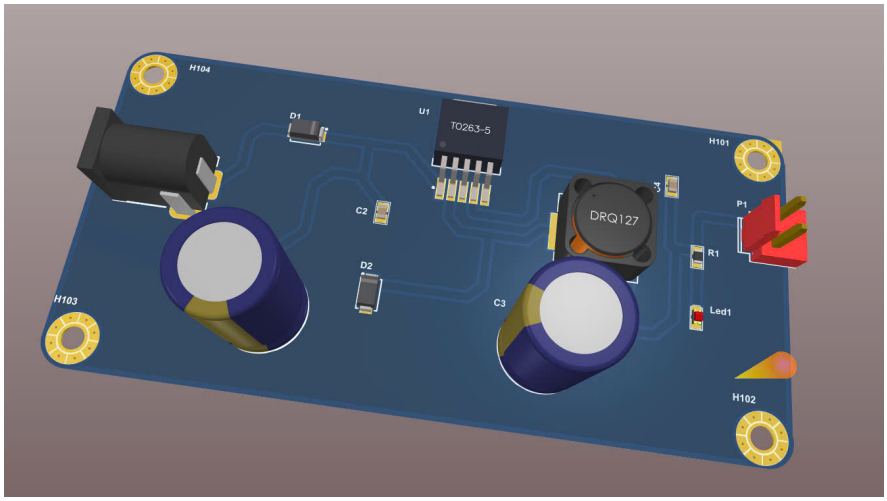

Figure 1.12: Voltage regulator using LM2596 3D image in Altium Designer