VIETNAM NATIONAL UNIVERSITY HO CHI MINH CITY

HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY

FACULTY OF COMPUTER SCIENCE AND ENGINEERING

LAB_1 REPORT

CLASS CC01 – GROUP 1

SUBJECT:

LOGIC DESIGN

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2 Exercises

2.1 Exercise 1

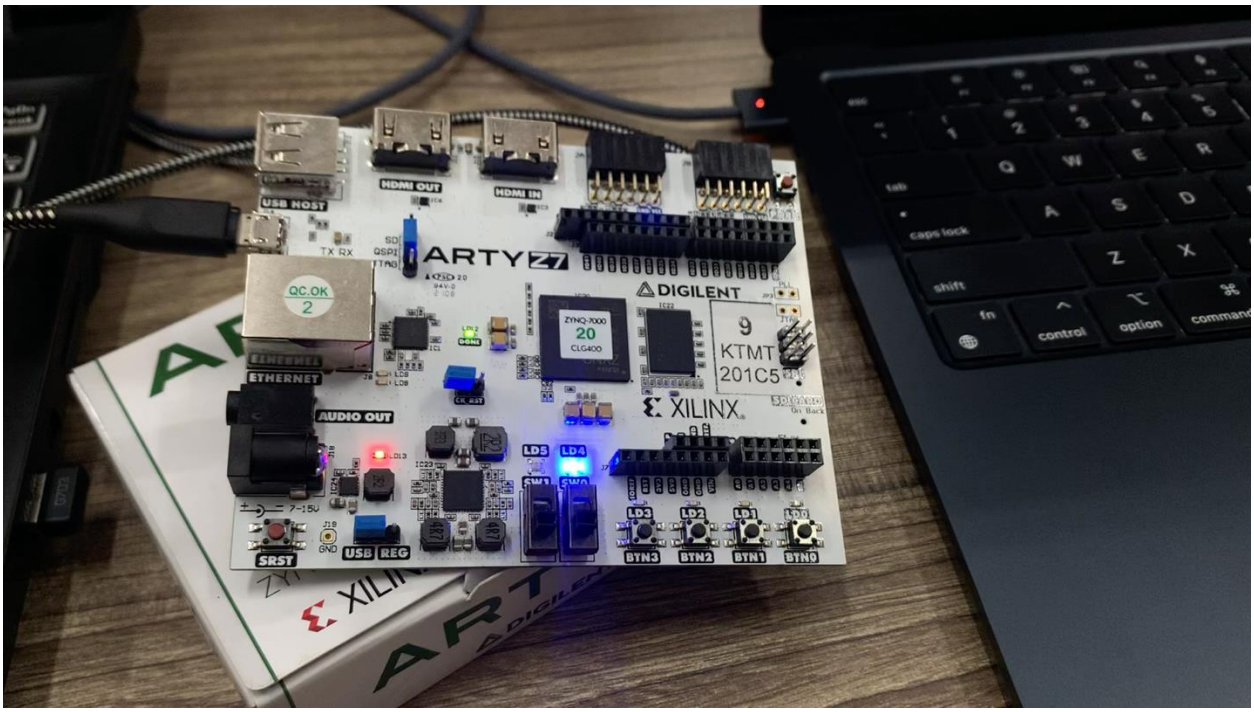
Clock Frequency Divider Police Siren: Design a circuit that generate a 1 Hz output signal using Behavioral Model. This signal is connected to 2 RGB LEDs (1 displays the blue color, 1 display the red color) on Arty-Z7 FPGA Board to make it blink interleave with each other (turn on for 0.5s - turn off for 0.5s). Know that the input clock frequency is 125 MHz. Write test benches to simulate the circuits. Test the circuits on FPGA board using LEDs and RGB LED:

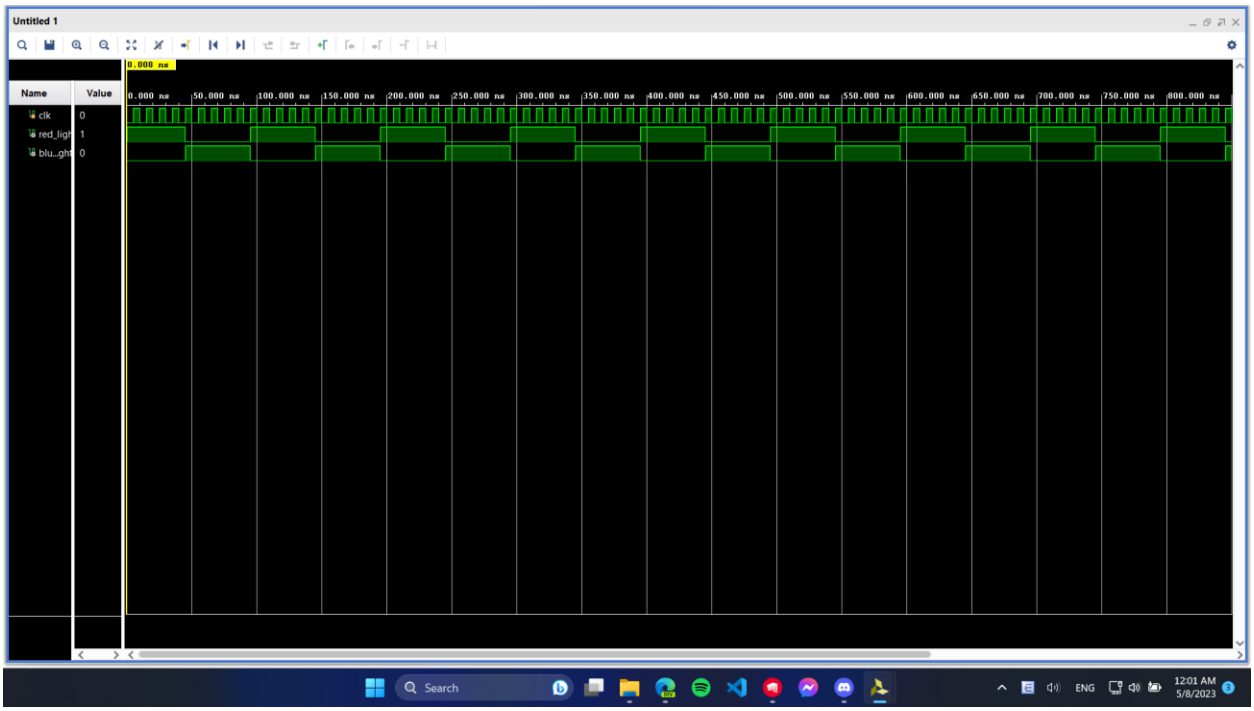
```
`timescale 1ns/1ps

module work_space(clk,blue_light,red_light);

input clk;

input clk;

output   blue_light,red_light;

reg [30:0]cnt =0;

always @(posedge clk) begin

if (clk ==1) cnt <=  cnt + 1;

if (cnt == 9)

cnt <=0 ;

end

assign red_light = (cnt < 5)?1:0;

assign blue_light = (cnt <5 )?0:1;
```

endmodule

TEST BENCH:

```
`timescale 1ns / 1ps

module lab3_tb();

    reg clk;

    wire red_light,blue_light;

    initial begin

    forever #5 clk = ~clk;

    end

    initial begin

    clk = 0;

    end

    work_space somthing(clk,blue_light,red_light);

endmodule
```





2.2 Exercise 2

a. Edge Detection circuit. a. Design a Rising Edge Detection circuit. This circuit will use at least 2 flip-flops. The behavior of the circuit is similar to the waveform in Figure 1. Assume that the in signal's HIGH levels last equal to or longer than a clock cycle. The output is active HIGH in 1 cycle of clock when a rising edge occurs in input signal. Delay is within 0-2 clock cycles.

Write RTL code and test benches to simulate the circuit:

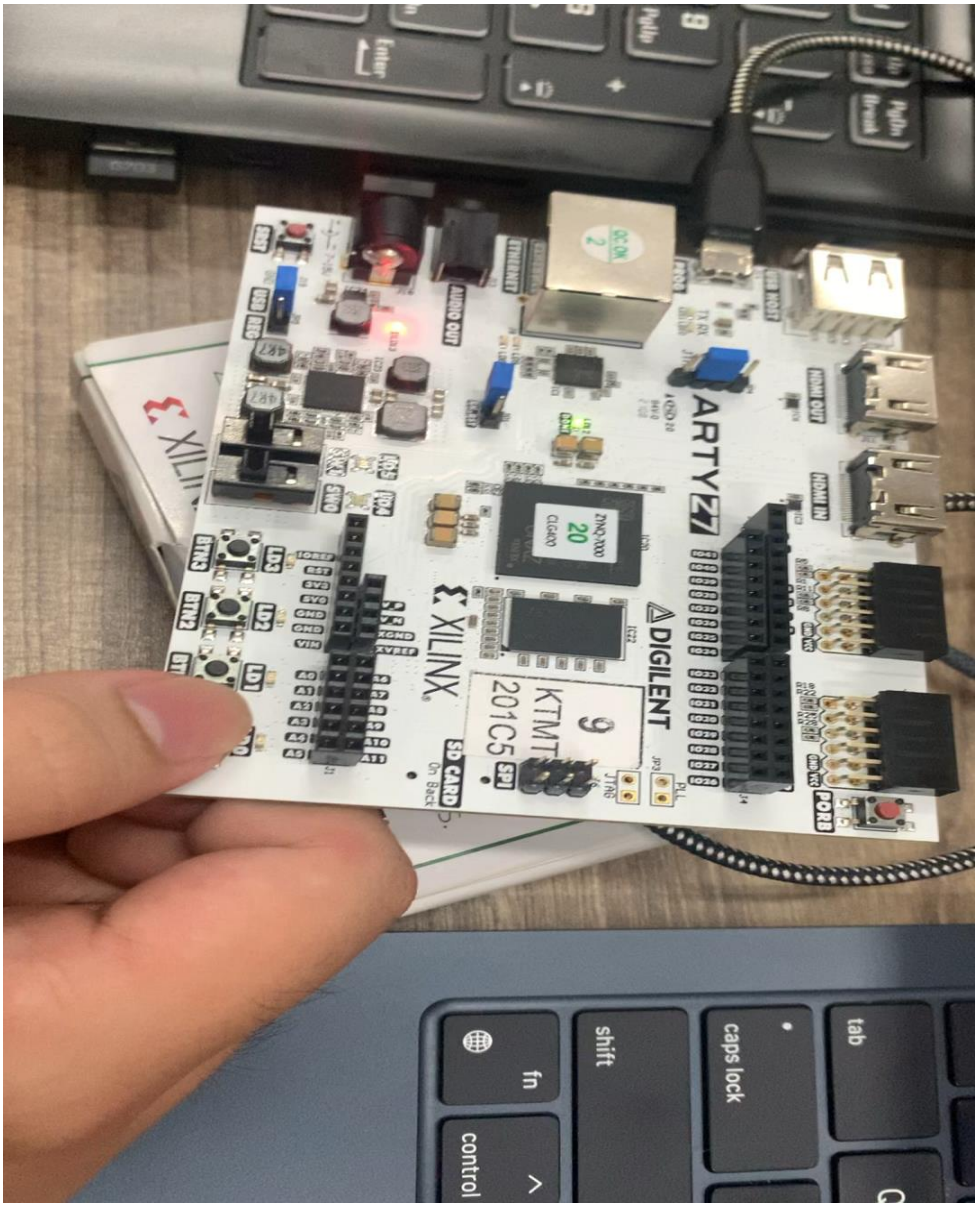
```
`timescale 1ns / 1ps

module work_space(enb,output_d,clk);

    input clk,enb;
```

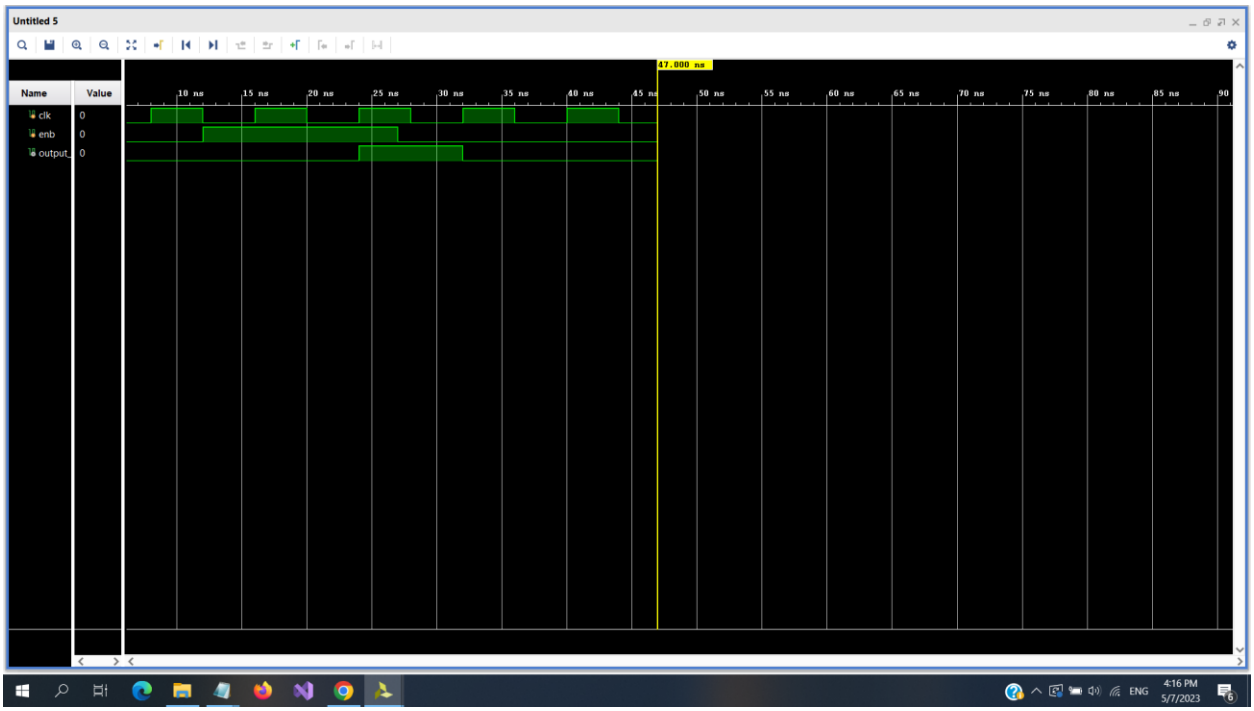
```
    output output_d;
    reg sig_delay, sec_delay;
    always @(posedge clk) begin
    sig_delay <= enb;
    end
    always @(posedge clk) begin
    sec_delay <= sig_delay;
    end
    assign output_d = sig_delay & sec_delay;

endmodule
```

TEST BENCH:

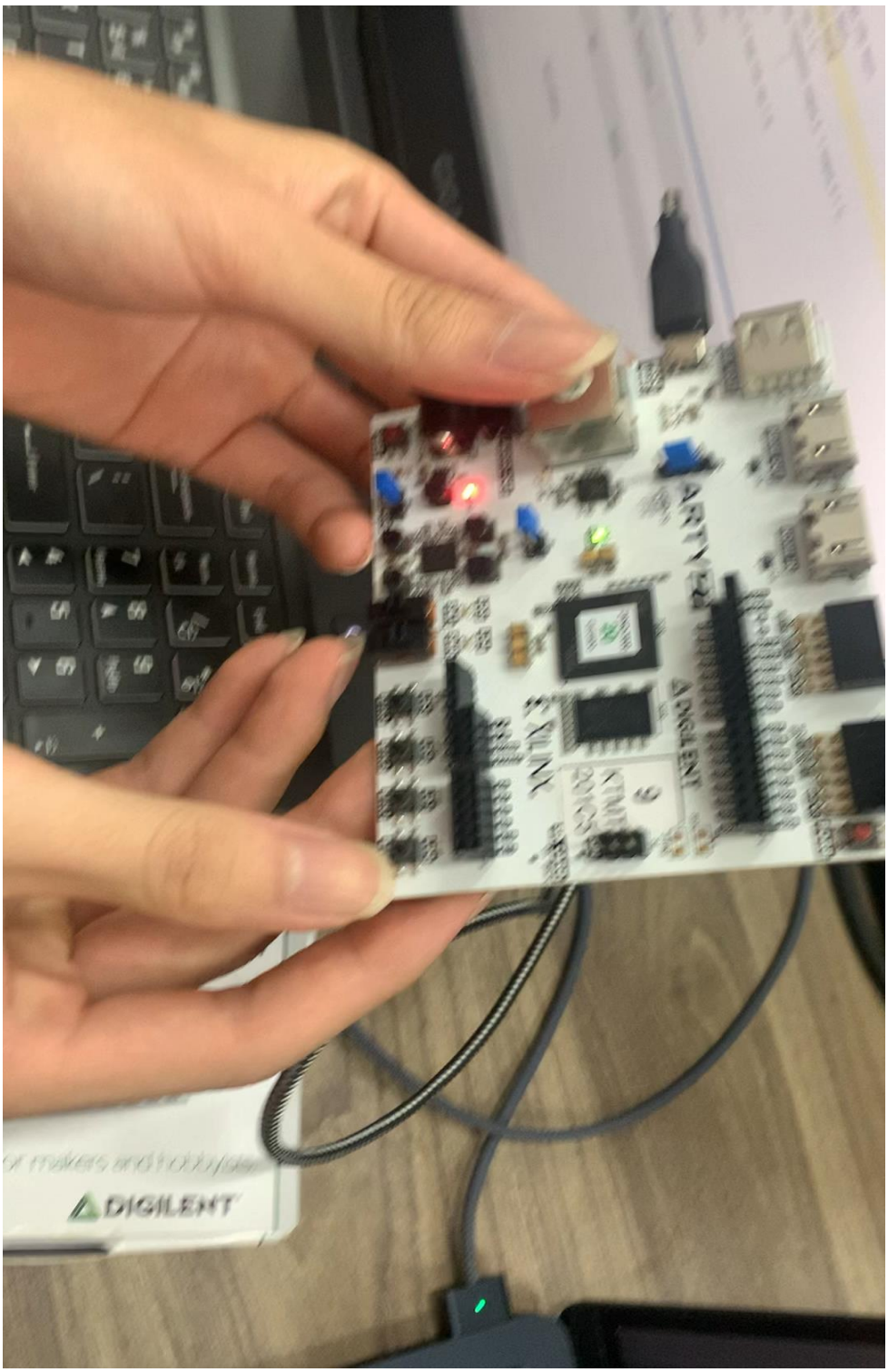
```
`timescale 1ns / 1ps
module lab3_tb(

    );
    reg clk, enb;
    wire output_d;
    initial begin
    forever #5 clk = ~clk;
    end
    initial begin
    clk = 0;

    end
    initial begin
```

```
    enb = 0;
    #12
    enb = 1;
    #15 enb = 0;
    #20 $stop;
    end
    work_space somthingg(enb,output_d,clk);
endmodule
```





b. Write a 4-bit binary counter that counts up 1 unit when a button is pushed. Use the edge detection circuit to generate an enable signal for the counter when pushing the button. Test the design on FPGA board.



2.3

Exercise 3

Change mode String bit LED circuit. Use Verilog HDL to model a state machine for a circuit that changes display mode of a bit string. In initial, LEDs show the default 4-bit random string which is performed by a reset signal, example string: 0011. And buttons in board will set the display mode as follow:

• Button 0: Mode Reset: Show the default 4-bit string on LEDs.

• Button 1: Mode Circular Shift Left Ring : Shift 4-bit string to left in a ring every 1s.

• Button 2: Mode Circular Shift Right Ring: Shift 4-bit string to right in a ring every 1s.

• Button 3: Pause: Pause the current shifting string.

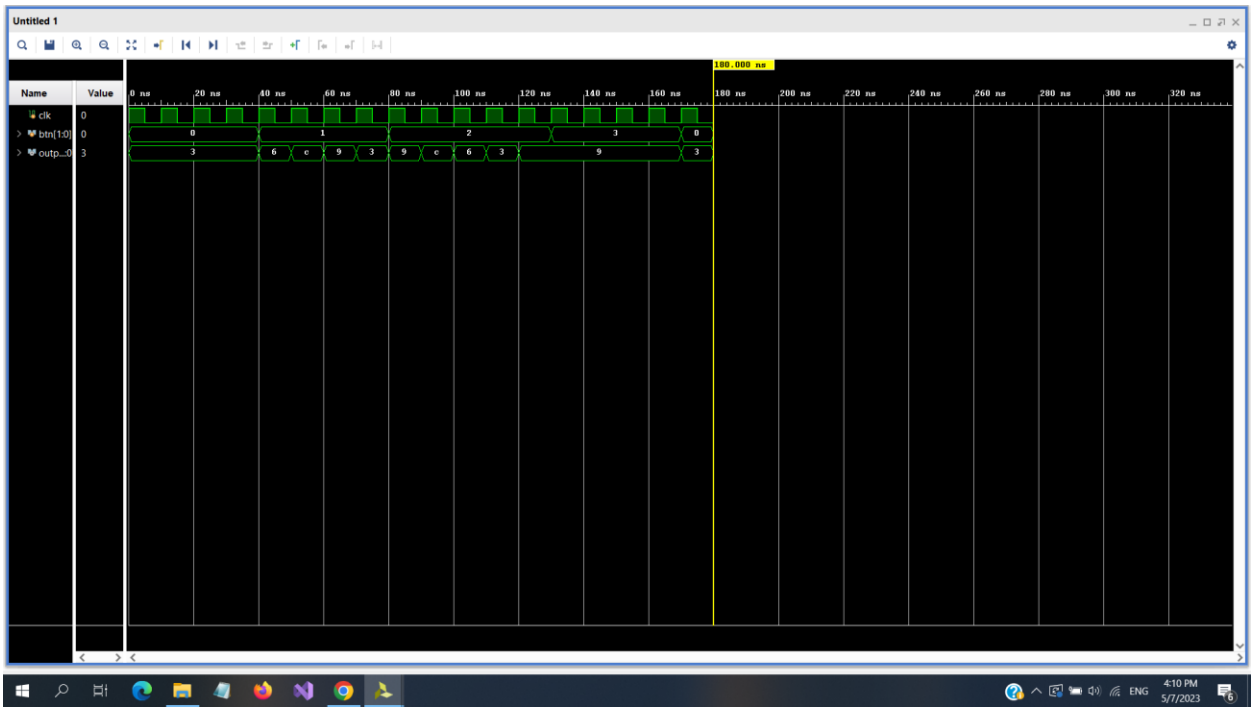
Draw a state diagram to illustrate the designed FSM. Student can use Moore or Mealy model. Write a test bench to simulate the circuit and test the circuit on the Arty-Z7 board:

```
`timescale 1ns / 1ps

module workspce(btn,clk,output_led);

input [1:0] btn;

input clk;

output reg [3:0] output_led;

reg [30:0] cnt;

always @(posedge clk) begin

if (btn == 0) begin

output_led = 4'b0011;

end
```

```
else if (btn ==1) begin

 output_led <= {output_led[2:0],output_led[3]};

end

else if (btn ==2) begin

output_led <= {output_led[0],output_led[3:1]};

 end

else if (btn ==4) output_led <= output_led;

end

endmodule
```

TEST BENCH:

```
`timescale 1ns / 1ps
module lab3_tb();
   reg clk;
   reg [1:0] btn;
   wire [3:0] output_led;
   initial begin
   clk =1 ;
   forever #5 clk = ~clk;
   end
   initial begin
   btn = 2'b00;
   #40
   btn = 2'b01;
   #40
   btn = 2'b10;
   #50
   btn = 2'b11;
   #40
   btn = 2'b00;
   #10 $stop;
   end
   workspce somthing(btn,clk,output_led);
endmodule
```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Name
Value
clk
btn[1:0]
outp...0
100.000 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns
220 ns
240 ns
260 ns
280 ns
300 ns
320 ns
ENG
4:10 PM
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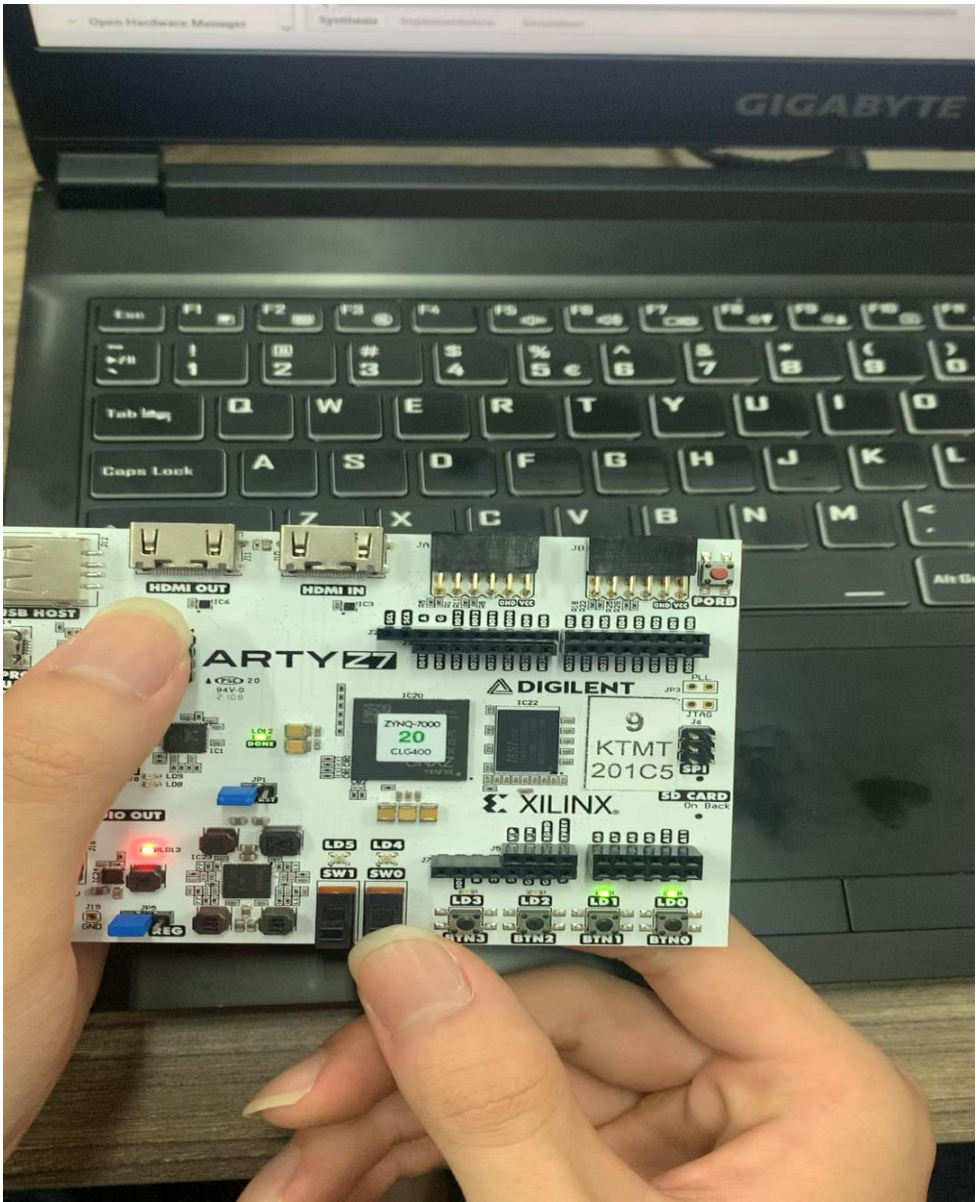
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ARTY Z7
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CLG400
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LD4
SW1
SW0
LD3
LD2
LD1
LD0
BTN3
BTN2
BTN1
BTN0