



WEEK 3**Sequential Logic Circuit**

1 Introduction

1.1 Aims

- Practice in designing sequential logic circuits using Verilog HDL behavioral model.
- Understand the blocking/non-blocking assignment to design a combinational/sequential circuit.
- Understand finite state machine models and practice in model FSMs using Verilog HDL.

1.2 Preparation

- Read the laboratory materials before class.
- Review chapter 5-6 about Behavioral Model and Finite State Machine.
- Each group prepares at least one laptop with Vivado software installed.

1.3 Report requirements

- Lab exercises will be reviewed directly in class.
- Write report (with circuit/simulation screenshots inserted) in pdf.
- Must have group ID, group member's names and student IDs in the report.
- Compress the report with code files (only .v files) in only one .zip file, name the .zip the group ID (for example: Group1.zip).
- Submit on BK-elearning by deadline.

2 Exercises

2.1 Exercise 1

Clock Frequency Divider

Police Siren: Design a circuit that generate a **1 Hz** output signal using Behavioral Model. This signal is connected to 2 RGB LEDs (1 displays the blue color, 1 display the red color) on Arty-Z7 FPGA

Board to make it blink interleave with each other (turn on for 0.5s - turn off for 0.5s). Know that the input clock frequency is 125 MHz.

Write test benches to simulate the circuits.

Test the circuits on FPGA board using LEDs and RGB LED.

2.2 Exercise 2

Edge Detection circuit.

a. Design a Rising Edge Detection circuit. This circuit will use at least 2 flip-flops. The behavior of the circuit is similar to the waveform in Figure 1. Assume that the in signal's HIGH levels last equal to or longer than a clock cycle.

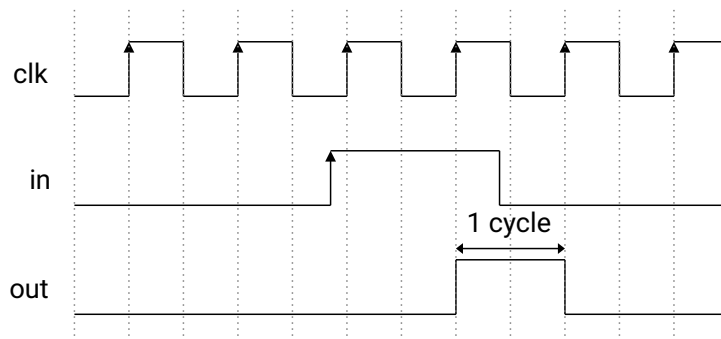


Figure 1: Rising Edge Detector behavior

The output is active HIGH in 1 cycle of clock when a rising edge occurs in input signal. Delay is within 0-2 clock cycles.

Write RTL code and test benches to simulate the circuit.

NOTICE: This circuit is very important. Please complete it regardless of whether you can do it by deadline or not.

b. Write a 4-bit binary counter that counts up 1 unit when a button is pushed. Use the edge detection circuit to generate an enable signal for the counter when pushing the button. Test the design on FPGA board.

2.3 Exercise 3

Change mode String bit LED circuit.

Use Verilog HDL to model a state machine for a circuit that changes display mode of a bit string.

In initial, LEDs show the default 4-bit random string which is performed by a reset signal, example string: 0011. And buttons in board will set the display mode as follow:

- Button 0: Mode Reset: Show the default 4-bit string on LEDs.
- Button 1: Mode Circular Shift Left Ring : Shift 4-bit string to left in a ring every 1s.
- Button 2: Mode Circular Shift Right Ring: Shift 4-bit string to right in a ring every 1s.
- Button 3: Pause: Pause the current shifting string.

Draw a state diagram to illustrate the designed FSM. Student can use Moore or Mealy model.

Write a test bench to simulate the circuit and test the circuit on the Arty-Z7 board.

Hint: Students should do the following steps:

- Partitioning the design into blocks, may draw a block diagram. Separate the state machine and the string display logic.
- Define the inputs, outputs of the FSM, then design the FSM.
- Modeling the FSM using Verilog HDL. Use the FSM's outputs to control the string display.
- Simulate and test the circuit on board.