Ho Chi Minh City University of Technology
Faculty of Computer Science and Engineering

LOGIC DESGIN WITH HDL

Practical session - Semester 222

WEEK 2

Combinational Logic Circuit

1 Introduction

1.1 Aims

- Practice in designing combinational logic circuits using Verilog HDL continuous assignment.
- Practice in designing combinational logic circuits using Verilog HDL blocking assignment in behavioral model.

1.2 Preparation

- Read the laboratory materials before class.
- Review chapter 4-5 about Dataflow model and continuous assignment, Behavioral model.

1.3 Report requirements

- Lab exercises will be reviewed directly in class.
- Write report (with circuit/simulation screenshots inserted) in pdf.
- Must have group ID, group member's names and student IDs in the report.
- Compress the report with code files (only .v files) in **only one .zip** file, name the .zip the group ID (for example: Group1.zip).
- Submit on BK-elearning by deadline.

2 Exercises

2.1 Exercise 1

Design a circuit that has one 4-bit input and 4-bit output with functions as follow (all outputs are active HIGH):

- Output 0: active when there are even number of bit 1 in the input.
- Output 1: active when there are only 1 bit 1 in the input.

- Output 2: active when there is no bit 1 in the input.
- Output 3: active when all bit in the input are 1.

Write Verilog HDL RTL code and test bench for the design.

Test the circuit on FPGA using buttons and LEDs.

Hint: Students should use reduction operators.

2.2 Exercise 2

Design a circuit that generate a **1 Hz** output signal using structural model. This signal connect to LED on Arty-Z7 FPGA Board to make it blink (turn on for 0.5s - turn off for 0.5s). Know that the input clock frequency is 125 MHz and the FlipFlop can include from Vivado library.

Write test benches to simulate the circuits.

Test the circuits on FPGA board using LEDs or RGB LED.

2.3 Exercise 3

Design a 7-segment LED decoder which will accept a 4-bit input and generate a 7-bit output.

- Interface: **module bin2led7(enable, bin_in, led_out);**
- The *enable* signal controls LEDs. If enable = 0, LEDs are turned off.
- The bin_in is a 4-bit binary input signal.
- The led_out is a 7-bit output signal for 7-segment LED display.

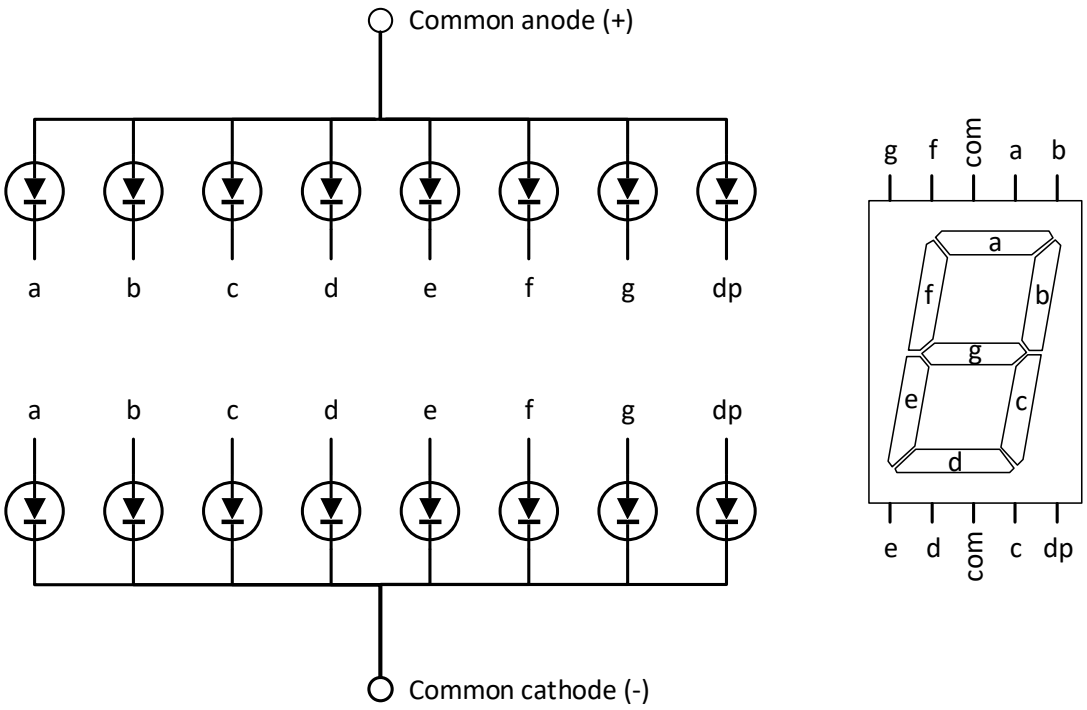

Figure 1: 7 segment LED

Write a test bench to simulate the implemented circuit.

Test the circuit on Arty-Z7 FPGA board using switches/buttons and external 7-seg LEDs.

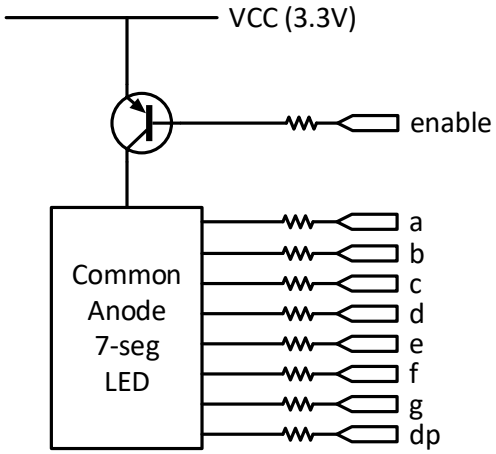

Figure 2: Common anode 7 segment LED circuit

2.4 Exercise 4

Design a circuit to control the RGB LEDs on Arty-Z7 board as follow:

- Switch 0: select display mode - 1 LED or 2 LEDs.
- Switch 1:

  - to select left or right LED in 1-LED display mode.
  - to select color code as table below.

- Buttons: select colors.

Buttons	Color		
	1-LED mode	2-LED mode	
		Switch 1 = 0	Switch 1 = 1
0000	OFF	OFF	OFF
0001	Blue	Blue	Cyan (Blue & Green)
0010	Green	Green	Yellow (Green & Red)
0100	Red	Red	Purple (Red & Blue)
1000	White	White	White
Other	OFF	Mixed of above	OFF

Write Verilog HDL RTL code and test bench for the design.

Test the circuit on FPGA using switches, buttons and RGB LEDs on the Arty-Z7 board.