

# FDN306P

# P-Channel 1.8V Specified PowerTrench® MOSFET

### **General Description**

This P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

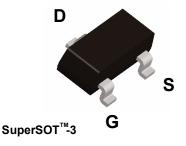
## **Applications**

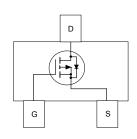
- · Battery management
- · Load switch
- Battery protection

### **Features**

• -2.6 A, -12 V.  $R_{DS(ON)}$  = 40 m $\Omega$  @  $V_{GS}$  = -4.5 V  $R_{DS(ON)}$  = 50 m $\Omega$  @  $V_{GS}$  = -2.5 V  $R_{DS(ON)}$  = 80 m $\Omega$  @  $V_{GS}$  = -1.8 V

- · Fast switching speed
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS(ON)}}$
- SuperSOT<sup>™</sup> -3 provides low R<sub>DS(ON)</sub> and 30% higher power handling capability than SOT23 in the same footprint





Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		<b>–12</b>	V
V <sub>GSS</sub>	Gate-Source Voltage		±8	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	-2.6	Α
	– Pulsed		<b>–</b> 10	
P <sub>D</sub>	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

## **Thermal Characteristics**

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
306	FDN306P	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics			l		
BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = -250 \mu\text{A}$	-12			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A,Referenced to 25°C		-3		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -10 \text{ V}, \qquad V_{GS} = 0 \text{ V}$			-1	μΑ
I <sub>GSSF</sub>	Gate–Body Leakage, Forward	$V_{GS} = 8 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -8 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.4	-0.6	-1.5	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A,Referenced to 25°C		2.5		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$\begin{array}{l} V_{GS} = -4.5 \ V, & I_D = -2.6 \ A \\ V_{GS} = -2.5 \ V, & I_D = -2.3 \ A \\ V_{GS} = -1.8 V, & I_D = -1.8 \ A \\ V_{GS} = -4.5 \ V, I_D = -2.6 A \ , T_J = 125 ^{\circ} C \end{array}$		30 39 54 40	40 50 80 54	mΩ
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = -4.5 \text{ V},  V_{DS} = -5 \text{ V}$	-10			Α
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5 \text{ V}, \qquad I_{D} = -2.6 \text{ A}$		10		S
Dynamic	: Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -6 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		1138		pF
Coss	Output Capacitance	f = 1.0 MHz		454		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			302		pF
Switchin	g Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = -6 \text{ V}, \qquad I_D = -1 \text{ A},$		11	20	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = -4.5 \text{ V}, \qquad R_{GEN} = 6 \Omega$		10	20	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			38	61	ns
t <sub>f</sub>	Turn-Off Fall Time			35	56	ns
Qg	Total Gate Charge	$V_{DS} = -6 \text{ V}, \qquad I_{D} = -2.6 \text{ A},$		12	17	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = -4.5 V		2		nC
$Q_{gd}$	Gate-Drain Charge			3		nC
Drain-S	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Sourc	<u> </u>			-0.42	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{S} = -0.42 \text{ (Note 2)}$		-0.6	-1.2	V

#### Notes

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



 a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.



b) 270°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300~\mu s,~Duty~Cycle \leq 2.0\%$ 

## **Typical Characteristics**

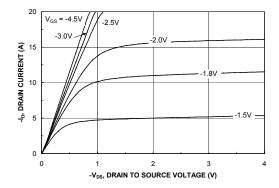


Figure 1. On-Region Characteristics.

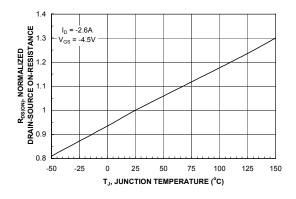


Figure 3. On-Resistance Variation with Temperature.

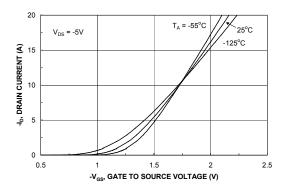


Figure 5. Transfer Characteristics.

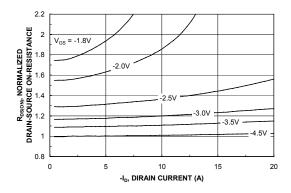


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

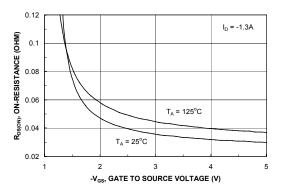


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

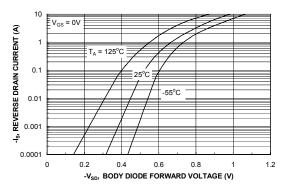
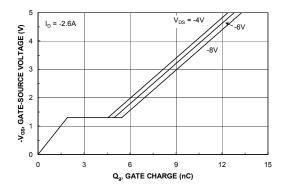


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## **Typical Characteristics**



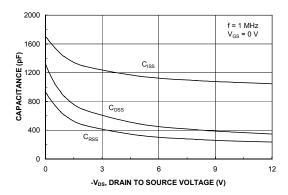
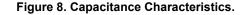
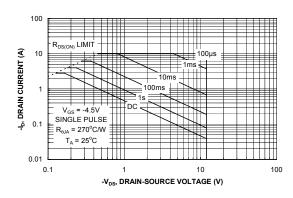


Figure 7. Gate Charge Characteristics.





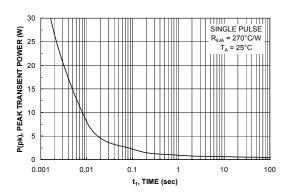


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

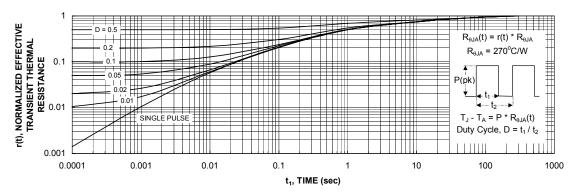


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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