CHINNAKOTLA PAVAN KUMAR

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DESIGN VERIFICATION ENGINEER

PROFILE

Aiming to join a dynamic team of professionals as a VLSI Engineer where I can share my expertise and contribute to the success of the organization.

PROFESSIONAL TRAINING

Advanced VLSI Design and Verification Course July 2023 - May 2024

- At Maven Silicon VLSI Softech pvt.ltd Bangalore, Karnataka
- Course Work : Digital Electronics,Verilog,System Verilog,Universal Verification Methodology

EDUCATION

B.Tech Electrical & Electronics Engineering 2020 - Nov 2023

- GPA: 7.52
- Sreenivasa Institute of Technology and Management Studies - Chittoor

Diploma Electrical & Electronics Engineering 2017-2020

- Percentage:70.06%
- Government Polytechnic, Kadiri

Secondary Education

- CGPA: 9.0 2017
- Municipal High School, Punganur

TECHNICAL SKILLS

- HDL: Verilog
- HVL: System Verilog, UVM, SVA
- PROTOCOLS: AHBtoAPB | SPI | I2C
- PROGRAMMING LANGUAGES:C programming
- SCRIPTING LANGUAGES: PERL
- DOMAIN: ASIC, FPGA frontend Design and Verification
- EDA TOOLS: Modelsim & Questasim | Synopsys Design Compiler | Xilinx Vivado | VC Spyglass*

CERTIFICATIONS

- NPTEL Advances in UHV Transmission and Distribution
- NPTEL VLSI design flow: RTL to GDS, NPTL

PROJECTS

Router 1x3 – RTL Design and Verification

- HDL: Verilog
- HVL: System Verilog
- TB Methodology: UVM
- EDA Tools: Questasim and ISE
- Description: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

Serial Peripheral Interface - Verification

- HVL: SystemVerilog
- TB Methodology: UVM
- EDA Tools: Synopsys Verdi (VCS),Questasim
- Description: SPI is a synchronous serial communication interface widely used for interfacing microcontrollers with peripheral devices such as sensors, displays, and memory chips

AHB2APB Bridge IP Core Verification

- HVL: System Verilog
- TB Methodology: UVM
- EDA Tools: Synopsys Verdi (VCS),Questasim
- Description: The AHB to APB bridge is an AHB slave which works as an interface between the high speed AHB and the low performance APB buses.

Automatic Power Factor Corrector with Microcontroller Based Capacitor Bank Switching

- The modified switching of the capacitor banks in order to correct the power factor of inductive loads.
- In industrialization inductive loading increases. It affects the PF so the power system losses the efficiency.
- Achieve the power factor by using programmable device.

STRENGTHS

- Adaptability
- Desire to learn new things
- Patience

DECLARATION

I hereby declare that the facts given above are genuine to the best of my knowledge and belief.

Date:

Place: Bangalore Chinnakotla PavanKumar