Lab1 寄存器堆与存储器及其应用

李远航

PB20000137

1. 实验内容

- 行为方式参数化描述寄存器堆，功能仿真
- IP 例化分布式和块式 16 x 8 位单端口 RAM，功能仿真和对比
- 设计 FIFO 队列电路的数据通路和控制器，结构化方式描述数据通路，Moore 型 FSM 描述控制器，功能仿真
- FIFO 队列电路下载至 FPGA 中测试

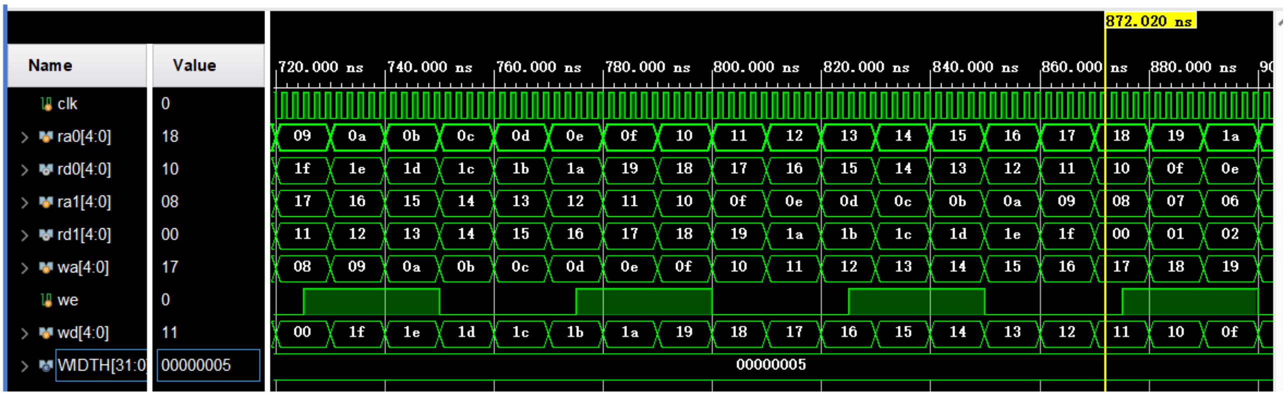
2. 实验过程

(1)行为方式参数化描述 32×WIDTH 寄存器堆

- verilog代码

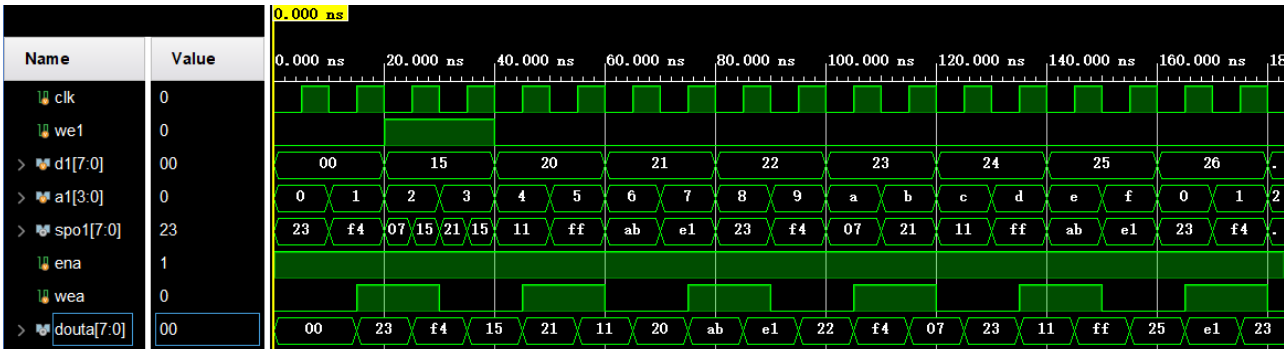
```verilog
module register_file #(parameter WIDTH = 32)(
    input clk,
    input [4:0] ra0,
    output [WIDTH-1:0] rd0,
    input [4:0] ra1,
    output [WIDTH-1:0] rd1,
    input [4:0] wa,
    input we,
    input [WIDTH-1:0] wd
);
    reg [WIDTH-1:0] regfile[0:31];

    assign rd0 = regfile[ra0];
    assign rd1 = regfile[ra1];

    always @(posedge clk) begin
        if (we == 1)
            regfile[wa] <= wd;
    end
endmodule
```

- 功能仿真


872.020 ns
Name
Value
720.000 ns
740.000 ns
760.000 ns
780.000 ns
800.000 ns
820.000 ns
840.000 ns
860.000 ns
880.000 ns
clk 0
ra0[4:0] 18
09 0a 0b 0c 0d 0e 0f 10 11 12 13 14 15 16 17 18 19 1a
rd0[4:0] 10
1f 1e 1d 1c 1b 1a 19 18 17 16 15 14 13 12 11 10 0f 0e
ra1[4:0] 08
17 16 15 14 13 12 11 10 0f 0e 0d 0c 0b 0a 09 08 07 06
rd1[4:0] 00
11 12 13 14 15 16 17 18 19 1a 1b 1c 1d 1e 1f 00 01 02
wa[4:0] 17
08 09 0a 0b 0c 0d 0e 0f 10 11 12 13 14 15 16 17 18 19
we 0
wd[4:0] 11
00 1f 1e 1d 1c 1b 1a 19 18 17 16 15 14 13 12 11 10 0f
WIDTH[31:0] 00000005
00000005

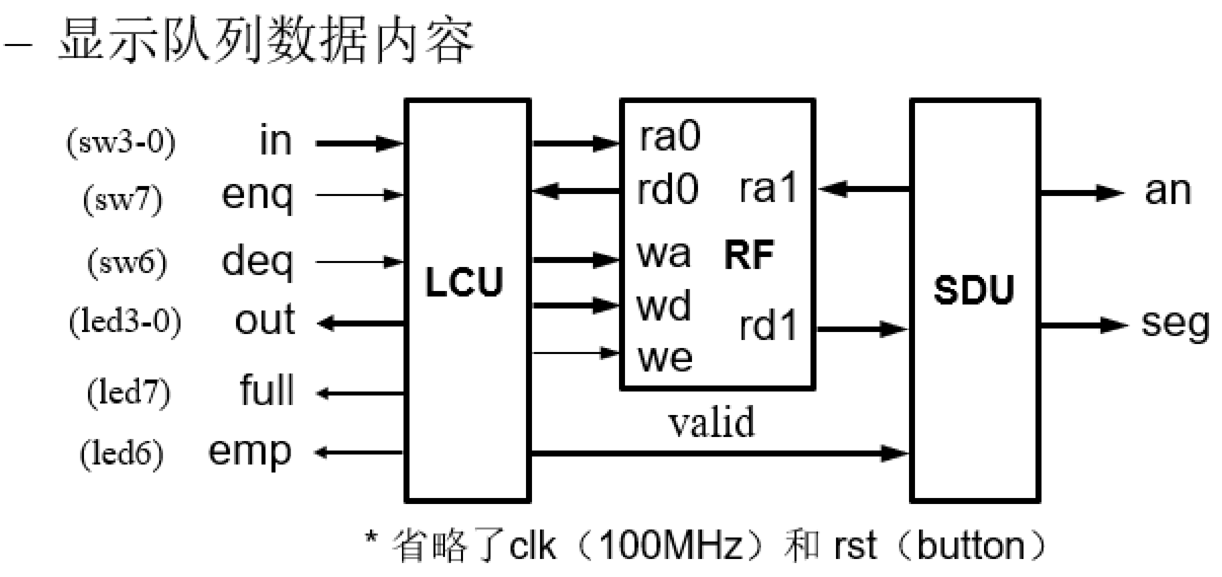
(2)IP 例化分布式和块式 16 x 8 位单端口 RAM

- 功能仿真 spo1 端口为分布式 RAM 输出，douta 为块式 RAM 输出，两种 ip 核共用 a1 地址端口和 d1 数据端口



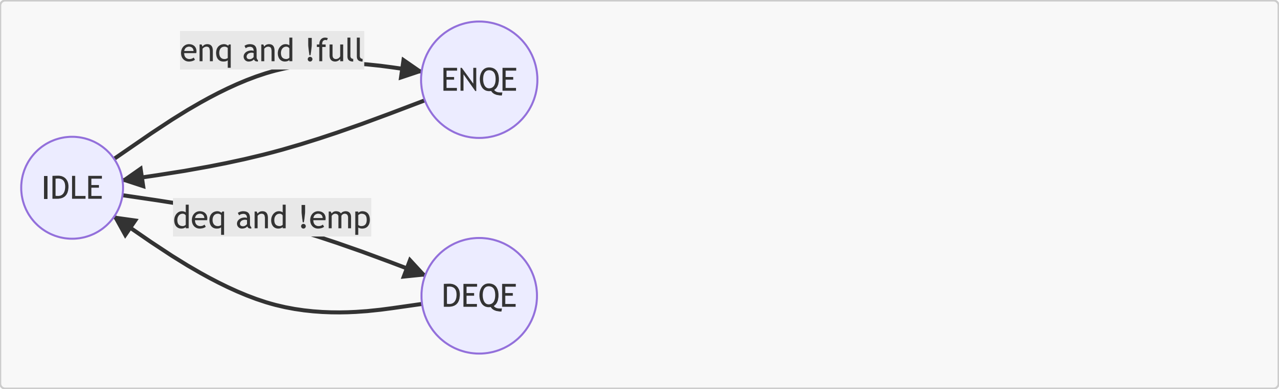
(3)用三端口 8×4 寄存器堆实现最大长度为 8 的 FIFO 队列

- 逻辑结构


– 显示队列数据内容

* 省略了clk（100MHz）和 rst（button）

- 状态机设计：



- verilog代码

异步信号取边沿(SEDG)

```verilog
module SEDG(
        input a,
        input clk,
        output p    //
    );
    reg st, pt, s;
    always@(posedge clk)
        st <= a;
    always@(posedge clk)
        s <= st;
    always@(posedge clk)
        pt <= s;
    assign p = (~pt) & s;
endmodule
```

寄存器文件(RF)

```verilog
module register_file(
    input clk,
    input [2:0] ra0,
    output [3:0] rd0,
    input [2:0] ra1,
    output [3:0] rd1,
    input [2:0] wa,
    input we,
    input [3:0] wd
);
    reg [3:0] regfile[0:7];
    assign rd0 = regfile[ra0];
    assign rd1 = regfile[ra1];
    always@(posedge clk) begin
        if (we == 1)
            regfile[wa]  <=  wd;
    end
endmodule
```

数码管显示单元(SDU)

```
module SDU(
        input rst, clk,
        input [3:0] rd,
        input [7:0] valid,
        output [2:0] ra,
        output [2:0] an,
        output [3:0] seg
    );
    reg [23:0] count;
    assign an = ra;
    assign ra = count[12:10];
    always@(posedge clk)
    begin
        if (rst) begin
            count <= 24'd0;
        end else begin
            count <= count + 1;
        end
    end
    assign seg = valid[ra] ? rd : 0;
endmodule
```

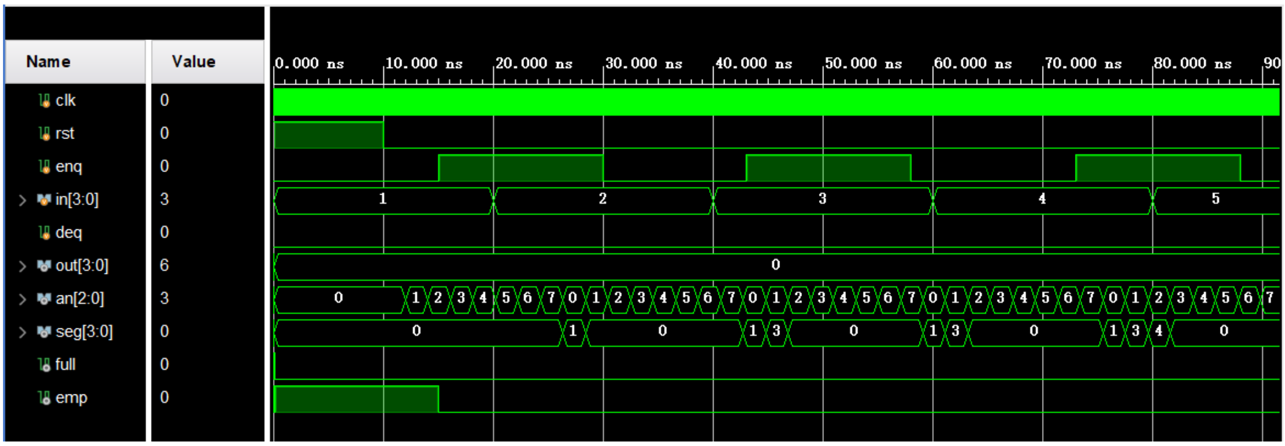
队列控制单元(LCU)

```
module LCU(
    input clk, rst,
    input [3:0] in, rd0,
    input enq, deq,
    output reg [3:0] out,
    output full, emp, we,
    output [2:0] ra0, wa,
    output [3:0] wd,
    output reg [7:0] valid
);
    assign wa = tail;
    assign wd = in;
    assign we = enq;
    assign ra0 = head;
    parameter IDLE = 2'b00;
    parameter ENQU = 2'b01;
    parameter DEQU = 2'b10;
    reg [1:0] cs, ns;
    reg [2:0] head, tail;
    reg [3:0] count;
    always@(posedge clk) begin
        if (rst == 1)
            cs <= IDLE;
        else
            cs <= ns;
    end
    always @(*) begin
        case (cs)
            IDLE: begin
                if (enq & !full)
                    ns <= ENQU;
                else if (deq & !emp)
                    ns <= DEQU;
                else
                    ns <= IDLE;
            end
            ENQU: ns <= IDLE;
            DEQU: ns <= IDLE;
        endcase
    end
    always@(posedge clk)begin
        if (rst == 1) begin
            tail <= 0;
            head <= 0;
            valid <= 0;
            count <= 0;
            out <= 0;
        end
        else if (cs == ENQU) begin
            valid[tail] <= 1;
            tail <= tail + 1;
            count <= count + 1;
        end
        else if (cs == DEQU) begin
            valid[head] <= 0;
            head <= head + 1;
            count <= count - 1;
            out <= rd0;
        end
    end
    assign full = (count == 4'd8) ? 1 : 0;
    assign emp = (count == 4'd0) ? 1 : 0;
endmodule
```

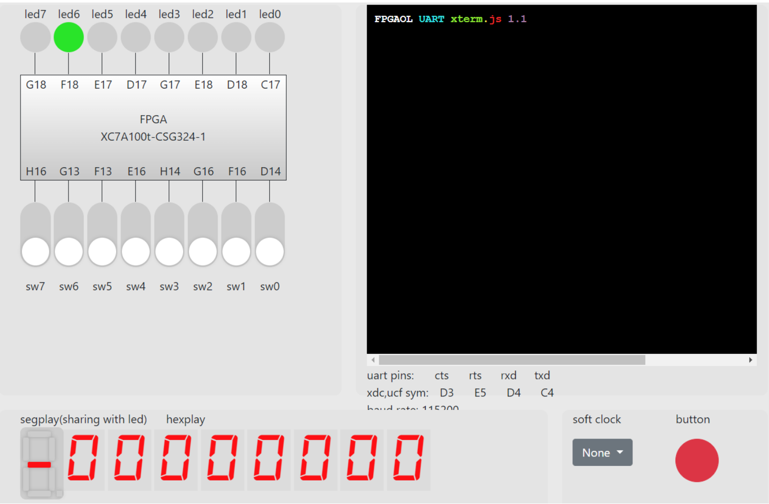
顶层模块

```
module fifo(
    input clk, rst,     //时钟（上升沿有效）、同步复位（高电平有效）
    input enq,          //入队列使能，高电平有效
    input [3:0] in,     //入队列数据
    input deq,          //出队列使能，高电平有效
    output [3:0] out,   //出队列数据
    output [2:0] an,    //数码管选择
    output [3:0] seg,   //数码管数据
    output full,emp
);
    wire [2:0]ra0, ra1, wa;
    wire [3:0]rd0, rd1, wd;
    wire we_0,we;
    wire enq_edge;
    wire deq_edge;
    wire [7:0] valid;
    wire [3:0] out_;
    SEDG edg_enq(enq, clk, enq_edge);
    SEDG edg_deq(deq, clk, deq_edge);
    LCU LCU(clk, rst, in, rd0, enq_edge, deq_edge, out_, full, emp, we_0, ra0, wa, wd, valid);
    register_file regfile(clk, ra0, rd0, ra1, rd1, wa, we, wd);
    SDU SDU(rst, clk, rd1, valid, ra1, an, seg);
    assign we = (full == 1) ? 0 : we_0;
    assign out = (emp == 1) ? 0 : out_;
endmodule
```

- 功能仿真

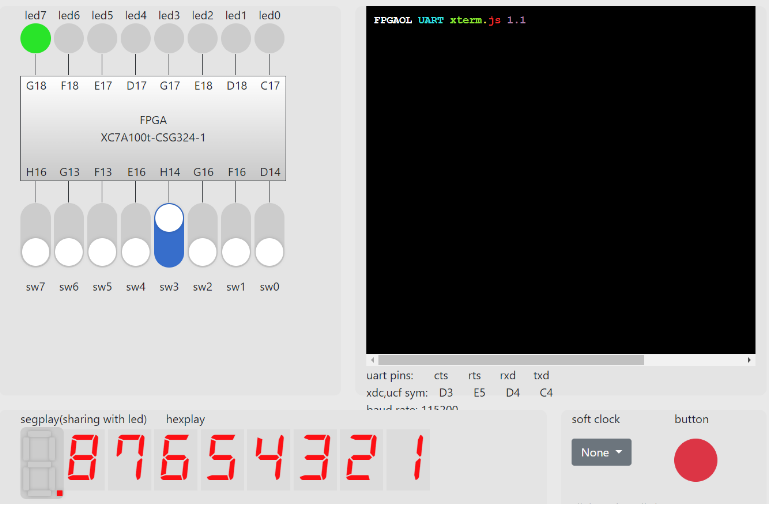


- VGA 测试


led7 led6 led5 led4 led3 led2 led1 led0
G18 F18 E17 D17 G17 E18 D18 C17
FPGA
XC7A100t-CSG324-1
H16 G13 F13 E16 H14 G16 F16 D14
sw7 sw6 sw5 sw4 sw3 sw2 sw1 sw0
segplay(sharing with led)
hexplay
00000000
soft clock
None
button

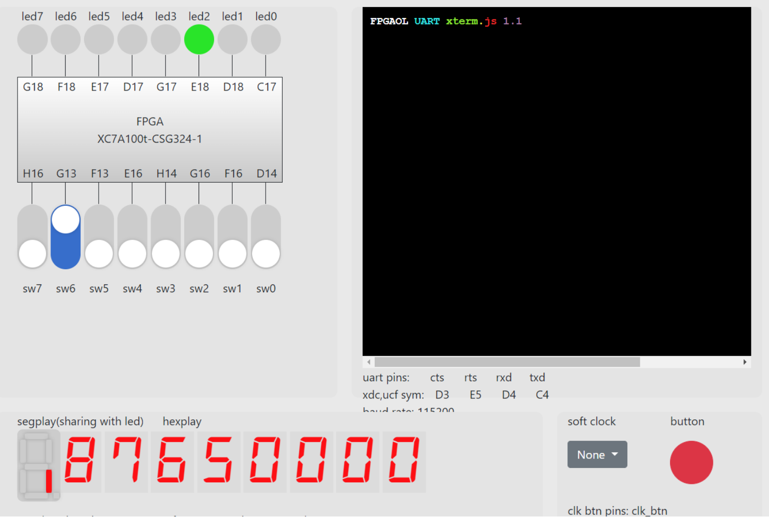
```
FPGAOL UART xterm.js 1.1
```

```
uart pins:      cts   rts   rxd   txd
xdc,ucf sym:    D3    E5    D4    C4
baud rate: 115200
```


led7 led6 led5 led4 led3 led2 led1 led0
G18 F18 E17 D17 G17 E18 D18 C17
FPGA
XC7A100t-CSG324-1
H16 G13 F13 E16 H14 G16 F16 D14
sw7 sw6 sw5 sw4 sw3 sw2 sw1 sw0
segplay(sharing with led)
hexplay
8765432 1
soft clock
None
button

```
FPGAOL UART xterm.js 1.1
```

```
uart pins:      cts   rts   rxd   txd
xdc,ucf sym:    D3    E5    D4    C4
baud rate: 115200
```


led7 led6 led5 led4 led3 led2 led1 led0
G18 F18 E17 D17 G17 E18 D18 C17
FPGA
XC7A100t-CSG324-1
H16 G13 F13 E16 H14 G16 F16 D14
sw7 sw6 sw5 sw4 sw3 sw2 sw1 sw0
segplay(sharing with led)
hexplay
87650000
soft clock
None
button
clk btn pins: clk_btn

```
FPGAOL UART xterm.js 1.1
```

```
uart pins:      cts   rts   rxd   txd
xdc,ucf sym:    D3    E5    D4    C4
baud rate: 115200
```