Vinay Padma

Electrical Engineering

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TECHNICAL SKILLS

- Prior electrical R&D lab experience (PCB rework and testing, circuitry, machinery/power tools, etc.)
- Experience using test equipment including oscilloscopes, DMMs, etc.
- Schematic capture and simulation experience using Multisim
- Previous experience working with C#, C++, Java (Android), T-SQL, VBA, VBAScript and JavaScript
- Implementation of FPGA (VHDL), ARM ISA and MatLab through school labs
- Work experience drafting using AutoCAD

INTERPERSONAL SKILLS

- Strong analytical and adaptive skills; learned roles quickly with little supervision in prior co-ops
- Gained strong interpersonal, communication and leadership skills through extra-curricular activities such as being an Engineering Ambassador for UW
- Developing project coordination/management skills obtained through volunteer experience such as chairing the FYELC conference for UW
- Results-oriented ethic gained through working at start-up; measure work in deliverables not hours

RELEVANT EXPERIENCE

Integration Engineer

May 2014 - August 2014

Solink Corporation, Hardware Integration Team, Kanata, ON

- Developed client wrappers integrating 3rd party cameras into Solink product (utilise vendor APIs)
- Integrated both desktop (.NET framework, C#) and web (JavaScript) SDKs into product
- Engineered clean, reliable code designed to handle several concurrent instances over network
- Embraced start-up and a results-oriented culture, oversaw projects from start to finish

R&D Lab/Junior Design Technologist

August 2013 - December 2013

Fifth Light Technologies, Cooper Industries, Mississauga, ON

- Performed PCB assembly and testing, gained proficiency soldering (through-hole and SMT) and utilising test equipment (power supplies, DMMs, scopes)
- Wired and developed circuits as part of an interface to test lighting control products (DALI)
- Drafted and designed lighting control floor plans using AutoCAD and product specifications
- Gained experience with power tools and electrical standards while building test units

Developer/Analyst

January 2013 - April 2013

CIBC, Retail Treasury Middle Office, Toronto, ON

- Re-engineered processes, analyzed SQL to identify legacy function and readjust to requirements. Automated processes using Windows batch and Microsoft DTS
- Developed cross-platform processes, utilised ADO libraries when required to work with VBA
- Project delivery; analyzed current and future states with process maps for presentations
- Required to learn banking finance basics, assisted Office of CIO with time-series analysis

EDUCATION

Candidate for Bachelor's Degree of Applied Science

2012 - 2017

Honours Electrical Engineering, University of Waterloo, ON

 Relevant Courses: Linear/Electronic Circuits, Data Structures & Algorithms, Eng. Design with Embedded Systems, Digital Systems (intro circuit/hardware design, VHDL), Digital Computers (ARM ISA), Signals & Systems, Electronic Properties of Materials, Discrete Math

International Baccalaureate Diploma

2008 - 2012

Turner Fenton Secondary School, Brampton, ON

RELEVANT ASSIGNMENTS/PROJECTS

Design Optimized Djikstra's Algorithm (C++)

March 2014

- Designed optimizations for implementing Djikstra's Algorithm, ECE 250 final assignment (view code)
- Memory allocations for arrays within same space in memory, memo-ized node lookups into a hash

Lighting Testing Wall - PCB Rework and Circuitry

October 2013 - December 2013

- Built/wired wall with over 300 DALI protocol devices for product validation at Fifth Light
- PCB rework and soldering DALI master modules in order to network wall devices together
- Experience with terminals and power supplies; were used to power the validation wall

VHDL Programming

July 2013

- Programming an Altera FPGA using Quartus II, implemented a traffic light controller (view code)
- Labs involving low-level programming, implemented sequential/non-sequential design and finite state machines.

AWARDS AND ACHIEVEMENTS

•	Industrial Undergraduate Student Research Award (IUSRA - NSERC)	2014
•	Waterloo Engineering Society President's Award - Excellence for work in Education Outreach	2014
•	Ontario Scholar, graduated with Ontario Top Six Average of 95%	2012
•	Principal's Award (Turner Fenton S.S.)	2012
•	University of Waterloo Euclid Math Contest, top 25% globally	2011

INTERESTS AND ACTIVITIES

- University of Waterloo First Year Engineering Leadership Conference (FYELC) Chair, inaugural conference
- Engineering Society ECE Class Representative, Voting Member, UWaterloo
- Education Outreach Director, encourage STEM through organizing events at local museums
- UWaterloo Engineering Ambassador Electrical Department Representative
- University of Waterloo Engineering Orientation Week Leader 2013, 2014
- Literary arts, volleyball, researching technology/start-ups