ECE 571
Introduction to SystemVerilog
Winter 2021
Final Project

You and as many as three teammates will choose your own final project with instructor approval. For your final project you will describe a digital system in SystemVerilog and create a SystemVerilog testbench to verify it.

Suitable projects

You can create a design of your own and describe it in SystemVerilog, or use a design (partial or complete) for another source (e.g. a 5-stage pipelined RISC-V processor with bypassing and forwarding from the Hennessey and Patterson computer architecture textbook) that may be described in detail but for which there isn't an existing description in SystemVerilog. You can even start with a design for which there is already a description in another HDL (e.g. VHDL or Verilog). You can find these on www.opencores.org and other sites.

Consider both the amount of work and the kind of work you'll need to do to get a working SystemVerilog description of the design. Your work should be focused primarily on creating and verifying a SystemVerilog model, not necessarily designing a complicated system. However, if you start with existing design code you'll be required to do much more work and coding on the verification part of the project.

Project Proposal

Your project proposal should be brief but describe the work you propose doing and the names of all team members. Identify any existing design work you intend to use and its source. Be clear about your team's contribution. Briefly describe your verification approach.

Note that if you're starting with a *working* HDL design, the only errors your testbench will find are those that you accidentally introduced in the design when translating to SystemVerilog (though there have been some surprises finding bugs in designs that have been around for a long time). You may need to intentionally inject a few errors into the design in this case in order to exercise your testbench.

Presentation

You will make a 20-minute presentation in class at the end of the term. Each teammate must participate in the presentation.

Grading

Your grade will be based on several factors:

- The difficulty of your project, considering both the difficulty and amount of effort to create the SystemVerilog description of the design and to a lesser extent, the complexity of the design itself. This will take into consideration your starting point (e.g. a completely original design, an existing design but no HDL, existing HDL that you convert to SystemVerilog). Naturally, the more original work you do, the better your grade can be. For example, while it's a suitable project, if you begin with a working Verilog description of a simple MIPS processor and you only need to convert parts of it to SystemVerilog that's a less ambitious project than, say, writing the SystemVerilog from scratch for an existing design that's described in a textbook.

- The appropriate use you make of SystemVerilog constructs in the model and testbench. Aside from specific constructs for design (e.g. new procedural blocks), consider the use of interfaces if appropriate. Consider using assertions. In your testbench give thought to structure and reusability. Where appropriate consider both directed and constrained random approaches to verification.

- Your in-class presentation. Be sure to walk the class through your project, describing your starting point (what is the design, what existing design descriptions -- if any -- did you use), what was your test strategy, what is the structure of the implementation?