

Project 2: MIPS SIM on Python

Activity log:

Time / Location	Activity	Achieved / To-Do	Member(s)
Feb 22, 2019 SEL 2nd floor Computer lab	In-person group meeting	discussed overall meeting schedule, various approaches for PRPG selection. Arithmetic, logic functions, github setup	Alex, Vishal, Vitaly
Feb 24, 2019 WhatsApp Group	Remotely,	arrays for instructions, test cases, some transformations of code to allow for branching instructions.	Alex, Vishal, Vitaly
Feb 26, 2019 Library	In-person group discussion	discuss the lw/sw formula and worked on jump and some test cases	Alex, Vishal, Vitaly
Feb 25, 2019 After class, classroom	In-person group meeting	LW, SW, jump, or, xor, test cases, bug fixing	Alex, Vishal, Vitaly
Feb 27, 2019 After class, classroom	In-person group meeting	Discussion of responsibilities for the remainder of the project. PRPG code, Test cases, Report	Alex, Vishal, Vitaly
Feb 28, 2019 WhatsApp Group	Remotely,	Finishing touches, report, testing	Alex, Vishal, Vitaly

List of activities by yourself:

VISHAL
Mon Feb 25: we had a meeting before class, after class started working on lw/sw memory instructions, spent 4-5 hours.
Tue Feb 26: had some issues with lw/sw address calculations, I went to see prof. Rao at 3pm By the end of the day figured out the right equation to calculate right address in python Also worked on some test cases.
Wed Feb 27: worked on test case 4a and 4b also figured out issues with program and spent few hours debugging, also I took my project 1 code and changed into Hex code and started running prpg program on python which led to more issues, I spent almost half of my day working on project. Eventually started testing seeds and was able to get expected result for 4 seeds by the end of the day
Thu Feb 28: as I had issues with prpg, I spent a lot of time debugging in mips as well as in python, solved many issues with help of group partners, at the end I was able to get simulator working. Then, I started working on report and double checked all test cases and organized repository.
In short, I implemented memory instructions, add instruction, part of prpg program and a lot of debugging and few test cases.

I) Test cases

#1A

0x20080019 #addi \$8, \$0, 25

0x2108ffdc #addi \$8, \$8, -36

0x01084821 #addu \$9, \$8, \$8

0x01284821 #addu \$9, \$9, \$8

0x00095022 #sub \$10, \$0, \$9

0x010a4822 #sub \$9, \$8, \$10

0x0009502a #slt \$10, \$0, \$9

0x010a582a #slt \$11, \$8, \$10

0x1000ffff #end: beq \$0, \$0, end

The screenshot displays a MIPS simulator interface with three main components: a console window on the left, a registers window on the right, and an instruction statistics window at the bottom right.

Console Window: Shows the execution of a MIPS program. The PC is 32. The instruction count is 9. The register values are as follows:

Register	Value
Register 0	0
Register 1	0
Register 2	0
Register 3	0
Register 4	0
Register 5	0
Register 6	0
Register 7	0
Register 8	-11
Register 9	-44
Register 10	0
Register 11	1
Register 12	0
Register 13	0
Register 14	0
Register 15	0
Register 16	0
Register 17	0
Register 18	0
Register 19	0
Register 20	0
Register 21	0
Register 22	0
Register 23	0

Memory values at addresses 0x2000 to 0x2010 are all 0.

Registers Window: Shows the state of the MIPS registers. The registers are organized into three tabs: Registers, Coproc 1, and Coproc 0. The registers are listed with their names, numbers, and values.

Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	-11
\$t1	9	-44
\$t2	10	0
\$t3	11	1
\$t4	12	0
\$t5	13	0
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	6144
\$sp	29	16380
\$fp	30	0
\$ra	31	0
pc		32
hi		0
lo		0

Instruction Statistics Window: Shows the distribution of instruction types. The total number of instructions is 9.

Instruction Type	Count	Percentage
Total	9	
ALU	4	44%
Jump	0	0%
Branch	1	11%
Memory	0	0%
Other	4	44%

The window also includes a Tool Control section with buttons for Disconnect from MIPS, Reset, and Close.

#1B

```
0x200c0038 #addi $12, $0, 56
0x200d000c #addi $13, $0, 12
0x200effea #addi $14, $0, -22
0x01cd7022 #sub $14, $14, $13
0x018e802a #slt $16, $12, $14
0x018d6022 #sub $12, $12, $13
0x01c0782a #slt $15, $14, $0
0x020f8822 #sub $17, $16, $15
0x1000ffff #end: beq $0, $0, end
```

The screenshot displays a MIPS simulator interface. On the left, a black console window shows the execution of a program, including the instruction count (9) and the final values of registers \$0 through \$23. Below the console is a table with two columns: 'Value (+18)' and 'Value (+1c)'. The main window is divided into two panes. The top pane, titled 'Registers', shows a list of registers from \$zero to \$lo, with their corresponding numbers and values. The bottom pane, titled 'Instruction Statistics, Version 1.0 (Ingo Kofler)', displays the total number of instructions (9) and a breakdown by type: ALU (6, 67%), Branch (1, 11%), Memory (0), and Other (2, 22%). At the bottom of the statistics pane are buttons for 'Disconnect from MIPS', 'Reset', and 'Close'.

END PROGRAM
PC: 32
Instruction Count: 9
Register 0 : 0
Register 1 : 0
Register 2 : 0
Register 3 : 0
Register 4 : 0
Register 5 : 0
Register 6 : 0
Register 7 : 0
Register 8 : 0
Register 9 : 0
Register 10 : 0
Register 11 : 0
Register 12 : 44
Register 13 : 12
Register 14 : -34
Register 15 : 1
Register 16 : 0
Register 17 : -1
Register 18 : 0
Register 19 : 0
Register 20 : 0
Register 21 : 0
Register 22 : 0
Register 23 : 0
0x2000 : 0
0x2004 : 0
0x2008 : 0
0x200c : 0
0x2010 : 0
0x2014 : 0
0x2018 : 0

Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	0
\$t1	9	0
\$t2	10	0
\$t3	11	0
\$t4	12	44
\$t5	13	12
\$t6	14	-34
\$t7	15	1
\$s0	16	0
\$s1	17	-1
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	6144
\$sp	29	16380
\$fp	30	0
\$ra	31	0
pc		32
hi		0
lo		0

Instruction Statistics, Version 1.0 (Ingo Kofler)

Total: 9

ALU: 6 (67%)

Jump: 0

Branch: 1 (11%)

Memory: 0

Other: 2 (22%)

Tool Control

Disconnect from MIPS Reset Close

```
0x34080019 #ori $8, $0, 25
0x3509abcd #ori $9, $8, 0xabcd
0x340aff00 #ori $10, $0, 0xff00
0x012a5024 #and $10, $9, $10
0x00094c00 #sll $9, $9, 16
0x3529ef80 #ori $9, $9, 0xEF80
0x000958c2 #srl $11, $9, 3
0x000b6042 #srl $12, $11, 1
0x1000ffff #end: beq $0, $0, end
```

```

END PROGRAM
PC: 32

Instruction Count: 9
Register 0 : 0
Register 1 : 0
Register 2 : 0
Register 3 : 0
Register 4 : 0
Register 5 : 0
Register 6 : 0
Register 7 : 0
Register 8 : 25
Register 9 : -1411518592
Register 10 : 43776
Register 11 : 360431088
Register 12 : 180215544
Register 13 : 0
Register 14 : 0
Register 15 : 0
Register 16 : 0
Register 17 : 0
Register 18 : 0
Register 19 : 0
Register 20 : 0
Register 21 : 0
Register 22 : 0
Register 23 : 0

0x2000 : 0
0x2004 : 0
0x2008 : 0
0x200c : 0
0x2010 : 0

```

Register	Coproc 1	Coproc 0
Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	25
\$t1	9	-1411518592
\$t2	10	43776
\$t3	11	360431088
\$t4	12	180215544
\$t5	13	0
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	6144
\$sp	29	16380
\$fp	30	0
\$ra	31	0
pc		32
hi		0
lo		0

Value (+18)	Value (+1c)
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0

Instruction Statistics, Version 1.0 (Ingo Kofler)

Total: 9

ALU: 8 89%

Jump: 0 0%

Branch: 1 11%

Memory: 0 0%

Other: 0 0%

Tool Control

Disconnect from MIPS
Reset
Close

```
0x340d002c #ori $13,$0,44
0x340ef4ea #ori $14,$0,62698
0x01ae7824 #and $15,$13,$14
0x000f7902 #srl $15,$15,4
0x01ed8024 #and $16,$15,$13
0x00108200 #sll $16,$16,8
0x000d6882 #srl $13,$13,2
0x36110ff0 #ori $17,$16,4080
0x1000ffff #end: beq $0, $0, end
```

```

END PROGRAM
PC: 32

Instruction Count: 9
Register 0 : 0
Register 1 : 0
Register 2 : 0
Register 3 : 0
Register 4 : 0
Register 5 : 0
Register 6 : 0
Register 7 : 0
Register 8 : 0
Register 9 : 0
Register 10 : 0
Register 11 : 0
Register 12 : 0
Register 13 : 11
Register 14 : 62698
Register 15 : 2
Register 16 : 0
Register 17 : 4080
Register 18 : 0
Register 19 : 0
Register 20 : 0
Register 21 : 0
Register 22 : 0
Register 23 : 0

0x2000 : 0
0x2004 : 0
0x2008 : 0
0x200c : 0
0x2010 : 0
0x2014 : 0
0x2018 : 0

```

Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	0
\$t1	9	0
\$t2	10	0
\$t3	11	0
\$t4	12	0
\$t5	13	11
\$t6	14	62698
\$t7	15	2
\$s0	16	0
\$s1	17	4080
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	6144
\$sp	29	16380
\$fp	30	0
\$ra	31	0
pc		32
hi		0
lo		0

Value (+18)	Value (+1c)
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0

Instruction Statistics, Version 1.0 (Ingo Kofler)

Total:

ALU:

Jump:

Branch:

Memory:

Other:

Disconnect from MIPS
Reset
Close


```
0x20080020
0x3409abcd
0x00094c00
0x3529ef12
0x200a0001
0x00005821
0x012a6024
0x11800001
0x216b0001
0x00094842
0x2108ffff
0x1500ffa
0x1000ffff
```

[illegible]

```
0x08000002 #j jump
0x200d000d #addi $13, $0, 13
```

#jump:

```
0x2008000a #addi $8, $0, 10
```

```
0x20140000 #addi $20, $0, 0
```

```
0x11800004 #beq $12, $0, skip
```

```
#loop:
```

```
0x3529ef12 #ori $9, $9, 0xef12
```

0x214a0002 #addi \$10, \$10, 2

```
0x00005821 #addu $11, $0, $0
```

```
0x22940001 #addi $20, $20,1
```

#skip:

```
0x2108ffff #addi $8, $8, -1
```

```
0x1500fffa #bne $8, $0, loop
```

0x1000ffff

The screenshot displays the MIPS simulator interface with three main panels:

- Registers Panel (Top):** Shows the state of 32 registers. Registers 0-10 contain 0, Register 11 contains 61202, Register 12 contains 18, and Register 13 contains 61202. Registers 14-23 contain 0. The memory dump below shows addresses 0x2000 to 0x2018, all containing 0.
- Instruction Statistics Panel (Bottom Left):** A table showing the distribution of instruction types:

Value (+18)	Value (+1c)
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
0	0
- Registers Panel (Bottom Right):** A detailed view of the registers, showing the Name, Number, and Value. The registers are grouped into Coprocessor 0 and Coprocessor 1. The values are: \$zero (0), \$at (1), \$v0 (2), \$v1 (3), \$a0 (4), \$a1 (5), \$a2 (6), \$a3 (7), \$t0 (8), \$t1 (9), \$t2 (10), \$t3 (11), \$t4 (12), \$t5 (13), \$t6 (14), \$t7 (15), \$s0 (16), \$s1 (17), \$s2 (18), \$s3 (19), \$s4 (20), \$s5 (21), \$s6 (22), \$s7 (23), \$t8 (24), \$t9 (25), \$k0 (26), \$k1 (27), \$gp (28), \$sp (29), \$fp (30), \$ra (31), pc (44), hi (0), lo (0).

Text Segment

Brkt	Address	Code	Basic	Source
<input type="checkbox"/>	0x00000000	0x20082000	addi \$8,\$0,8192	1: addi \$8, \$0, 0x2000
<input type="checkbox"/>	0x00000004	0x2009ffff	addi \$9,\$0,-2	2: addi \$9, \$0, -2
<input type="checkbox"/>	0x00000008	0xad090000	sw \$9,0(\$8)	3: sw \$9, (\$8)
<input type="checkbox"/>	0x0000000c	0xad090004	sw \$9,4(\$8)	4: sw \$9, 4(\$8)
<input type="checkbox"/>	0x00000010	0xad080008	sw \$8,8(\$8)	5: sw \$8, 8(\$8)
<input type="checkbox"/>	0x00000014	0x21080014	addi \$8,\$8,20	6: addi \$8, \$8, 20
<input type="checkbox"/>	0x00000018	0xad09ffff	sw \$9,-4(\$8)	7: sw \$9, -4(\$8)
<input type="checkbox"/>	0x0000001c	0xad09ffff	sw \$9,-8(\$8)	8: sw \$9, -8(\$8)
<input type="checkbox"/>	0x00000020	0xad080000	sw \$8,0(\$8)	9: sw \$8, (\$8)
<input type="checkbox"/>	0x00000024	0x8d0bfff4	lw \$11,-12(\$8)	10: lw \$11, -12(\$8)
<input type="checkbox"/>	0x00000028	0x8db00000	lw \$11,0(\$11)	11: lw \$11, (\$11)
<input type="checkbox"/>	0x0000002c	0x1000ffff	beq \$0,\$0,-1	12: end: beq \$0, \$0, end

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)	Value (+c)	Value (+10)	Value (+14)
0x00002000	-2	-2	8192	-2	-2	8212
0x00002020	0	0	0	0	0	0
0x00002040	0	0	0	0	0	0
0x00002060	0	0	0	0	0	0
0x00002080	0	0	0	0	0	0
0x000020a0	0	0	0	0	0	0
0x000020c0	0	0	0	0	0	0
0x000020e0	0	0	0	0	0	0
0x00002100	0	0	0	0	0	0
0x00002120	0	0	0	0	0	0
0x00002140	0	0	0	0	0	0
0x00002160	0	0	0	0	0	0
0x00002180	0	0	0	0	0	0
0x000021a0	0	0	0	0	0	0

END PROGRAM

PC: 44

Instruction Count: 12

Register 0 : 0
Register 1 : 0
Register 2 : 0
Register 3 : 0
Register 4 : 0
Register 5 : 0
Register 6 : 0
Register 7 : 0
Register 8 : 8212
Register 9 : -2
Register 10 : 0
Register 11 : -2
Register 12 : 0
Register 13 : 0
Register 14 : 0
Register 15 : 0
Register 16 : 0
Register 17 : 0
Register 18 : 0
Register 19 : 0
Register 20 : 0
Register 21 : 0
Register 22 : 0
Register 23 : 0

0x2000 : -2
0x2004 : -2
0x2008 : 8192
0x200c : -2
0x2010 : -2
0x2014 : 8212
0x2018 : 0
0x201c : 0
0x2020 : 0
0x2024 : 0
0x2028 : 0
0x202c : 0
0x2030 : 0
0x2034 : 0
0x2038 : 0
0x203c : 0
0x2040 : 0
0x2044 : 0
0x2048 : 0
0x204c : 0
0x2050 : 0

Registers

Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	8212
\$t1	9	-2
\$t2	10	0
\$t3	11	-2
\$t4	12	0
\$t5	13	0
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	6144
\$sp	29	16380
\$fp	30	0
\$ra	31	0
\$pc		44
\$hi		0
\$lo		0

Instruction Statistics, Version 1.0 (Ingo Kofler)
✕

Total: 12

ALU: 3 25%

Jump: 0 0%

Branch: 1 8%

Memory: 8 67%

Other: 0 0%

Disconnect from MIPS
Reset
Close

```

#4B      #.asm for 4B
0x20082014 #addi $8, $0, 0x2014
0x20090004 #addi $9, $0, 4
0xad090000 #sw $9, ($8)
0xad090004 #sw $9, 4($8)
0xad080008 #sw $8, 8($8)
0x21080014 #addi $8, $8, 20
0xad09fffc #sw $9, -4($8)
0xad09fff8 #sw $9, -8($8)
0xad080000 #sw $8, ($8)
0x8d0bfff4 #lw $11, -12($8)
0x8d6b0000 #lw $11, ($11)
0x1000ffff #end: beq $0, $0, end

```

The screenshot displays a MIPS assembly simulator interface. The main window shows the assembly code being executed, with the instruction count at 12. The registers window on the right shows the state of the MIPS registers, with the PC register at 44. The instruction statistics window at the bottom right shows the breakdown of instructions: 3 ALU, 0 Jump, 1 Branch, 8 Memory, and 0 Other.

Text Segment

Blkpt	Address	Code	Basic
	0x00000000	0x20082014	addi \$8, \$0, 0x2014
	0x00000004	0x20090004	addi \$9, \$0, 4
	0x00000008	0xad090000	sw \$9, (\$8)
	0x0000000c	0xad090004	sw \$9, 4(\$8)
	0x00000010	0xad080008	sw \$8, 8(\$8)
	0x00000014	0x21080014	addi \$8, \$8, 20
	0x00000018	0xad09fffc	sw \$9, -4(\$8)
	0x0000001c	0xad09fff8	sw \$9, -8(\$8)
	0x00000020	0xad080000	sw \$8, (\$8)
	0x00000024	0x8d0bfff4	lw \$11, -12(\$8)
	0x00000028	0x8d6b0000	lw \$11, (\$11)
	0x0000002c	0x1000ffff	end: beq \$0, \$0, end

Registers

Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	8232
\$t1	9	4
\$t2	10	0
\$t3	11	4
\$t4	12	0
\$t5	13	0
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$s8	24	0
\$s9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	6144
\$sp	29	16380
\$fp	30	0
\$ra	31	0
pc		44
hi		0
lo		0

Instruction Statistics, Version 1.0 (Ingo Koffler)

Total: 12

ALU: 3 (25%)

Jump: 0 (0%)

Branch: 1 (8%)

Memory: 8 (67%)

Other: 0

Tool Control: Disconnect from MIPS, Reset, Close

II) PRPG

Q1: Which level does your project achieve? Which PRPG algorithm did your group choose? Why? (up to 5pts will be given to the group(s) which chose the rarest PRPG algorithm.)

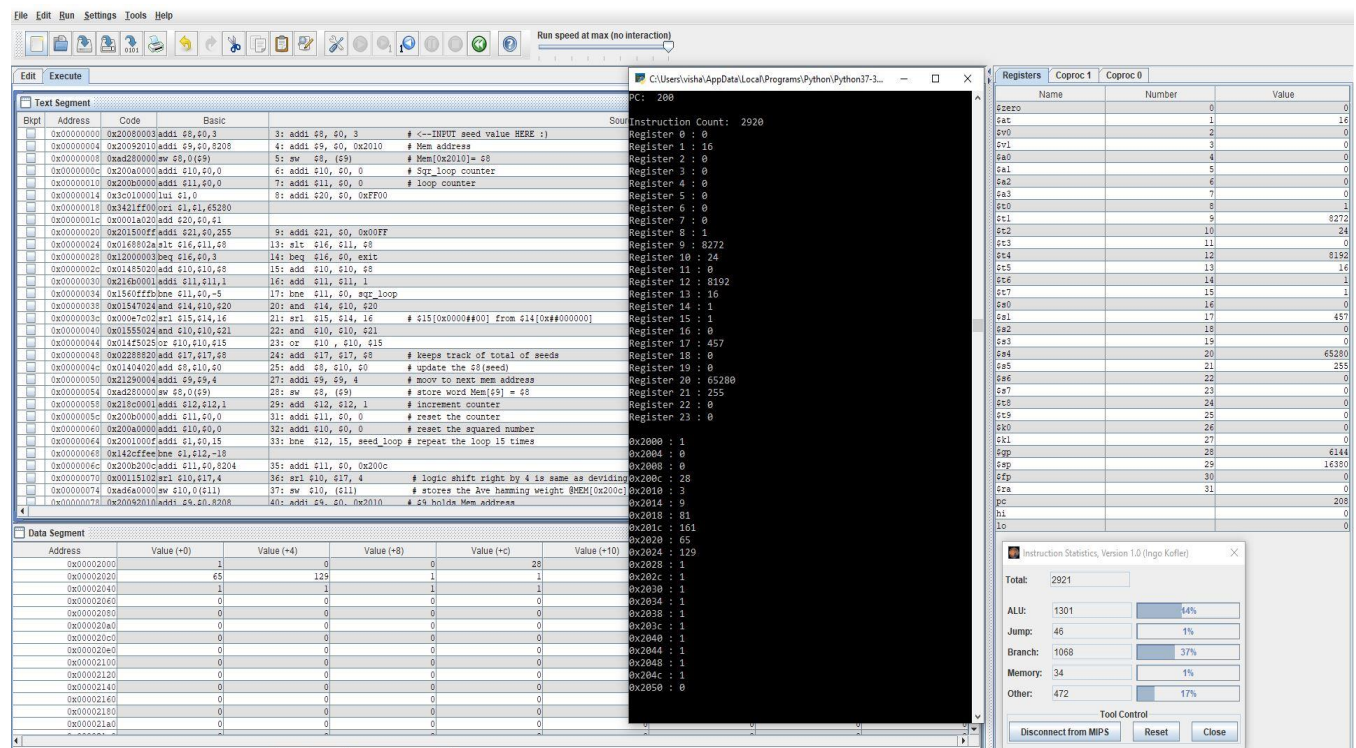
Our project achieves all levels except the “special instruction”. Our program can simulate all the required instructions in Python as well as a few others in order to allow our PRPG implementation to work properly. The PRPG algorithm we used to be the same algorithm from Project 1, squaring the number, dropping the middle 16 bits, and then combining the first and last 8 bits to create another 16-bit number. We chose this method mainly because it was already a working implementation and it allowed us to focus more on the unfinished parts of the Python Simulator.

Q2: How do you verify the correctness of your python simulator, and PRPG code? What kind of resources (productivity tools, collaboration tools) did your group use to work on this project? Give an example of a bug (either in MIPS or python) that your group found out.

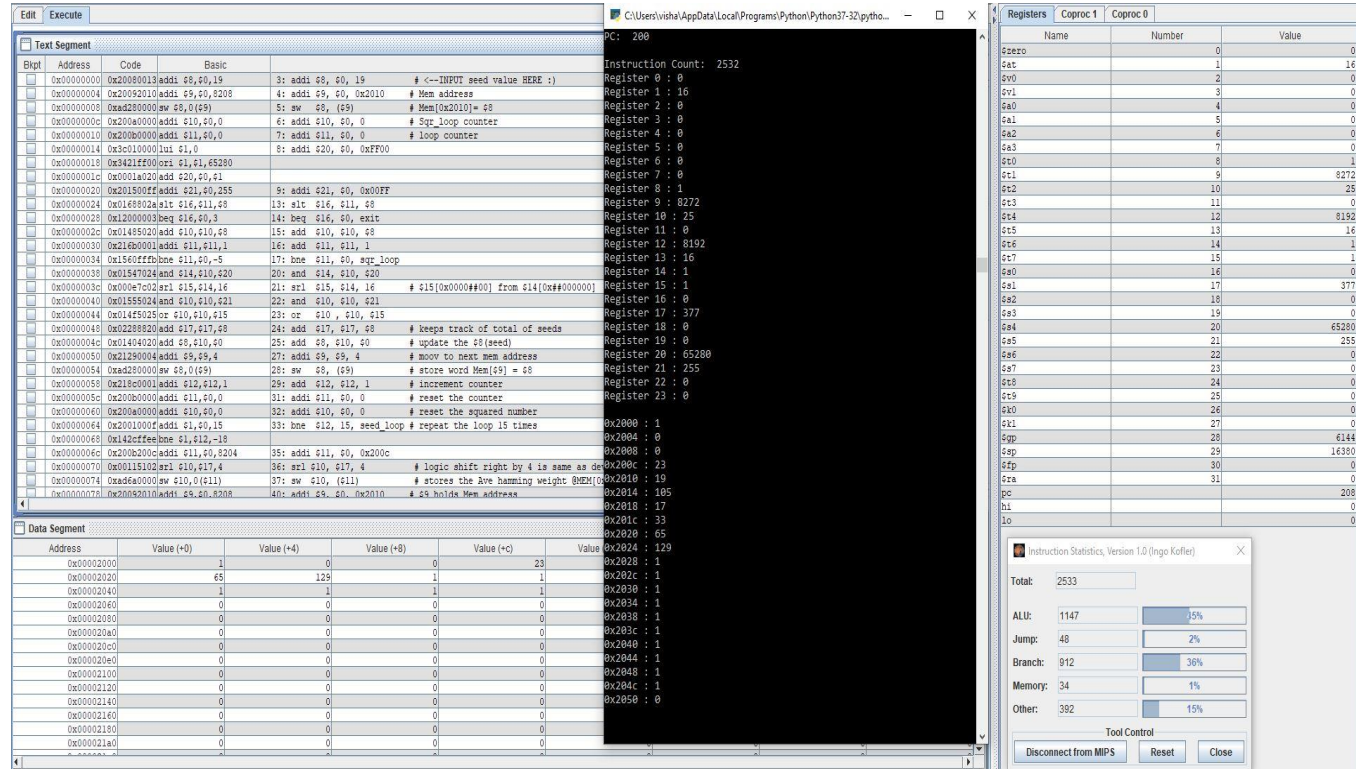
To verify the correctness of our Python Simulator, we constantly referred to MARS with our specific test cases from our project 1 throughout the entirety of the project. Every time we would implement a new section of code for an instruction, we would create a small test case in assembly code to run it in MARS and then verify that we would get the same result from our Python Simulator. Our PRPG code was verified in a similar way. Since we used the original algorithm for our PRPG from Project 1, we already knew that it was fully functional. All we had to do was convert this code from assembly to hexadecimal and then use that in our Python Simulator to verify that the results were the same in both cases. A few collaboration tools our group used to work on the project included GitHub for our version control and WhatsApp for communication. One bug that we encountered during the project was dealing with some of the edge cases for the SLL instruction. In our previous implementations, we always ran into a problem with positive numbers not being shifted correctly because of how `bin()` works in Python. We did not consider that the leading 0's in the binary representation of a number would be left out when the length of the binary string was less than 32 bits. Because of this, the MSB in each binary string would always be a 1, something we obviously did not intend to happen because our code treated all these numbers as negative. To get around this issue, we simply always extended the binary string to 32-bits to allow our code to detect both positive and negative numbers correctly. Also, while I was running the hex code of PRPG on python I encountered issue with large number for example mips tends to convert addi instruction with 34567 immediate into 3 different instructions also mips uses the regular binary bandwidth not the 2's complimented. So as our addi instruction was designed for negative and positive number But for some reason our code was treating 34567 number as 2's complimented negative number. To assure that I commented out 3 lines of code which was treating large number as 2's complemented signed negative number. I tested seed being 34567 and it produced correct output. In the end we all did very good job. It was fun experience working with Alex and vitaly.

Show the results and screenshots of your python simulator for your PRPG code.

S0 = 3



S0 = 19



S0 = 24

Text Segment

Inst	Address	Code	Basic
0x00000000	0x20090018	addi \$s0, 24	3: addi \$s, \$0, 24 # <--INPUT seed value HERE :)
0x00000004	0x20092010	addi \$s, \$0, 0x2010	4: addi \$s, \$0, 0x2010 # Mem address
0x00000008	0x20092000	sw \$s, 0(\$s)	5: sw \$s, (\$s) # Mem[0x2010] = \$s
0x0000000c	0x20092000	addi \$t0, \$0, 0	6: addi \$t0, \$0, 0 # Sqr loop counter
0x00000010	0x20092000	addi \$t1, \$0, 0	7: addi \$t1, \$0, 0 # loop counter
0x00000014	0x30010000	lui \$t1, 0	8: addi \$t0, \$0, 0x7F00
0x00000018	0x3421FF00	ori \$t1, \$t1, 65280	
0x0000001c	0x0001A020	add \$t0, \$t0, \$t1	
0x00000020	0x201500FF	addi \$t1, \$0, 0xFF	9: addi \$t1, \$0, 0xFF
0x00000024	0x0168902e	slt \$t1, \$t1, \$s	13: slt \$t1, \$t1, \$s
0x00000028	0x21200003	beq \$t1, \$0, \$t0	14: beq \$t1, \$0, \$t0
0x0000002c	0x01450202	add \$t0, \$t0, \$s	15: add \$t0, \$t0, \$s
0x00000030	0x21200001	addi \$t1, \$t1, 1	16: add \$t1, \$t1, 1
0x00000034	0x1540FFFF	bne \$t1, \$0, \$t0	17: bne \$t1, \$0, \$t0
0x00000038	0x01547024	and \$t4, \$t0, \$t2	20: and \$t4, \$t0, \$t2
0x0000003c	0x000e7C02	ori \$t5, \$t4, 16	21: ori \$t5, \$t4, 16 # \$t5[0x0000#000] from \$t4[0x#0000000]
0x00000040	0x01555024	and \$t0, \$t0, \$t2	22: and \$t0, \$t0, \$t2
0x00000044	0x01450205	or \$t0, \$t0, \$t5	23: or \$t0, \$t0, \$t5
0x00000048	0x02288820	add \$t7, \$t7, \$s	24: add \$t7, \$t7, \$s # keeps track of total of seeds
0x0000004c	0x01404020	add \$t0, \$t0, \$s	25: add \$t0, \$t0, \$s # update the \$t0(seed)
0x00000050	0x21290004	addi \$t5, \$s, 4	27: addi \$t5, \$s, 4 # move to next mem address
0x00000054	0x20200000	sw \$s, 0(\$s)	28: sw \$s, (\$s) # store word Mem[\$s] = \$s
0x00000058	0x21200001	addi \$t2, \$t2, 1	29: add \$t2, \$t2, 1 # increment counter
0x0000005c	0x20200000	addi \$t1, \$t0, 0	31: addi \$t1, \$t0, 0 # reset the counter
0x00000060	0x20200000	addi \$t0, \$t0, 0	32: addi \$t0, \$t0, 0 # reset the squared number
0x00000064	0x2001000F	addi \$t1, \$t0, 15	33: bne \$t2, 15, seed_loop # repeat the loop 15 times
0x00000068	0x142CFFee	bne \$t1, \$t2, -18	
0x0000006c	0x2020200c	addi \$t1, \$t0, 0x200c	35: addi \$t1, \$t0, 0x200c
0x00000070	0x01310202	ori \$t0, \$t7, 4	36: ori \$t0, \$t7, 4 # logic shift right by 4 is same as dividing
0x00000074	0x20400000	sw \$t0, 0(\$t1)	37: sw \$t0, (\$t1) # stores the Ave hamming weight [MEM[0x200c]
0x00000078	0x20092010	addi \$s, \$t0, 0x2010	40: addi \$s, \$t0, 0x2010 # \$s holds Mem address

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)	Value (+c)	Value (+10)
0x00002000	0	0	0	0	0
0x00002004	0	0	0	0	0
0x00002008	0	0	0	0	0
0x0000200c	0	0	0	0	0
0x00002010	0	0	0	0	0
0x00002014	0	0	0	0	0
0x00002018	0	0	0	0	0
0x0000201c	0	0	0	0	0
0x00002020	0	0	0	0	0
0x00002024	0	0	0	0	0
0x00002028	0	0	0	0	0
0x0000202c	0	0	0	0	0
0x00002030	0	0	0	0	0
0x00002034	0	0	0	0	0
0x00002038	0	0	0	0	0
0x0000203c	0	0	0	0	0
0x00002040	0	0	0	0	0
0x00002044	0	0	0	0	0
0x00002048	0	0	0	0	0
0x0000204c	0	0	0	0	0
0x00002050	0	0	0	0	0
0x00002054	0	0	0	0	0
0x00002058	0	0	0	0	0
0x0000205c	0	0	0	0	0
0x00002060	0	0	0	0	0
0x00002064	0	0	0	0	0
0x00002068	0	0	0	0	0
0x0000206c	0	0	0	0	0
0x00002070	0	0	0	0	0
0x00002074	0	0	0	0	0
0x00002078	0	0	0	0	0
0x0000207c	0	0	0	0	0
0x00002080	0	0	0	0	0
0x00002084	0	0	0	0	0
0x00002088	0	0	0	0	0
0x0000208c	0	0	0	0	0
0x00002090	0	0	0	0	0
0x00002094	0	0	0	0	0
0x00002098	0	0	0	0	0
0x0000209c	0	0	0	0	0
0x000020a0	0	0	0	0	0
0x000020a4	0	0	0	0	0
0x000020a8	0	0	0	0	0
0x000020ac	0	0	0	0	0
0x000020b0	0	0	0	0	0
0x000020b4	0	0	0	0	0
0x000020b8	0	0	0	0	0
0x000020bc	0	0	0	0	0
0x000020c0	0	0	0	0	0
0x000020c4	0	0	0	0	0
0x000020c8	0	0	0	0	0
0x000020cc	0	0	0	0	0
0x000020d0	0	0	0	0	0
0x000020d4	0	0	0	0	0
0x000020d8	0	0	0	0	0
0x000020dc	0	0	0	0	0
0x000020e0	0	0	0	0	0
0x000020e4	0	0	0	0	0
0x000020e8	0	0	0	0	0
0x000020ec	0	0	0	0	0
0x000020f0	0	0	0	0	0
0x000020f4	0	0	0	0	0
0x000020f8	0	0	0	0	0
0x000020fc	0	0	0	0	0
0x00002100	0	0	0	0	0
0x00002104	0	0	0	0	0
0x00002108	0	0	0	0	0
0x0000210c	0	0	0	0	0
0x00002110	0	0	0	0	0
0x00002114	0	0	0	0	0
0x00002118	0	0	0	0	0
0x0000211c	0	0	0	0	0
0x00002120	0	0	0	0	0
0x00002124	0	0	0	0	0
0x00002128	0	0	0	0	0
0x0000212c	0	0	0	0	0
0x00002130	0	0	0	0	0
0x00002134	0	0	0	0	0
0x00002138	0	0	0	0	0
0x0000213c	0	0	0	0	0
0x00002140	0	0	0	0	0
0x00002144	0	0	0	0	0
0x00002148	0	0	0	0	0
0x0000214c	0	0	0	0	0
0x00002150	0	0	0	0	0
0x00002154	0	0	0	0	0
0x00002158	0	0	0	0	0
0x0000215c	0	0	0	0	0
0x00002160	0	0	0	0	0
0x00002164	0	0	0	0	0
0x00002168	0	0	0	0	0
0x0000216c	0	0	0	0	0
0x00002170	0	0	0	0	0
0x00002174	0	0	0	0	0
0x00002178	0	0	0	0	0
0x0000217c	0	0	0	0	0
0x00002180	0	0	0	0	0
0x00002184	0	0	0	0	0
0x00002188	0	0	0	0	0
0x0000218c	0	0	0	0	0
0x00002190	0	0	0	0	0
0x00002194	0	0	0	0	0
0x00002198	0	0	0	0	0
0x0000219c	0	0	0	0	0
0x000021a0	0	0	0	0	0
0x000021a4	0	0	0	0	0
0x000021a8	0	0	0	0	0
0x000021ac	0	0	0	0	0
0x000021b0	0	0	0	0	0
0x000021b4	0	0	0	0	0
0x000021b8	0	0	0	0	0
0x000021bc	0	0	0	0	0
0x000021c0	0	0	0	0	0
0x000021c4	0	0	0	0	0
0x000021c8	0	0	0	0	0
0x000021cc	0	0	0	0	0
0x000021d0	0	0	0	0	0
0x000021d4	0	0	0	0	0
0x000021d8	0	0	0	0	0
0x000021dc	0	0	0	0	0
0x000021e0	0	0	0	0	0
0x000021e4	0	0	0	0	0
0x000021e8	0	0	0	0	0
0x000021ec	0	0	0	0	0
0x000021f0	0	0	0	0	0
0x000021f4	0	0	0	0	0
0x000021f8	0	0	0	0	0
0x000021fc	0	0	0	0	0
0x00002200	0	0	0	0	0
0x00002204	0	0	0	0	0
0x00002208	0	0	0	0	0
0x0000220c	0	0	0	0	0
0x00002210	0	0	0	0	0
0x00002214	0	0	0	0	0
0x00002218	0	0	0	0	0
0x0000221c	0	0	0	0	0
0x00002220	0	0	0	0	0
0x00002224	0	0	0	0	0
0x00002228	0	0	0	0	0
0x0000222c	0	0	0	0	0
0x00002230	0	0	0	0	0
0x00002234	0	0	0	0	0
0x00002238	0	0	0	0	0
0x0000223c	0	0	0	0	0
0x00002240	0	0	0	0	0
0x00002244	0	0	0	0	0
0x00002248	0	0	0	0	0
0x0000224c	0	0	0	0	0
0x00002250	0	0	0	0	0
0x00002254	0	0	0	0	0
0x00002258	0	0	0	0	0
0x0000225c	0	0	0	0	0
0x00002260	0	0	0	0	0
0x00002264	0	0	0	0	0
0x00002268	0	0	0	0	0
0x0000226c	0	0	0	0	0
0x00002270	0	0	0	0	0
0x00002274	0	0	0	0	0
0x00002278	0	0	0	0	0
0x0000227c	0	0	0	0	0
0x00002280	0	0	0	0	0
0x00002284	0	0	0	0	0
0x00002288	0	0	0	0	0
0x0000228c	0	0	0	0	0
0x00002290	0	0	0	0	0
0x00002294	0	0	0	0	0
0x00002298	0	0	0	0	0
0x0000229c	0	0	0	0	0
0x000022a0	0	0	0	0	0
0x000022a4	0	0	0	0	0
0x000022a8	0	0	0	0	0
0x000022ac	0	0	0	0	0
0x000022b0	0	0	0	0	0
0x000022b4	0	0	0	0	0
0x000022b8	0	0	0	0	0
0x000022bc	0	0	0	0	0
0x000022c0	0	0	0	0	0
0x000022c4	0	0	0	0	0
0x000022c8	0	0	0	0	0
0x000022cc	0	0	0	0	0
0x000022d0	0	0	0	0	0
0x000022d4	0	0	0	0	0
0x000022d8	0	0	0	0	0
0x000022dc	0	0	0	0	0
0x000022e0	0	0	0	0	0
0x000022e4	0	0	0	0	0
0x000022e8	0	0	0	0	0
0x000022ec	0	0	0	0	0
0x000022f0	0	0	0	0	0
0x000022f4	0	0	0	0	0
0x000022f8	0	0	0	0	0
0x000022fc	0	0	0	0	0
0x00002300	0	0	0	0	0
0x00002304	0	0	0	0	0
0x00002308	0	0	0	0	0
0x0000230c	0	0	0	0	0
0x00002310	0	0	0	0	0
0x00002314	0	0	0	0	0
0x00002318	0	0	0	0	0
0x0000231c	0	0	0	0	0
0x00002320	0	0	0	0	0
0					

S0 = 2019

Text Segment

Bxpt	Address	Code	Basic
0x00000000	0x200007e7	addi \$s, \$0, 2019	3: addi \$s, \$0, 2019 # <--INPUT seed value HERE :)
0x00000004	0x20042010	addi \$s, \$0, 8208	4: addi \$s, \$0, 0x2010 # Mem address
0x00000008	0x20042000	sw \$s, 0(\$s)	5: sw \$s, (\$s) # Mem(0x2010) = \$s
0x0000000c	0x20042000	addi \$t0, \$0, 0	6: addi \$t0, \$0, 0 # Sqr loop counter
0x00000010	0x20042000	addi \$t1, \$0, 0	7: addi \$t1, \$0, 0 # loop counter
0x00000014	0x20010000	lui \$t0, 0	8: addi \$t0, \$0, 0x7f00
0x00000018	0x3421f000	ori \$t1, \$t1, 65280	
0x0000001c	0x0001a020	add \$t0, \$t0, \$t1	
0x00000020	0x201500ff	addi \$t2, \$0, 0x0fff	9: addi \$t2, \$0, 0x0fff
0x00000024	0x0168002e	slt \$t6, \$t1, \$s	13: slt \$t6, \$t1, \$s
0x00000028	0x12000003	beq \$t6, \$0, exit	14: beq \$t6, \$0, exit
0x0000002c	0x01450020	add \$t0, \$t0, \$s	15: add \$t0, \$t0, \$s
0x00000030	0x21600001	addi \$t1, \$t1, 1	16: add \$t1, \$t1, 1
0x00000034	0x1540ff00	bne \$t1, \$0, sqr_loop	17: bne \$t1, \$0, sqr_loop
0x00000038	0x01547024	and \$t4, \$t0, \$t0	20: and \$t4, \$t0, \$t0
0x0000003c	0x000e7c00	ori \$t5, \$t4, 16	21: srl \$t5, \$t4, 16 # \$t5(0x000e7c00) from \$t4(0x#00000000)
0x00000040	0x01555024	and \$t0, \$t0, \$t1	22: and \$t0, \$t0, \$t1
0x00000044	0x014f5028	or \$t0, \$t0, \$t5	23: or \$t0, \$t0, \$t5
0x00000048	0x02288020	add \$t7, \$t7, \$s	24: add \$t7, \$t7, \$s # keeps track of total of seeds
0x0000004c	0x01404020	add \$t0, \$t0, \$s	25: add \$t0, \$t0, \$s # update the \$s(seed)
0x00000050	0x21290004	addi \$s, \$s, 4	27: addi \$s, \$s, 4 # move to next mem address
0x00000054	0x202f0000	sw \$s, 0(\$s)	28: sw \$s, (\$s) # store word Mem(\$s) = \$s
0x00000058	0x21800001	addi \$t2, \$t2, 1	29: add \$t2, \$t2, 1 # increment counter
0x0000005c	0x202b0000	addi \$t1, \$t0, 0	31: addi \$t1, \$t0, 0 # reset the counter
0x00000060	0x202a0000	addi \$t0, \$t0, 0	32: addi \$t0, \$t0, 0 # reset the squared number
0x00000064	0x2001000f	addi \$t0, \$t0, 15	33: bne \$t2, 15, seed_loop # repeat the loop 15 times
0x00000068	0x142cffee	bne \$t2, \$t2, -18	
0x0000006c	0x200b000c	addi \$t1, \$t0, 8204	35: addi \$t1, \$t0, 0x200c
0x00000070	0x01151028	srl \$t0, \$t7, 4	36: srl \$t0, \$t7, 4 # logic shift right by 4 is same as deviding
0x00000074	0x204e0000	sw \$t0, 0(\$t1)	37: sw \$t0, (\$t1) # stores the Ave hanning weight (BHM(0x204e0000))
0x00000078	0x20042001	addi \$s, \$0, 8208	40: addi \$s, \$0, 0x2010 # \$s holds Mem address

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)	Value (+c)	Value (+10)
0x00002000	2	0	0	166	0x2028 : 1
0x00002020	65	129	1	1	0x202c : 1
0x00002040	1	1	1	1	0x2030 : 1
0x00002060	0	0	0	0	0x2034 : 1
0x00002080	0	0	0	0	0x2038 : 1
0x000020a0	0	0	0	0	0x203c : 1
0x000020c0	0	0	0	0	0x2040 : 1
0x000020e0	0	0	0	0	0x2044 : 1
0x00002100	0	0	0	0	0x2048 : 1
0x00002120	0	0	0	0	0x204c : 1
0x00002140	0	0	0	0	0x2050 : 0
0x00002160	0	0	0	0	
0x00002180	0	0	0	0	
0x000021a0	0	0	0	0	

Registers

Name	Number	Value
\$zero	0	0
\$at	1	16
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	1
\$t1	9	8272
\$t2	10	32
\$t3	11	0
\$t4	12	8192
\$t5	13	16
\$t6	14	1
\$t7	15	1
\$s0	16	0
\$s1	17	2665
\$s2	18	0
\$s3	19	0
\$s4	20	65280
\$s5	21	255
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	6144
\$sp	29	16380
\$fp	30	0
\$ra	31	0
\$pc		208
\$hi		0
\$lo		0

Instruction Statistics, Version 1.0 (Ingo Koller)

Total: 14042

ALU: 5759 (41%)

Jump: 59 (0%)

Branch: 5510 (39%)

Memory: 34 (0%)

Other: 2880 (19%)

Tool Control: Disconnect from MIPS, Reset, Close

S0 = 34567

Text Segment

Bxpt	Address	Code	Basic
0x00000000	0x3c010000	lui \$t0, 0	3: addi \$s, \$0, 34567 # <--INPUT seed value HERE :)
0x00000004	0x34218707	ori \$t1, \$t1, 34567	
0x00000008	0x00014020	add \$s, \$0, \$t0	
0x0000000c	0x20042010	addi \$s, \$0, 8208	4: addi \$s, \$0, 0x2010 # Mem address
0x00000010	0x20042000	sw \$s, 0(\$s)	5: sw \$s, (\$s) # Mem(0x2010) = \$s
0x00000014	0x20042000	addi \$t0, \$0, 0	6: addi \$t0, \$0, 0 # Sqr loop counter
0x00000018	0x20042000	addi \$t1, \$0, 0	7: addi \$t1, \$0, 0 # loop counter
0x0000001c	0x20010000	lui \$t0, 0	8: addi \$t0, \$0, 0x7f00
0x00000020	0x3421f000	ori \$t1, \$t1, 65280	
0x00000024	0x0001a020	add \$t0, \$t0, \$t1	
0x00000028	0x201500ff	addi \$t2, \$0, 0x0fff	9: addi \$t2, \$0, 0x0fff
0x0000002c	0x0168002e	slt \$t6, \$t1, \$s	13: slt \$t6, \$t1, \$s
0x00000030	0x12000003	beq \$t6, \$0, exit	14: beq \$t6, \$0, exit
0x00000034	0x01450020	add \$t0, \$t0, \$s	15: add \$t0, \$t0, \$s
0x00000038	0x21600001	addi \$t1, \$t1, 1	16: add \$t1, \$t1, 1
0x0000003c	0x1540ff00	bne \$t1, \$0, sqr_loop	17: bne \$t1, \$0, sqr_loop
0x00000040	0x01547024	and \$t4, \$t0, \$t0	20: and \$t4, \$t0, \$t0
0x00000044	0x000e7c00	ori \$t5, \$t4, 16	21: srl \$t5, \$t4, 16 # \$t5(0x000e7c00) from \$t4(0x#00000000)
0x00000048	0x01555024	and \$t0, \$t0, \$t1	22: and \$t0, \$t0, \$t1
0x0000004c	0x014f5028	or \$t0, \$t0, \$t5	23: or \$t0, \$t0, \$t5
0x00000050	0x02288020	add \$t7, \$t7, \$s	24: add \$t7, \$t7, \$s # keeps track of total of seeds
0x00000054	0x01404020	add \$t0, \$t0, \$s	25: add \$t0, \$t0, \$s # update the \$s(seed)
0x00000058	0x21290004	addi \$s, \$s, 4	27: addi \$s, \$s, 4 # move to next mem address
0x0000005c	0x202f0000	sw \$s, 0(\$s)	28: sw \$s, (\$s) # store word Mem(\$s) = \$s
0x00000060	0x21800001	addi \$t2, \$t2, 1	29: add \$t2, \$t2, 1 # increment counter
0x00000064	0x202b0000	addi \$t1, \$t0, 0	31: addi \$t1, \$t0, 0 # reset the counter
0x00000068	0x202a0000	addi \$t0, \$t0, 0	32: addi \$t0, \$t0, 0 # reset the squared number
0x0000006c	0x2001000f	addi \$t0, \$t0, 15	33: bne \$t2, 15, seed_loop # repeat the loop 15 times
0x00000070	0x142cffee	bne \$t2, \$t2, -18	
0x00000074	0x200b000c	addi \$t1, \$t0, 8204	35: addi \$t1, \$t0, 0x200c
0x00000078	0x01151028	srl \$t0, \$t7, 4	36: srl \$t0, \$t7, 4 # logic shift right by 4 is same as deviding

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)	Value (+c)	Value (+10)
0x00002000	1	0	0	2190	3150x2028 : 1
0x00002020	129	1	1	1	0x202c : 1
0x00002040	1	1	1	1	0x2030 : 1
0x00002060	0	0	0	0	0x2034 : 1
0x00002080	0	0	0	0	0x2038 : 1
0x000020a0	0	0	0	0	0x203c : 1
0x000020c0	0	0	0	0	0x2040 : 1
0x000020e0	0	0	0	0	0x2044 : 1
0x00002100	0	0	0	0	0x2048 : 1
0x00002120	0	0	0	0	0x204c : 1
0x00002140	0	0	0	0	0x2050 : 0
0x00002160	0	0	0	0	
0x00002180	0	0	0	0	
0x000021a0	0	0	0	0	

Registers

Name	Number	Value
\$zero	0	0
\$at	1	16
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	1
\$t1	9	8272
\$t2	10	28
\$t3	11	0
\$t4	12	8192
\$t5	13	16
\$t6	14	1
\$t7	15	1
\$s0	16	0
\$s1	17	35045
\$s2	18	0
\$s3	19	0
\$s4	20	65280
\$s5	21	255
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	6144
\$sp	29	16380
\$fp	30	0
\$ra	31	0
\$pc		216
\$hi		0
\$lo		0

Instruction Statistics, Version 1.0 (Ingo Koller)

Total: 175920

ALU: 70509 (41%)

Jump: 56 (0%)

Branch: 70254 (39%)

Memory: 34 (1%)

Other: 35060 (19%)

Tool Control: Disconnect from MIPS, Reset, Close

Appendix

Link to all files:

<https://drive.google.com/open?id=1UNxpsjGiUnXR3a7GlyPbui5rhCf-JpTB>