1. Description

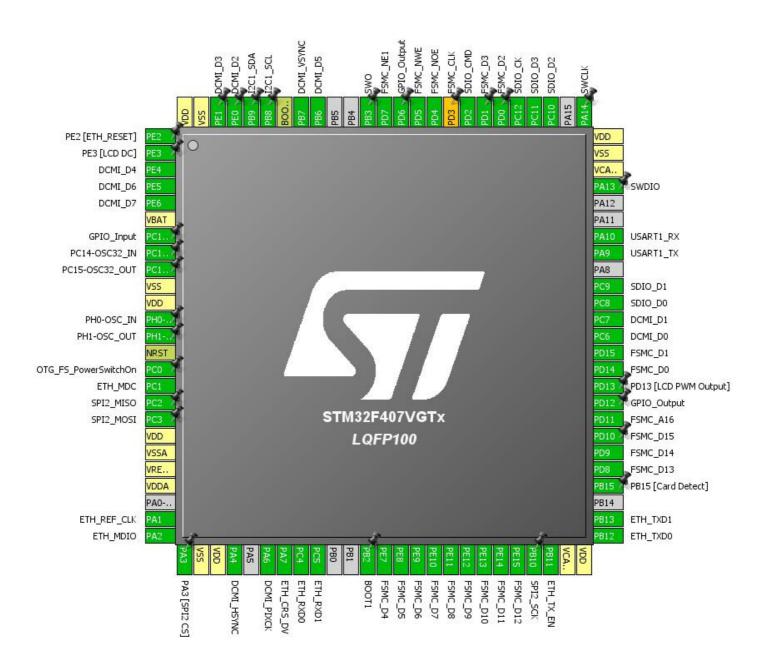
1.1. Project

Project Name	EmbestBoard
Board Name	STM32F407G-DISC1
Generated with:	STM32CubeMX 4.12.0
Date	01/27/2016

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	PE2 [ETH_RESET]
2	PE3 *	I/O	GPIO_Output	PE3 [LCD DC]
3	PE4	I/O	DCMI_D4	
4	PE5	I/O	DCMI_D6	
5	PE6	I/O	DCMI_D7	
6	VBAT	Power		
7	PC13-ANTI_TAMP *	I/O	GPIO_Input	
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	PC14-OSC32_IN
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	PC15-OSC32_OUT
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	PH0-OSC_IN
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	PH1-OSC_OUT
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	OTG_FS_PowerSwitchOn
16	PC1	I/O	ETH_MDC	
17	PC2	I/O	SPI2_MISO	
18	PC3	I/O	SPI2_MOSI	
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
24	PA1	I/O	ETH_REF_CLK	
25	PA2	I/O	ETH_MDIO	
26	PA3 *	I/O	GPIO_Output	PA3 [SPI2 CS]
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	DCMI_HSYNC	
31	PA6	I/O	DCMI_PIXCK	
32	PA7	I/O	ETH_CRS_DV	
33	PC4	I/O	ETH_RXD0	
34	PC5	I/O	ETH_RXD1	
37	PB2 *	I/O	GPIO_Input	BOOT1
38	PE7	I/O	FSMC_D4	
39	PE8	I/O	FSMC_D5	
40	PE9	I/O	FSMC_D6	

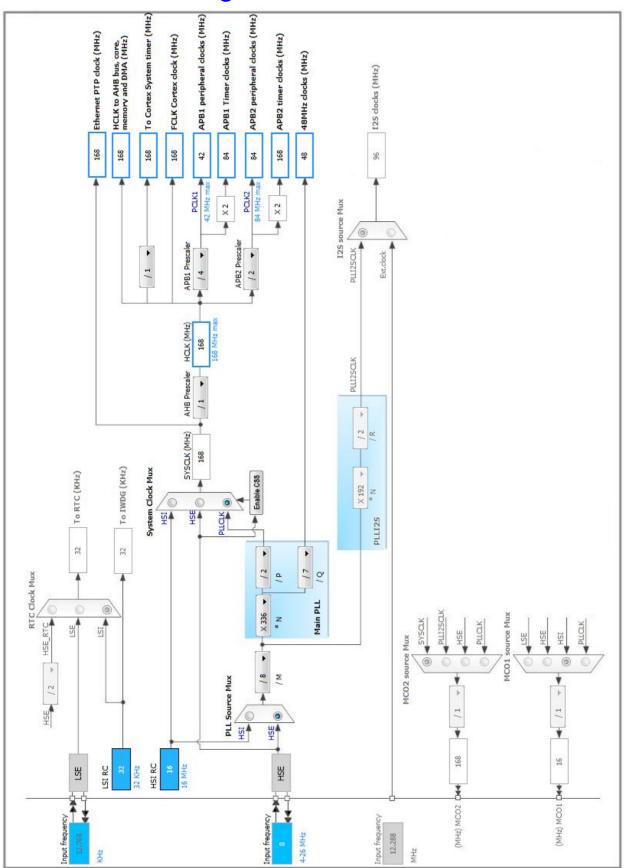
LQFP100	Pin Number	Pin Name	Pin Type	Alternate	Label
Head	LQFP100	LQFP100 (function after		Function(s)	
Head		reset)			
42	41		I/O	FSMC_D7	
Head	42		I/O		
Head	43	PE12	I/O		
Mathematical Part Math	44	PE13	I/O		
47	45	PE14	I/O	FSMC_D11	
Mathematical Part	46	PE15	I/O	FSMC_D12	
Mathematical Property Math	47	PB10	I/O	SPI2_SCK	
SO	48	PB11	I/O	ETH_TX_EN	
51 PB12 I/O ETH_TXD0 52 PB13 I/O ETH_TXD1 54 PB15 * I/O GPIO_Input PB15 [Card Detect] 55 PD8 I/O FSMC_D13 56 PD9 I/O FSMC_D14 57 PD10 I/O FSMC_D15 58 PD11 I/O FSMC_D15 59 PD12 * I/O GPIO_Output 60 PD13 * I/O GPIO_Output PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D0 PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D0 PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D1 PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D1 PD13 [LCD PWM Output] 62 PD15 I/O DCMI_D0 PD13 [LCD PWM Output] 63 PC6 I/O DCMI_D0 PD13 [LCD PWM Output] 64 PC7 I/O DCMI_D0 PD	49	VCAP_1	Power		
52 PB13 I/O ETH_TXD1 54 PB15 * I/O GPIO_Input PB15 [Card Detect] 55 PD8 I/O FSMC_D13 56 PD9 I/O FSMC_D14 57 PD10 I/O FSMC_D15 58 PD11 I/O FSMC_A16 59 PD12 * I/O GPIO_Output 60 PD13 * I/O GPIO_Output PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D0 PD15 [LCD PWM Output] 61 PD14 I/O FSMC_D1 PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D1 PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D1 PD13 [LCD PWM Output] 62 PD15 I/O DCMI_D0 PD13 [LCD PWM Output] 63 PC6 I/O DCMI_D0 PD13 [LCD PWM Output] 64 PC7 I/O DCMI_D0 PD13 [LCD PWM Output] 65 PC8 I/O	50	VDD	Power		
54 PB15 ' I/O GPIO_Input PB15 [Card Detect] 55 PD8 I/O FSMC_D13 56 PD9 I/O FSMC_D14 57 PD10 I/O FSMC_D15 58 PD11 I/O FSMC_D15 59 PD12 ' I/O GPIO_Output 60 PD13 ' I/O GPIO_Output PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D0 PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D1 PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D1 PD13 [LCD PWM Output] 62 PD15 I/O FSMC_D1 PD13 [LCD PWM Output] 63 PC6 I/O DCMI_D0 PD13 [LCD PWM Output] 64 PC7 I/O DCMI_D0 PD13 [LCD PWM Output] 65 PC8 I/O DCMI_D0 DCMI_D0 66 PC9 I/O SDIO_D0 SDIO_D0 68 PA9 I/O	51	PB12	I/O	ETH_TXD0	
S5	52	PB13	I/O	ETH_TXD1	
S66	54	PB15 *	I/O	GPIO_Input	PB15 [Card Detect]
57 PD10 I/O FSMC_D15 58 PD11 I/O FSMC_A16 59 PD12 * I/O GPIO_Output 60 PD13 * I/O GPIO_Output PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D0 PD13 [LCD PWM Output] 61 PD14 I/O FSMC_D1 PD14 [LD PWM Output] PD15 [LD PWM Output] PD14 [LD PWM Output] PD14 [LD PWM Output] PD13 [LCD PWM Output] PD14 [LD PWM Output] PD15 [LD PWM Output] PD15 [LD PWM Output] PD14 [LD PWM Output] PD15 [LD P	55	PD8	I/O	FSMC_D13	
S8	56	PD9	I/O	FSMC_D14	
S9	57	PD10	I/O	FSMC_D15	
Box Box	58	PD11	I/O	FSMC_A16	
61 PD14 I/O FSMC_D0 62 PD15 I/O FSMC_D1 63 PC6 I/O DCMI_D0 64 PC7 I/O DCMI_D1 65 PC8 I/O SDIO_D0 66 PC9 I/O SDIO_D1 68 PA9 I/O USART1_TX 69 PA10 I/O USART1_RX 72 PA13 I/O SYS_JTMS-SWDIO SWDIO 73 VCAP_2 Power 74 VSS Power 75 VDD Power 76 PA14 I/O SYS_JTCK-SWCLK SWCLK 78 PC10 I/O SDIO_D2 79 PC11 I/O SDIO_D3 80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D3 82 PD1 I/O SDIO_CMD	59	PD12 *	I/O	GPIO_Output	
62	60	PD13 *	I/O	GPIO_Output	PD13 [LCD PWM Output]
63	61	PD14	I/O	FSMC_D0	
64 PC7 I/O DCMI_D1 65 PC8 I/O SDIO_D0 66 PC9 I/O SDIO_D1 68 PA9 I/O USART1_TX 69 PA10 I/O USART1_RX 72 PA13 I/O SYS_JTMS-SWDIO SWDIO 73 VCAP_2 Power	62	PD15	I/O	FSMC_D1	
65 PC8 I/O SDIO_D0 66 PC9 I/O SDIO_D1 68 PA9 I/O USART1_TX 69 PA10 I/O USART1_RX 72 PA13 I/O SYS_JTMS-SWDIO SWDIO 73 VCAP_2 Power	63	PC6	I/O	DCMI_D0	
66 PC9 I/O SDIO_D1 68 PA9 I/O USART1_TX 69 PA10 I/O USART1_RX 72 PA13 I/O SYS_JTMS-SWDIO SWDIO 73 VCAP_2 Power 74 VSS Power 75 VDD Power 76 PA14 I/O SYS_JTCK-SWCLK SWCLK 78 PC10 I/O SDIO_D2 79 PC11 I/O SDIO_D3 80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D2 82 PD1 I/O SDIO_CMD	64	PC7	I/O	DCMI_D1	
68 PA9 I/O USART1_TX 69 PA10 I/O USART1_RX 72 PA13 I/O SYS_JTMS-SWDIO SWDIO 73 VCAP_2 Power 74 VSS Power 75 VDD Power 76 PA14 I/O SYS_JTCK-SWCLK SWCLK 78 PC10 I/O SDIO_D2 79 PC11 I/O SDIO_D3 80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D2 82 PD1 I/O SDIO_CMD	65	PC8	I/O	SDIO_D0	
69 PA10 I/O USART1_RX 72 PA13 I/O SYS_JTMS-SWDIO SWDIO 73 VCAP_2 Power Power <td>66</td> <td>PC9</td> <td>I/O</td> <td>SDIO_D1</td> <td></td>	66	PC9	I/O	SDIO_D1	
72 PA13 I/O SYS_JTMS-SWDIO SWDIO 73 VCAP_2 Power 74 VSS Power 75 VDD Power 76 PA14 I/O SYS_JTCK-SWCLK SWCLK 78 PC10 I/O SDIO_D2 79 PC11 I/O SDIO_D3 80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D2 82 PD1 I/O FSMC_D3 83 PD2 I/O SDIO_CMD	68	PA9	I/O	USART1_TX	
73 VCAP_2 Power 74 VSS Power 75 VDD Power 76 PA14 I/O SYS_JTCK-SWCLK SWCLK 78 PC10 I/O SDIO_D2 79 PC11 I/O SDIO_D3 80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D2 82 PD1 I/O FSMC_D3 83 PD2 I/O SDIO_CMD	69	PA10	I/O	USART1_RX	
74 VSS Power 75 VDD Power 76 PA14 I/O SYS_JTCK-SWCLK SWCLK 78 PC10 I/O SDIO_D2 79 PC11 I/O SDIO_D3 80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D2 82 PD1 I/O FSMC_D3 83 PD2 I/O SDIO_CMD	72	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
75 VDD Power 76 PA14 I/O SYS_JTCK-SWCLK SWCLK 78 PC10 I/O SDIO_D2 79 PC11 I/O SDIO_D3 80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D2 82 PD1 I/O FSMC_D3 83 PD2 I/O SDIO_CMD	73	VCAP_2	Power		
76 PA14 I/O SYS_JTCK-SWCLK SWCLK 78 PC10 I/O SDIO_D2 79 PC11 I/O SDIO_D3 80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D2 82 PD1 I/O FSMC_D3 83 PD2 I/O SDIO_CMD	74	VSS	Power		
78 PC10 I/O SDIO_D2 79 PC11 I/O SDIO_D3 80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D2 82 PD1 I/O FSMC_D3 83 PD2 I/O SDIO_CMD	75	VDD	Power		
79 PC11 I/O SDIO_D3 80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D2 82 PD1 I/O FSMC_D3 83 PD2 I/O SDIO_CMD	76	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
80 PC12 I/O SDIO_CK 81 PD0 I/O FSMC_D2 82 PD1 I/O FSMC_D3 83 PD2 I/O SDIO_CMD	78	PC10	I/O	SDIO_D2	
81 PD0 I/O FSMC_D2 82 PD1 I/O FSMC_D3 83 PD2 I/O SDIO_CMD	79	PC11	I/O	SDIO_D3	
82 PD1 I/O FSMC_D3 83 PD2 I/O SDIO_CMD	80	PC12	I/O	SDIO_CK	
83 PD2 I/O SDIO_CMD	81	PD0	I/O	FSMC_D2	
	82	PD1	I/O	FSMC_D3	
0	83	PD2	I/O	SDIO_CMD	
84 PD3 *** I/O FSMC_CLK	84	PD3 **	I/O	FSMC_CLK	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
85	PD4	I/O	FSMC_NOE	
86	PD5	I/O	FSMC_NWE	
87	PD6 *	I/O	GPIO_Output	
88	PD7	I/O	FSMC_NE1	
89	PB3	I/O	SYS_JTDO-SWO	swo
92	PB6	I/O	DCMI_D5	
93	PB7	I/O	DCMI_VSYNC	
94	воото	Boot		
95	PB8	I/O	I2C1_SCL	
96	PB9	I/O	I2C1_SDA	
97	PE0	I/O	DCMI_D2	
98	PE1	I/O	DCMI_D3	
99	VSS	Power		
100	VDD	Power		

^{*} The pin is affected with an I/O function

^{**} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. DCMI

DCMI: Slave 8 bits External Synchro

5.1.1. Parameter Settings:

Mode Config:

Pixel clock polarity Active on Falling edge

Vertical synchronization polarity Active Low Horizontal synchronization polarity Active Low

Frequency of frame capture All frames are captured

JPEG mode Disabled

5.2. ETH

Mode: RMII

5.2.1. Parameter Settings:

Advanced: Ethernet Media Configuration:

Auto Negotiation Enabled

General: Ethernet Configuration:

Ethernet MAC Address 00:80:E1:00:00:00

PHY Address 1

Ethernet Basic Configuration:

Rx Mode Interrupt Mode
TX IP Header Checksum Computation By hardware

5.2.2. Advanced Parameters:

External PHY Configuration:

PHY Reset delay these values are based on a 1 ms 0x000000FF *

Systick interrupt

PHY Configuration delay

Ox00000FFF *

PHY Read TimeOut

Ox0000FFFF *

Ox0000FFFF *

Common: External PHY Configuration:

Transceiver Basic Control Register	0x00 *
Transceiver Basic Status Register	0x01 *
PHY Reset	0x8000 *
Select loop-back mode	0x4000 *
Set the full-duplex mode at 100 Mb/s	0x2100 *
Set the half-duplex mode at 100 Mb/s	0x2000 *
Set the full-duplex mode at 10 Mb/s	0x0100 *
Set the half-duplex mode at 10 Mb/s	0x0000 *
Enable auto-negotiation function	0x1000 *
Restart auto-negotiation function	0x0200 *
Select the power down mode	0x0800 *
Isolate PHY from MII	0x0400 *
Auto-Negotiation process completed	0x0020 *
Valid link established	0x0004 *
Jabber condition detected	0x0002 *

Extended: External PHY Configuration:

PHY status register Offset	0x10 *
MII Interrupt Control Register	0x11 *
MII Interrupt Status and Misc. Control Register	0x12 *
PHY Link mask	0x0001 *
PHY Speed mask	0x0002 *
PHY Duplex mask	0x0004 *
PHY Enable interrupts	0x0002 *
PHY Enable output interrupt events	0x0001 *
Enable Interrupt on change of link status	0x0020 *
HY link status interrupt mask	0x2000 *

5.3. FSMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: set

Memory type: LCD Interface LCD Register Select: A16

Data: 16 bits

5.3.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type LCD Interface

Bank 1 NOR/PSRAM 1

Write operation Enabled
Extended mode Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles 15

Data setup time in HCLK clock cycles 255

Bus turn around time in HCLK clock cycles 15

5.4. I2C1

12C: 12C

5.4.1. Parameter Settings:

Master Features:

I2C Speed Mode Standard Mode

I2C Clock Speed (Hz) 100000

Slave Features:

Clock No Stretch Mode Disabled

Primary Address Length selection 7-bit

Dual Address Acknowledged Disabled

Primary slave address 0

General Call address detection Disabled

5.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

5.5.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled

Prefetch Buffer Enabled

Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

Power Parameters:

Power Regulatror Voltage Scale Power Regulator Voltage Scale 1

5.6. SDIO

Mode: SD 4 bits Wide bus

5.6.1. Parameter Settings:

SDIO parameters:

SDIOCLK clock divide factor

5.7. SPI2

Mode: Full-Duplex Master

5.7.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 2

Baud Rate 21.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled
NSS Signal Type Software

5.8. SYS

Debug: SWD and Asynchronous Trace

5.9. USART1

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

5.10. FATFS

mode: SD Card

5.10.1. Set Defines:

Version:

FATFS version R0.11

Function Parameters:

FS_TINY (Tiny mode)

FS_READONLY (Read-only mode)

Disabled

FS_MINIMIZE (Minimization level)

Disabled

USE_STRFUNC (String functions) Enabled with LF -> CRLF conversion

USE_FIND (Find functions)

USE_MKFS (Make filesystem function)

USE_FORWARD (Forward function)

USE_LABEL (Volume label functions)

USE_FASTSEEK (Fast seek function)

Disabled

USE_FASTSEEK (Fast seek function)

Locale and Namespace Parameters:

CODE_PAGE (Code page on target) Latin 1 (Windows)

USE_LFN (Use Long Filename) Disabled

MAX_LFN (Max Long Filename) 255

LFN_UNICODE (Enable Unicode)

STRF_ENCODE (Character encoding)

FS_RPATH (Relative Path)

Disabled

Physical Drive Parameters:

VOLUMES (Logical drives) 1

MAX_SS (Maximum Sector Size) 512

MIN_SS (Minimum Sector Size) 512

MULTI_PARTITION (Volume partitions feature) Disabled

USE_TRIM (Erase feature) Disabled

FS_NOFSINFO (Force full FAT scan) 0

System Parameters:

FS_NORTC (Timestamp feature) Dynamic timestamp

NORTC_YEAR (Year for timestamp) 2015

NORTC_MON (Month for timestamp) 6

NORTC_MDAY (Day for timestamp) 4

WORD_ACCESS (Platform dependent access option) Byte access FS_REENTRANT (Re-Entrancy) Enabled FS_TIMEOUT (Timeout ticks) 1000

SYNC_t (O/S sync object) osSemaphoreld

FS_LOCK (Number of files opened simultaneously) 2

5.10.2. IPs instances:

SDIO/SDMMC:

SDIO instance SDIO1

5.11. FREERTOS

mode: Enabled

5.11.1. Config parameters:

Versions:

CMSIS-RTOS version 1.02
FreeRTOS version 8.2.1

Kernel settings:

USE_PREEMPTION Enabled

CPU_CLOCK_HZ SystemCoreClock

TICK_RATE_HZ 1000

MAX_PRIORITIES 7 MINIMAL_STACK_SIZE 128 MAX_TASK_NAME_LEN 16 Disabled USE_16_BIT_TICKS Enabled IDLE_SHOULD_YIELD Enabled USE_MUTEXES Enabled USE_RECURSIVE_MUTEXES Enabled USE_COUNTING_SEMAPHORES QUEUE_REGISTRY_SIZE 8 Disabled USE_APPLICATION_TASK_TAG TOTAL_HEAP_SIZE 15360 Memory Management scheme heap_4 USE_ALTERNATIVE_API Disabled ENABLE_BACKWARD_COMPATIBILITY Enabled USE_PORT_OPTIMISED_TASK_SELECTION Disabled Disabled USE_TICKLESS_IDLE

Hook function related definitions:

USE_IDLE_HOOK Disabled
USE_TICK_HOOK Disabled
USE_MALLOC_FAILED_HOOK Disabled
CHECK_FOR_STACK_OVERFLOW Disabled

Run time and task stats gathering related definitions:

USE_TRACE_FACILITY Enabled
GENERATE_RUN_TIME_STATS Disabled

Co-routine related definitions:

USE_CO_ROUTINES Disabled MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Disabled
TIMER_TASK_PRIORITY 2
TIMER_QUEUE_LENGTH 10

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

5.11.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled uxTaskPriorityGet Enabled vTaskDelete Enabled

vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled

5.12. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

5.12.1. General:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX)

1.4.1

DHCP Option:

LWIP_DHCP (DHCP Module) Enabled

RTOS Settings:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)

Enabled

Protocols Options:

 LWIP_ICMP (ICMP Module Activation)
 Enabled

 LWIP_IGMP (IGMP Module)
 Disabled

 LWIP_DNS (DNS Module)
 Disabled

 LWIP_UDP (UDP Module)
 Enabled

 MEMP_NUM_UDP_PCB (Number of UDP Connections)
 4

 LWIP_TCP (TCP Module)
 Enabled

 MEMP_NUM_TCP_PCB (Number of TCP Connections)
 5

5.12.2. All LwIP Options:

Platform Specific Locking:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Disabled
NO_SYS (LwIP Facilities)	LwIP Facilities Enabled
NO_SYS_NO_TIMERS (Drop Support For sys_timeout)	Disabled
Memory Options:	
MEM_SIZE (Heap Memory Size)	1600
Internal Memory Pool Sizes:	
MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1
Pbuf Options:	
PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592
ARP Options:	
LWIP_ARP (ARP Functionality)	Enabled
SNMP Options:	
LWIP_SNMP (SNMP Module)	Disabled
TCP Options:	
TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9
Network Interfaces Options:	
LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Disabled
LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled
Thread Options:	
TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	3
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	0
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	0
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	0
Sequential Layer options:	

LWIP_NETCONN (NETCONN API) Enabled

Socket Options:

LWIP_SOCKET (Socket API) Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names) Enabled

Statistics Options:

LWIP_STATS (Statictics Collection) Disabled

Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **) Disabled CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets) Disabled CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets) Disabled CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets) Disabled CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets) Disabled CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets) Disabled CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets) Disabled CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets) Disabled

5.12.3. Debug:

Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)

ΑII

^{*} User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
DCMI	PE4	DCMI_D4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	DCMI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	DCMI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	DCMI_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	DCMI_PIXCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	DCMI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	DCMI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	DCMI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	DCMI_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE0	DCMI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE1	DCMI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	High *	
FSMC	PE7	FSMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE8	FSMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE9	FSMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE10	FSMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE11	FSMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE12	FSMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE13	FSMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE14	FSMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE15	FSMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD8	FSMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD9	FSMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD10	FSMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max	User Label
	PD11	FOMO A46	Alternate Function Push Pull		Speed	
	PD11	FSMC_A16 FSMC_D0	Alternate Function Push Pull	No pull-up and no pull-down No pull-up and no pull-down	High	
	PD14	FSMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PDIS PD0	FSMC_D1	Alternate Function Push Pull		High	
	PD1	FSMC_D2	Alternate Function Push Pull	No pull-up and no pull-down No pull-up and no pull-down	High High	
	PD4	FSMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD5	FSMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD7	FSMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	High	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	High *	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	High *	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	PC14-OSC32_IN
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	PC15-OSC32_OUT
	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	PH0-OSC_IN
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	PH1-OSC_OUT
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	High	
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	High *	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	SWCLK
	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	SWO
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	High *	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	High *	
Single Mapped Signals	PD3	FSMC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PE2 [ETH_RESET]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PE3 [LCD DC]
	PC13- ANTI_TAMP	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OTG_FS_PowerSwitchOn
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PA3 [SPI2 CS]
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BOOT1
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PB15 [Card Detect]
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PD13 [LCD PWM Output]
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
DCMI	DMA2_Stream1	Peripheral To Memory	Low

DCMI: DMA2_Stream1 DMA request Settings:

Mode: Circular *

Use fifo: Enable *

FIFO Threshold: Full
Peripheral Increment: Disable
Memory Increment: Disable
Peripheral Data Width: Word *
Memory Data Width: Word
Peripheral Burst Size: Single
Memory Burst Size: Single

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	15	0
DMA2 stream1 global interrupt	true	5	0
Ethernet global interrupt	true	5	0
DCMI global interrupt	true	5	0
Non maskable interrupt		unused	
Hard fault interrupt		unused	
Memory management fault		unused	
Pre-fetch fault, memory access fault		unused	
Undefined instruction or illegal state		unused	
Debug monitor		unused	
PVD interrupt through EXTI line 16		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
I2C1 event interrupt		unused	
I2C1 error interrupt		unused	
SPI2 global interrupt		unused	
USART1 global interrupt		unused	
SDIO global interrupt		unused	
Ethernet wake-up interrupt through EXTI line 19		unused	

^{*} User modified value

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VGTx
Datasheet	022152_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	EmbestBoard
Project Folder	C:\Users\Vergil\Documents\Projects\EmbestBB\EmbestBoard
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.10.1

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	