Victor **Perrin**

IC Digital · Verification Engineer

Avenue Tivoli 8, Lausanne, 1007, Switzerland

(+41) 78 613 19 20 | victor.perrin22@gmail.com | vperrin59 | victor-perrin-35707418

Summary

- Very systematic and structured work method.
- Accustomed on learning quickly and facing problems on his own as well as with a team.
- Reliable and able to adapt to any situation, good at mastering new tools.
- Eager to deliver good quality releases with the help of Continuous Integration
- Good knowledge of RTL-GDSII flow. Strong RTL coding skills. Experience in advanced nodes: 16nm
- Covered many aspects of verification: Firmware driven, Assertion based, coverage closure, formal verification, UVM, Verification Planning.

Skills

Front-End	Verilog, SystemVerilog, UVM, SVA, VUnit, DPI, Formal apps (CDC, Lint, ...)
Back-end	Genus, Innovus, Tempus, Voltus, Conformal, Quantus
Continuous Integration	Jenkins, GitLab CI, Git, Mercurial, SOS
Scripting	Shell, Tcl, Python, Makefile, Sphinx
Languages	French, English, Spanish

Experience

KandouBus Switzerland *Lausanne, Switzerland*

Digital IC engineer *May. 2017 - Now*

- Digital design
  - **Top chip lead role in PCIe SoC**
    - Collaboration with cross-functional teams, including architect, hardware, software, and PD teams to ensure that the project's deliverables met the necessary specifications.
    - Experience on designing and implementing LTSSM equalization techniques for PCIe Gen5.
    - Collaborated closely with the IC architecture team, offering expert insights and suggestions to improve their proposed specifications, ultimately resulting in the successful implementation of the project's goals.
    - Conducted thorough review of the verification plan, identified and addressed missing critical checkers, which greatly improved the overall quality and completeness of the verification effort.
  - **Lead role on CPU system implementation**
    - Successfully configured and integrated third-party IPs (I2C, SMB, SPI, ...) into the design, meeting project requirements and resulting in a timely delivery of the project's deliverables.
    - Setup and configured the C toolchain in the simulation environment, enabling efficient and accurate testing and validation of designs.
    - Effectively interfaced with external Design Verification (DV) contractors to ensure seamless integration of their deliverables into the project, resulting in successful project completion.
  - **Implementation of high speed USB SERDES RX blocks (833MHz)**
    - BIST, Eyescope and various calibration blocks (CTLE, equalizers, ...)
    - Implemented CDC scheme block and validated them with CDC formal app.
    - Logic timing optimizations using timing report feedback.
    - Linting analysis with formal app.
    - Wrote detailed documentation of the implemented blocks for the verification and AE team.
    - Developed high level analog model of the whole RX analog chain in SystemVerilog.
    - **Dynamic power analysis and manual data/clock gating insertion**.
  - **Work flow improvement**
    - Developed Jenkins CI flow from scratch, which greatly improved the quality of the RTL releases.
    - **Delivered SVA training for the designers inside the company**.
    - Continuous improvement of the digital development flow (checkers, automation, reconfigurability).
    - Implemented and enforced a Git message policy to ensure clear and consistent communication within the project's code repository.
- Silicon validation
  - **Development of Python scripts and programs for integrated circuit validation, characterization and ATE.**
  - Delivered bring-up and characterization results through Jupyter notebooks
  - Extensive use of python libs (pandas, numpy, matplotlib).
- Functional verification
  - Verification of the SERDES design.
  - Drove coverage analysis and reviewed list of waivers with the design/management team.
  - Optimization of the verification working flow.
    - Setup verification scripting environment based on Python.
    - Development of company UVM base classes and UVCs.
      - Clock and reset agents.
      - Agent and environment base classes.
    - Development of company assertion libraries.
    - **Defined UVM/SVA verification methodology / coding guidelines for the company**.
- Physical design
  - Responsible of **Synthesis and Place and Route flow for a digital SERDES IP in 16nm**.
    - SDC Timing constraints development and validation.
    - Signoff checks:
      - EMIR and power analysis with Voltus.
      - DRC verification.
      - Static Timing Analysis and block-level timing closure with Tempus.
      - Mixed signal STA between analog and digital datapath.

Marvell Switzerland. *Etoy, Switzerland*

Senior Digital IC engineer *Sep. 2011 - May. 2017*

- Functional verification.
  - Assertion Based Verification.
    - Formal model checking of MAC and control based blocks.
    - **Assertions profiling with simulators. Optimization of assertions for Simulation/Formal model checking**.
  - UVM methodology.
    - Constrained Random verification of MAC/PHY blocks.
    - Development of agents, drivers, monitors, scoreboards, observers, sequencers.
    - Developed RAL mechanism into the UVM testbench.
    - Developed full verification environment for LDPC importing System DPI C.
  - Static verification.
    - **Strong experience in formal apps: connectivity, register check, assertion generation**
    - Clock domain crossing / Reset verification with 0in cdc
  - Coverage analysis.
    - Structural coverage (line/expression/condition/toggle/fsm)
    - Functional coverage: defined and implemented covergroups from verification plan
  - Verification Planning.
    - **Verification Lead role on FM project**.
    - **Discussion with design and system team for defining the top verification plan**.
- Digital design.
  - Architecture design, documentation and implementation of LDPC input/output controllers.
  - Set up FPGA scripts for plotting LDPC BER/SNR graph
  - **Optimized memory architecture of front end LDPC** for throughput optimization.
  - DFT LBIST architecture review and designed test control block.

Marvell Switzerland. *Etoy, Switzerland*

Master final internship *Feb. 2011 - Sep. 2011*

- Formal model checking of MAC controller.
- Developed verification plans from specification.
- Implemented assertions, constraints from verification plan (SVA).
- Performed formal model checking.

Education

Politecnico di Torino / Grenoble INP / EPFL *Italy / France / Switzerland*

Master's Degree in Micro and Nano Technologies for Integrated Systems *2006 - 2011*

Lycee Henri Wallon *France*

French High school diploma with honors in Science and Engineering *2006*