IUSC Clocking Tree

Receiver

Transmitter

RxC Pin (Output)

TxC Pin (Output)

When RxC or TxC is an Output, it can still be used as a clock source within the IUSC.

.clk_tree.A

rxclk.clk_pin

txclk.clk_pin

None

RxC Pin (Input)

TxC Pin (Input)

DPLL

Special Receiver Signals (x2)

Special Transmitter Signals (x2)

.clk_tree.B

RxC Pin (Input)

TxC Pin (Input)

BRG-0

BRG-1

Both CTR's ByPassed

Both CTR's ByPassed

.clk_tree.C

RxC Pin (Input)

TxC Pin (Input)

CTR-0

CTR-1

Both CTR's ByPassed

Both CTR's ByPassed

Both CTR's ByPassed

Both CTR's ByPassed

.clk_tree.D

CTR-0 only

CTR-1 only

Internal Reference (18.432 MHz)

Off

RxC Pin (Input)

TxC Pin (Input)

External Reference (use t/rclk.ref_freq to indicate frequency)

CTR-0 and CTR-1 are "By-passed" either by an explicit selection at a particular "clk_tree" level,
or by a bit rate computation which yields a divisor which excludes the use of a Counter.

The counters are by-passed together (because there is only one bit in the IUSC that controls the counter by-pass selection).