PC/104 Specification

Version 2.5

November 2003

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REVISION HISTORY

Version 1.0, March 1992 - Initial release.

Version 2.1, July 1994 - Revised specification incorporating changes to conform with IEEE P996.1 draft version D1.00:
a. Changed bus options. Eliminated the "option 2" configurations having right-angle P1 and P2 connectors. Created new "option 2" configurations similar to "option 1," but without the stackthrough pins. Added a statement indicating that a P2 connector may be included on 8-bit modules, if desired.
b. Added two additional mounting holes to 8-bit bus versions, making the mounting hole patterns of both 8- and 16-bit modules identical.
c. Added an I/O connector region along the bus edge of the module.
d. Increased widths of I/O mating-connector regions from 0.4" to 0.5".
e. Changed lengths of I/O mating-connector regions so that their edges align with the outer edges of the annular rings of adjacent mounting holes.
f. Reduced the bus drive requirement on the signals that had been specified at 6 mA to 4 mA.
g. Added specification of module power requirements.
h. In Appendix C, Section 3, changed minimum value of pullup resistance on shared interrupt line from 10K to 15K ohms.
i. Added a section defining levels of PC/104 conformance.

Version 2.2, September 1994
a. Added correction sheet showing revised schematic for Appendix C.

Version 2.3, June 1996
a. Incorporated correction to Appendix C schematic.
b. Changed P2 connector Pin 1 designation in 16-bit module dimension drawings.
c. Added metric dimensions, including metric versions of module dimension drawings.
d. Minor formatting changes.

Version 2.4, August 2001
a. Added Appendix D Connector Specifications.
b. Removed all specific company references.
c. Corrected Consortium address and phone numbers
d. Added new reference for ISA specification
e. Cleaned up mechanical drawings

Version 2.5, November 2003
a.   Reformatted and updated
   1.   New Chapter 2 "ISA Signal Definition" has been added
   2.   Chapter 3 "Electrical Specification" is now Chapter 4.
   3.   Chapter 4 "Levels of Conformance" is now Chapter 5.
   4.   Appendix D "Connector Specifications has been combined with Appendix A
b.   Signal names have been updated to reflect the names referenced in Edward Solari's book "ISA & EISA Theory & Operation"
   1.   IOCHCHK* relabeled to IOCHK*
   2.   RESETDRV relabeled to RESET
   3.   ENDXFR* relabeled to SRDY*
   4.   SYSCLK relabeled to BCLK
   5.   MASTER* relabeled to MASTER16*
c.   Mechanical drawings have been redone in AutoCAD showing both English and Metric units.
d.   Contact finish female interface has been changed from 20 micoinches minimum to 15 microinches in Figure 5
e.   Mechanical performance withdrawal force has been change from 1 ounce minimum average to 1 ounce per pin minimum in Figure 5

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PC/104 SPECIFICATION
Version 2.5 – March 2003

1.   INTRODUCTION

While the PC and PC/AT architectures have become extremely popular in both general purpose (desktop) and dedicated (non-desktop) applications, its use in *embedded* microcomputer applications has been limited due to the large size of standard PC and PC/AT motherboards and expansion cards.

This document supplies the mechanical and electrical specifications for a compact version of the ISA (PC and PC/AT) bus, optimized for the unique requirements of embedded systems applications. The specification is herein referred to as "PC/104," based on the 104 signal contacts on the two bus connectors (64 pins on P1, plus 40 pins on P2).

Briefly, the needs of embedded applications have been satisfied by PC/104, through the following key differences from standard ISA bus:

■   Reducing the form-factor, to 3.550 by 3.775 inches (90 by 96 mm).

■   Eliminating the need for backplanes or card cages, through its self-stacking bus.

■   Minimizing component count and power consumption (to typically 1-2 Watts per module), by reducing required bus drive on most signals to 4 mA.

PC/104 specifies two module versions — 8-bit and 16-bit — which correspond to the PC and PC/AT bus implementations, respectively.

1.1   References

The remainder of this specification covers the ***differences*** from the ISA bus as detailed in Edward Solari's book ***ISA and EISA Theory and Operation*** published by Annabooks. Designers of modules and systems based on PC/104 should be familiar with the ISA specification. It is available from:

<div align="center">

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12860 Danielson Court
Poway, CA USA 92064
Tel 800.462.1042 or 858.435.2000
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2.   MECHANICAL SPECIFICATIONS

2.1   Module Dimensions

PC/104 modules can be of two bus types, 8-bit and 16-bit. These correspond to the PC and PC/AT buses, respectively. The detailed mechanical dimensions of these two PC/104 bus types are provided in Appendix A.

2.2   Module Stack Options

As shown in the figures in Appendix A, each of the two bus types (8-bit and 16-bit) offers two *bus options*, according to whether or not the P1 and P2 bus connectors extend through the module as "stackthrough" connectors. These options are provided to help meet the tight space requirements of embedded applications.

Figure 1 illustrates a typical module stack including both 8- and 16-bit modules, and shows the use of both the "stackthrough" and "non-stackthrough" bus options. As shown in Figure 1, when 8- and 16-bit modules are combined in a stack, the 16-bit modules must be stacked below (i.e., on the "secondary side" of) the 8-bit modules. A "passive" P2 bus connector may optionally be included in the design of 8-bit modules, to allow the use of these modules anywhere in a stack.

2.3   Key Locations

Key locations - consisting of omitted pins on P1 and P2, and plugged holes on J1 and J2 - have been designated on each bus connector, to help assure proper connector mating. See Appendix B.

Figure 1: A Possible Module Stack Configuration

8-BIT (ISA)
PC/104
MODULE

0.6" (15 MM) SPACERS (4 PLACES)

16-BIT (ISA)
PC/104
MODULE

0.6" (15 MM) SPACERS (4 PLACES)

16-BIT (ISA)
PC/104
MODULE

0.435" (11 MM)

APPROX.
2.0" (50 MM)

0.6" (15 MM)

0.6" (15 MM)
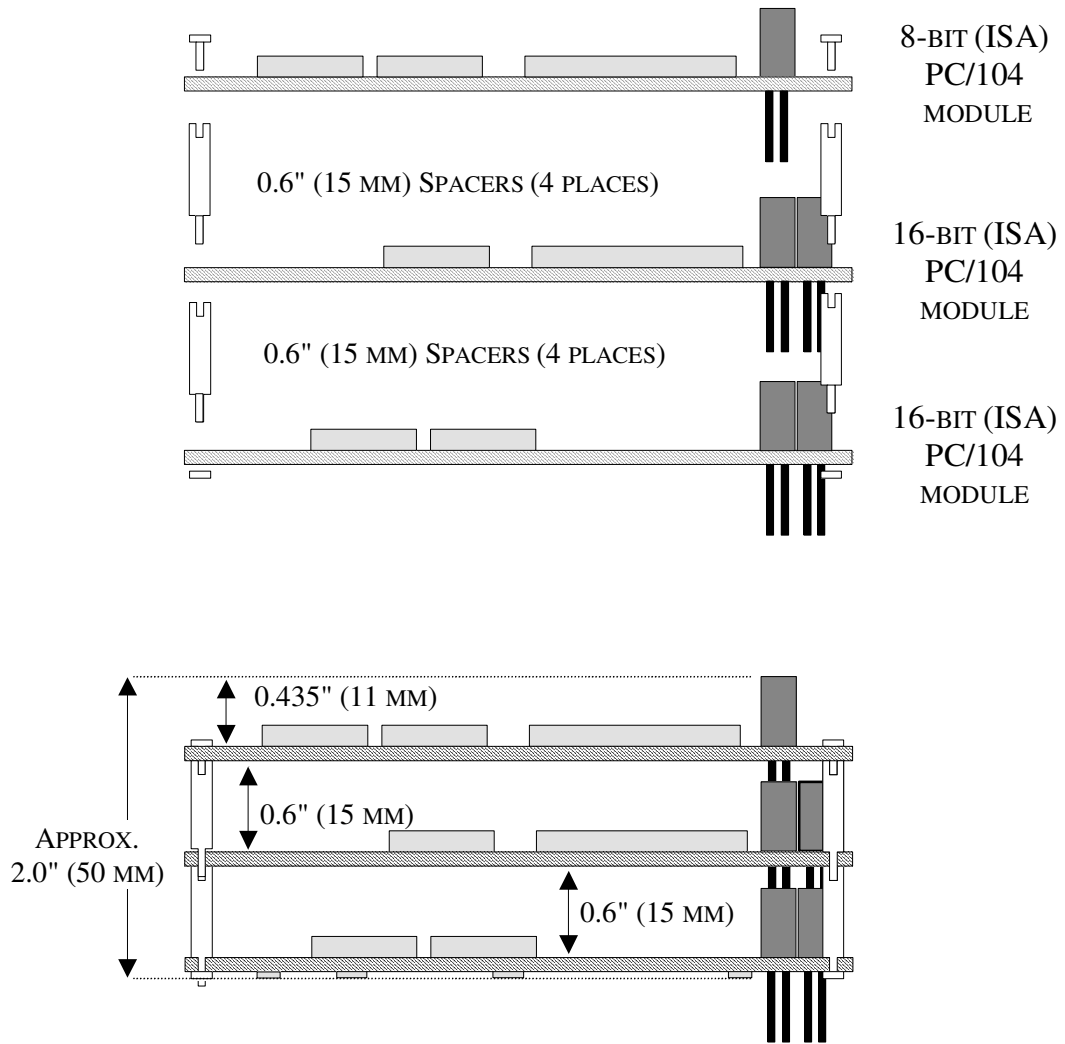
3.   ISA SIGNAL DEFINITION

For full details on the electrical requirements for the ISA bus and a complete description of ISA bus signal definitions, reference Edward Solari's book ***ISA and EISA Theory and Operation***

3.1   Address and Data

BALE **Bus Address Latch Enable** line is driven by the platform CPU to indicate when SA<19:0>, LA<23:17>, AENx, and SBHE# are valid. It is also driven to a logical one when an ISA add-on card or DMA controller owns the bus.

SA<19:0> **Address** lines are driven by the ISA bus master to define the lower 20 address signal lines needed for the lower 1 MB of the memory address space.

LA<23:17> **Latched Address** lines are driven by the ISA bus master or DMA controler to provide the additional address lines required for the 16 MB memory address space.

SBHE# **System Byte High Enable** line is driven by the ISA bus master to indicate that valid data resides on the SD<15:8> lines.

AENx **Address Enable** line is driven by the platform circuity as an indication to ISA resources not to respond to the ADDRESS and I/O COMMAND lines. This line is the method by which I/O resources are informed that a DMA transfer cycle is occurring and that only the I/O resource with an active DACKx# signal line can respond to the I/O signal lines.

SD<15:0> **Data** lines 0 – 7 or 8 – 15 are driven for an 8 data bit cycle, and 0 – 15 are driven for a 16 data bit cycle.

3.2   Cycle Control

MEMR# **Memory Read** line is driven by the ISA bus master or DMA controller to request a memory resource to drive data onto the bus during the cycle.

SMEMR# **System Memory Read** line is to request a memory resource to drive data onto the bus during the cycle.   This line is active when MEMR# is active and the LA<23:20> signal lines indicate the first 1 MB of address space.

MEMW# **Memory Write** line is to request a memory resource to accept data from the data lines.

SMEMW# **System Memory Write** line is to request a memory resource to drive data onto the bus during the cycle.   This line is active when MEMW# is active and the LA<23:20> signal lines indicate the first 1 MB of address space.

IOR# **I/O Read** line is driven by the ISA bus master or DMA controller to request an I/O resource to drive data onto the data bus during the cycle.

IOW# **I/O Write** requests an I/O resource to accept data from the data bus.

MEMCS16# **Memory Chip Select 16** line is driven by the memory resource to indicate that it is an ISA resource that supports a 16 data bit access cycle. It also allows the ISA bus master to execute shorter cycles.

IOCS16# **I/O Chip Select 16** line is driven by an I/O resource to indicate that it is an ISA resource that supports a 16 data bit access cycle. It also allows the ISA bus master to execute shorter default cycles

IOCHRDY **I/O Channel Ready** line allows resources to indicate to the ISA bus master that additional cycle time is required.

SRDY#   **Synchronous Ready** (or NOWS# No-Wait-State) line is driven active by the accessed resource to indicate that an access cycle shorter than the standard access cycle can be executed.

3.3 Bus Control

REFRESH#   **Memory Refresh** is driven by the refresh controller to indicate a refresh cycle

MASTER16# **MASTER16#** line is only driven active by an ISA add-on bus owner card that has been granted bus ownership by the DMA controller.

IOCHK#   **I/O Channel Check** line is driven by any resource. It is active for a general error condition that has no specific interpretation.

RESET   **Reset** line is driven active by the platform circuitry. Any bus resource that senses an active RESET signal line must immediately tri-state all output drivers and enter the appropriate reset condition.

BCLK   **System Bus Clock** line is a clock driven by the platform circuitry. It has a 50% $\pm$ approximately 5% (57 to 69 nanoseconds for 8 MHz) duty cycle, at a frequency of 6 to 8 MHz ($\pm$ 500 ppm).

OSC   **Oscillator** line is a clock driven by the platform circuitry. It has a 45 – 55 % duty cycle, at a frequency of 14.31818 MHz ($\pm$ 500 ppm). It is not synchronized to any other bus signal line.

3.4 Interrupt

IRQx   **Interrupt Request** lines allow add-on cards to request interrupt service by the platform CPU.

3.5 DMA

DRQx   **DMA Request** lines are driven active by I/O resources to request service by the platform DMA controller.

DACKx#   **DMA Acknowledge** lines are driven active by the platform DMA controller to select the I/O resource that requested a DMA transfer cycle.

TC   **Terminal Count** line is driven by the platform DMA controller to indicate that all the data has been transferred.

4.   ELECTRICAL SPECIFICATIONS

4.1   Signal Assignments

Signals are assigned in the same order as on the edgecard connectors of ISA, but transformed to the corresponding header connector pins. Signal assignments for the J1/P1 and J2/P2 connectors are given in Appendix B.

4.2   Added Grounds

Several ground pins have been added, to maximize bus integrity. See Appendix B.

4.3   AC Signal Timing

All PC/104 bus signals are identical in signal timing to their ISA counterparts.

4.4   DC Signal Levels

All PC/104 bus signal DC logic high and logic low voltage levels are identical to their ISA counterparts.

4.5   Bus Drive Current

To reduce component count and minimize power consumption and heat dissipation most bus signals have a reduced bus drive requirement of 4 mA. The exception is open collector driven signals which must drive 330 ohm pullup resistors defined by the ISA specification. This allows direct driving of the bus by many ASIC devices, and by HCT family logic.

Specifically, the following signals must be driven with devices capable of providing 20 mA sink current (as indicated in ISA):

MEMCS16*
IOCS16*
MASTER16*
SRDY*

All other signals may be driven with devices capable of providing 4 mA sink current.

4.6   Interrupt-Sharing Option

There is an optional means to share a single bus interrupt line among multiple interrupting devices. Appendix C provides a design guideline which can help ensure compatibility of interrupt-sharing among PC/104 modules.

4.7   Bus Termination Option

Termination of the 8-bit and 16-bit ISA bus signals may be desired in some systems to increase data integrity and system reliability. When termination is included, *AC termination* networks must be used to provide termination close to the characteristic impedance of the signal lines without exceeding the DC output current capabilities of the drivers.

As in the ISA standard, the recommended network consists of a resistor-capacitor network of 40-60 ohms in series with 30-70 pF, connected between each bus signal and ground.

Whether termination is needed, and where it should be located, is dependent on the specific system configuration and must be determined by the system designer.

4.8   Module Power Requirements

The operating voltage range and maximum power requirements of each module are given in Table 1. Each module shall not draw more than the operating current indicated. The total power requirement of a PC/104 module stack is the sum of that required by each of the modules in the stack. Operating voltages, which refer to the voltage measured at the appropriate bus connector pins of any given module, are specified to ±5 percent. Only those voltages required by modules in a system need be supplied to the bus.

Table 1: Module Power Requirements

Nominal Voltage	Maximum Voltage	Minimum Voltage	Maximum Current
+12 Volts	+12.6 Volts	+11.4 Volts	1.0 Amp
+5 Volts	+5.25 Volts	+4.75 Volts	2.0 Amp
-5 Volts	-4.75 Volts	-5.25 Volts	0.2 Amp
-12 Volts	-11.4 Volts	-12.6 Volts	0.3 Amp

5.   LEVELS OF CONFORMANCE

This section provides terminology intended to assist manufacturers and users of PC/104 bus-compatible products in defining and specifying conformance with the PC/104 Specification.

5.1   PC/104 "Compliant"

This refers to "PC/104 form-factor" devices that conform to all non-optional aspects of the PC/104 Specification, including both *mechanical* and *electrical* specifications.

5.2   PC/104 "Bus-compatible"

This refers to devices which are not "PC/104 form-factor" (i.e., do not comply with the module dimensions of the PC/104 Specification), but provide a male or female PC/104 *bus connector* that meets both the *mechanical* and *electrical* specifications provided for the PC/104 bus connector.
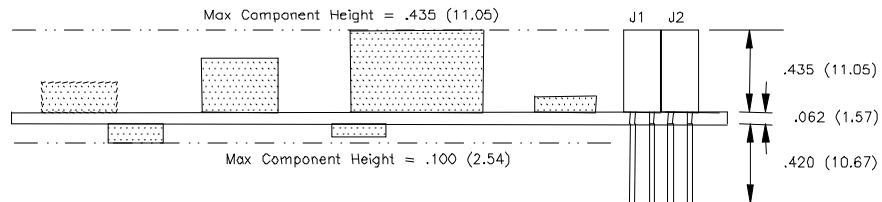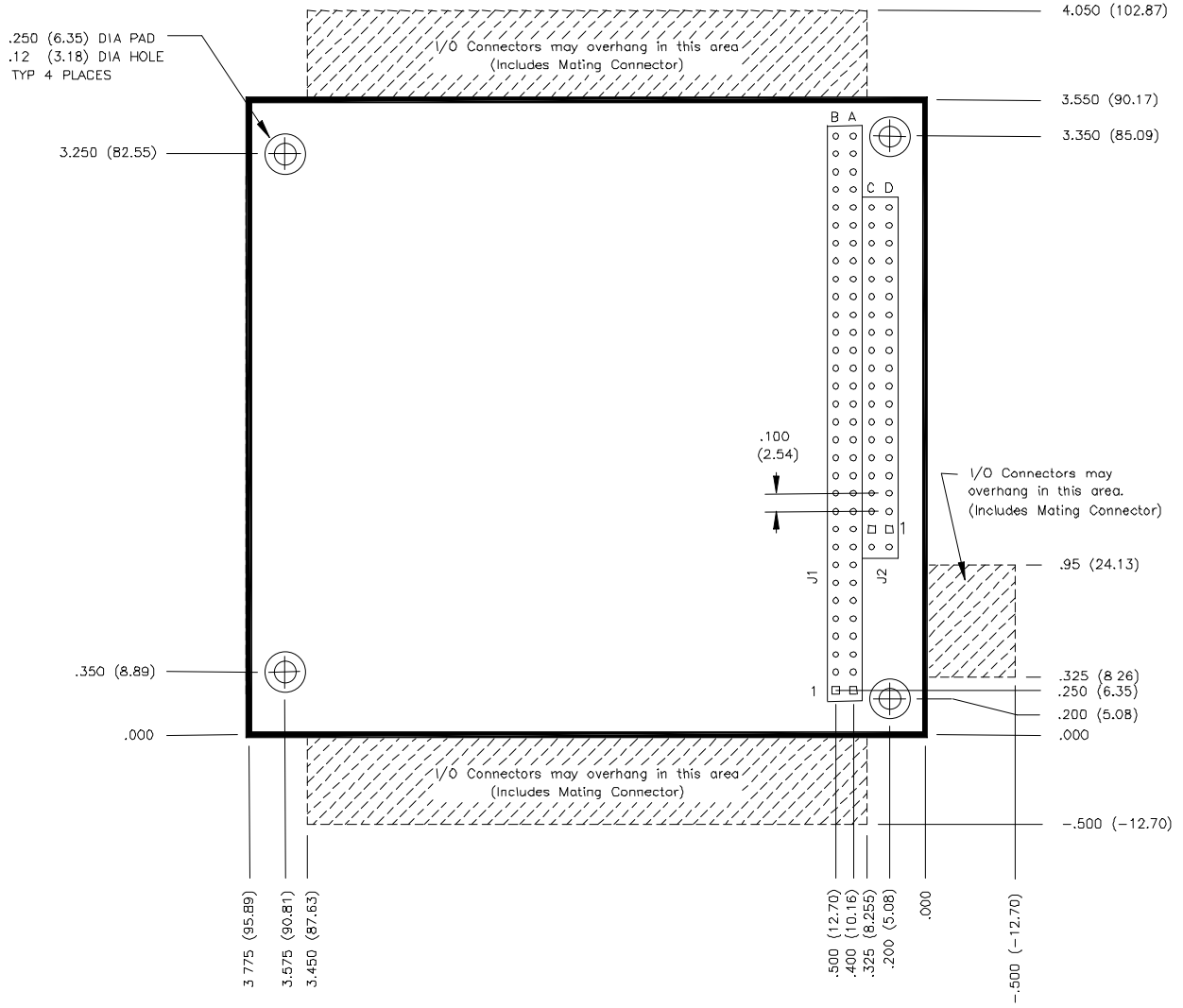
APPENDIX A

MECHANICAL DIMENSIONS

Figure 2: PC/104 8-bit Module Dimensions

Dimensions are in inches / (millimeters)
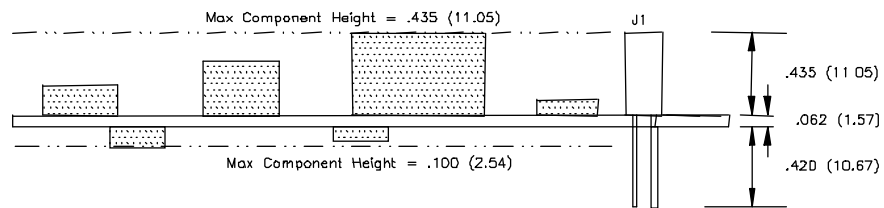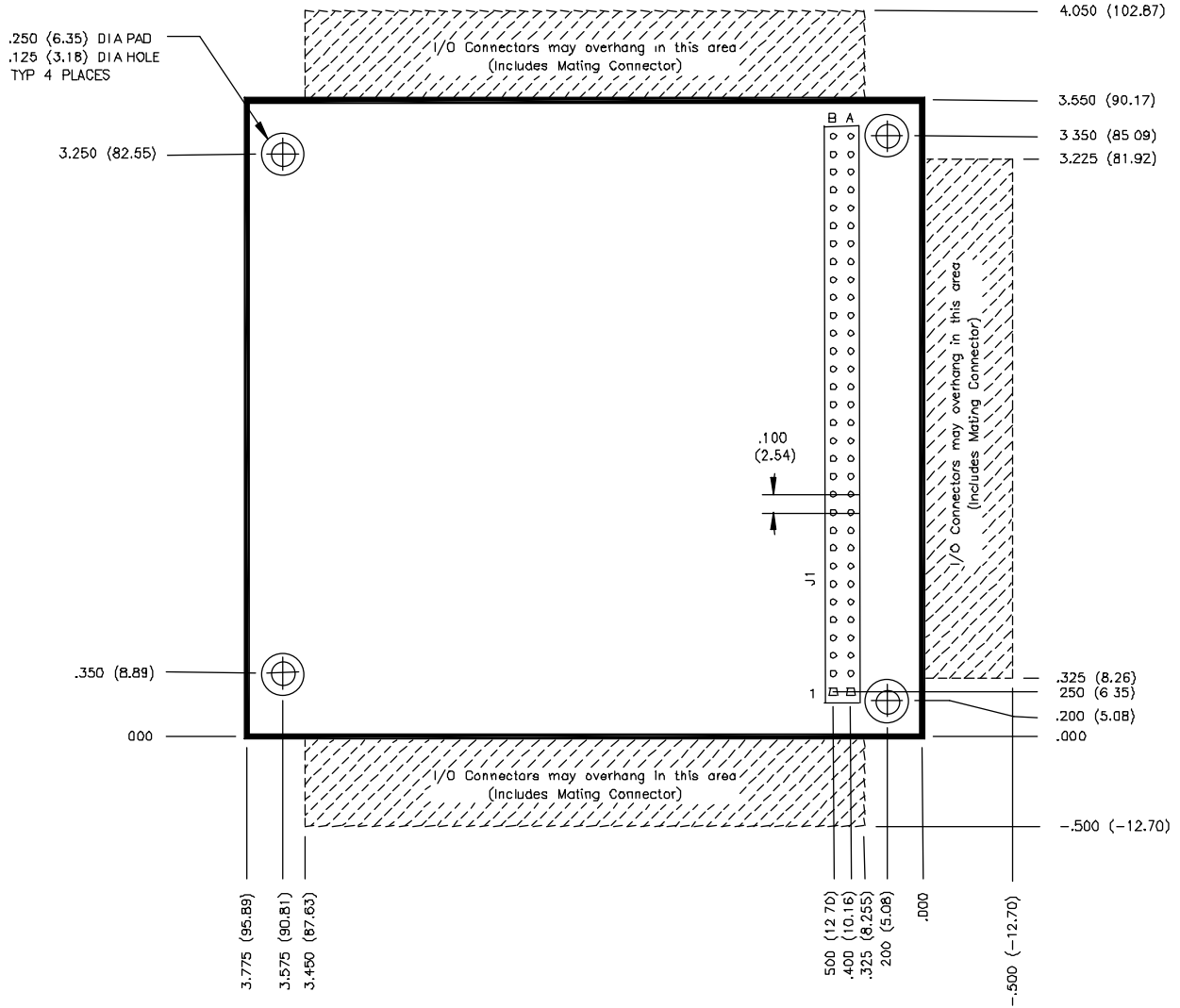
Figure 3: PC/104 16-bit Module Dimensions

Dimensions are in inches / (millimeters)

Figure 4: 8-bit and 16-bit ISA Bus Connector Dimensions

Dimensions are in inches/(millimeters)

NOTES:

⚠1 PRESS FIT COMPLIANT PINS PER DIN 41612 PART 5 AND IEC 352-5 CAN BE USED INSTEAD OF SQUARE PINS AS SHOWN.

2 CONFIGURATION CAN BE MADE OF ONE OR MORE PIECES.

.195 (4.95)

.140 (3.56) / .260 (6.60) PIN INSERTION

.435 ±.010 (11.05 ±.25)

SOLDER RINGS, IF USED, MUST NOT PROJECT BEYOND THE .435 BASE OUTLINE.

.090 (2.29)

.480 (12.19)

⚠1

.025 (0.64) SQ ±.001 (.0254)

.100 (2.54)

.100 (2.54)

.195 (4.95)

3.220 ±.010 (81.79 ±.25)

.395 ±.010 (10.03 ±.25)

.06 (1.52)

.800 (20.32)

1.900 (48.26)

.400 (10.16)

.800 (20.32)

2.820 (71.63)
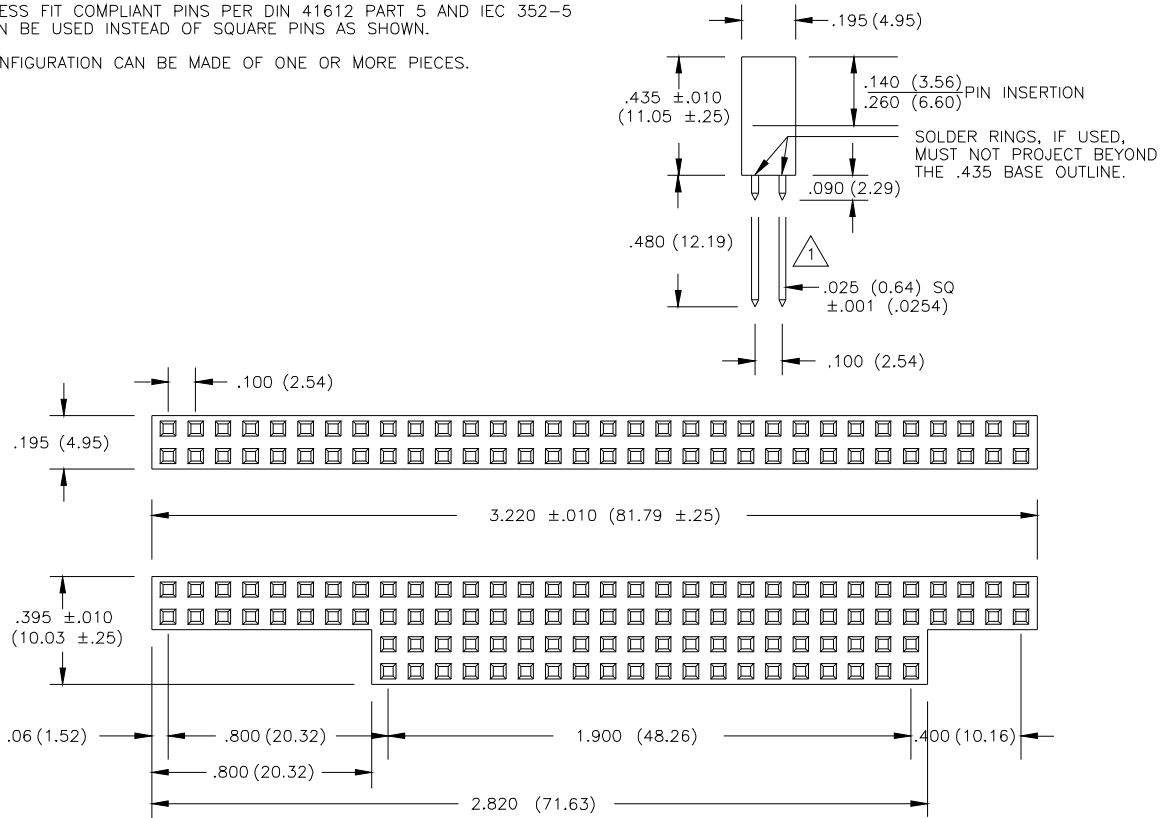
Figure 5: 8-bit and 16-bit ISA Bus Connector Specifications

MATERIALS

Housing: High Temp Thermoplastic, UL Rated 94-V0
Contact: Phosphor Bronze
Solder: Tin-Lead (63-37), If Applicable
Solder Clip: Aluminum Alloy, If Applicable

CONTACT FINISH

Female Interface: 15 Microinches Minimum Hard Gold
Male Interface: Gold Flash Minimum
Solder Tail: 100 Microinches Minimum Solder
Underplate: 50 Microinches Minimum Nickel

MECHANICAL PERFORMANCE

Insertion Force: 3.5 Ounce Per Pin Maximum
Withdrawal Force: 1 Ounce Per Pin Minimum
Normal Force: 50 Grams Minimum (Per Beam)
Durability: 50 Cycles Minimum
Operating Temp: -55° C To +85° C

ELECTRICAL PERFORMANCE

Contact Resistance: <30 Milliohms Maximum
Current Capacity: 1 Amp Continuous Per Pin
Dielectric Strength: 1000 Vac
Insulation Resistance: 5,000 Megohms Minimum

APPENDIX B

BUS SIGNAL ASSIGNMENTS

Table 2: 8-bit and 16-bit ISA Bus Signal Assignments

J1/P1		
Pin	**Row A**	**Row B**
1	IOCHK*	GND
2	SD7	RESET
3	SD6	+5V
4	SD5	IRQ9
5	SD4	-5V
6	SD3	DRQ2
7	SD2	-12V
8	SD1	SRDY*
9	SD0	+12V
10	IOCHRDY	KEY
11	AEN	SMEMW*
12	SA19	SMEMR*
13	SA18	IOW*
14	SA17	IOR*
15	SA16	DACK3*
16	SA15	DRQ3
17	SA14	DACK1*
18	SA13	DRQ1
19	SA12	REFRESH*
20	SA11	BCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2*
27	SA4	TC
28	SA3	BALE
29	SA2	+5V
30	SA1	OSC
31	SA0	GND
32	GND	GND

J2/P2		
Pin	**Row D**	**Row C**
0	GND	GND
1	MEMCS16*	SBHE*
2	IOCS16*	LA23
3	IRQ10	LA22
4	IRQ11	LA21
5	IRQ12	LA20
6	IRQ15	LA19
7	IRQ14	LA18
8	DACK0*	LA17
9	DRQ0	MEMR*
10	DACK5*	MEMW*
11	DRQ5	SD8
12	DACK6*	SD9
13	DRQ6	SD10
14	DACK7*	SD11
15	DRQ7	SD12
16	+5V	SD13
17	MASTER*	SD14
18	GND	SD15
19	GND	KEY

NOTES:
1. Rows C and D are not required on 8-bit modules. See Section 2.2.
2. B10 and C19 are key locations. See Section 2.3.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values. See Section 4.5.

**APPENDIX C**

INTERRUPT-SHARING OPTION

C.1 Introduction

The Interrupt Request lines (IRQn) on the ISA bus are *active high*. Consequently, the usual technique of wire-ORing open-collector driven *active low* bus signals cannot be used for interrupt-sharing in the PC bus architecture.

There is an optional means to share a single bus interrupt line among multiple interrupting devices. This appendix provides design guidelines which can help assure compatibility of interrupt-sharing among PC/104 modules.

C.2 Recommended Circuit

A circuit similar to that shown in Figure 6 below can provide interrupt-sharing of the *active high* IRQ signals on the ISA bus, given a few system-level restrictions (see below).

> *NOTE: This recommendation does not comply with the ISA standard, since it is not possible to implement interrupt-sharing in an ISA compatible manner.*

Figure 6: Typical Interrupt-Sharing Circuit
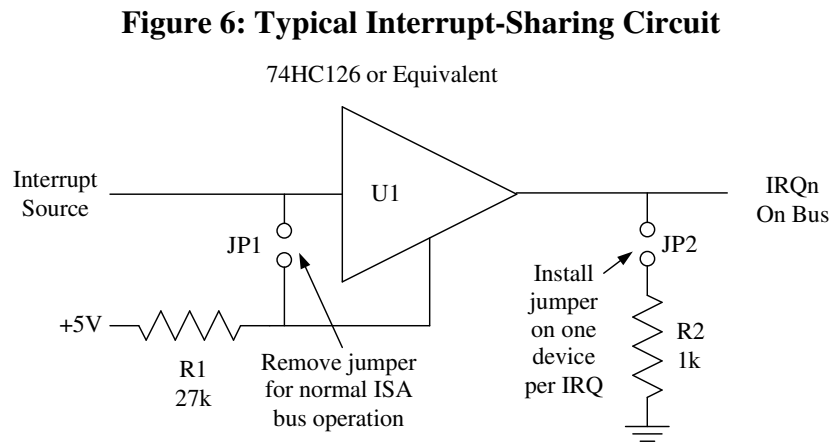
C.3 Restrictions

All bus devices sharing a common interrupt must be equipped with a suitable interrupt-sharing circuit (see the Figure 6, above) and must meet the following two restrictions:

■ The interrupt line being shared must not have a pullup resistance (to +5 volts) less than 15k ohms anywhere in the system. (Typically, the pullup resistance is located on the CPU module, so this is generally a restriction on the design of the CPU module.) Resistive bus termination will generally violate this restriction; use AC termination instead (Section 4.7).

■ The interrupt line being shared must have one (and only one) pulldown resistor (1k ohms) connected between the IRQ line and ground. Resistive bus termination will generally violate this restriction; use AC termination instead.

C.4 "ISA Compatibility" Option Jumper

The ISA specification calls for using a 2.2k pullup resistor on each of the IRQ lines, which violates the 15k minimum pullup resistance allowed with the recommended interrupt-sharing circuit. In systems having this value of pullup, devices with the circuit shown in Figure 6 can be made compatible by disabling their interrupt-sharing circuit. This is accomplished by unshorting both JP1 and JP2, resulting in a normal ISA (non-shared) interrupt configuration (but with the reduced bus drive common to other PC/104 bus signals)