

Aligned Scheduling: Cache-efficient Instruction Scheduling for VLIW Processors

Vasileios Porpodas[†] and Marcelo Cintra^{†★}

School of Informatics, University of Edinburgh[†]
Intel Labs Braunschweig[★]

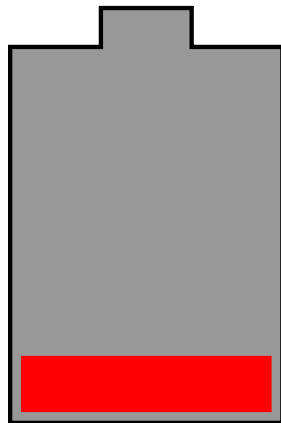
LCPC 2013

Energy efficiency, VLIWs and Scheduling

- Mobile era

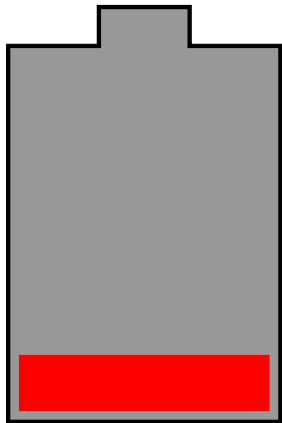
Energy efficiency, VLIWs and Scheduling

- Mobile era
- Energy becomes a major design constraint



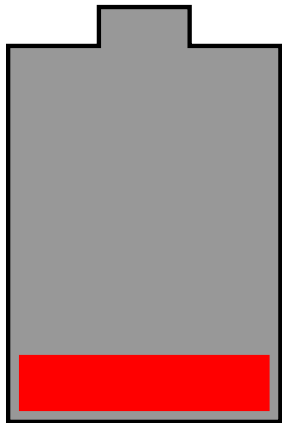
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- Hardware Instruction scheduling consumes a lot of energy



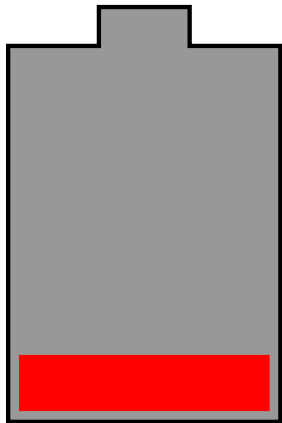
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- Mobile era
- Energy becomes a major design constraint
- Hardware Instruction scheduling consumes a lot of energy
- VLIW processors: high-performance and statically scheduled
- Suffer from unpredictable cache latencies



Hardware Load-Use interlocking (1/3)

- Out-Of-Order Processors support full scoreboarding
- Performance model (Karkhanis & Smith ISCA'04)



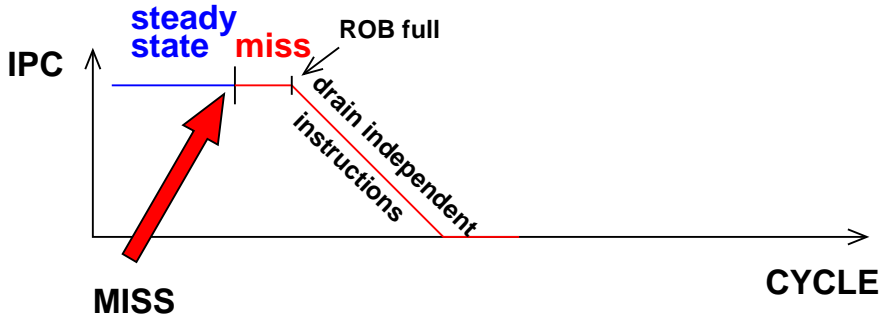
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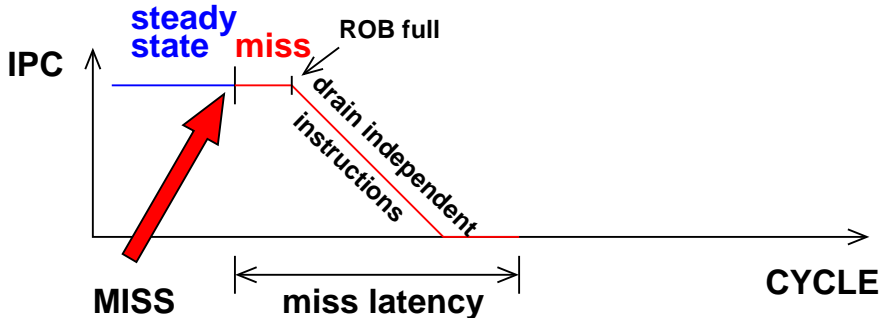
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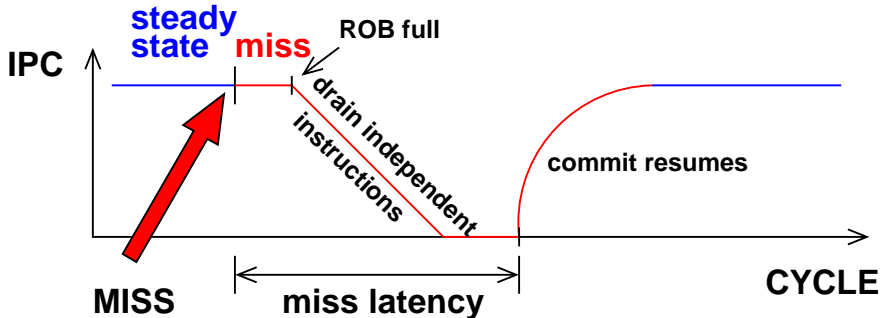
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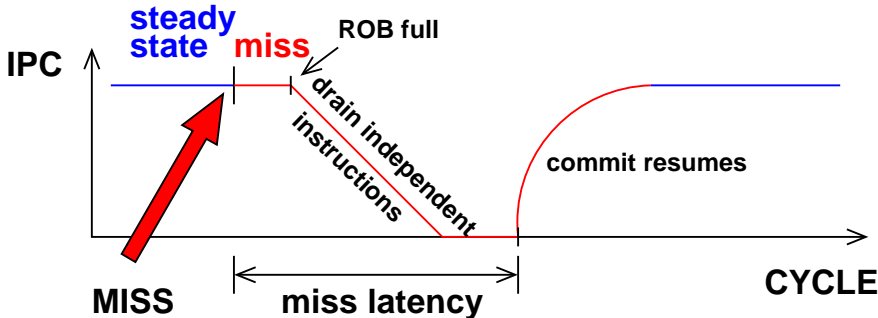
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Hardware Load-Use interlocking (1/3)

- Out-Of-Order Processors support full scoreboarding
- Performance model (Karkhanis & Smith ISCA'04)
- Most effective at hiding latency - Expensive hardware



Hardware Load-Use interlocking (2/3)

- VLIW Processors with VLIW-word-level scoreboarding (Stall-On-Use)



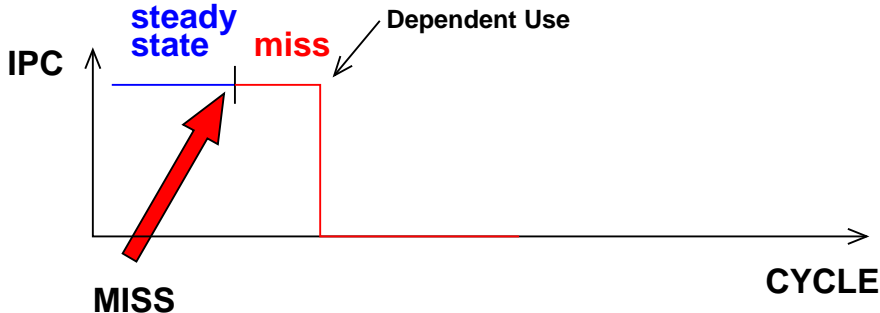
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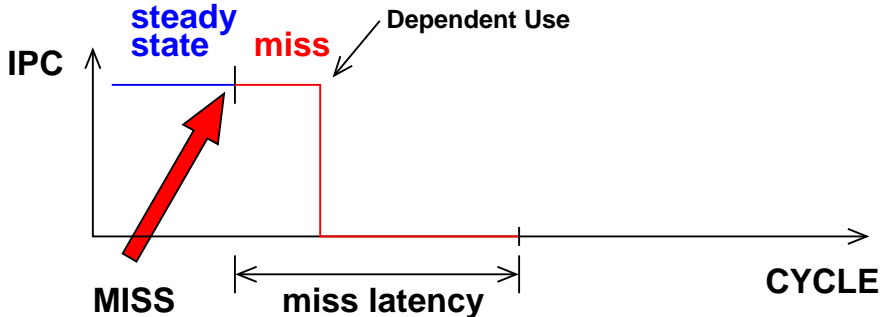
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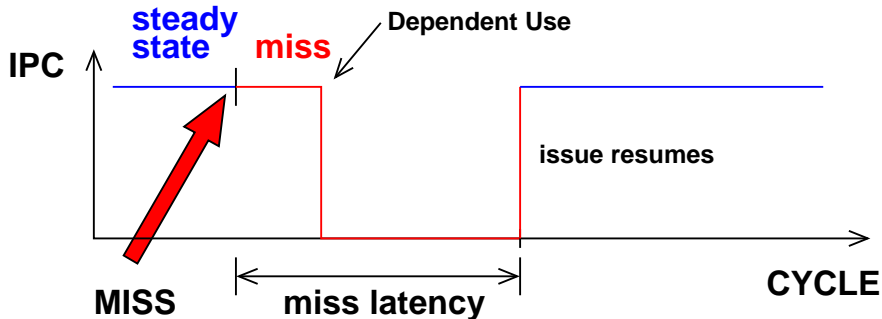
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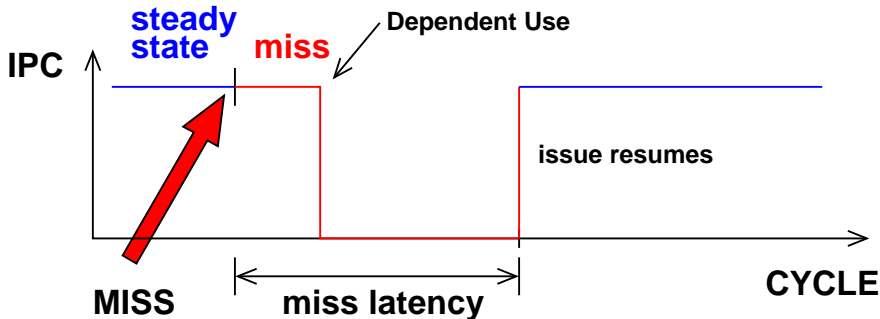
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Hardware Load-Use interlocking (2/3)

- VLIW Processors with VLIW-word-level scoreboarding (Stall-On-Use)
- Effective at hiding some latency



Hardware Load-Use interlocking (3/3)

- VLIW Processors with **NO** Load-Use Interlocking (Stall-On-Miss)



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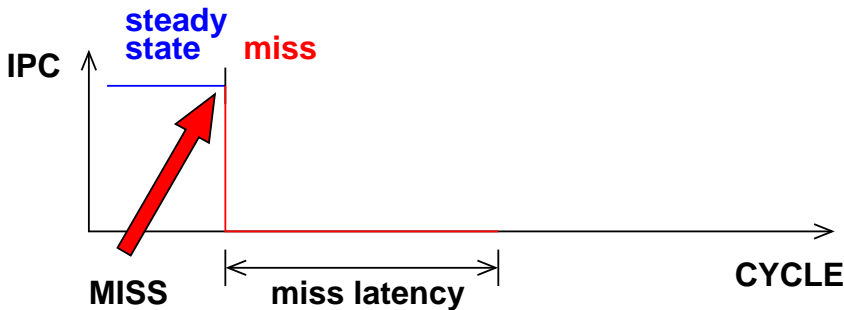
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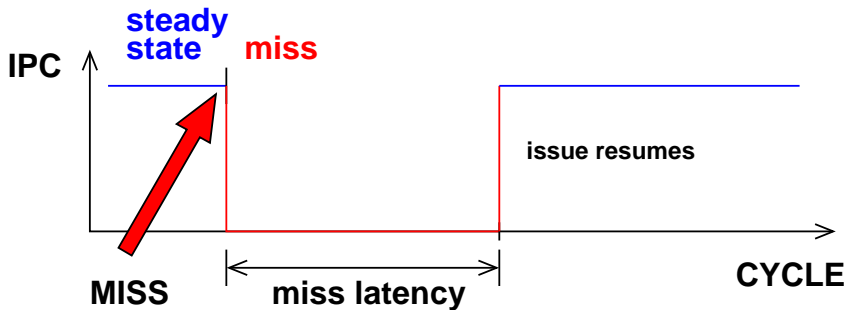
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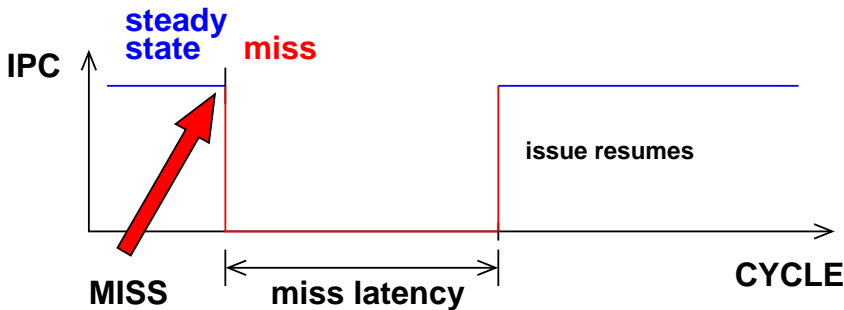
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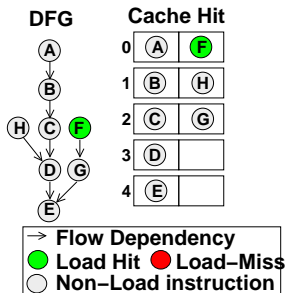


Hardware Load-Use interlocking (3/3)

- VLIW Processors with **NO** Load-Use Interlocking (Stall-On-Miss)
- Poor performance under lots of misses



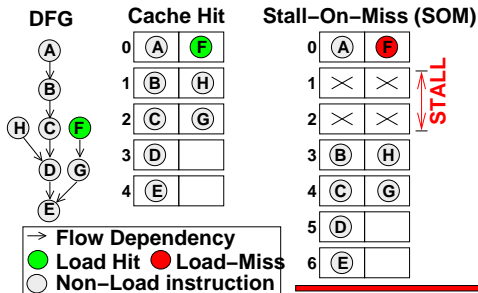
Levels of Load-Use interlocking



Increasing Hardware Complexity

Levels of Load-Use interlocking

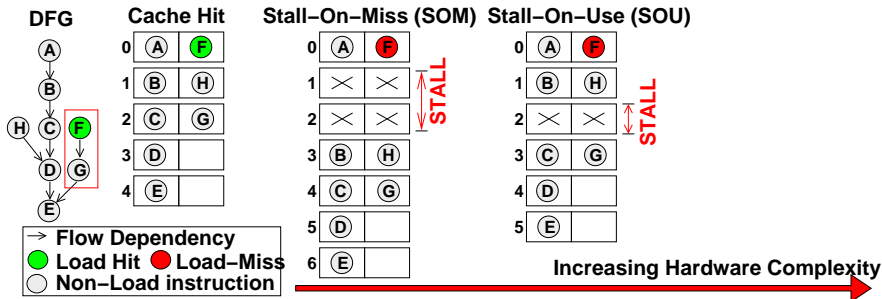
- No interlocks (Stall-On-Miss SOM)



Increasing Hardware Complexity

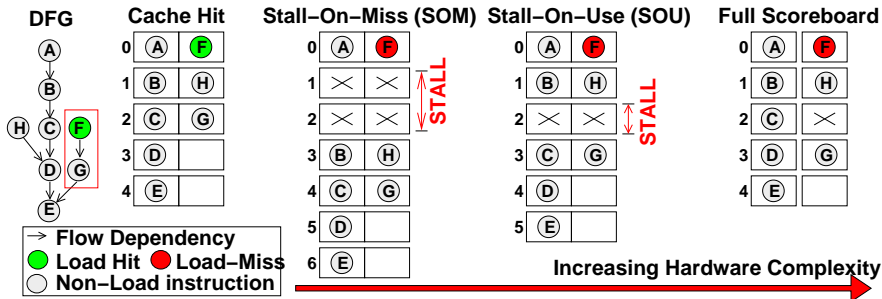
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- VLIW-level interlocks (Stall-On-Use SOU)



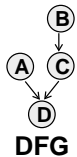
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- VLIW-level interlocks (Stall-On-Use SOU)
- Instruction-level Full Scoreboarding



Observation: Load Semantics on SOM

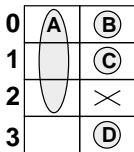
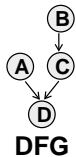
- Missing Loads have different semantics from Long-Latency instructions



**Non-Load instruction
Or Cache-HIT**

Observation: Load Semantics on SOM

- Missing Loads have different semantics from Long-Latency instructions
- Existing schedulers treat them as equivalent



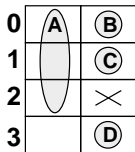
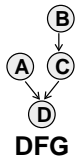
a. Execution overlap of long-latency A with B,C



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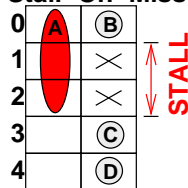
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Stall-On-Miss

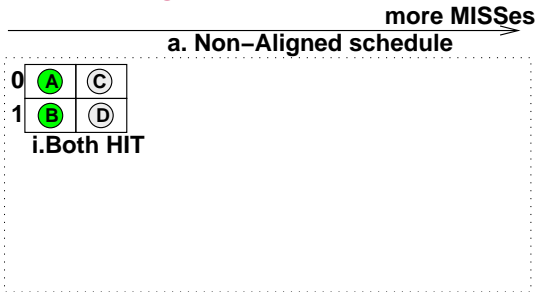


b. No execution overlap of Load-MISS A (only B)



Motivation: Miss Overlapping

- Baseline Scheduler not effective on SOM



Non-Load instruction



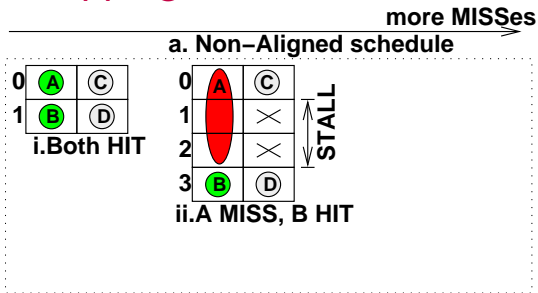
Load-HIT instr.



Load-MISS instr.

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Non-Load instruction



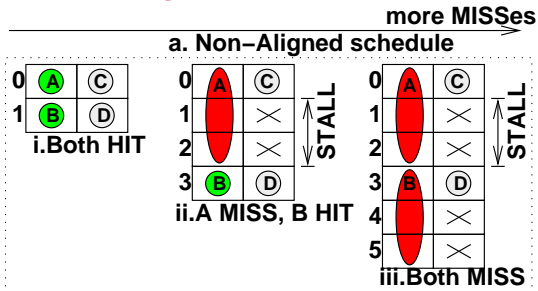
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Load-MISS instr.

Motivation: Miss Overlapping

- Baseline Scheduler not effective on SOM
- Suffers from consecutive stalls



Non-Load instruction



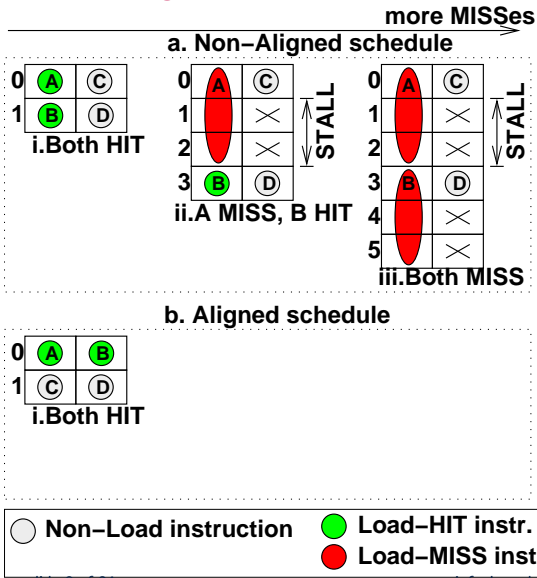
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Load-MISS instr.

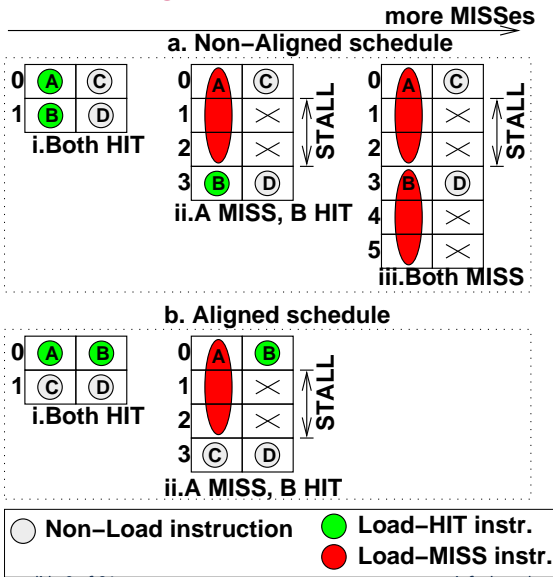
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- Suffers from consecutive stalls
- Aligned Scheduling optimized for SOM



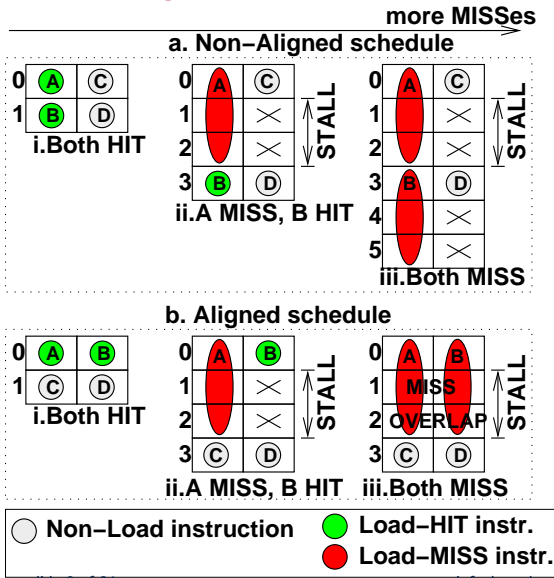
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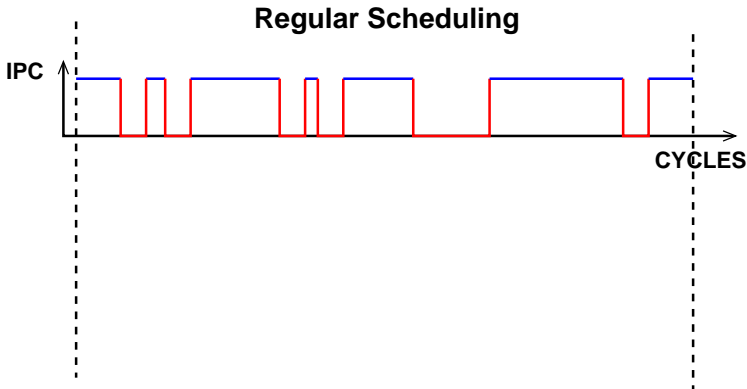
Motivation: Miss Overlapping

- Baseline Scheduler not effective on SOM
- Suffers from consecutive stalls
- Aligned Scheduling optimized for SOM
- Exploit Multiple simultaneous Misses



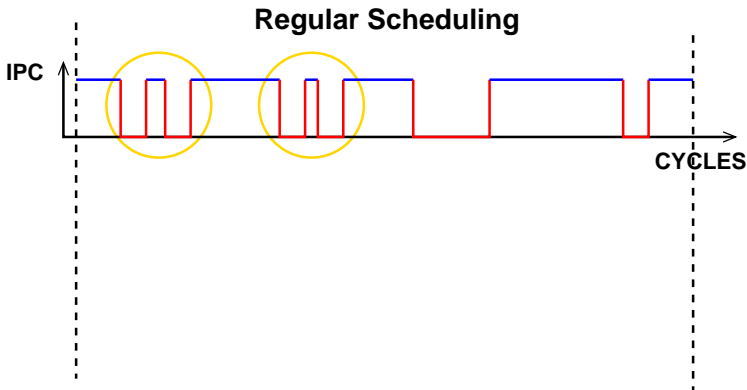
Motivation: Aligning Multiple Loads

- SOM hardware is incapable of hiding misses



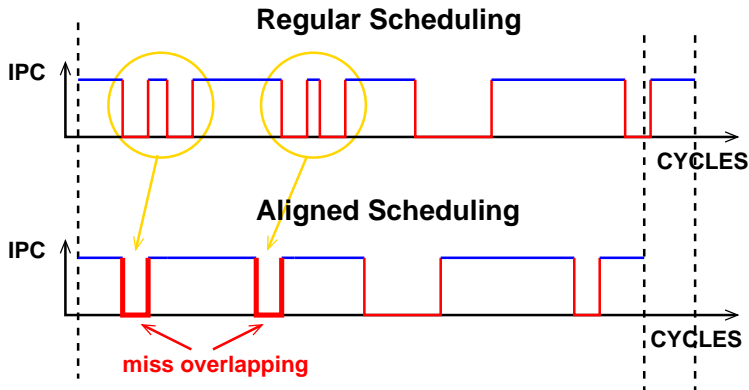
Motivation: Aligning Multiple Loads

- SOM hardware is incapable of hiding misses
- Improve performance by aligning Loads



Motivation: Aligning Multiple Loads

- SOM hardware is incapable of hiding misses
- Improve performance by aligning Loads
- Multiple misses occur simultaneously \rightarrow fewer stalls



Outline

Introduction

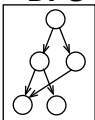
Aligned Scheduling

Experimental Setup and Results

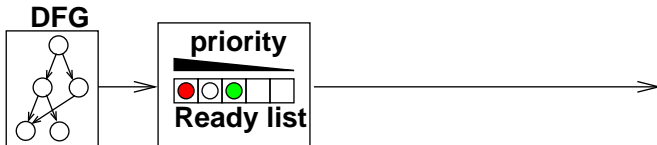
Conclusion

Aligned Scheduling

DFG



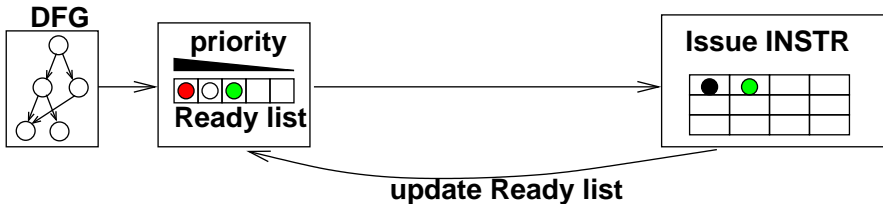
Aligned Scheduling



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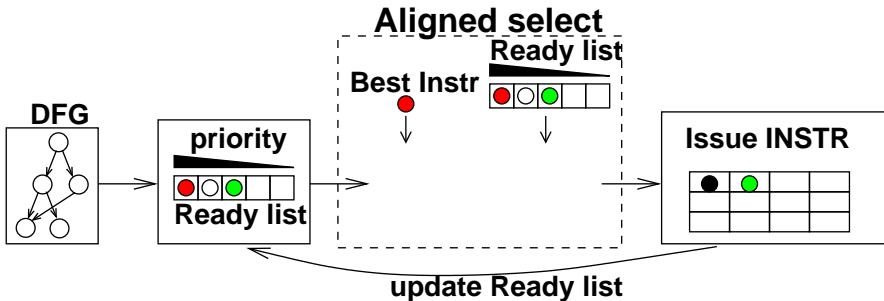


Aligned Scheduling



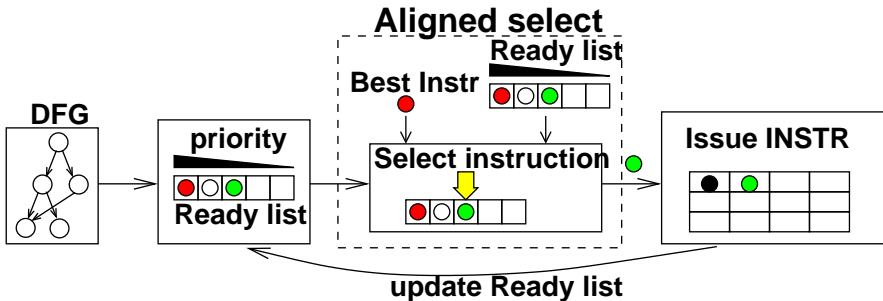
Aligned Scheduling

- Plug-in to well established scheduler structure



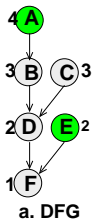
Aligned Scheduling

- Plug-in to well established scheduler structure
- Better selection of instruction to be scheduled
- Override default priorities



Aligned-HLPL (Hoist Low Priority Loads)

- Unaligned Loads



	All Hits	Stall-On-Miss	Stall-On-Use										
Baseline Scheduler	<table><tr><td>0</td><td>A</td><td>C</td></tr><tr><td>1</td><td>B</td><td>E</td></tr><tr><td>2</td><td>D</td><td></td></tr><tr><td>3</td><td>F</td><td></td></tr></table> 	0	A	C	1	B	E	2	D		3	F	
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→ True dependence



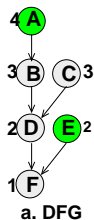
Non-LOAD instr.



LOAD instr.

Aligned-HLPL (Hoist Low Priority Loads)

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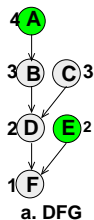
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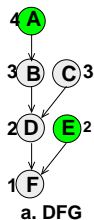
→ True dependence

⊙ Non-LOAD instr.

⊗ LOAD instr.

Aligned-HLPL (Hoist Low Priority Loads)

- Unaligned Loads
- Prefer Low Priority Load if already scheduled a Load



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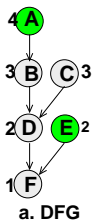
→ True dependence

⊙ Non-LOAD instr.

⊗ LOAD instr.

Aligned-HLPL (Hoist Low Priority Loads)

- Unaligned Loads
- Prefer Low Priority Load if already scheduled a Load
- Miss overlapping
- Faster execution



	All Hits	Stall-On-Miss	Stall-On-Use																																																									
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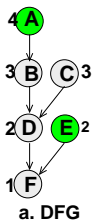
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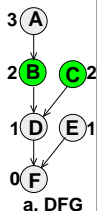
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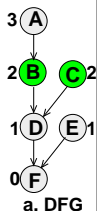
- Unaligned Loads



	All Hits	Stall-On-Miss	Stall-On-Use										
Baseline Scheduler	<table><tr><td>0</td><td>A</td><td>C</td></tr><tr><td>1</td><td>B</td><td>E</td></tr><tr><td>2</td><td>D</td><td></td></tr><tr><td>3</td><td>F</td><td></td></tr></table> 	0	A	C	1	B	E	2	D		3	F	
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Aligned-LLPL (Lower Low Priority Loads)

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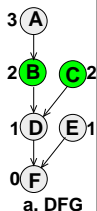
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LOAD HIT

LOAD MISS

Aligned-LLPL (Lower Low Priority Loads)

- Unaligned Loads



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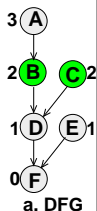
Non-LOAD instr.

LOAD HIT

LOAD MISS

Aligned-LLPL (Lower Low Priority Loads)

- Unaligned Loads
- Delay the execution of low-priority Loads



	All Hits	Stall-On-Miss	Stall-On-Use																																																						
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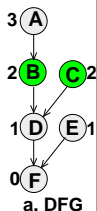
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LOAD HIT

LOAD MISS

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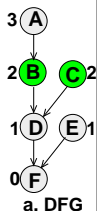
- Unaligned Loads
- Delay the execution of low-priority Loads
- Miss overlapping
- Increases chances that Loads will be aligned later



	All Hits	Stall-On-Miss	Stall-On-Use	
Baseline Scheduler	0 A C	0 A C	0 A C	
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	3 F	3 B E	3 <div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div></div> stall	3 <div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div></div> stall
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		5 <div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div></div> stall	5 F	
		6 D		
		7 F		
	b. Baseline (all HITS)	d. Baseline (all MISSES)	f. Baseline (all MISSES)	
Aligned-LLPL	0 A E	0 A E		
	1 B C	1 B C		
	2 D	2 <div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div></div> stall		
	3 F	3 <div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div></div> stall		
		4 D		
		5 F		
	c. HLPL (all HITS)	e. HLPL (all MISSES)		
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Aligned-LLPL (Lower Low Priority Loads)

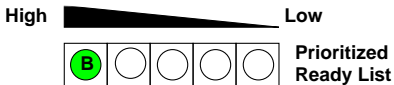
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Aligned-LLPL	<table><tr><td>0</td><td>A</td><td>E</td></tr><tr><td>1</td><td>B</td><td>C</td></tr><tr><td>2</td><td>D</td><td></td></tr><tr><td>3</td><td>F</td><td></td></tr></table> <p>c. HLPL (all HITS)</p>	0	A	E	1	B	C	2	D		3	F		<table><tr><td>0</td><td>A</td><td>E</td></tr><tr><td>1</td><td>B</td><td>C</td></tr><tr><td>2</td><td></td><td></td></tr><tr><td>3</td><td></td><td></td></tr><tr><td>4</td><td>D</td><td></td></tr><tr><td>5</td><td>F</td><td></td></tr></table> <p>e. HLPL (all MISSES)</p>	0	A	E	1	B	C	2			3			4	D		5	F		<table><tr><td>0</td><td>A</td><td>E</td></tr><tr><td>1</td><td>B</td><td>C</td></tr><tr><td>2</td><td></td><td></td></tr><tr><td>3</td><td></td><td></td></tr><tr><td>4</td><td>D</td><td></td></tr><tr><td>5</td><td>F</td><td></td></tr></table> <p>g. HLPL (all MISSES)</p>	0	A	E	1	B	C	2			3			4	D		5	F							
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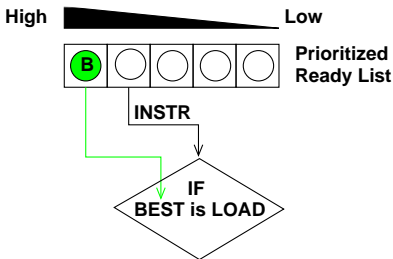
Alignment Heuristic

- Choose between HLPL and LLPL depending on highest priority instruction in the ready list (B)



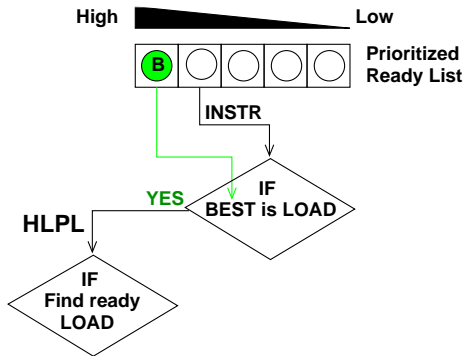
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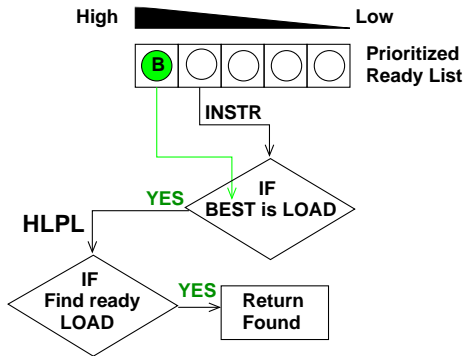
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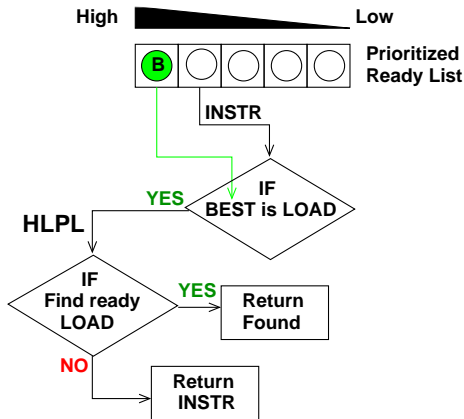
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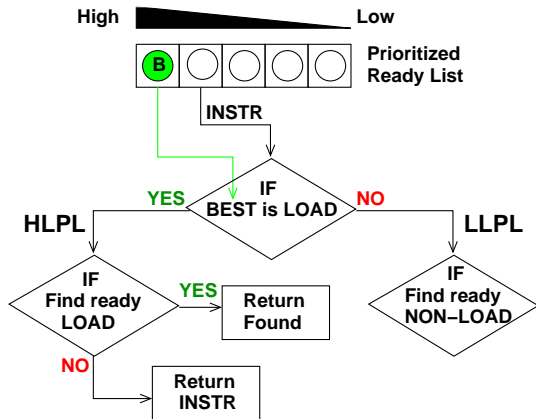
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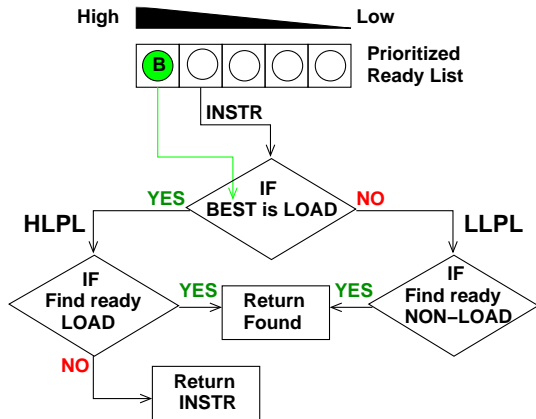
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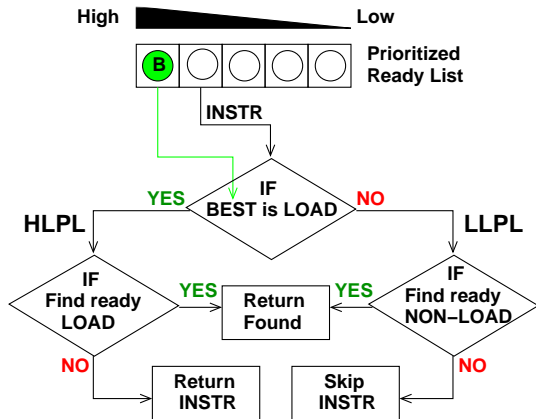
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Outline

Introduction

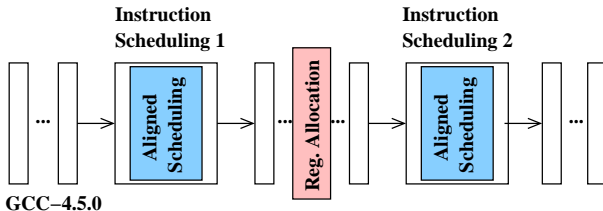
Aligned Scheduling

Experimental Setup and Results

Conclusion

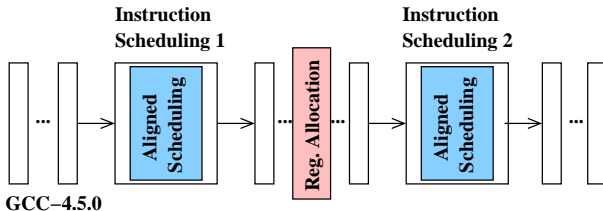
Experimental Setup

- Compiler: GCC-4.5.0, Modified Haifa-Scheduler



Experimental Setup

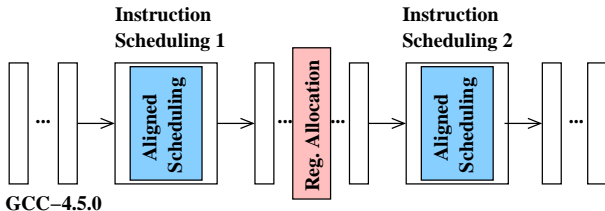
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- Architecture
 - IA64-based 4 issue VLIW
 - Modified SKI IA64 simulator

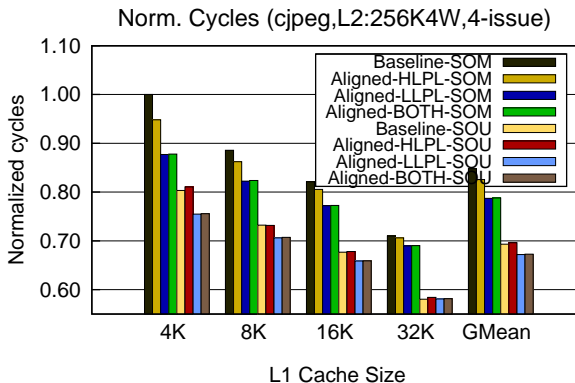
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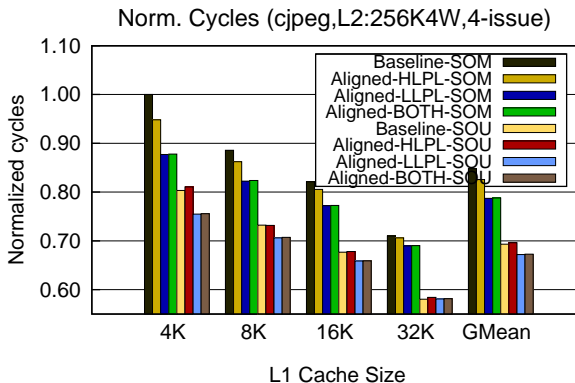
- Architecture
 - IA64-based 4 issue VLIW
 - Modified SKI IA64 simulator
- Benchmarks: SPEC CINT2000 and MediabenchII Video

Results: cjpeg (4-issue), Cycles



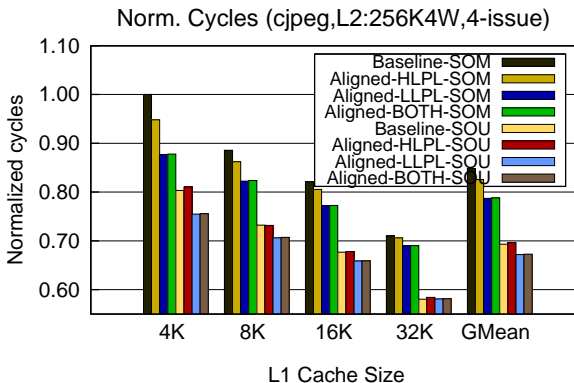
- Big improvement for small L1

Results: cjpeg (4-issue), Cycles



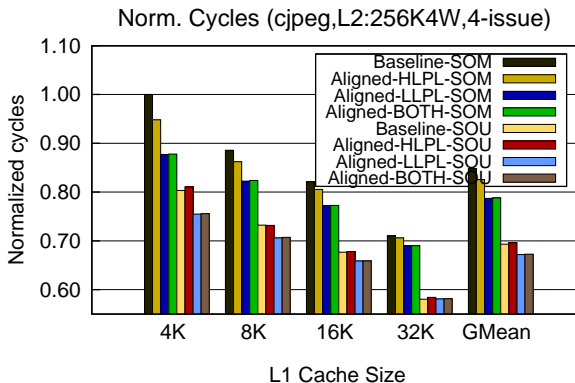
- Big improvement for small L1
- HLPL and LLPL act cooperatively

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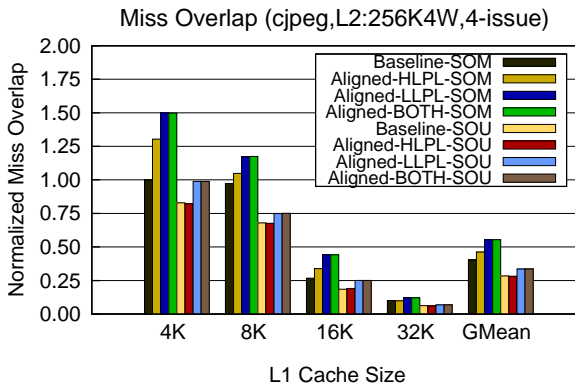
- Big improvement for small L1
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- Improves SOM, performance close to SOM on double the cache.

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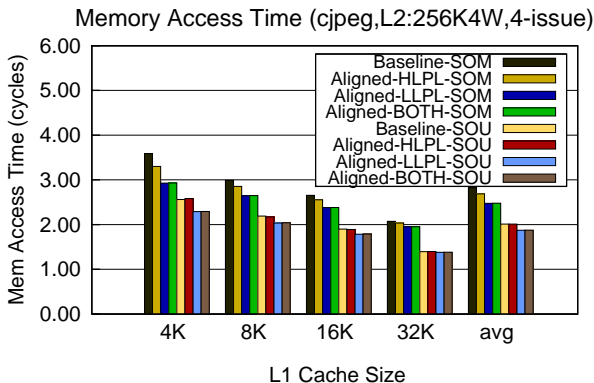
- Big improvement for small L1
- HLPL and LLPL act cooperatively
- Improves SOM, performance close to SOM on double the cache.
- Improves SOU

Results: cjpeg (4-issue), Miss-Overlap



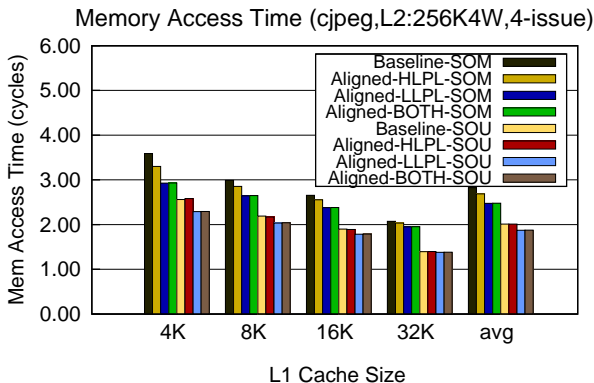
- Increase Miss overlapping, proof that Aligned Scheduling achieves its goal

Results: cjpeg (4-issue), Mem Access Time



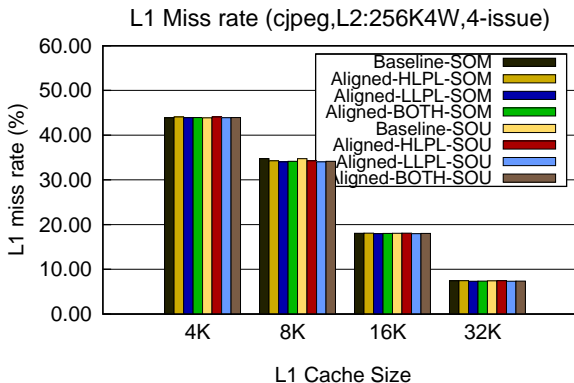
- Aligned scheduling improves the average memory access time

Results: cjpeg (4-issue), Mem Access Time



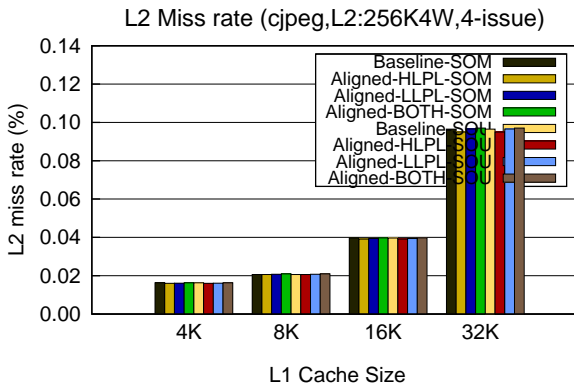
- Aligned scheduling improves the average memory access time
- Proof that Aligned Scheduling helps hide cache misses

Results: cjpeg (4-issue), Miss Rates



- Miss Rates don't change
- A miss is count as a miss even if it overlaps

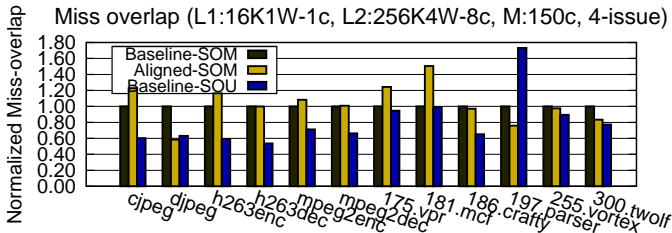
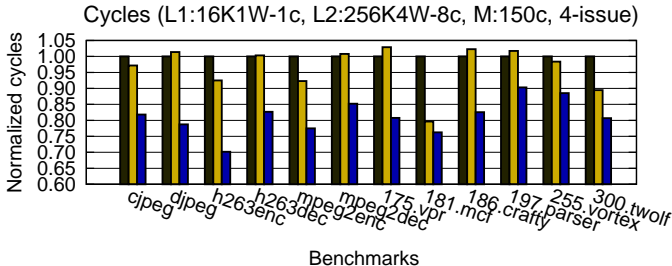
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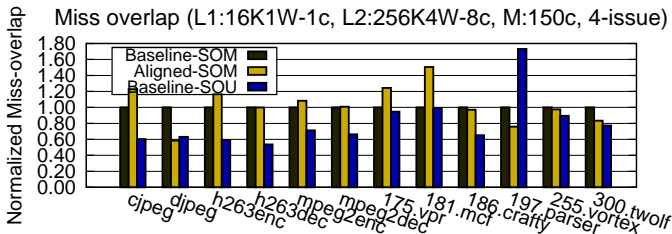
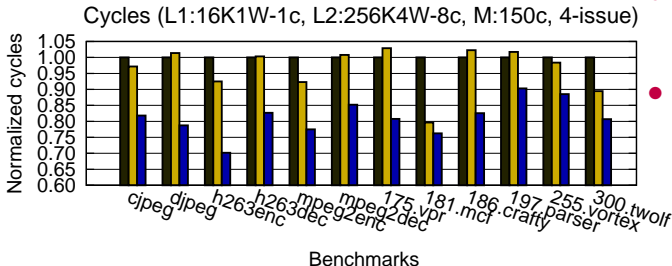
Results: All Benchmarks, Performance

- Improves SOM on avg

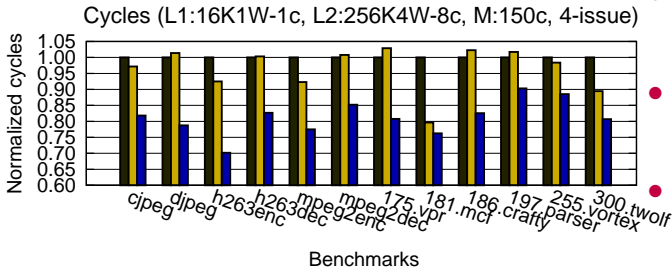


Results: All Benchmarks, Performance

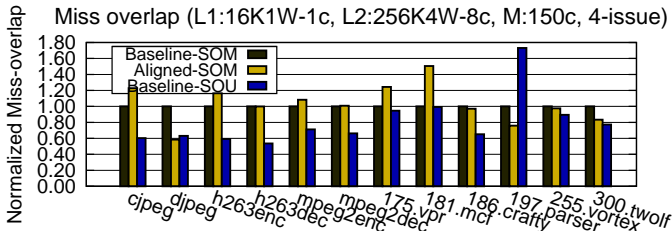
- Improves SOM on avg
- Up to 20% speedup



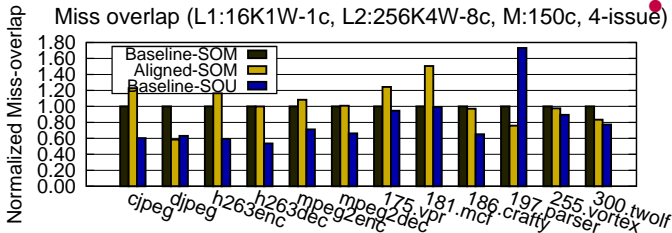
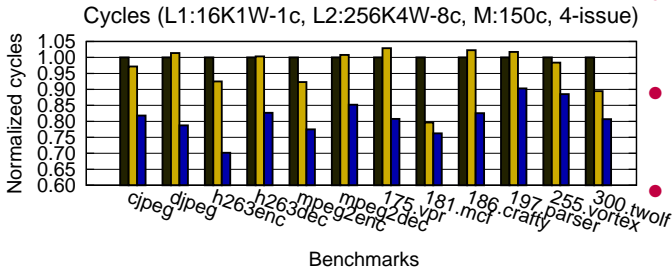
Results: All Benchmarks, Performance



- Improves SOM on avg
- Up to 20% speedup
- Up to 3% slowdown

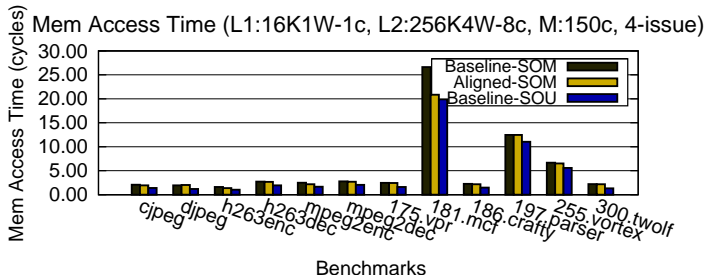


Results: All Benchmarks, Performance



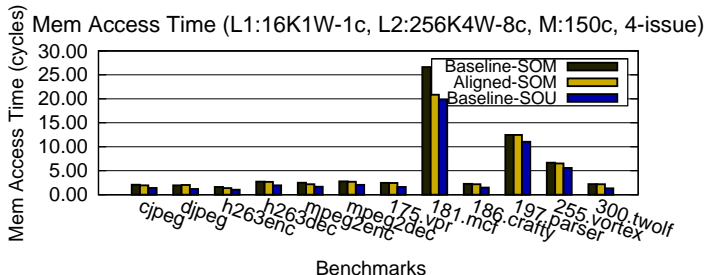
- Improves SOM on avg
- Up to 20% speedup
- Up to 3% slowdown
- Correlation between Miss overlapping and performance

Results: All Benchmarks, Mem Access Time



- Improved memory access latency

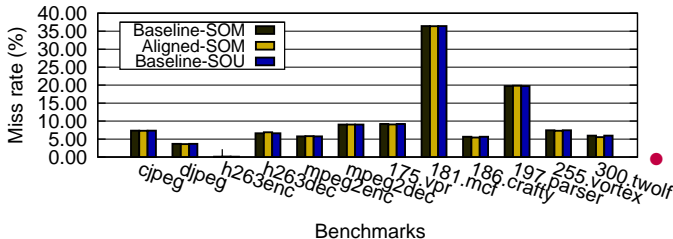
Results: All Benchmarks, Mem Access Time



- Improved memory access latency
- SOU consistently better at hiding latencies (hardware support)

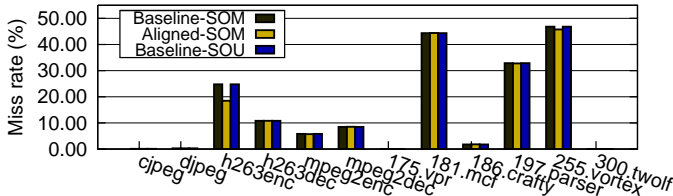
Results: All Benchmarks, Miss Rates

L1 Miss rate (L1:16K1W-1c, L2:256K4W-8c, M:150c, 4-issue)



• Miss rates remain largely unchanged

L2 Miss rate (L1:16K1W-1c, L2:256K4W-8c, M:150c, 4-issue)



Conclusion

Proposed Aligned Scheduling, a scheduler for VLIWs that:

- Incorporates micro-architectural knowledge of load-use interlocking hardware
- Exploits statically known MLP
- Generates schedules resilient to cache misses on VLIWs

Aligned Scheduling: Cache-efficient Instruction Scheduling for VLIW Processors

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School of Informatics, University of Edinburgh[†]
Intel Labs Braunschweig[★]

LCPC 2013