EE 301 Analog Circuits

Course Project Part-II:
INA, Filters, MOSFETs and Inverter

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2023EEB1252

October 30, 2025

Objective

The objective of this work is to simulate and study basic analog circuits. This includes analyzing the gain and common-mode rejection of a three Op-Amp instrumentation amplifier, observing the frequency response of an Op-Amp based band-pass filter, characterizing NMOS and PMOS transistors in 180 nm technology through their output and trans-conductance characteristics, and simulating a CMOS inverter to study its voltage transfer and switching behavior. These exercises help in understanding the practical operation of amplifiers, filters, MOSFETs, and inverters in analog circuit design.

1 Instrumentation Amplifier

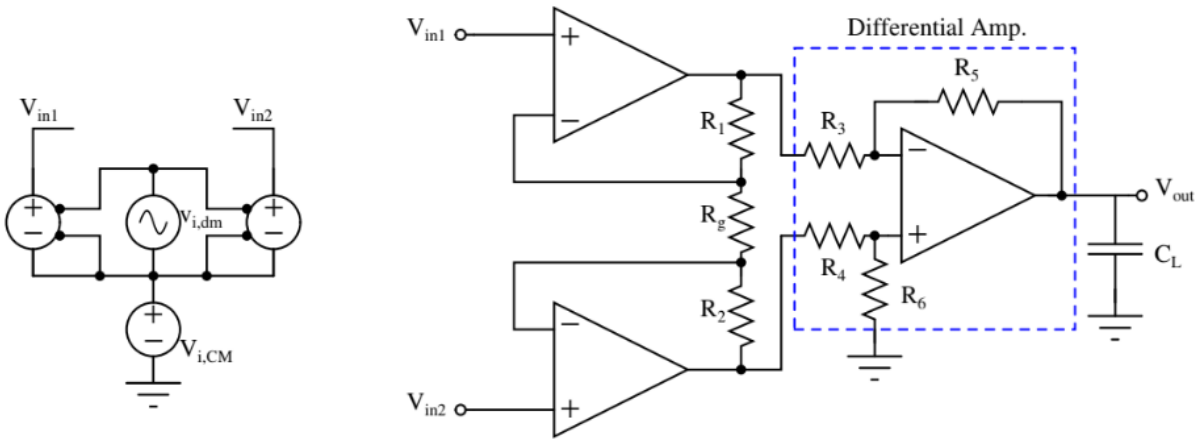

Figure 1: Instrumentation amplifier

1. Deriving the expression for the differential mode voltage gain ($A_{v,dm} = \frac{v_{out}}{v_{i,dm}}$) of the three Op-Amp INA, as shown in Figure 1.

   Differential Mode Gain Derivation:

   The three Op-Amp INA consists of two buffer/gain stages followed by a differential amplifier.

   The input stage produces an output difference:

$$v_{o2} - v_{o1} = \left(1 + \frac{2R_1}{R_g}\right) v_{i,dm},$$

   where $v_{i,dm} = v_{in2} - v_{in1}$. The differential amplifier stage scales this by R_5/R_3. Hence,

$$A_{v,dm} = \frac{v_{out}}{v_{i,dm}} = \frac{R_5}{R_3}\left(1 + \frac{2R_1}{R_g}\right).$$

2. Performing transient simulation by applying sinusoidal signal as differential signals $v_{i,dm}$.

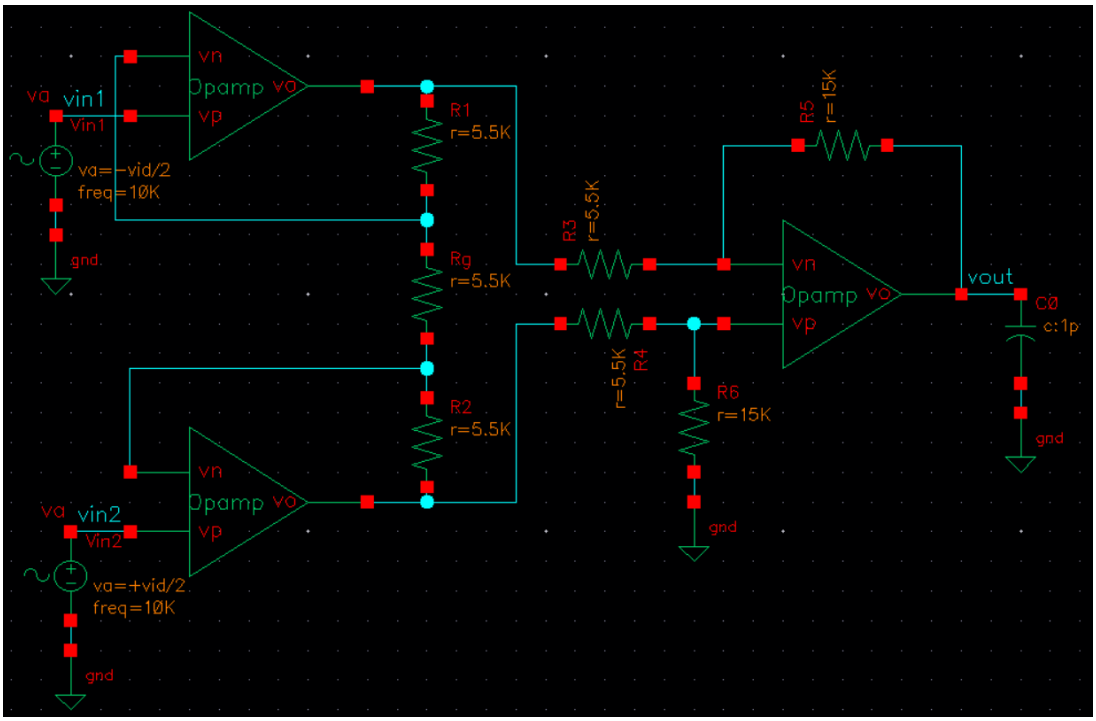

Figure 2: Circuit schematic for differential mode

Given values:

$$R_g = R_1 = R_2 = R_3 = R_4 = 5.5\ \text{k}\Omega, \quad R_5 = R_6 = 15\ \text{k}\Omega, \quad C_L = 1\ \text{pF}.$$

$$A_{v,dm} = \frac{15}{5.5}\left(1 + \frac{2 \cdot 5.5}{5.5}\right) \approx 8.18\ (\approx 18.26\ \text{dB}).$$

Observations :

$V_{i,dm}$ (mV)	V_{out} (mV)	$A_{v,dm}$ (mV/mV)	$A_{v,dm}$ (dB)
1	8.125	8.125	18.196
50	406.265	8.125	18.196
100	812.565	8.126	18.198
150	1218.866	8.126	18.198
200	1625.3	8.126	18.198

Table 1: Differential gain observations

The measured differential gains give a mean $\overline{A_{v,dm}} \approx 8.126$ with very small variation. The theoretical value is $A_{v,dm}^{\text{th}} \approx 8.182$ (18.26 dB), so the measured gain is lower by only about 0.7% (≈ 0.06 dB). This minor difference arises from numerical resolution, non-ideal Op-Amp behavior, and loading by C_L.

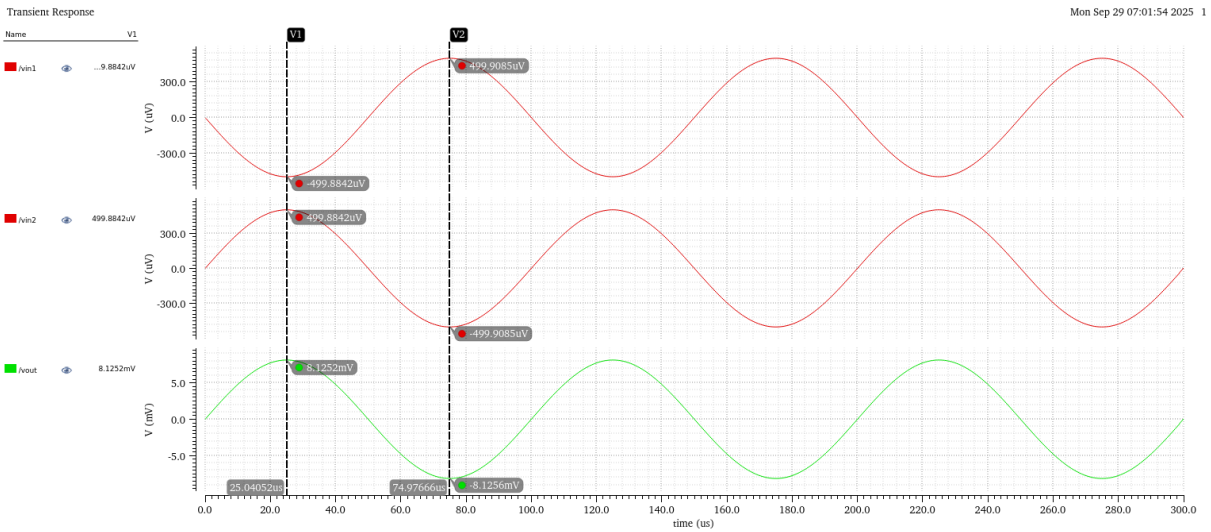

Figure 3: For $V_{i,dm} = 1mV$

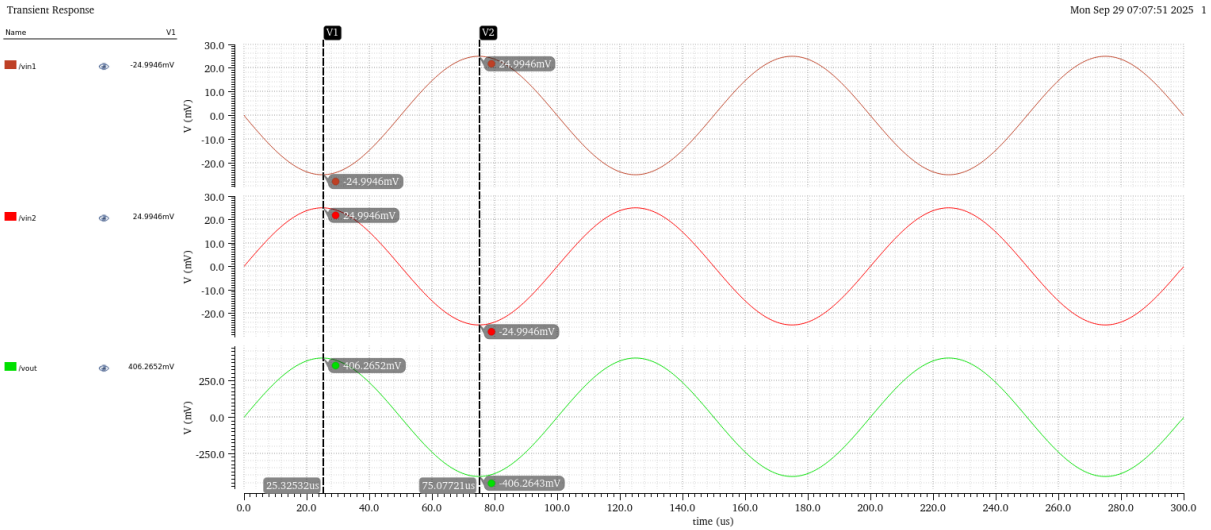

Figure 4: For $V_{i,dm} = 50mV$

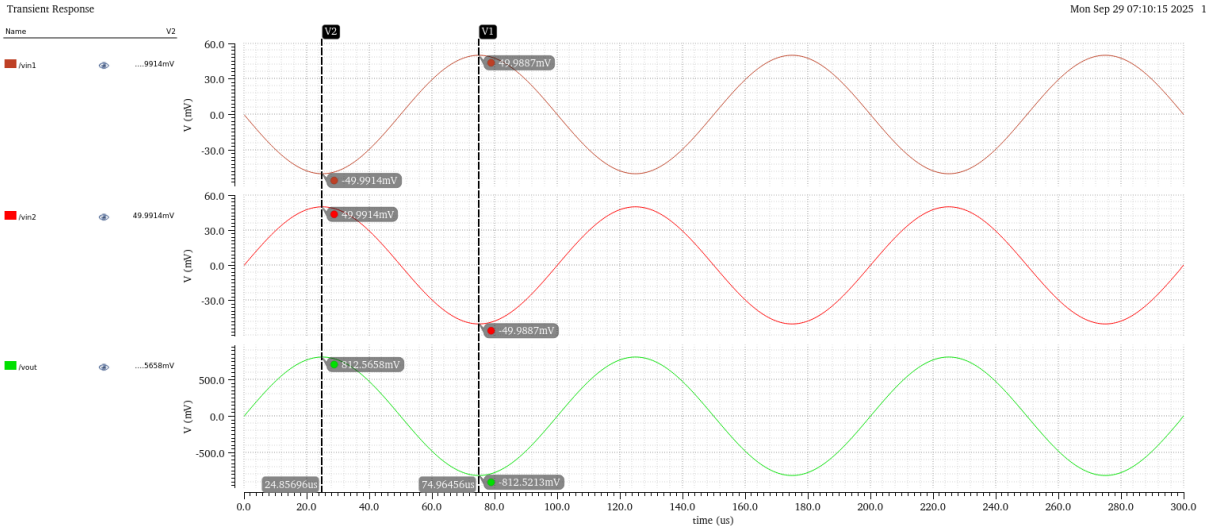

Figure 5: For $V_{i,dm} = 100mV$

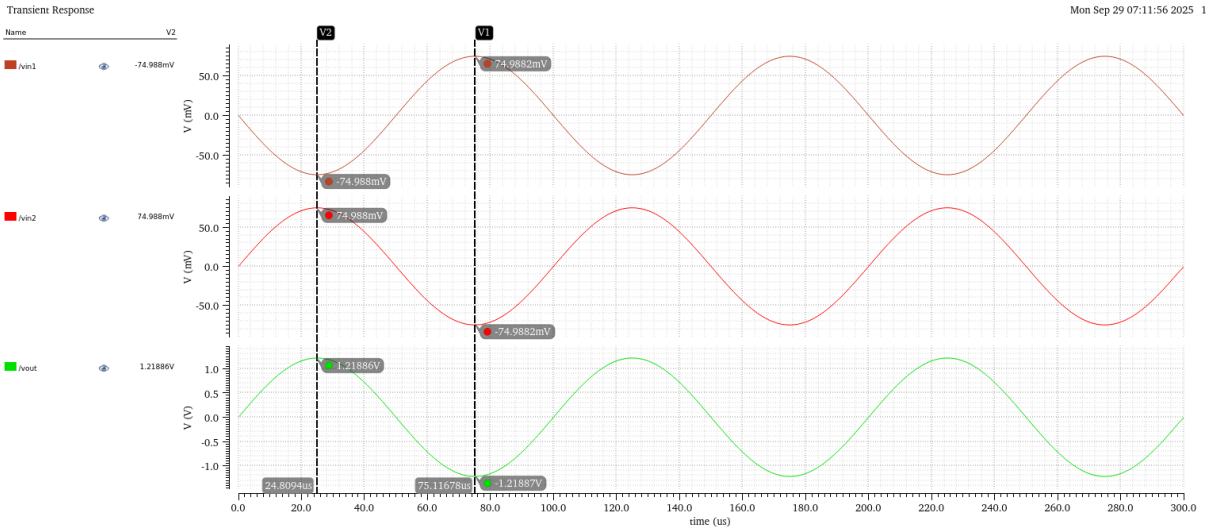

Figure 6: For $V_{i,dm} = 150mV$

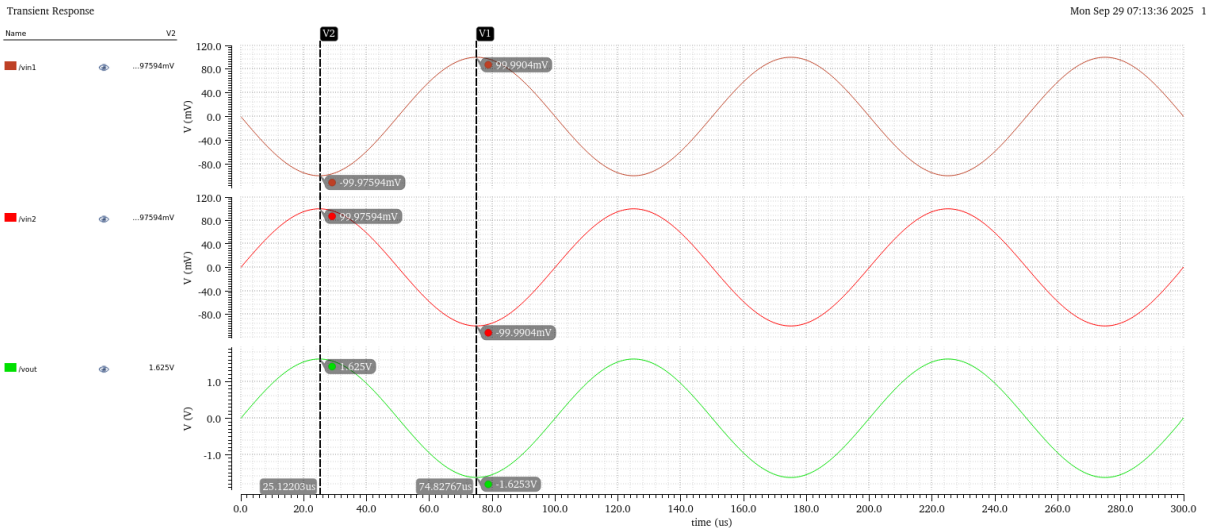

Figure 7: For $V_{i,dm} = 200mV$

3. Determining the common-mode gain by performing a transient simulation. Applying sinusoidal signals as common mode signals $V_{i,cm}$.

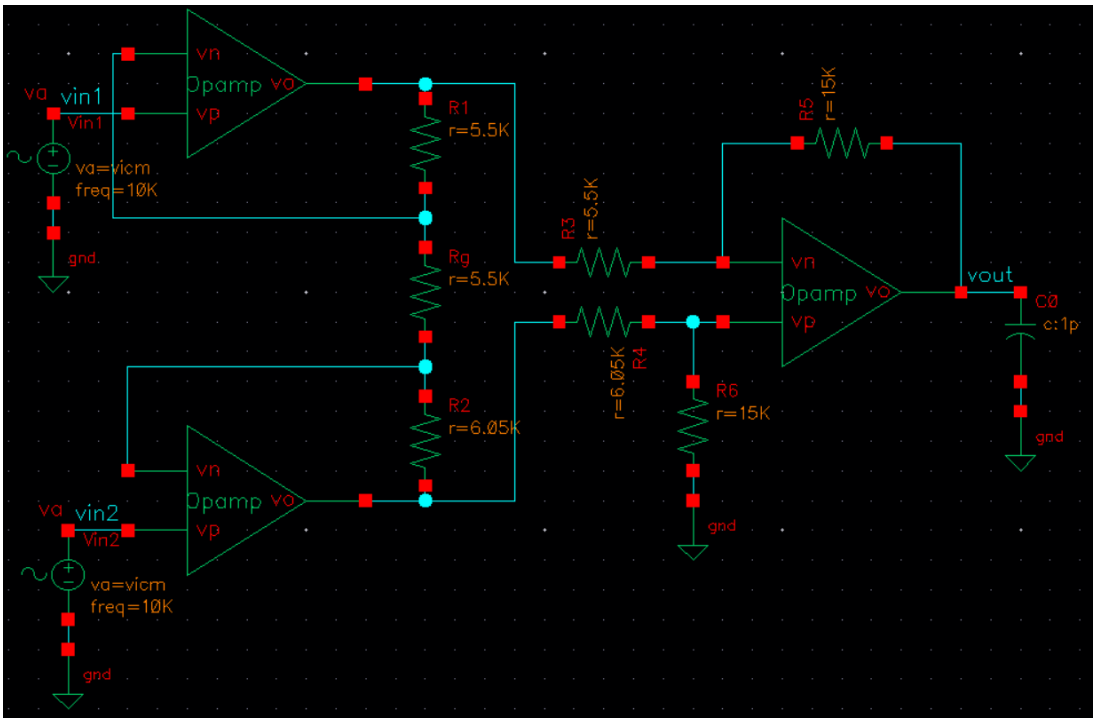

Figure 8: Circuit schematic for common mode

Resistor mismatch:

$$R_1 = 5.5\ \text{k}\Omega, \quad R_2 = R_1(1+0.1) = 6.05\ \text{k}\Omega,$$

$$R_3 = 5.5\ \text{k}\Omega, \quad R_4 = R_3(1+0.1) = 6.05\ \text{k}\Omega.$$

Observations :

$V_{i,cm}$ (mV)	V_{out} (mV)	$A_{v,cm}$ (mV/mV)	$A_{v,cm}$ (dB)
1	0.071	0.071	-22.975
50	3.546	0.071	-22.975
100	7.091	0.071	-22.975
150	10.636	0.071	-22.975
200	14.183	0.071	-22.975

Table 2: Common mode gain observations

The common-mode simulations give a nearly constant gain $A_{v,cm} \approx 0.071$ (-22.98 dB) across all tested input amplitudes, as shown in Table 2. This nonzero but very small value arises from resistor mismatch and finite Op-Amp non-idealities. Ideally the INA should reject all common-mode input, so the result confirms that common-mode components are strongly attenuated compared to the differential signal.

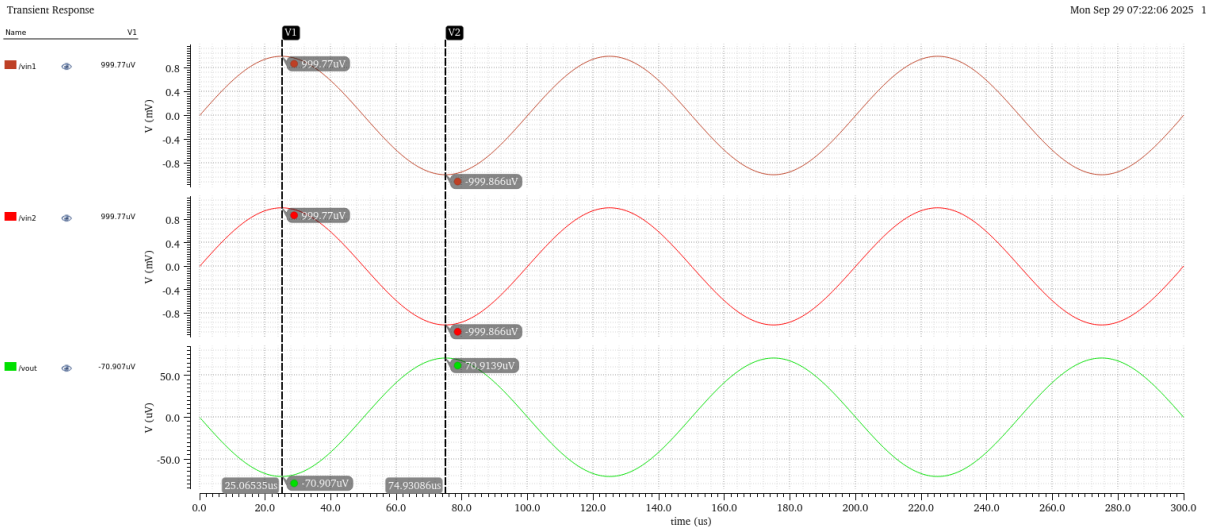

Figure 9: For $V_{i,cm} = 1mV$

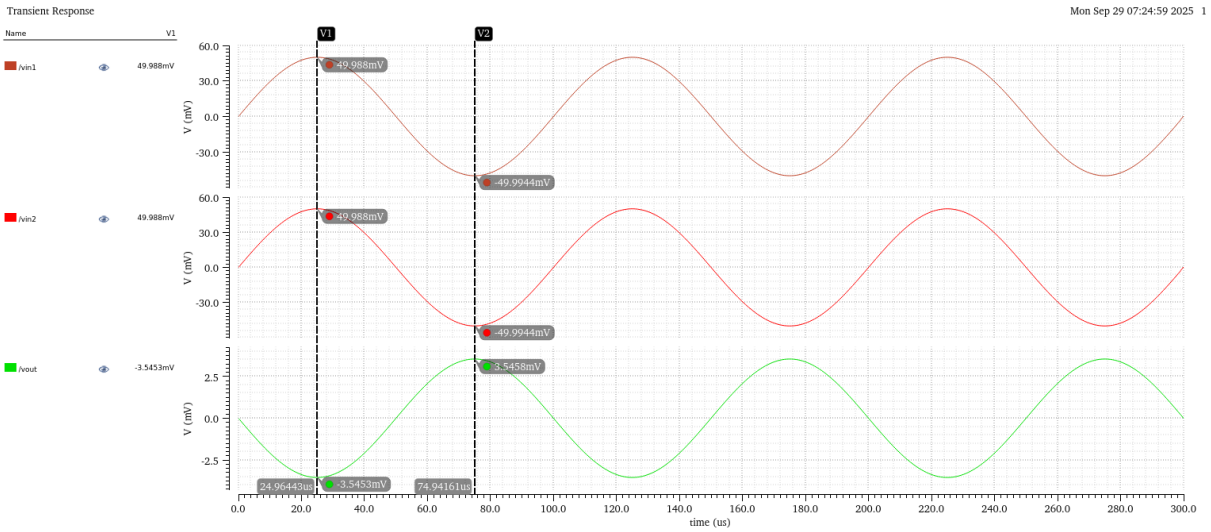

Figure 10: For $V_{i,cm} = 50mV$

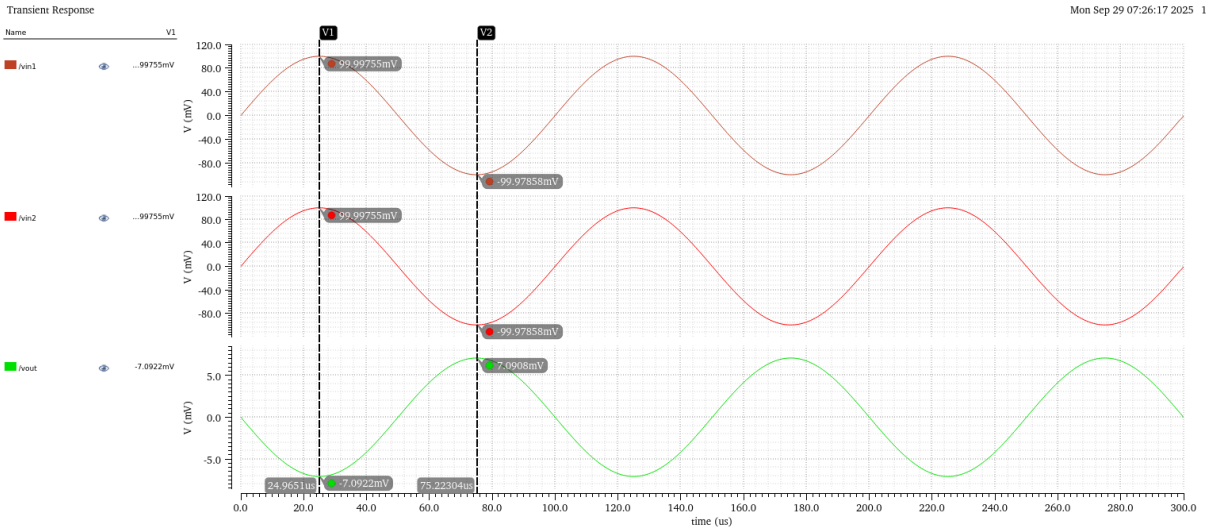

Figure 11: For $V_{i,cm} = 100mV$

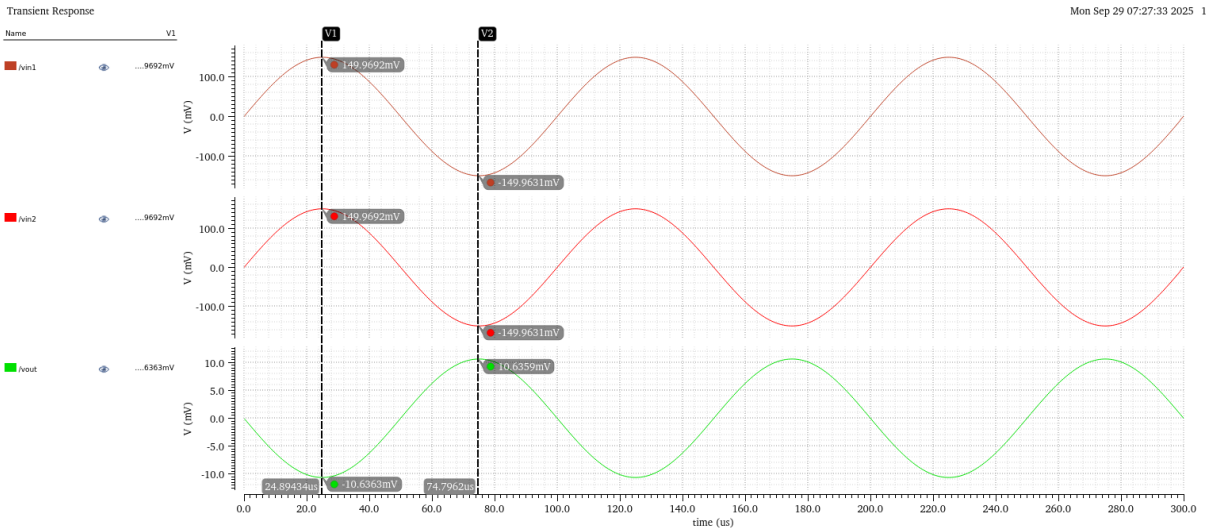

Figure 12: For $V_{i,cm} = 150mV$

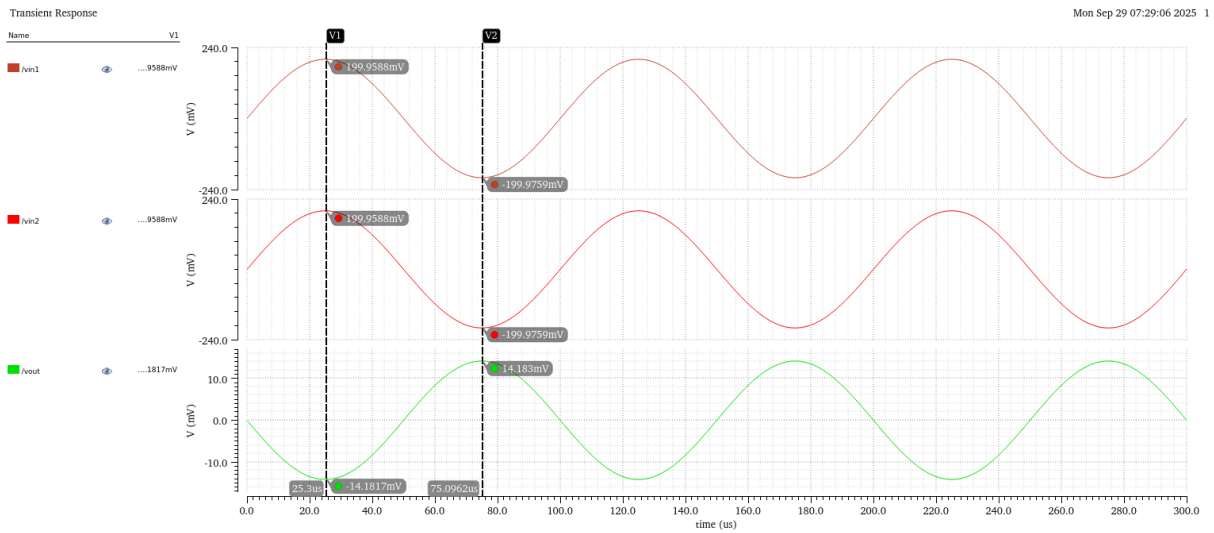

Figure 13: For $V_{i,cm} = 200mV$

4. Calculations of the common mode rejection ratio (CMRR).

   The measured differential gain is $\overline{A_{v,dm}} \approx 8.126$ (18.20 dB), and the measured common-mode gain is $A_{v,cm} \approx 0.071$ (-22.98 dB).

$$\text{CMRR} = \frac{A_{v,dm}}{A_{v,cm}} = \frac{8.126}{0.071} \approx 114.4, \qquad \text{CMRR}_{dB} = 20\log_{10}(114.4) \approx 41.2 \text{ dB}.$$

   A higher CMRR indicates better rejection of common-mode signals. The obtained value confirms good suppression of common-mode input, though not ideal due to resistor mismatch and Op-Amp non-idealities.

2 Band-pass Filter

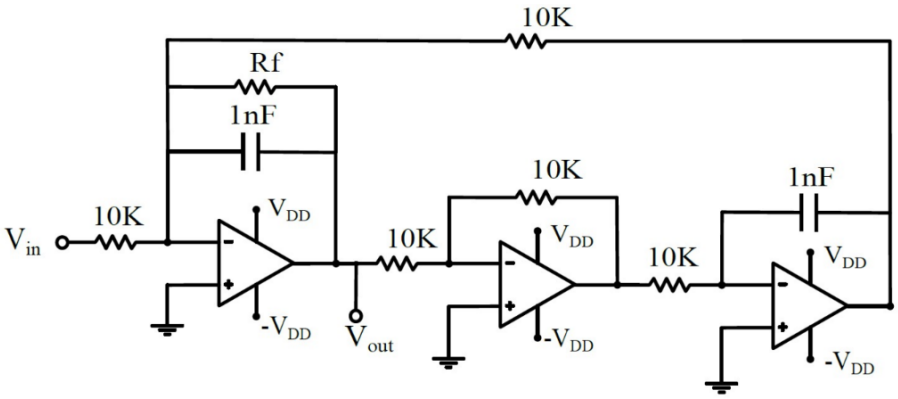

Figure 14: Band-pass filter using Op-Amp

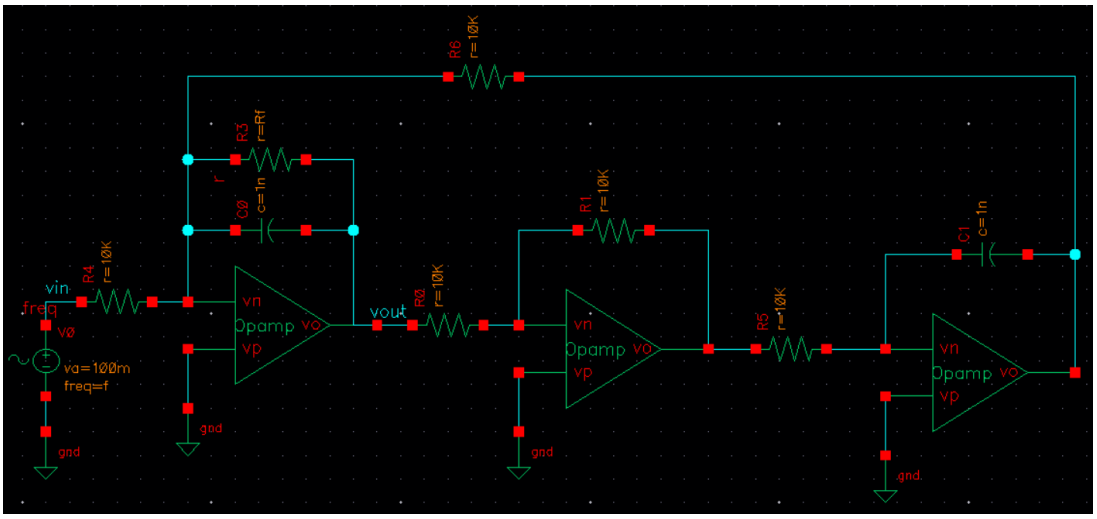

Figure 15: Circuit schematic on Cadence Virtuoso for band-pass filter using Op-Amp

1. Simulating the schematic of the band-pass filter shown in Figure 14 with $R_f = 100\,\text{K}\Omega$ (corresponding to $Q = 10$). Performing a transient simulation by applying a sinusoidal input signal of amplitude 100 mV, while varying the frequency from 1 KHz to 25 KHz in steps of 1 KHz.

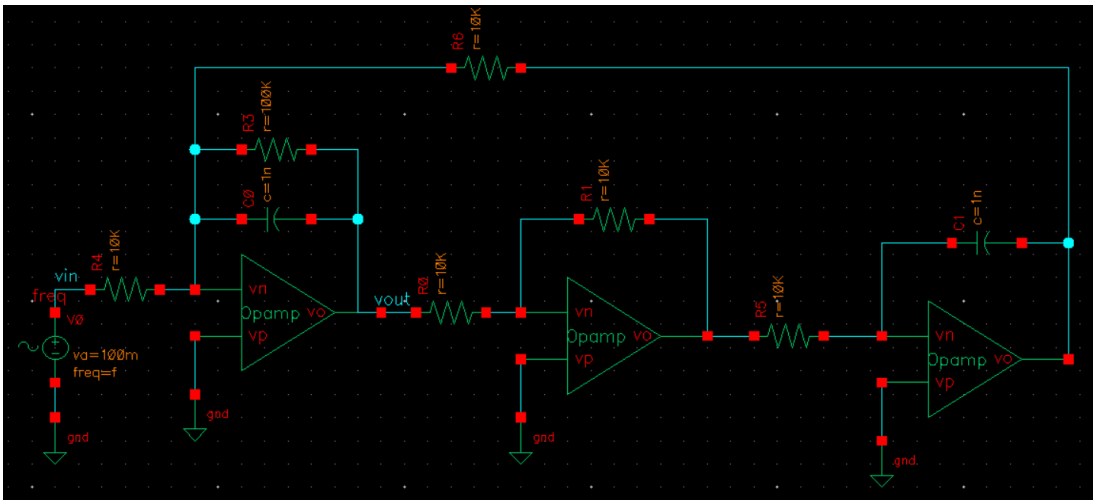

Figure 16: Band-pass filter with $R_f = 100\,\text{K}\Omega$ (corresponding to $Q = 10$)

Observations:

The band-pass filter allows frequencies around 16 KHz to pass with maximum amplitude, as seen from the output voltage reaching 931 mV and gain peaking at 19.38 dB at this frequency. Frequencies below 10 KHz and above 20 KHz are significantly attenuated, confirming the filter's stop-band behavior. The gain curve is roughly symmetric around the center frequency, consistent with the expected behavior of a filter with quality factor $Q = 10$. This demonstrates that the filter effectively selects the desired frequency range while suppressing unwanted frequencies.

Table 3: Band-pass filter (transient simulation)

Frequency f (Hz)	Gain (dB)	Output Voltage V_{out} (mV)
1000	-20.86	9.05
2000	-14.24	19.4
3000	-10.74	29.1
4000	-7.595	41.7
5000	-6.543	47.1
6000	-3.957	63.4
7000	-1.882	80.5
8000	-0.661	92.7
9000	1.941	125
10000	4.174	162
11000	5.964	199
12000	8.276	259
13000	10.66	341
14000	13.57	477
15000	17.16	721
16000	19.38	931
17000	16.11	639
18000	13.48	472
19000	11.53	377
20000	9.952	315
21000	8.552	268
22000	7.493	237
23000	6.306	207
24000	5.397	186
25000	4.743	173

2. Performing an AC simulation to find out the frequency response of the BPF and comparing the gain A_v w.r.t. the transient simulation gain, and finding out the center frequency.

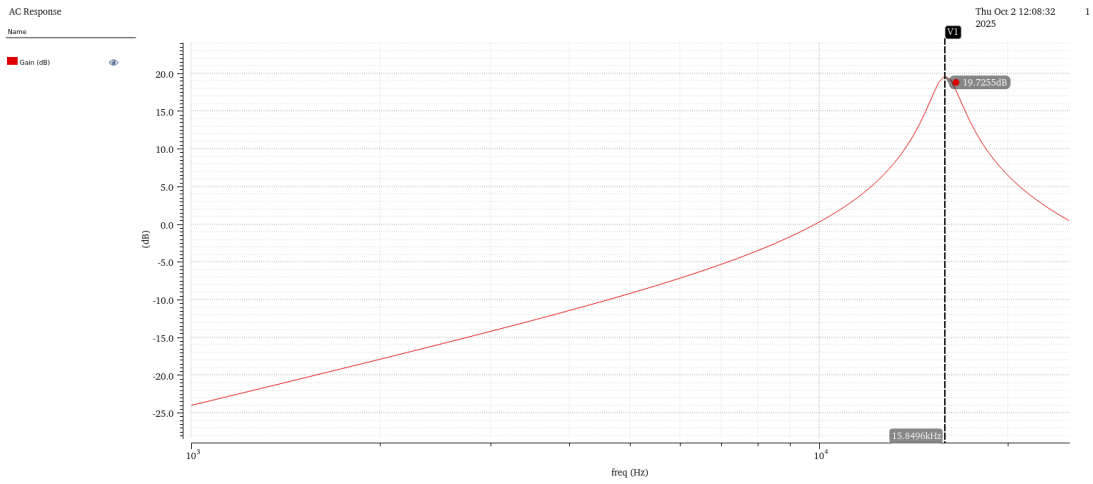

Figure 17: AC response of band-pass filter with $R_f = 100\,\text{K}\Omega$ (corresponding to $Q = 10$)

Observations:

Table 4: AC simulation gain of band-pass filter ($Q = 10$, $R_f = 100$ KΩ)

Frequency f (Hz)	Gain (dB)
1000	-23.98
2000	-17.85
3000	-14.16
4000	-11.40
5000	-9.131
6000	-7.12
7000	-5.248
8000	-3.429
9000	-1.595
10000	0.323
11000	2.409
12000	4.778
13000	7.625
14000	11.29
15000	16.25
16000	19.46
17000	15.37
18000	11.37
19000	8.545
20000	6.457
21000	4.821
22000	3.479
23000	2.346
24000	1.366
25000	0.508

From the AC analysis for $Q = 10$, the maximum gain is observed to be 19.7255 dB at a center frequency of approximately 15.8496 KHz. Comparing this with the transient simulation data, the peak gain matches closely, showing consistency between the two methods. The filter with $Q = 10$ exhibits a narrow pass-band and sharp selectivity, which is characteristic of a high–Q band-pass filter.

The approximate center frequency of the band-pass filter is given by

$$f_0 = \frac{1}{2\pi RC},$$

which depends only on R and C.

With $R = 10\,\text{K}\Omega$ and $C = 1\,\text{nF}$,

$$f_0 \approx 15.92\,\text{KHz}.$$

The AC analysis gives $f_0 \approx 15.8496$ KHz with a maximum gain of 19.7255 dB, which matches well with the theoretical value. The transient response also confirms the same behavior with a sharp, narrow pass-band.

3. Simulating the schematic of the band-pass filter shown in Figure 14 with $R_f = 20\,\text{K}\Omega$ (corresponding to $Q = 2$). Performing a transient simulation by applying a sinusoidal input signal of amplitude 100 mV, while varying the frequency from 1 KHz to 25 KHz in steps of 1 KHz.

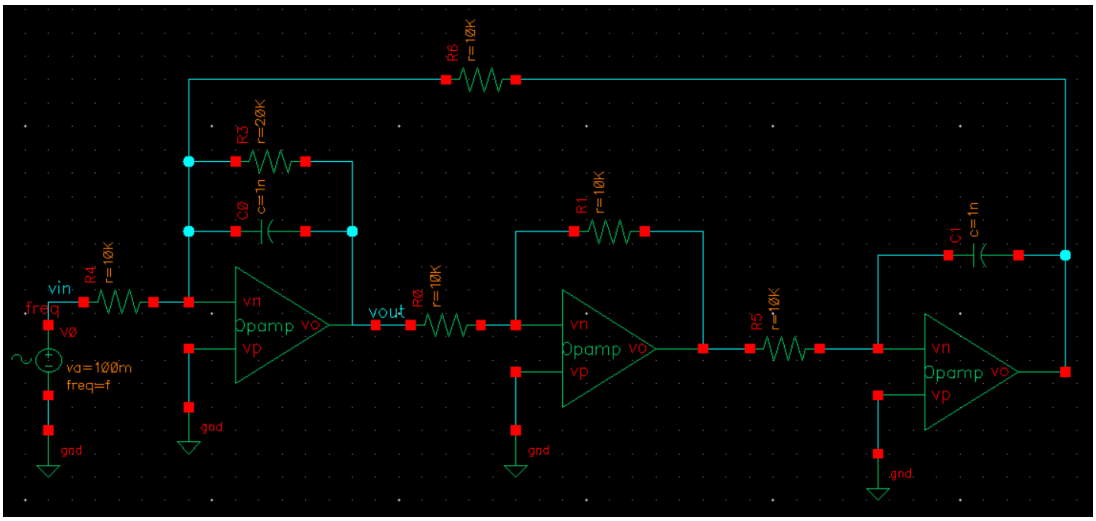

Figure 18: Band-pass filter with $R_f = 20\,\text{K}\Omega$ (corresponding to $Q = 2$)

Observations:

For $Q = 2$ and $R_f = 20$ KΩ, the band-pass filter exhibits a lower peak gain compared to the higher-Q case, with the maximum output voltage of 198 mV occurring around 16 KHz and a gain of 5.928 dB. The response is much broader, indicating a wider pass-band, and the filter attenuates frequencies less sharply outside the center frequency. Frequencies below 10 KHz and above 20 KHz are only moderately attenuated. This demonstrates that a lower quality factor reduces the selectivity of the filter, allowing a wider range of frequencies to pass while decreasing the peak gain.

Table 5: Band-pass filter (transient simulation)

Frequency f (Hz)	Gain (dB)	Output Voltage V_{out} (mV)
1000	-22.29	7.68
2000	-16.34	15.2
3000	-12.89	22.7
4000	-10.35	30.4
5000	-8.642	37.0
6000	-7.085	44.2
7000	-4.909	56.8
8000	-3.05	70.4
9000	-1.457	84.6
10000	0.100	101
11000	1.366	117
12000	2.769	138
13000	3.98	158
14000	5.046	179
15000	5.762	194
16000	5.928	198
17000	5.611	191
18000	5.081	180
19000	4.49	168
20000	3.907	157
21000	3.337	147
22000	2.683	136
23000	2.169	128
24000	1.76	123
25000	1.316	116

4. Performing an AC simulation to find out the frequency response of the BPF and comparing the gain A_v w.r.t. the transient simulation gain, and finding out the center frequency.

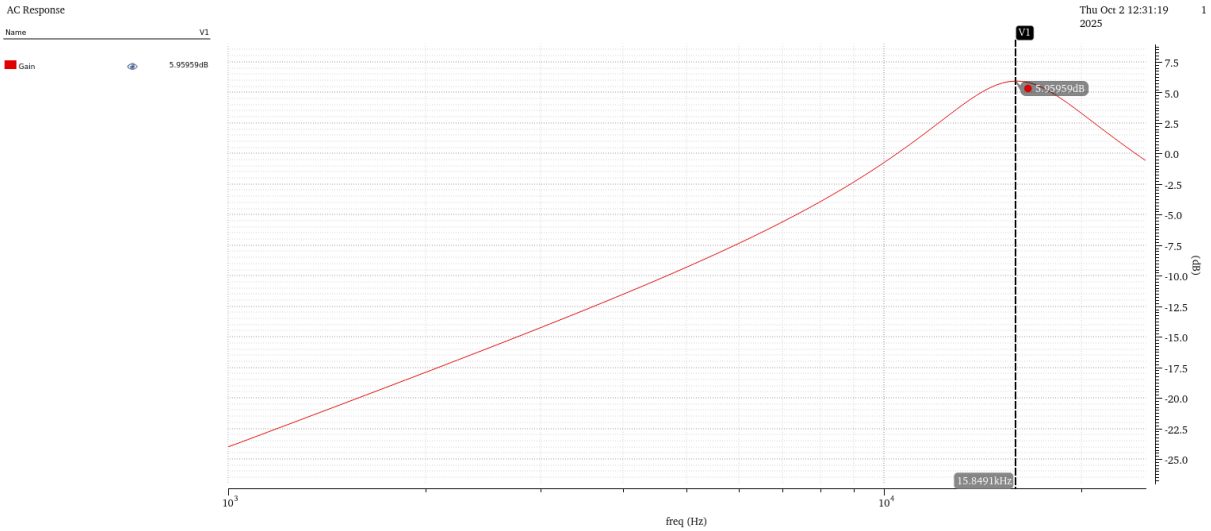

Figure 19: AC response of band-pass filter with $R_f = 200\,\text{K}\Omega$ (corresponding to $Q = 2$)

Observations:

Table 6: AC simulation gain of band-pass filter ($Q = 2$, $R_f = 20$ KΩ)

Frequency f (Hz)	Gain (dB)
1000	-23.98
2000	-17.87
3000	-14.20
4000	-11.48
5000	-9.262
6000	-7.324
7000	-5.556
8000	-3.888
9000	-2.275
10000	-0.691
11000	0.872
12000	2.392
13000	3.802
14000	4.974
15000	5.731
16000	5.948
17000	5.656
18000	4.999
19000	4.171
20000	3.289
21000	2.423
22000	1.601
23000	0.834
24000	0.121
25000	-0.539

From the AC analysis for $Q = 2$, the maximum gain is observed to be 5.9596 dB at a center frequency of approximately 15.8491 KHz. The transient simulation shows the same trend, though the gain is much lower and the pass-band is significantly broader, which is typical of a low–Q band-pass filter.

The approximate center frequency of the band-pass filter is given by

$$f_0 = \frac{1}{2\pi RC}.$$

With $R = 10\,\mathrm{K}\Omega$ and $C = 1\,\mathrm{nF}$,

$$f_0 \approx 15.92\,\mathrm{KHz}.$$

The AC analysis gives $f_0 \approx 15.8491$ KHz with a maximum gain of 5.9596 dB. The transient response shows good agreement as well, but the pass-band is much wider and the selectivity is lower compared to the $Q = 10$ case.

3 Characterization of MOSFETs in 180nm CMOS Technology Node

3.1 NMOS Transistor Characterization (using W = 10 μm and L = 1 μm)

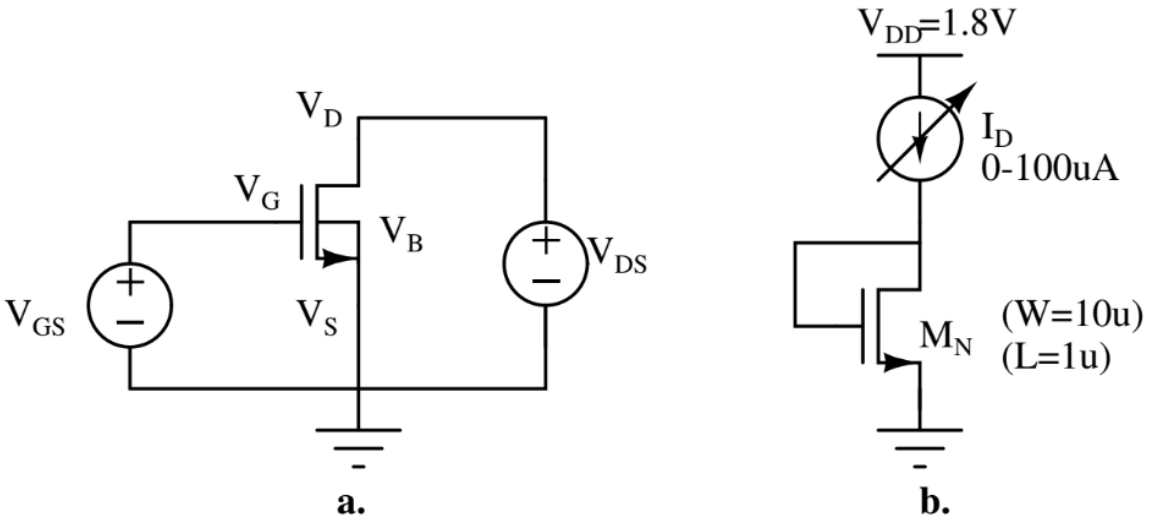

Figure 20: Schematic of the circuit a. for NMOS characterization and b. g_m simulation

1. Characterization of the NMOS transistor as shown in Figure 20a and simulation of the output characteristics plot. (i.e. I_D vs. V_{DS} for different V_{GS})

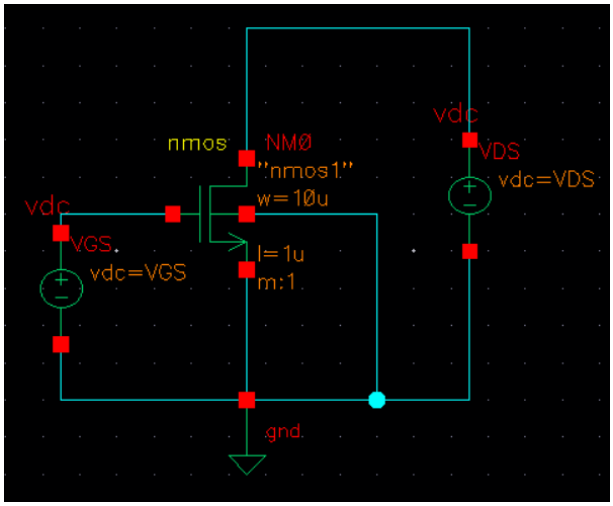

Figure 21: Schematic of the circuit on Cadence Virtuoso for NMOS characterization

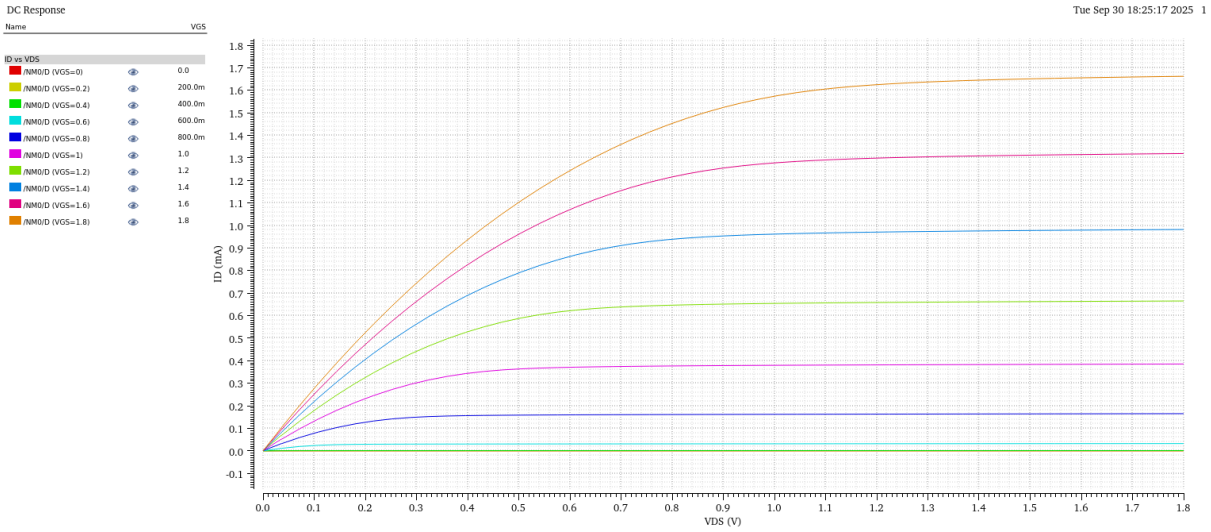

Figure 22: I_D vs. V_{DS} for different V_{GS}

Observations:

For the NMOS output characteristics, it is observed that the ID is zero till $V_{GS} - V_{th}$ and after that at low values of V_{DS} the transistor operates in the triode region, where the drain current increases almost linearly with V_{DS}. As V_{DS} increases beyond $(V_{GS} - V_{th})$, the device enters saturation and the drain current becomes nearly independent of V_{DS}. The saturation current rises with higher gate voltages, and a small slope appears in the saturation region due to channel length modulation.

2. Plotting the small-signal trans-conductance g_m as a function of drain current I_D for the transistor in Figure 20b by varing I_D.

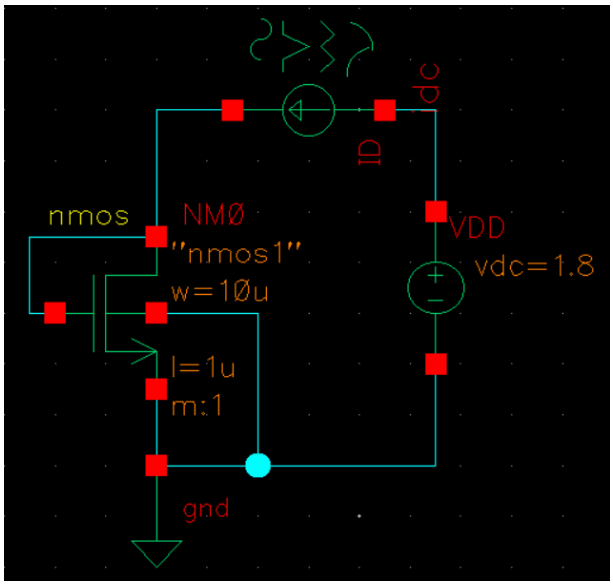

Figure 23: Schematic of the circuit on Cadence Virtuoso for g_m simulation.

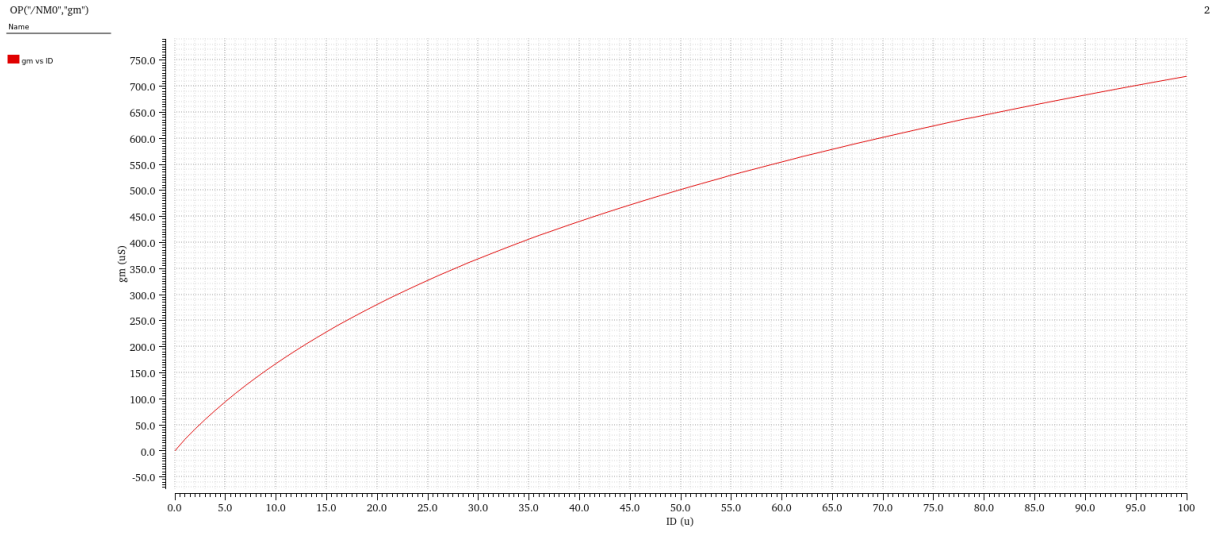

Figure 24: g_m vs I_D

Observations:

For the trans-conductance g_m plotted against the drain current I_D, the results show that g_m increases with I_D. In strong inversion, the relation follows a square-root dependence ($g_m \propto \sqrt{I_D}$), whereas in the subthreshold region g_m is approximately proportional to I_D with $g_m \approx I_D/(nV_T)$. The chosen aspect ratio of $W/L = 10$ enhances the trans-conductance for a given value of drain current.

3. Plotting I_D vs V_{DS} and explaining why this circuit is called a diode-connected NMOS transistor.

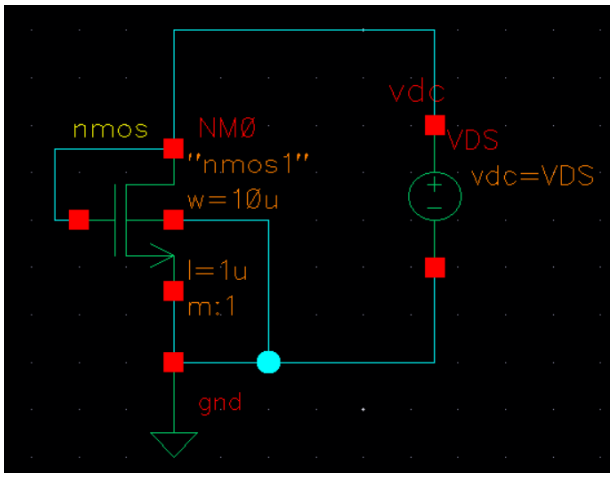

Figure 25: Schematic of the circuit on Cadence Virtuoso diode-connected NMOS transistor

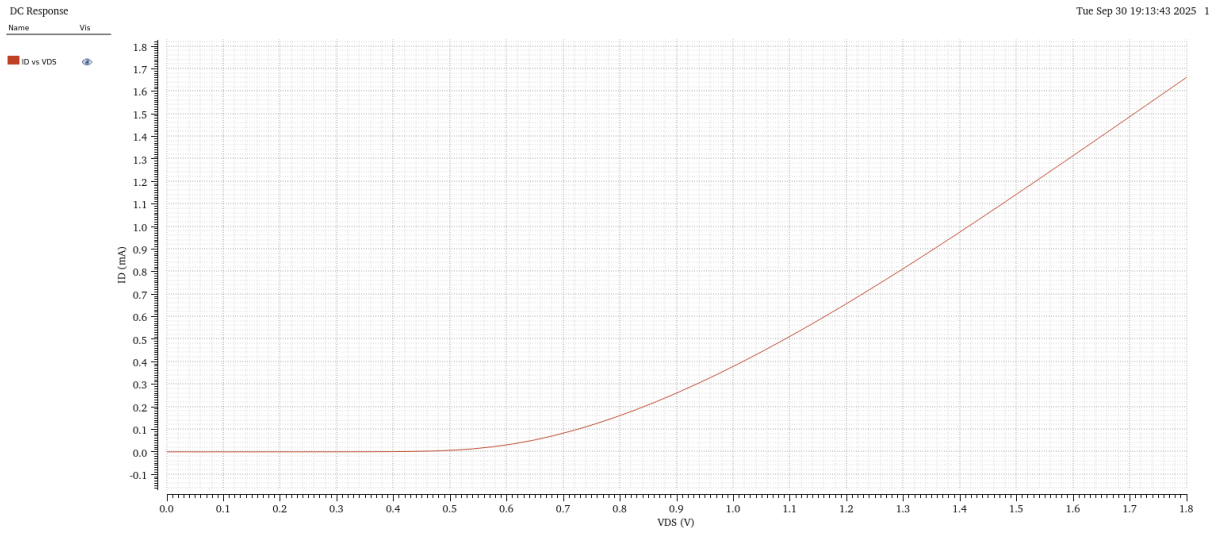

Figure 26: I_D vs V_{DS} for diode-connected NMOS transistor

Observations:

For the diode-connected NMOS, the I_D vs V_{DS} curve shows negligible current when V_{DS} is below the threshold voltage. Around $V_{DS} \approx V_{th}$ the current rises sharply, resembling the turn-on behavior of a diode. For voltages greater than the threshold, the transistor conducts strongly and the current follows the MOS conduction relation. With the gate and drain shorted together, the device behaves as a two-terminal element with diode-like characteristics, which is why it is called a diode-connected NMOS.

3.2 PMOS Transistor Characterization (using W = 10 μm and L = 1 μm)

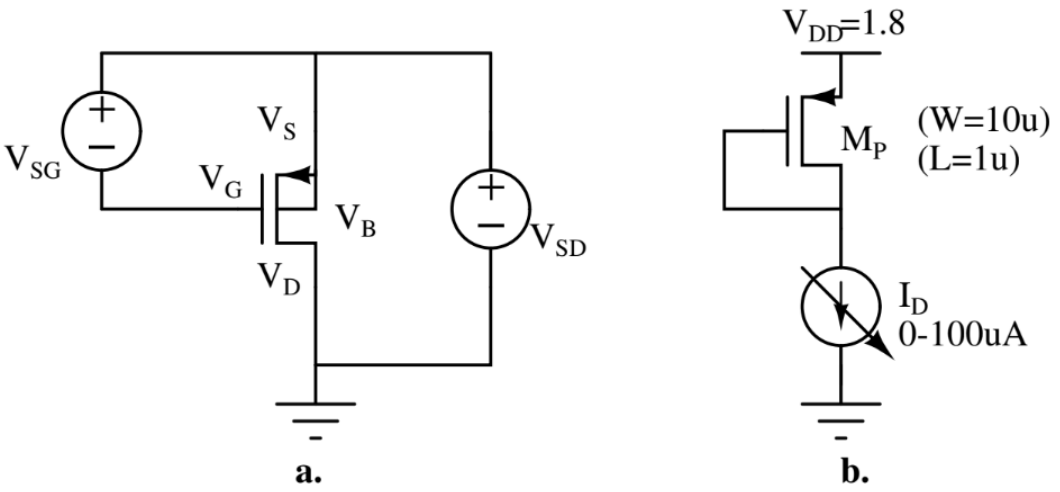

Figure 27: Schematic of the circuit a. for PMOS characterization and b. g_m simulation

1. Characterization of the PMOS transistor as shown in Figure 27a and simulation of the output characteristics plot. (i.e. I_D vs. V_{SD} for different V_{SG})

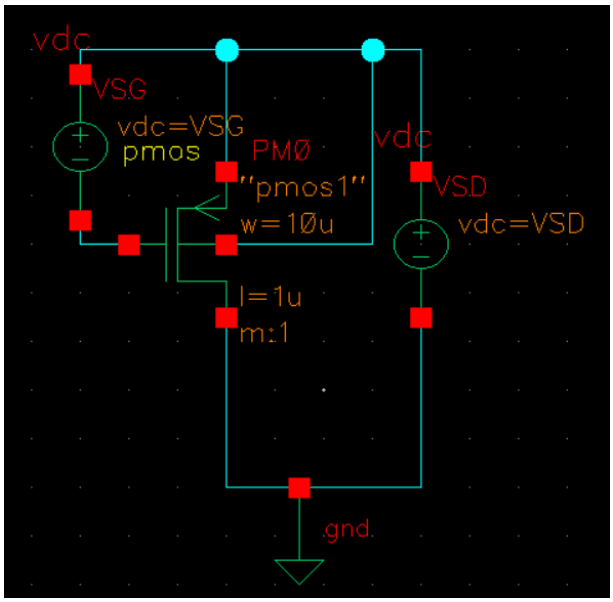

Figure 28: Schematic of the circuit on Cadence Virtuoso for PMOS characterization

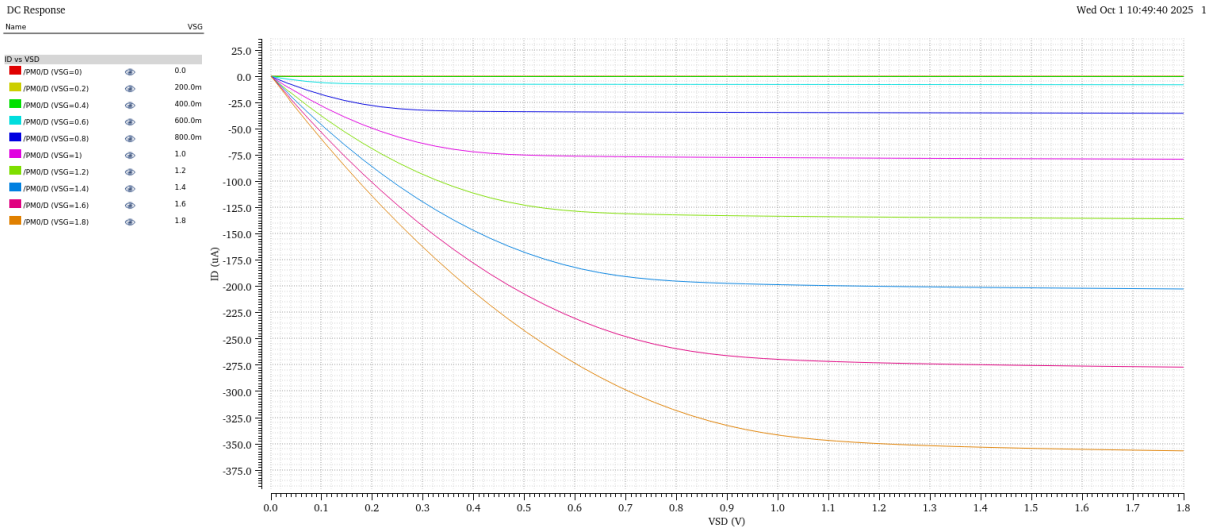

Figure 29: I_D vs. V_{SD} for different V_{SG}

Observations:

For the PMOS output characteristics, it is observed that at low values of V_{SD} the transistor operates in the triode region, where the drain current increases almost linearly with V_{SD}. As V_{SD} increases beyond $(V_{SG} - |V_{th}|)$, the device enters saturation and the drain current becomes nearly independent of V_{SD}. The saturation current rises with higher gate voltages (more negative V_{SG}), and a small slope appears in the saturation region due to channel length modulation.

2. Plotting the small-signal trans-conductance g_m as a function of drain current I_D for the transistor in Figure 27b by varying I_D.

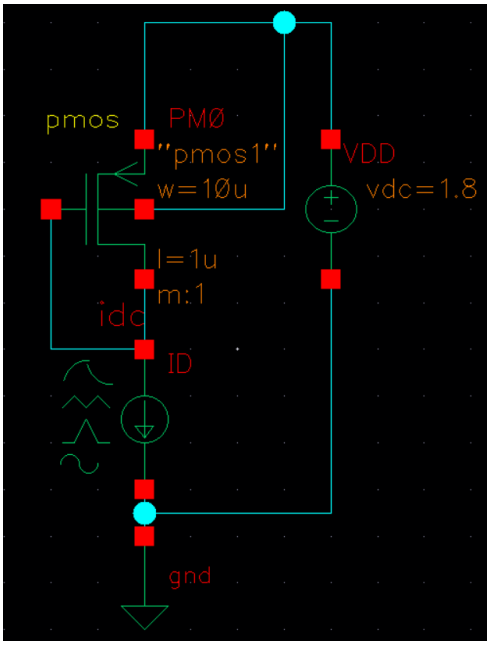

Figure 30: Schematic of the circuit on Cadence Virtuoso for g_m simulation.

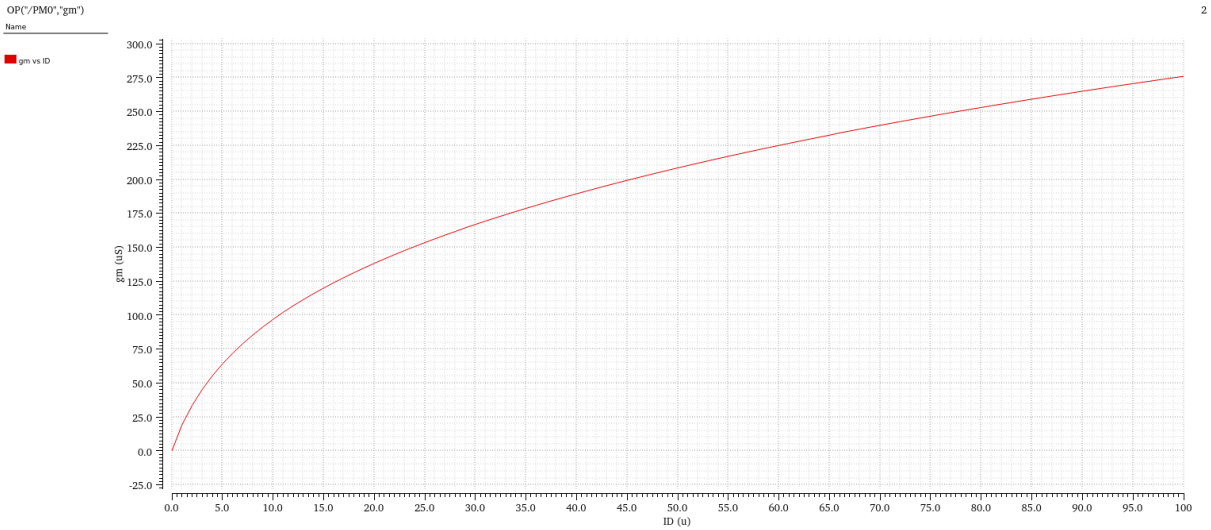

Figure 31: g_m vs I_D

Observations:

For the transconductance g_m plotted against the drain current I_D, the results show that g_m increases with I_D. In strong inversion, the relation follows a square-root dependence ($g_m \propto \sqrt{I_D}$), whereas in the subthreshold region g_m is approximately proportional to I_D with $g_m \approx I_D/(nV_T)$. The chosen aspect ratio of $W/L = 10$ enhances the transconductance for a given value of drain current.

3. Plotting I_D vs V_{SD} and explaining why this circuit is called a diode-connected PMOS transistor.

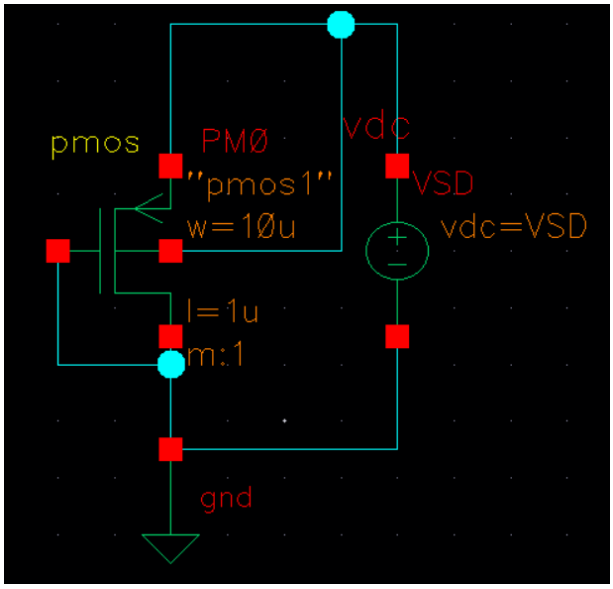

Figure 32: Schematic of the circuit on Cadence Virtuoso diode-connected PMOS transistor

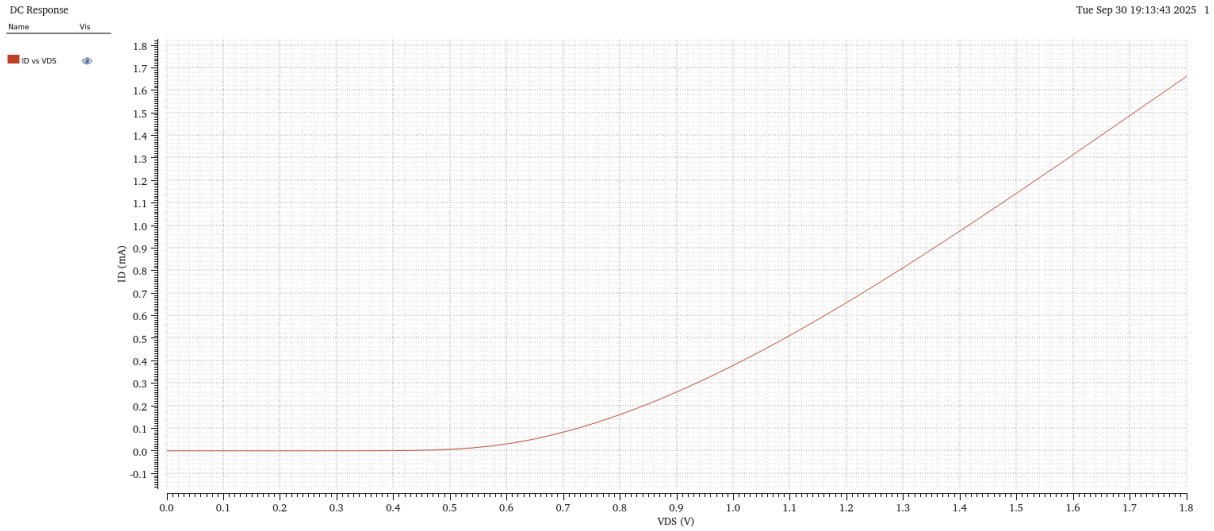

Figure 33: I_D vs V_{SD} for diode-connected PMOS transistor

Observations:

For the diode-connected PMOS, the I_D–V_{SD} curve shows negligible current when V_{SD} is below the threshold voltage. Around $V_{SD} \approx |V_{th}|$ the current rises sharply, resembling the turn-on behavior of a diode. For voltages greater than the threshold, the transistor conducts strongly and the current follows the MOS conduction relation. With the gate and drain shorted together, the device behaves as a two-terminal element with diode-like characteristics, which is why it is called a diode-connected PMOS.

4 CMOS Inverter Simulation

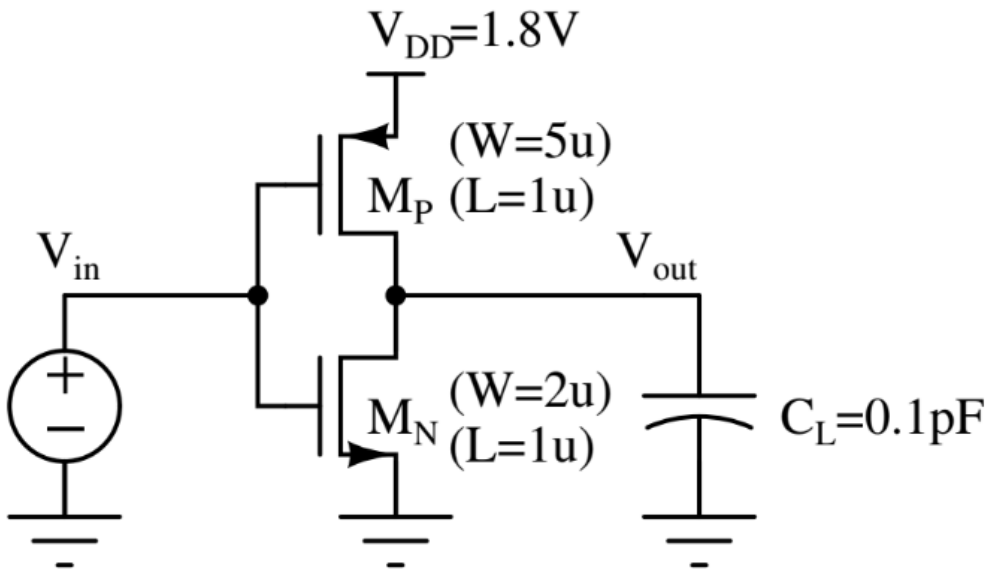

Figure 34: CMOS inverter

1. Simulating the CMOS inverter shown in Figure 34. Performing a DC Sweep of V_{in} from 0 to 1.8 V with a step size of 0.01 and plotting the voltage transfer characteristics of the CMOS inverter.

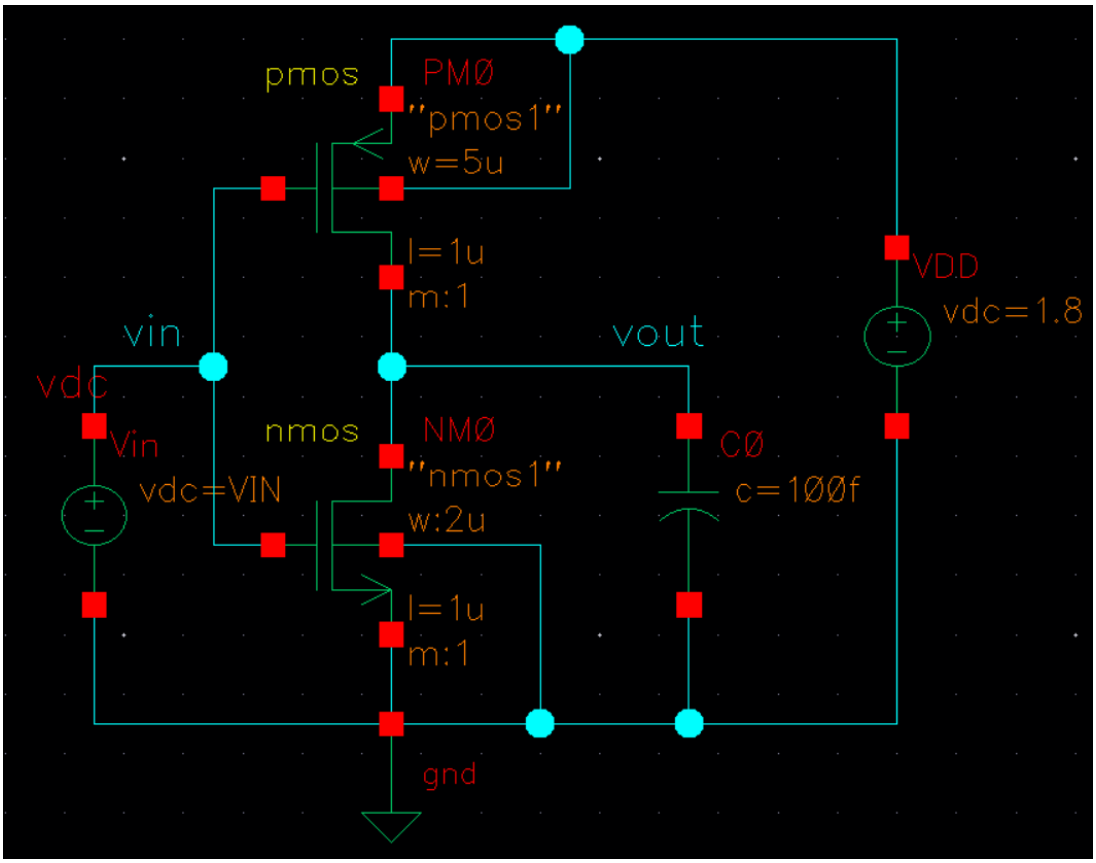

Figure 35: CMOS inverter schematic on Cadence Virtuoso

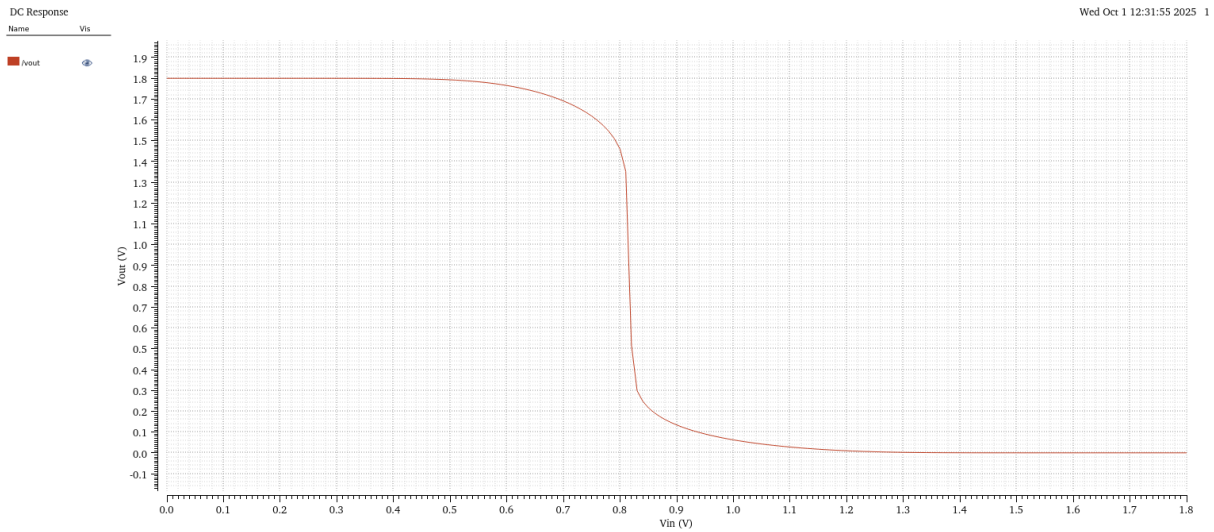

Figure 36: Voltage transfer characteristics of the CMOS inverter (V_{out} vs V_{in})

Observations:

For the DC sweep (voltage transfer characteristic) of the CMOS inverter with V_{in} swept from 0 to 1.8 V in 0.01 V steps, the output V_{out} remains near $V_{DD} = 1.8\,\text{V}$ for low V_{in}, then drops sharply in the transition region around the inverter switching threshold, and finally settles near 0 V for $V_{in} = 1.8\,\text{V}$. The transition region is steep, and the switching threshold is close to the point where $V_{out} = V_{in}$; its exact location depends on device sizing and models. A small finite slope in the high and low regions may be observed due to leakage and channel length modulation in the transistors. Plotting V_{out} versus V_{in} yields the S-shaped characteristic, with a nearly flat high region, a steep fall region, and a nearly flat low region.

2. Performing a transient simulation of the inverter by applying a square-wave input. Plotting both the input and output waveforms.

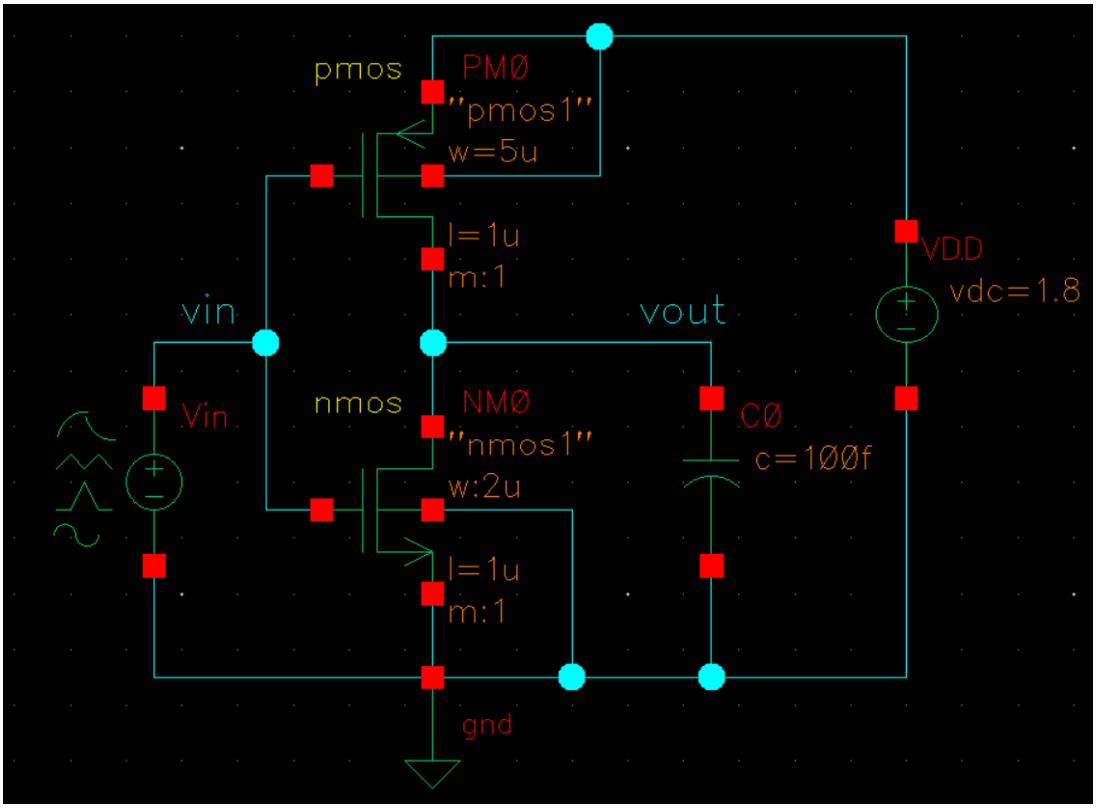

Figure 37: CMOS inverter schematic on Cadence Virtuoso with square wave input

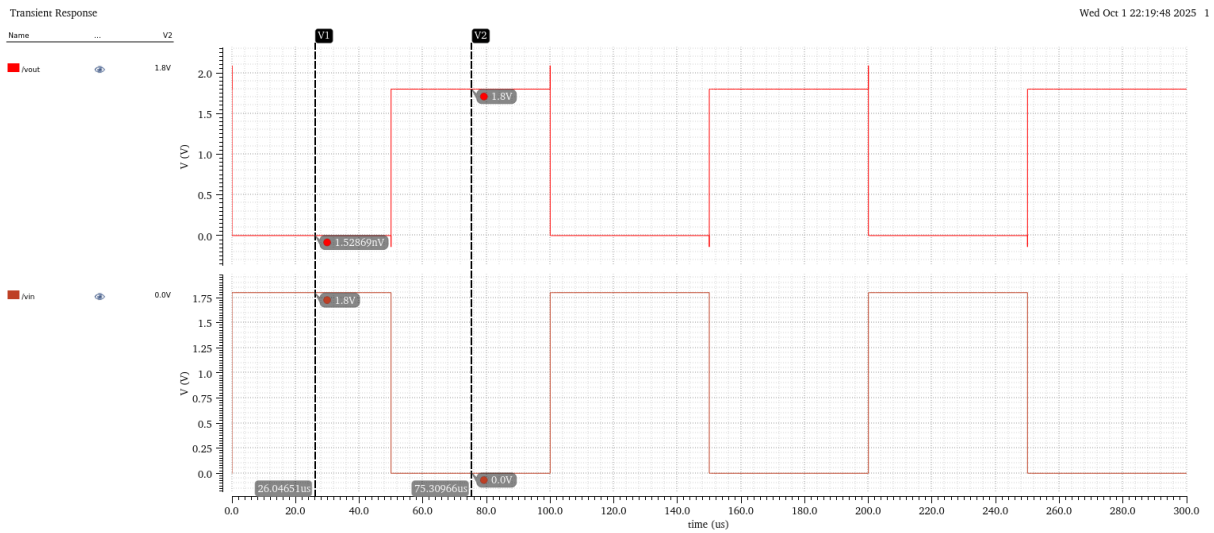

Figure 38: Transient simulation of both V_{in} and V_{out}

Observations:

For the transient simulation with a 10 kHz square-wave input (0 to 1.8 V, period 100 μs) run for 300 μs, the output is the inverted square wave with finite propagation delay and nonzero rise and fall times. Each input rising edge produces a delayed falling edge at the output, and each input falling edge produces a delayed rising edge at the output. The output amplitude swings between approximately 0 and 1.8 V, but the edges are rounded by the transistor switching dynamics and load capacitance. Depending on device sizes and load, small overshoot or ringing may appear at transitions and a short period of shoot-through current can occur during switching; overall the waveform shows clear inversion with measurable propagation delay and finite transition times.