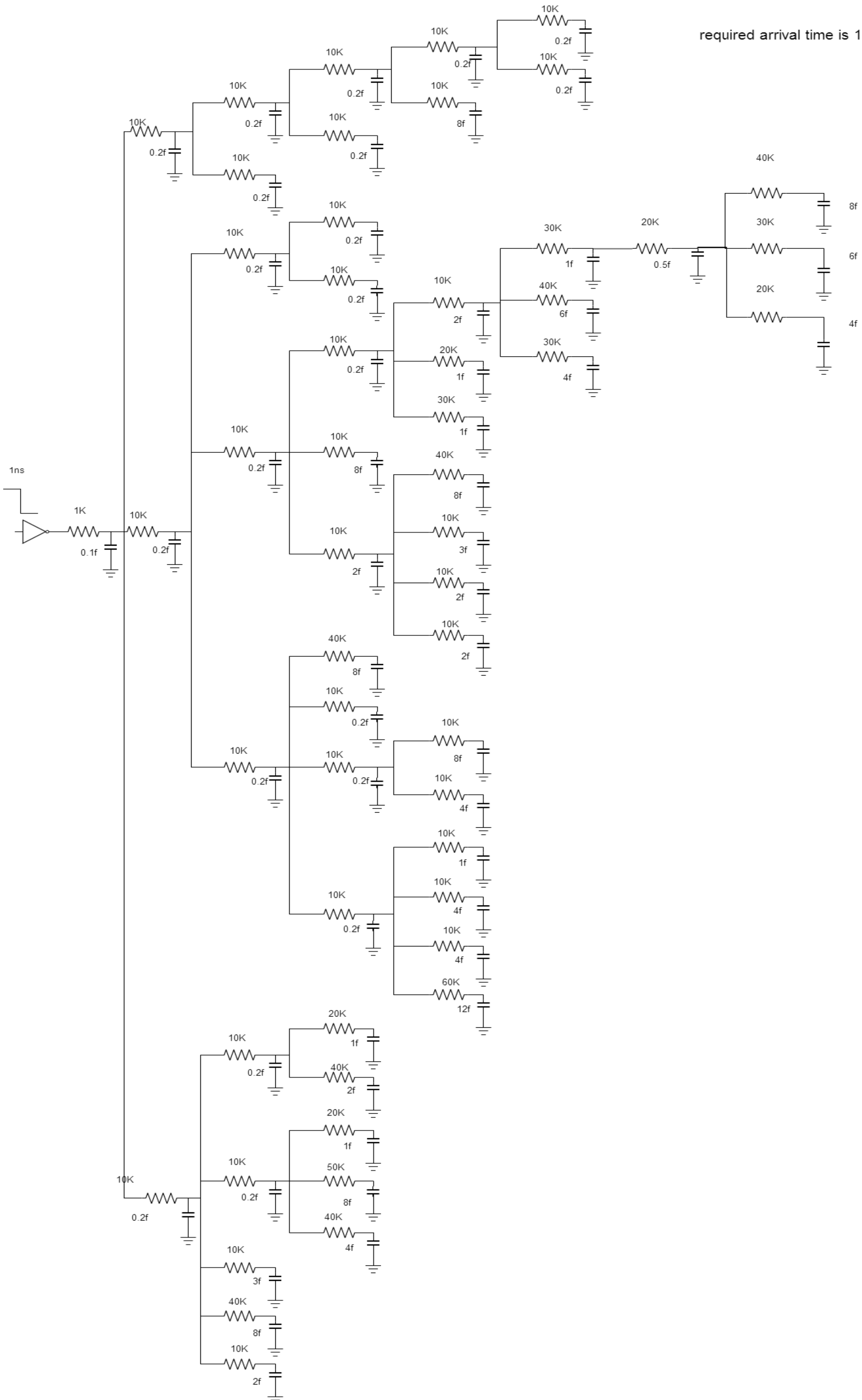
required arrival time is 1.9 ns



VLSI Timing: Assignment #2 Due: 11:00AM Tuesday (March 5, 2019)

You need to submit both hardcopy and electronic copy.

The input signal is a unit step, the voltage switches from “1” to “0” at 1ns. The required arrival time for all primary output load is 1.9n. You will need to insert buffers to achieve this.

In this assignment, we are using 45nm high performance CMOS model.

Here is the link: http://ptm.asu.edu/modelcard/HP/45nm_HP.pm

You need download it and include it in your Hspice netlist file (filename.sp)

Use “.include ./cmos45nm_PTM_HP “ to include your downloaded model;

Here is the buffer definition for this assignment

```
*Buf*
.MACRO  buf16  IN OUT VDD VSS L=45n W=45n
    M0p  N1  IN  VDD VDD  PMOS L=L W='16*W'
    M0n  N1  IN  VSS VSS  NMOS L=L W='16*W'
    M1p  OUT  N1 VDD VDD  PMOS  L=L W='32*W'
    M1n  OUT  N1 VSS VSS  NMOS  L=L W='32*W'
.EOM
```

Use the following command to insert this buffer

“x1 input_node output_node VCC 0 buf16”

X means it’s a circuit block;

VCC is the voltage source node;

0 is the default ground node;

Buf16 is the circuit block name;

As for elmore delay calculation:

R_{inv} = 18k

C_{buf} = 2f

R_{buf} = 0.5k

Dbuf = 20ps