For the circuit described below, perform the following two tasks. (1) Determine all gate sizes to minimize the overall circuit delay. (2) Determine all gate sizes to minimize overall area subject to the constraint that the overall circuit delay has to be less than or equal to (a) 5% (b) 10% (c) 20% above that obtained in (1).

Overall area is defined as the sum of gate sizes. The size of each gate can be 1, 2, 4, or 8. The characteristic of all size-1 gates are given in the table following the circuit netlist. Assume that each primary input is driven by an R_{drive} = 10 kΩ and each primary output is connected to a load C_{load} = 35 pF. It is assumed that the arrival times for all primary inputs are zero. The delay calculation will use Elmore delay model. Assume that the wire capacitance and resistance can be ignored.

For both tasks: You need to use a table to list arrival time at all gate outputs (including primary outputs). Draw the circuit and clearly highlight critical path(s) and write down arrival times at all gate outputs.

10 = NOT(1)
11 = AND(1, 2)
12 = NAND(2, 10)
13 = NOT(11)
14 = AND(3, 13)
15 = NAND(3, 12)
16 = NOT(4)
17 = NOT(14)
18 = AND(4, 17)
19 = NAND(12, 15, 16)
20 = OR(11, 14, 18)
21 = NOT(18)
22 = NAND(5, 21)
23 = NOT(5)
24 = NAND(20, 23)
25 = AND(5, 10, 19)
26 = AND(4, 15)
27 = OR(22, 25,26)
28 = NAND(19, 22, 24)

To solve this lab, we have to first plot the circuits based on the nodes given to us above.

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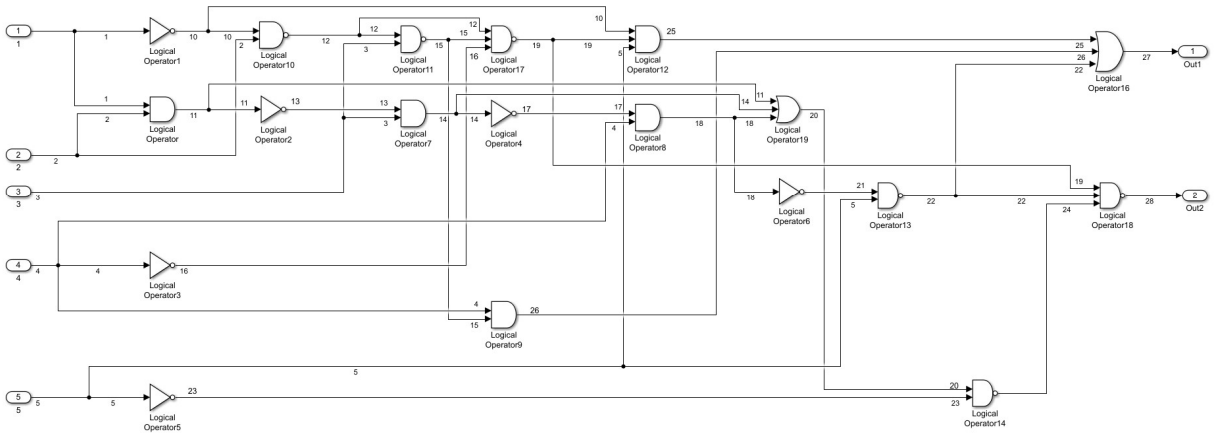
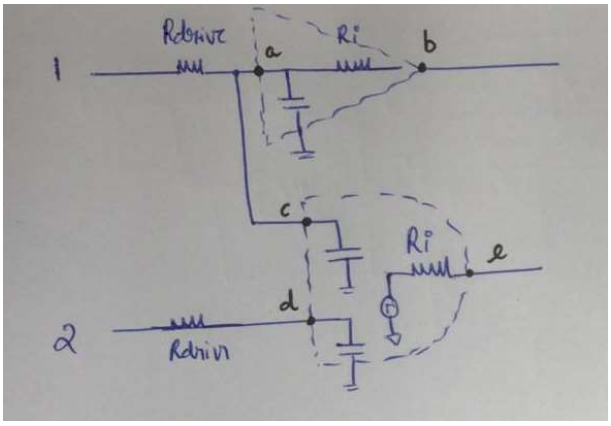
The plot is drawn using MATLAB Simulink as shown below



Now to determine delay at each stage, we must replace each logic gate by its cell resistance and input capacitance. The sample of the approach is shown below



To determine the delay,

$$\text{At A: } t_a = \text{Rdrive} * (C_{inv} + C_{and})$$

$$\text{At C: } t_c = \text{Rdrive} * (C_{inv} + C_{and})$$

$$\text{At D: } t_d = \text{Rdrive} * (C_{and})$$

Now, for the next stages,

$$\text{At B: } t_{next} = t_a + \text{Rinv} * (C_{next})$$

$$\text{At E: } t_{next} = \max(t_c, t_d) + \text{Rinv} * (C_{next})$$

Vinay Manjunath Prabhu
825088894

When we have two or more inputs as shown, we must consider the maximum delay of the two while moving forward. This can be done in excel using the MAX function.

The tabulated values at different nodes are as shown below. (Image of EXCEL sheet used attached in appendix)

Node	Delay (ns)
1	9
2	8.5
3	8.5
4	13
5	15.5
10	16.035
11	13.32516
12	19.6393
13	16.00516
14	20.33032
15	23.063385
16	16.685
17	23.01032
18	27.33548
19	26.693245
20	28.50548
21	30.35048
22	34.855855
23	18.515
24	30.487845
25	29.213245
26	25.586395
27	125.855855
28	145.329855

As we can see in the tabulated column, the output terminals, i.e 27 and 28 have different arrival times / Elmore delay. Using this we can plot the critical path as shown below

Vinay Manjunath Prabhu
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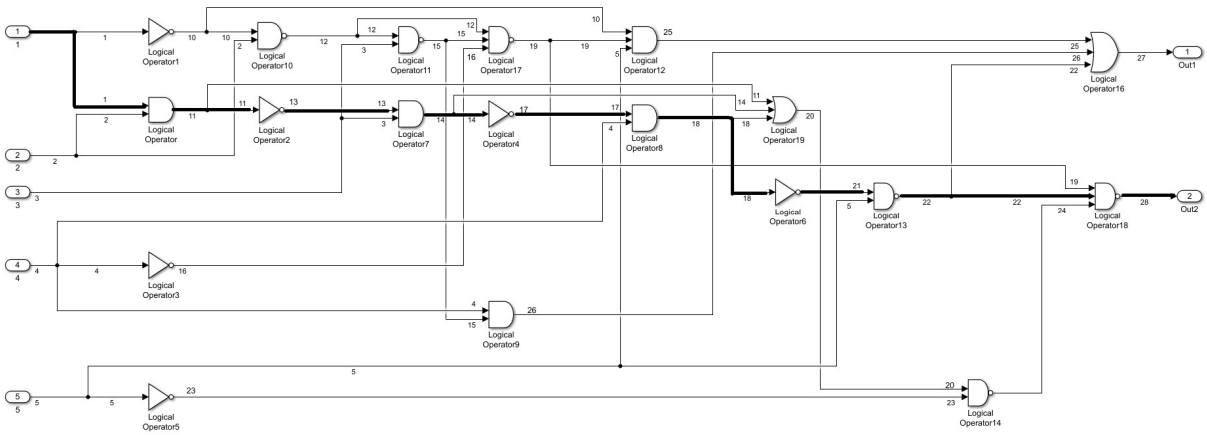

To optimize this design, we need to now choose a sizing (1, 2, 4 or 8 as per requirement) such that the critical path delay is reduced.

After trying several combination of sizing on the gates, the optimal sizing is found as shown below,

Gate	Sizing
NOT	2
NAND3	8
AND	2
AND3	2
NAND	2
OR3	2

Using this sizing the output delays are got down to

Node	Delay(ns)
27	95.30295
28	63.6122

As we can see, of the recognized critical path has gone down to 64.61ns from 145.32ns.

Hence we can conclude that the above sizing is optimal.

Vinay Manjunath Prabhu
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The second part of the lab requires us to reduce the area under three constraints. The delay is allowed 5%, 10%, and 20% above and we have to determine minimum area to achieve this. **The area is also said to be the sum of the sizes gates used.**

i.e Area = sum (num of gates * size)

For the optimal delay obtained, the area is calculated using the excel sheet as shown,

Gate	Total gates	Sizing of 1 * 1 gate area	Total area
NOT	6	2	12
NAND3	2	24	48
AND	4	4	16
AND3	1	6	6
NAND	5	4	20
OR3	2	6	12
		Overall Area	114

Now, let us determine if we can minimize the area under the given constaints.

a. **5%**

Allowed delay = Optimal Delay * 1.05

i.e

Node	Delay(ns)
27	100.068
28	66.7928

The optimal solution is as shown,

Gate	Sizing
NOT	2
NAND3	8
AND	2
AND3	1
NAND	2
OR3	2

The overall area and time is under condition is now shown this is now,

Gate	Total gates	Sizing of 1 * 1 gate area	Total area
NOT	6	2	12
NAND3	2	24	48
AND	4	4	16
AND3	1	3	3
NAND	5	4	20
OR3	2	6	12
		Overall Area	111

Node	Delay(ns)
27	95.303
28	63.6122

b. **10%**

Allowed delay = Optimal Delay * 1.10

i.e

Node	Delay(ns)
27	104.833
28	69.9734

The optimal solution is as shown,

Gate	Sizing
NOT	1
NAND3	8
AND	1
AND3	1
NAND	2
OR3	2

The overall area and time is under condition is now shown this is now,

Gate	Total gates	Sizing of 1 * 1 gate area	Total area
NOT	6	1	6
NAND3	2	24	48
AND	4	2	8
AND3	1	3	3
NAND	5	4	20
OR3	2	6	12
		Overall Area	97

Node	Delay(ns)
27	100.887
28	69.1962

c. **20%**

Allowed delay = Optimal Delay * 1.20

i.e

Node	Delay(ns)
27	114.36
28	76.3346

The optimal solution is as shown,

Gate	Sizing
NOT	1
NAND3	8
AND	1
AND3	1
NAND	1
OR3	2

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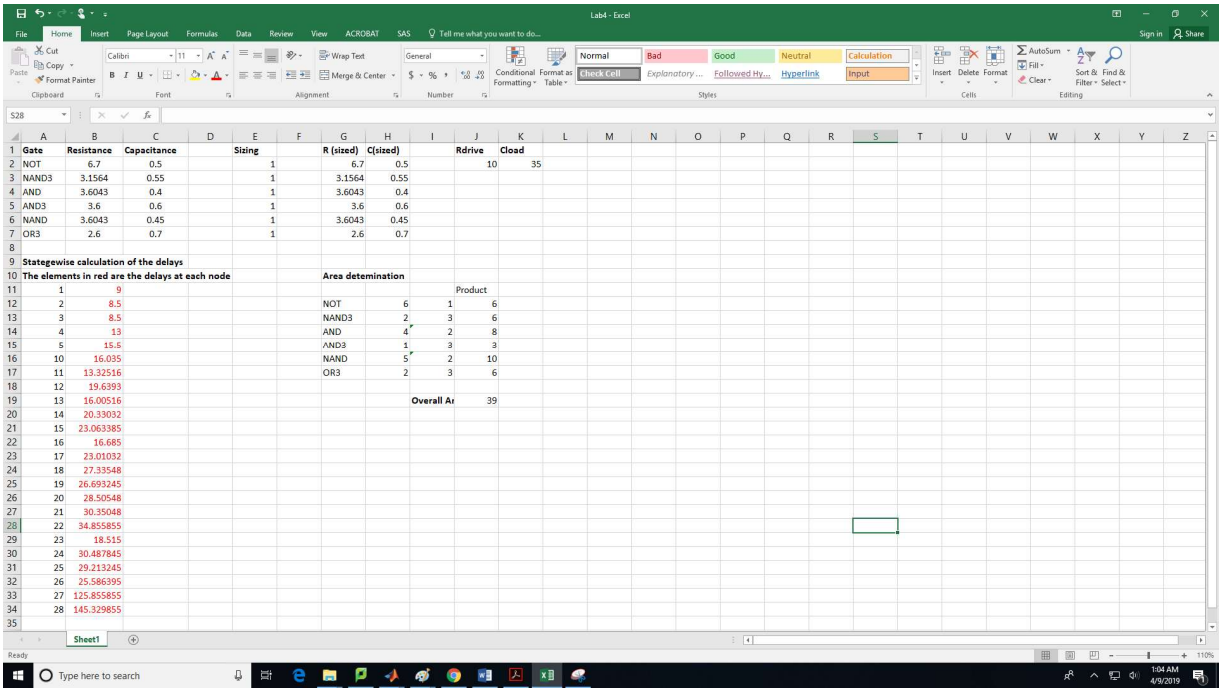
The overall area and time is under condition is now shown this is now,

Gate	**Total gates**	**Sizing of 1 * 1 gate area**	**Total area**
NOT	6	1	6
NAND3	2	24	48
AND	4	2	8
AND3	1	3	3
NAND	5	2	10
OR3	2	6	12
		Overall Area	87

Node	Delay(ns)
27	104.324
28	72.637

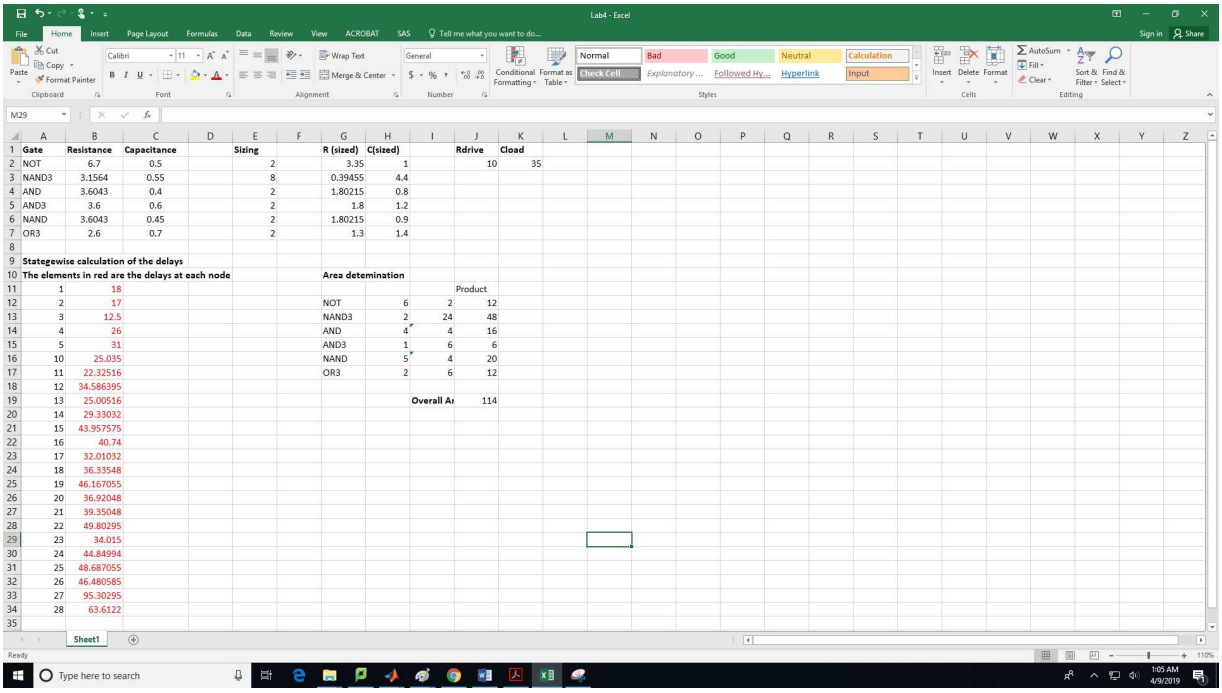
APPENDIX

1. Excel for initial sizing



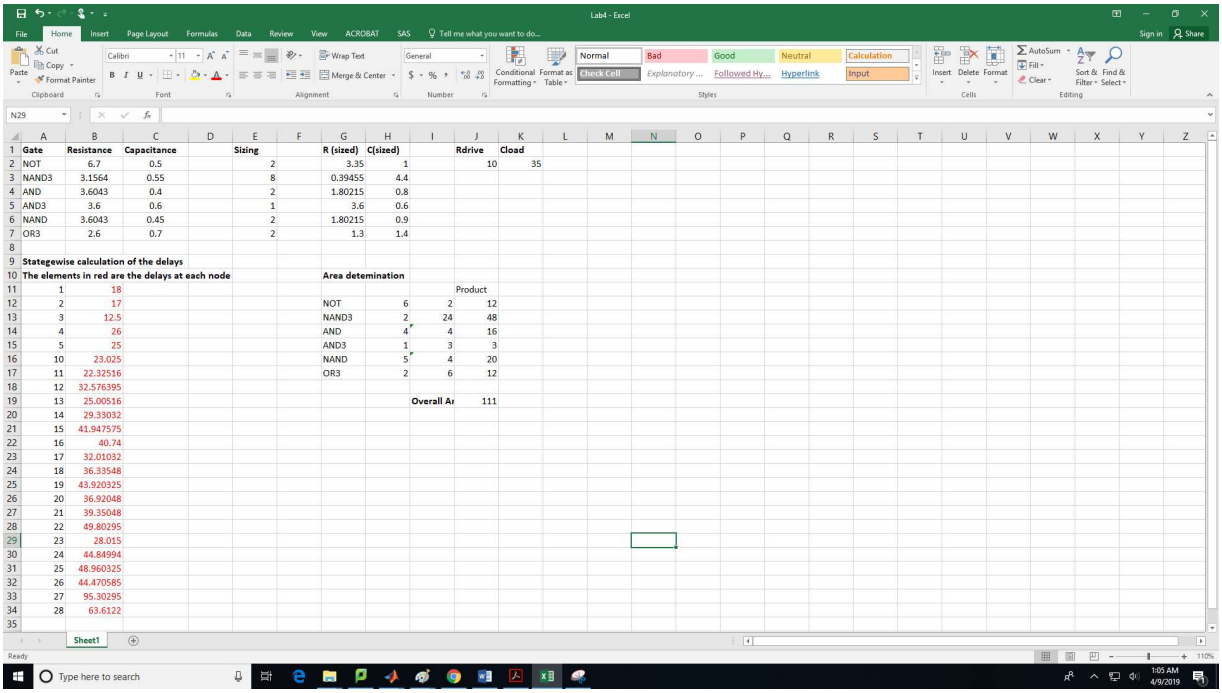
Gate	Resistance	Capacitance		Sizing		R (sized)	C(sized)		Rdrive	Cload
NOT	6.7	0.5		1		6.7	0.5		10	35
NAND3	3.1564	0.55		1		3.1564	0.55			
AND	3.6043	0.4		1		3.6043	0.4			
AND3	3.6	0.6		1		3.6	0.6			
NAND	3.6043	0.45		1		3.6043	0.45			
OR3	2.6	0.7		1		2.6	0.7			
Stategewise calculation of the delays										
The elements in red are the delays at each node						Area detemination				
1	9								Product	
2	8.5					NOT	6	1	6	
3	8.5					NAND3	2	3	6	
4	13					AND	4	2	8	
5	15.5					AND3	1	3	3	
10	16.035					NAND	5	2	10	
11	13.32516					OR3	2	3	6	
12	19.6393									
13	16.00516							Overall Ar	39	
14	20.33032									
15	23.063385									
16	16.685									
17	23.01032									
18	27.33548									
19	26.693245									
20	28.50548									
21	30.35048									
22	34.855855									
23	18.515									
24	30.487845									
25	29.213245									
26	25.586395									
27	125.855855									
28	145.329855									

2. Excel for optimal sizing



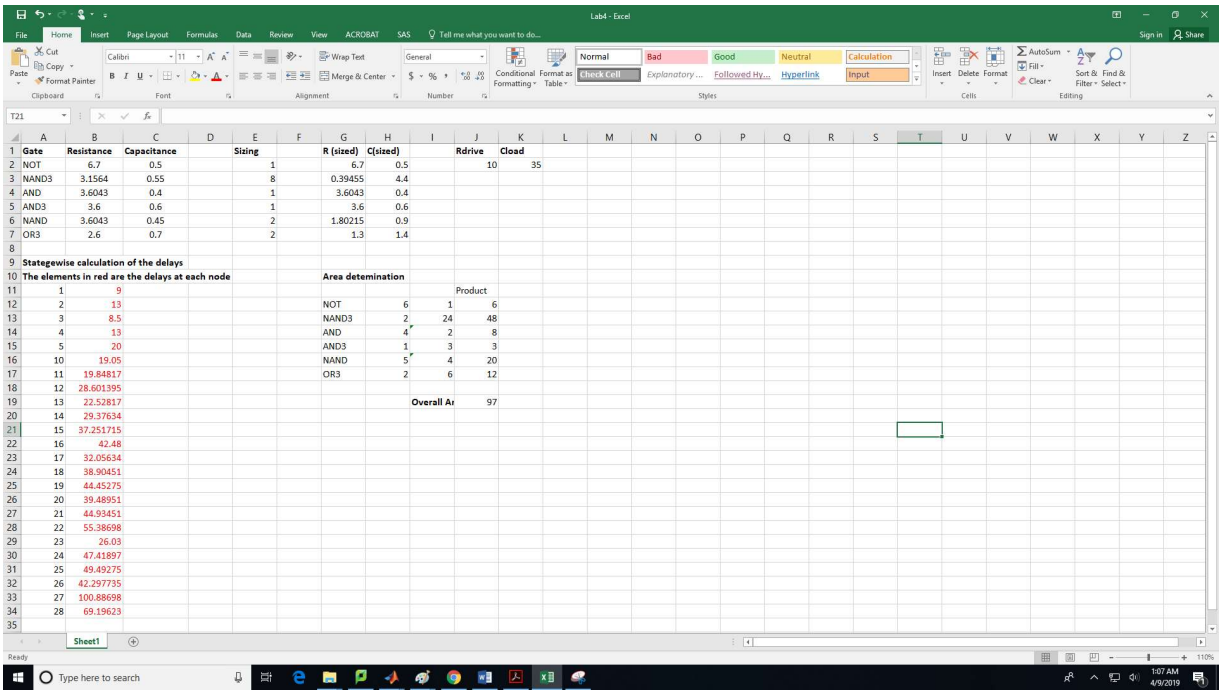
Gate	Resistance	Capacitance		Sizing		R (sized)	C(sized)		Rdrive	Cload
NOT	6.7	0.5		2		3.35	1		10	35
NAND3	3.1564	0.55		8		0.39455	4.4			
AND	3.6043	0.4		2		1.80215	0.8			
AND3	3.6	0.6		2		1.8	1.2			
NAND	3.6043	0.45		2		1.80215	0.9			
OR3	2.6	0.7		2		1.3	1.4			
Stategewise calculation of the delays										
The elements in red are the delays at each node						Area detemination				
1	18								Product	
2	17					NOT	6	2	12	
3	12.5					NAND3	2	24	48	
4	26					AND	4	4	16	
5	31					AND3	1	6	6	
10	25.035					NAND	5	4	20	
11	22.32516					OR3	2	6	12	
12	34.586395									
13	25.00516							Overall Ar	114	
14	29.33032									
15	43.957575									
16	40.74									
17	32.01032									
18	36.33548									
19	46.167055									
20	36.92048									
21	39.35048									
22	49.80295									
23	34.015									
24	44.84994									
25	48.687055									
26	46.480585									
27	95.30295									
28	63.6122									

3. Excel for 5% constraint to minimize area



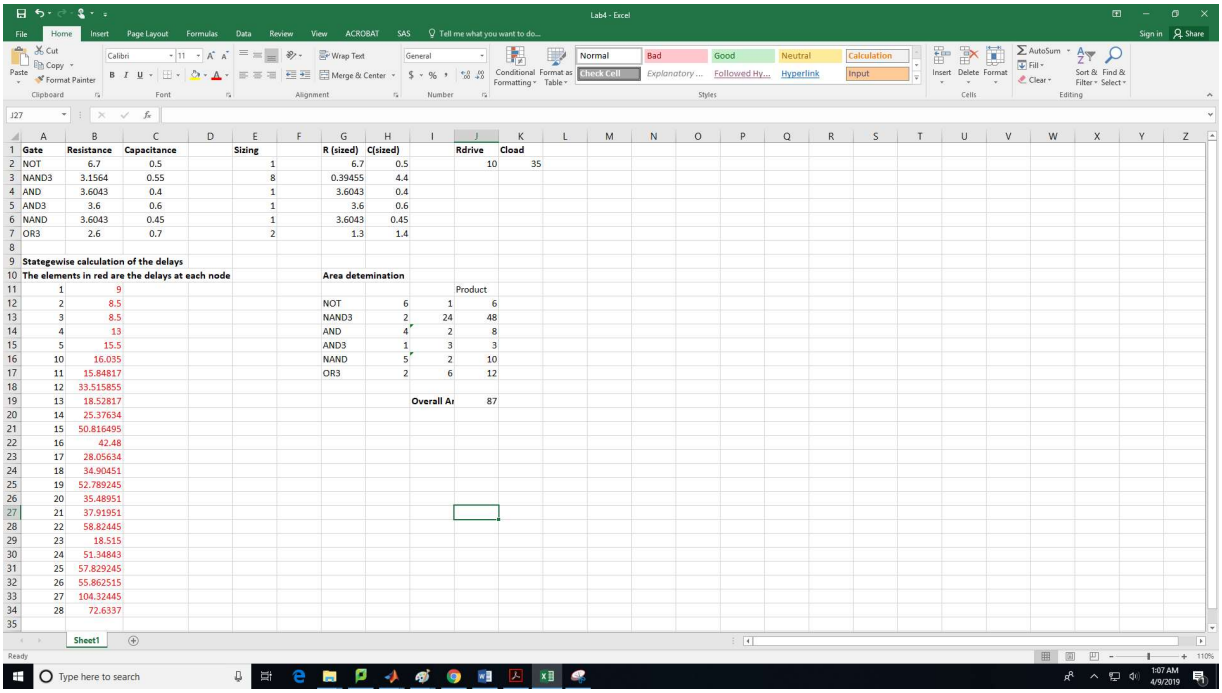
Gate	Resistance	Capacitance		Sizing		R (sized)	C(sized)		Rdrive	Cload
NOT	6.7	0.5		2		3.35	1		10	35
NAND3	3.1564	0.55		8		0.39455	4.4			
AND	3.6043	0.4		2		1.80215	0.8			
AND3	3.6	0.6		1		3.6	0.6			
NAND	3.6043	0.45		2		1.80215	0.9			
OR3	2.6	0.7		2		1.3	1.4			
Stategewise calculation of the delays										
The elements in red are the delays at each node						Area detemination				
1	18								Product	
2	17					NOT	6	2	12	
3	12.5					NAND3	2	24	48	
4	26					AND	4	4	16	
5	25					AND3	1	3	3	
10	23.025					NAND	5	4	20	
11	22.32516					OR3	2	6	12	
12	32.576395									
13	25.00516							Overall Ar	111	
14	29.33032									
15	41.947575									
16	40.74									
17	32.01032									
18	36.33548									
19	43.920325									
20	36.92048									
21	39.35048									
22	49.80295									
23	28.015									
24	44.84994									
25	48.960325									
26	44.470585									
27	95.30295									
28	63.6122									

4. Excel for 10% constraint to minimize area



Gate	Resistance	Capacitance		Sizing		R (sized)	C(sized)		Rdrive	Cload
NOT	6.7	0.5		1		6.7	0.5		10	35
NAND3	3.1564	0.55		8		0.39455	4.4			
AND	3.6043	0.4		1		3.6043	0.4			
AND3	3.6	0.6		1		3.6	0.6			
NAND	3.6043	0.45		2		1.80215	0.9			
OR3	2.6	0.7		2		1.3	1.4			
Stategewise calculation of the delays										
The elements in red are the delays at each node						Area detemination				
1	9								Product	
2	13					NOT	6	1	6	
3	8.5					NAND3	2	24	48	
4	13					AND	4	2	8	
5	20					AND3	1	3	3	
10	19.05					NAND	5	4	20	
11	19.84817					OR3	2	6	12	
12	28.601395									
13	22.52817							Overall Ar	97	
14	29.37634									
15	37.251715									
16	42.48									
17	32.05634									
18	38.90451									
19	44.45275									
20	39.48951									
21	44.93451									
22	55.38698									
23	26.03									
24	47.41897									
25	49.49275									
26	42.297735									
27	100.88698									
28	69.19623									

5. Excel for 20% constraint to minimize area



	A	B	C	D	E	F	G	H	I	J	K
1	**Gate**	**Resistance**	**Capacitance**		**Sizing**		**R (sized)**	**C(sized)**		**Rdrive**	**Cload**
2	NOT	6.7	0.5		1		6.7	0.5		10	35
3	NAND3	3.1564	0.55		8		0.39455	4.4			
4	AND	3.6043	0.4		1		3.6043	0.4			
5	AND3	3.6	0.6		1		3.6	0.6			
6	NAND	3.6043	0.45		1		3.6043	0.45			
7	OR3	2.6	0.7		2		1.3	1.4			
8											
9	**Stategewise calculation of the delays**										
10	**The elements in red are the delays at each node**						**Area detemination**				
11	1	9								Product	
12	2	8.5					NOT	6	1	6	
13	3	8.5					NAND3	2	24	48	
14	4	13					AND	4	2	8	
15	5	15.5					AND3	1	3	3	
16	10	16.035					NAND	5	2	10	
17	11	15.84817					OR3	2	6	12	
18	12	33.515855									
19	13	18.52817							**Overall Ar**	87	
20	14	25.37634									
21	15	50.816495									
22	16	42.48									
23	17	28.05634									
24	18	34.90451									
25	19	52.789245									
26	20	35.48951									
27	21	37.91951									
28	22	58.82445									
29	23	18.515									
30	24	51.34843									
31	25	57.829245									
32	26	55.862515									
33	27	104.32445									
34	28	72.6337									
35											