<u>COMBINED EXPERIMENTS</u>

BECE101P

L13-L14

Name: Vidhi Shah

Reg No: 21BCE1297

Reg. No. 21BCE1297 **Name: Vidhi Shah** **Date of Submission: 02/03/22**

Experiment 1: Study of Electronic Components and Electronic Measurement Devices

<u>Basic Points:</u>

Electronics: Mechanics of electron

There are 4 main type of analyses:
- DC analysis
- DC Operating Point analysis
- Transient analysis
- AC analysis

Ohm's Law: Current is directly proportional to the voltage and constant of proportionality is 1/R under constant temperature and pressure conditions. $\boxed{I = \frac{V}{R}}$

Limitation of KCL:
- Only applied when electric charge in the circuit is constant
- Not applicable for high frequency AC circuits
- Not applicable for non-conservative circuits

Limitation of KVL:
- Only applied when magnetic fields do not change
- Not applicable for high frequency AC circuits
- Not applicable for non-conservative circuits

Passive Devices: (Require no additional power source)

1) Resistor:

- Regulate or set the flow of electrons (current) through them.
- Electrical energy is lost in the form of heat in resistor.
- Resistors can be connected together in series or parallel combinations.
- Resistors are used as voltage droppers, voltage dividers and current limiters in the circuit.

$\boxed{I = \frac{V}{R}}$, Resistance(R) is measured in ohms(Ω).

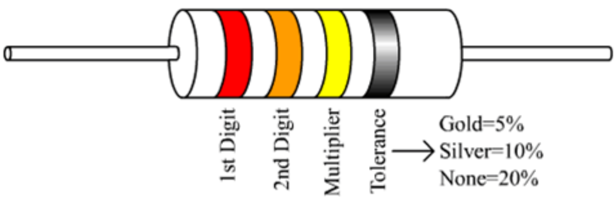
Symbol in circuit: 

Types of resistors:

- Carbon Composition Resistor
- Film or Cermet Resistor
- Wire – wound Resistor
- Semiconductor Resistor

Colour coding:

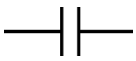
- 4 bands
- 5 bands
- 6 bands



Color	Digit	Multiplier	Tolerance (%)
Black	0	10^0 (1)	
Brown	1	10^1	1
Red	2	10^2	2
Orange	3	10^3	
Yellow	4	10^4	
Green	5	10^5	0.5
Blue	6	10^6	0.25
Violet	7	10^7	0.1
Grey	8	10^8	
White	9	10^9	
Gold		10^{-1}	5
Silver		10^{-2}	10
(none)			20

2) Capacitor:

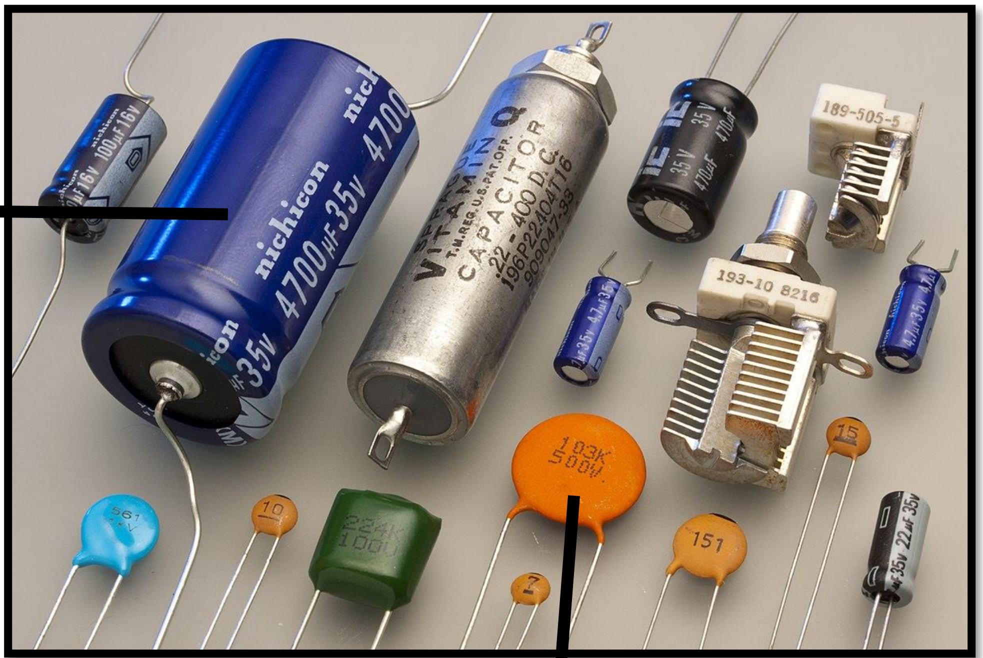
- Stores energy in the form of an electrical charge producing a potential difference across its plates.
- It consists of 2 or more parallel plates which are electrically separated by air or a good insulating material. This insulating layer is called the Dielectric.
- $\boxed{C = \frac{\varepsilon A}{d}}$, Capacitance(C) is measured in Farads(F).

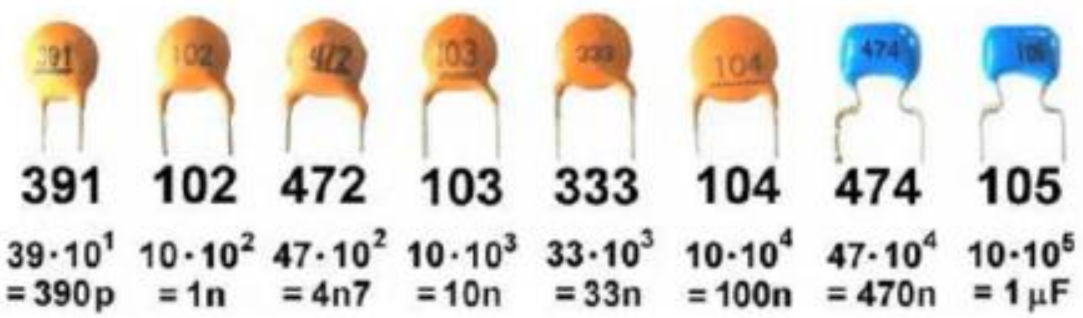
Symbol in circuit: 

Type of capacitors:

- Electrolyte Capacitors
- Ceramic Capacitors

Electrolyte Capacitor





3) Inductor:

- Inductor stores energy in a magnetic field when electric current flows through it.
- It consists of an insulated wire wound into a coil.
- Inductance is ratio of the voltage to the rate of change of current.
- $L = \frac{V}{\frac{I}{t}}$, Inductance (L) is measured in Henry(H) or weber/ampere\

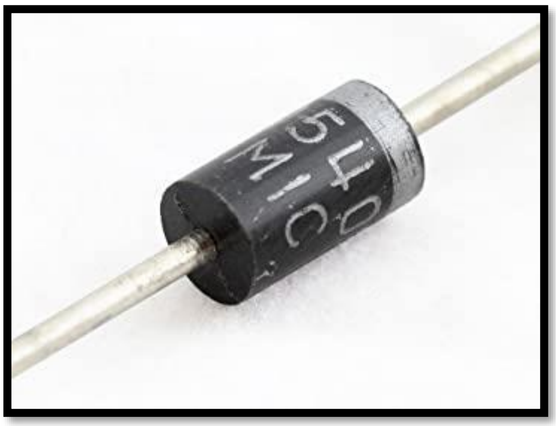
Symbol in circuit: 

Active Devices:

1) Diode:

- Diode allows the flow of current in only one direction.
- Most common type is the *p-n* junction diode. It has two poles: P - black (+ve) and N - white (-ve)

Symbol in circuit: 

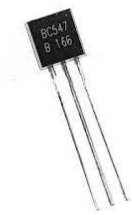


Zener Diode: (Breakdown diode)

- It is a semiconductor device that is designed to operate in the reverse direction.
- Zener Effect: When the voltage across the terminals of a Zener diode is reversed and the potential reaches the Zener Voltage, the junction breaks down and the current flows in the reverse direction.
- There are two types of breakdowns for a Zener Diode:
  - Avalanche Breakdown
  - Zener Breakdown

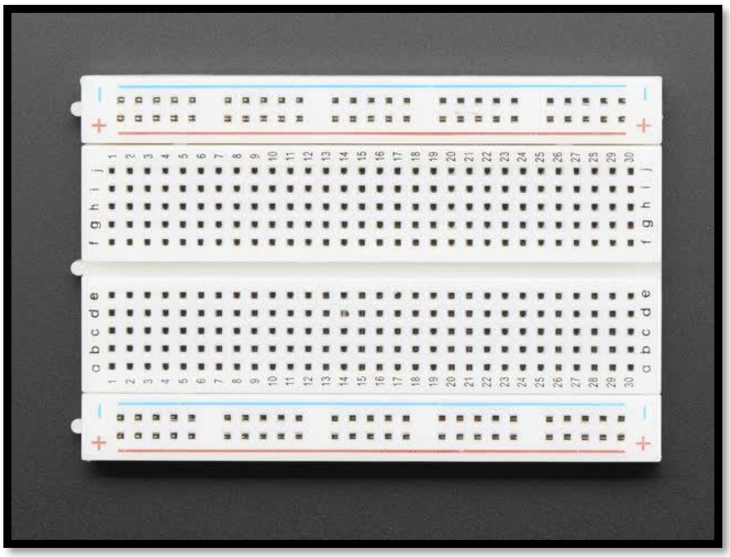
2) Transistor:

- It is a semiconductor device.
- Can be used as an amplifier, switch or an oscillator
- It is 3 terminals 2 port system



Breadboard:

- Breadboard used to connect electrical components.
- They are generally used for testing new circuits.
- The Horizontal holes at the top and bottom are internally horizontally shorted. The holes in the middle are shorted vertically internally.



Decade Boxes:

They utilise a series of internal resistors, capacitors, or inductors to replicate specific electrical values in an application.

Decade Resistance Box

Decade Capacitance Box (µF)

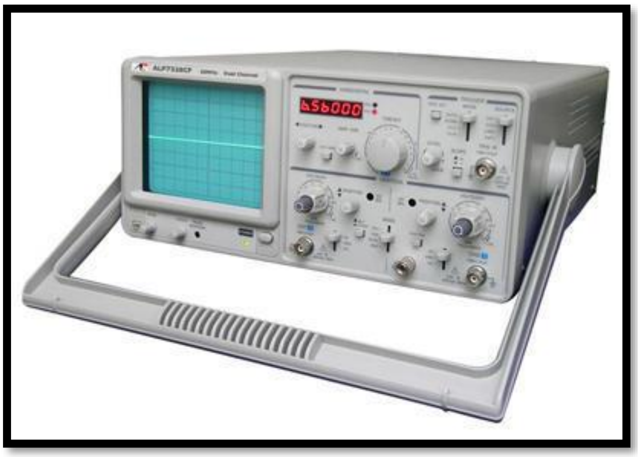
Decade Inductance Box (mH)

Multimeter:

A multimeter is a measuring instrument that can measure multiple electrical properties like Voltage, Resistance, Diode (sound), Capacitance, Frequency, Temp, Gain (hFE), Current (µA, mA, A)

Cathode Ray Oscilloscope (CRO):

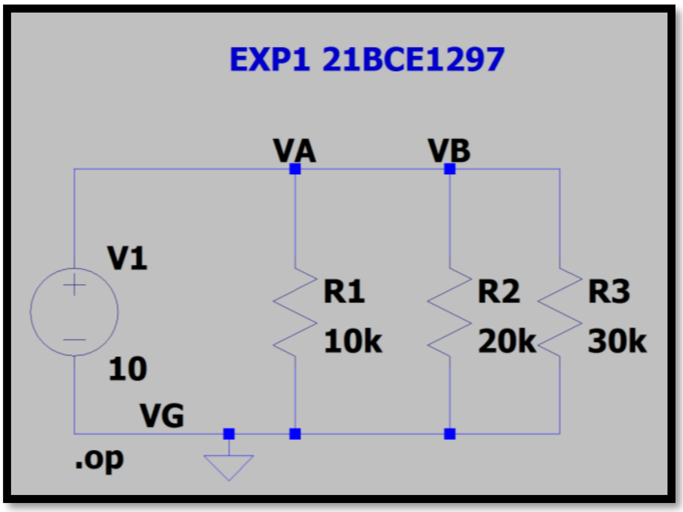
- It is an electronic test instrument
- It is used to obtain waveforms when the different input signals are given.
- By seeing the waveform, we can analyse some properties like amplitude, frequency, rise time, distortion, time interval.
- On adding capacitor to it will show ellipse graph. it is connected to function generator.



Power supply:

- It supplies electric power to an electrical load. The main purpose of a power supply is to convert electric current from a source to voltage, current, and frequency needed to power the load.

LTSpice:



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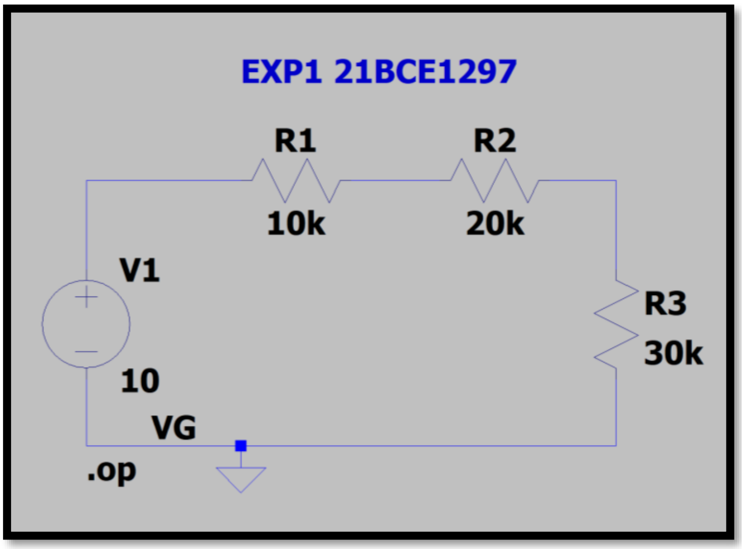
```
       --- Operating Point ---

V(vb):           10              voltage
I(R3):           0.000333333     device_current
I(R2):           0.0005          device_current
I(R1):           0.001           device_current
I(V1):           -0.00183333     device_current
```



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```
       --- Operating Point ---

V(n001):         10              voltage
V(n002):         8.33333         voltage
V(n003):         5               voltage
I(R3):           0.000166667     device_current
I(R2):           -0.000166667    device_current
I(R1):           -0.000166667    device_current
I(V1):           -0.000166667    device_current
```

Reg. No. 21BCE1297   Name: Vidhi Shah   Date of Submission: 11/03/22

Experiment 2

Aim:

- I-V Characteristics of diode and zener diode.
- Transient analysis of diode for AC source.

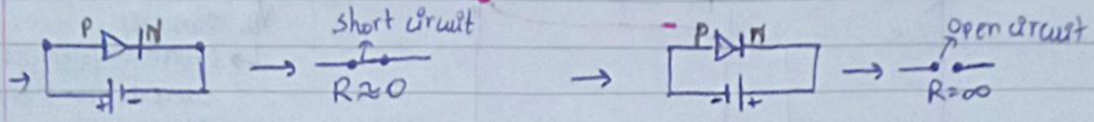
Tools and Apparatus:

- LTSpice
- Diode
- Zener Diode
- Resistor
- AC/DC Source

Theory and Design:

* PN Junction Theory :

- Ability to conduct in one direction.
- Very high resistance in opposite direction.

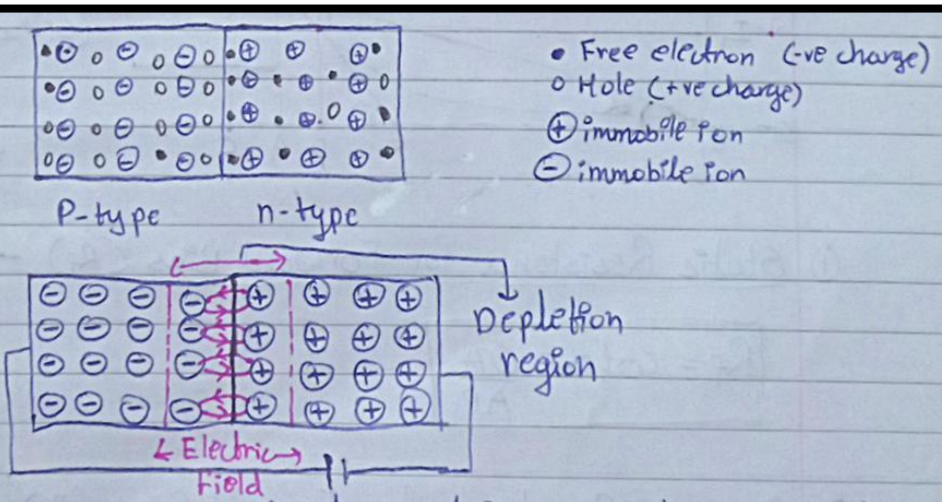


(Forward) bias   (Backward) bias

* PN Junction with no external voltage :

- Even when there is no voltage connected as soon as pn junction is formed :

① Holes from p-region diffuses into N-region
② Electron from N-region diffuses into P-region
③ Movement happens because of thermal energy
④ This phenomenon happens for very short time.

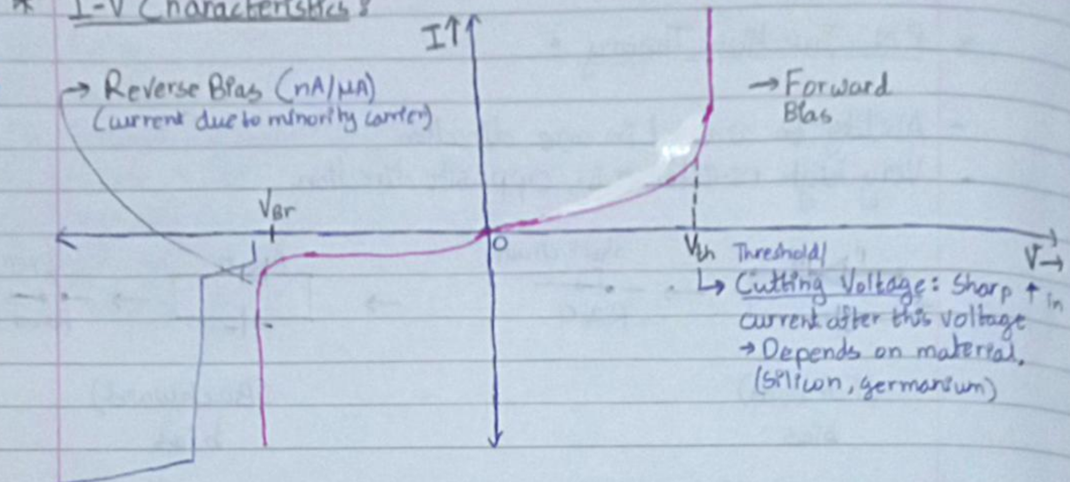


↳ Creates certain Potential barrier → We have to break it to get current flow

0.3 / 0.7

CELEBRO

* I-V Characteristics:

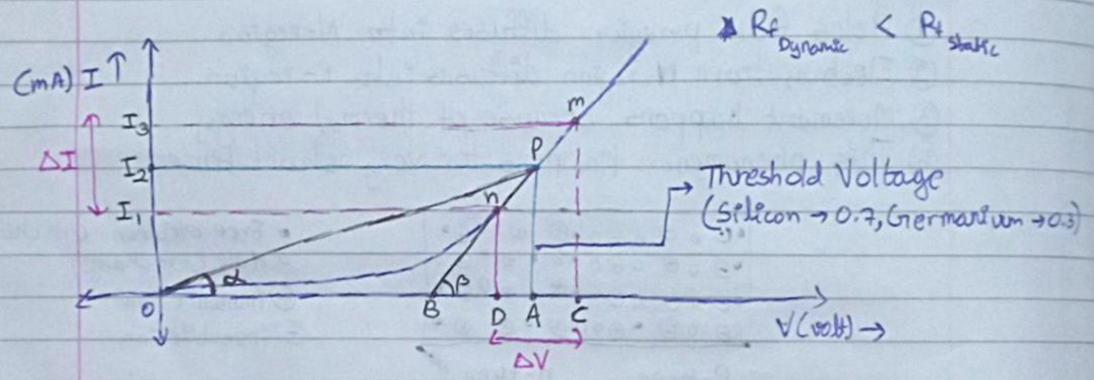


→ V_{BR} → Reverse Breakdown (Sharp ↑ in current)

① Avalanche Breakdown → Due to high potential applied

② Zener Breakdown → Due to increased electric field

* ↳ Zener diode has both but normal diode has only avalanche



① Static Resistance for Forward Bias (R_f) → DC

$$\boxed{R_f = \cot\alpha = \frac{OA}{AP}}$$

② Dynamic Resistance for Forward Bias (R_f) → AC

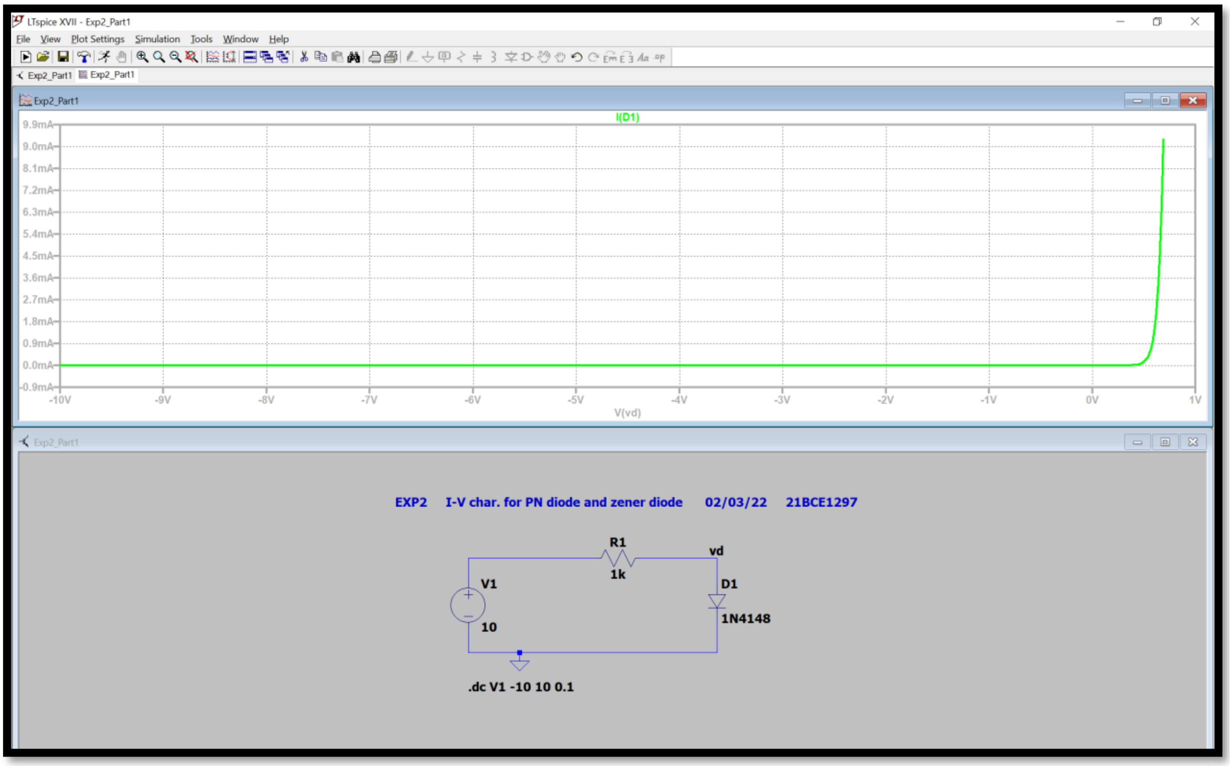
$\Delta V = C - V$

$\Delta I = I_3 - I_1$

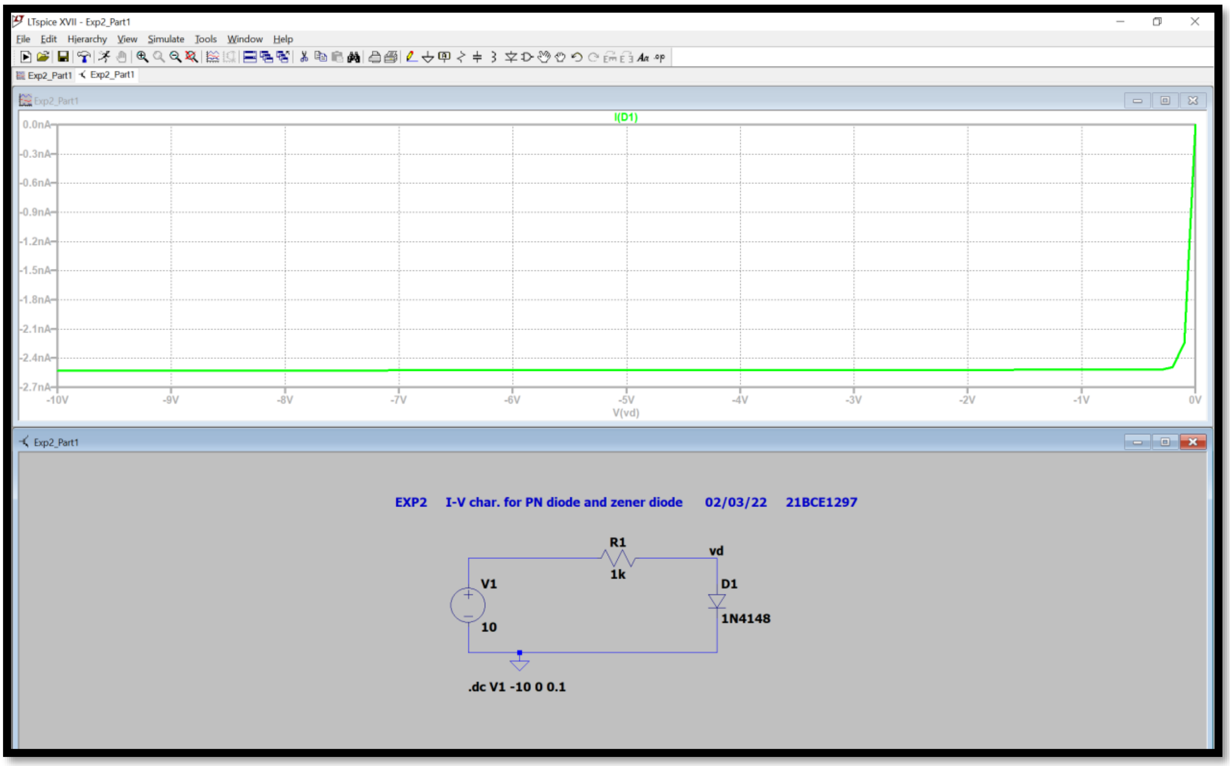
$$R_f = \frac{\Delta V}{\Delta I}$$

Simulation Results:

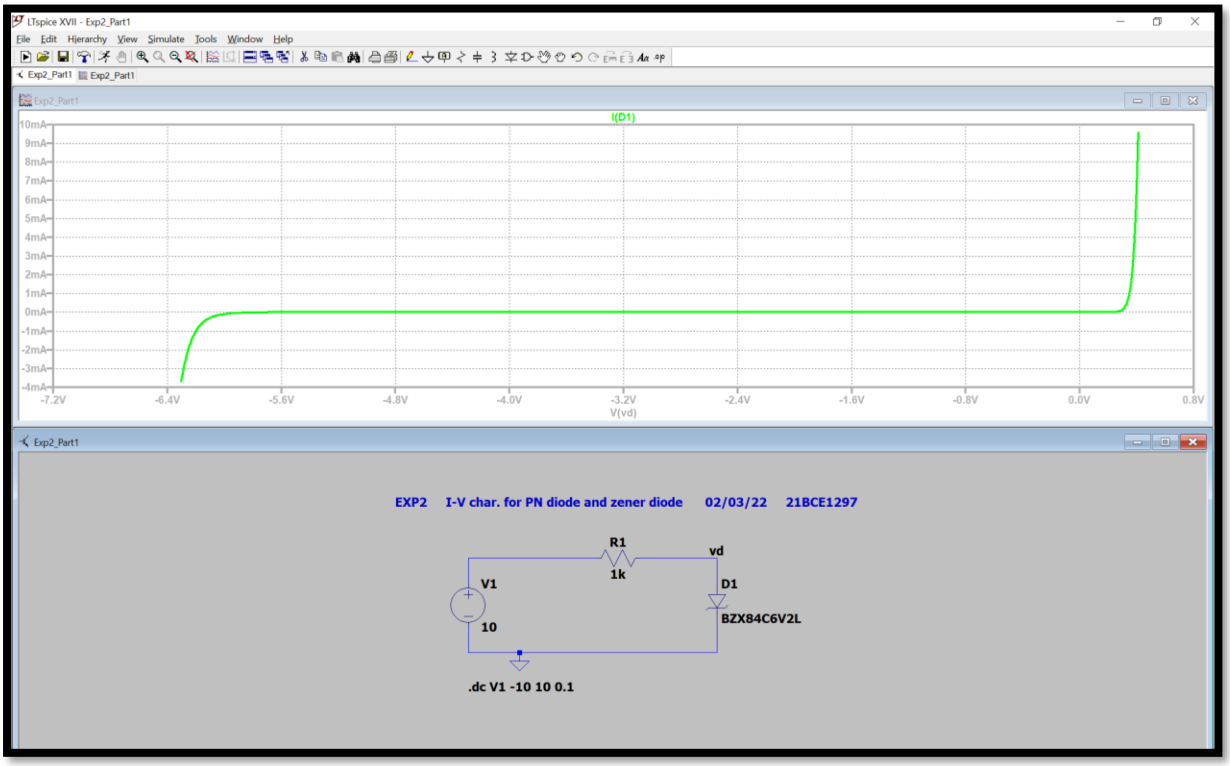
1) Forward Bias



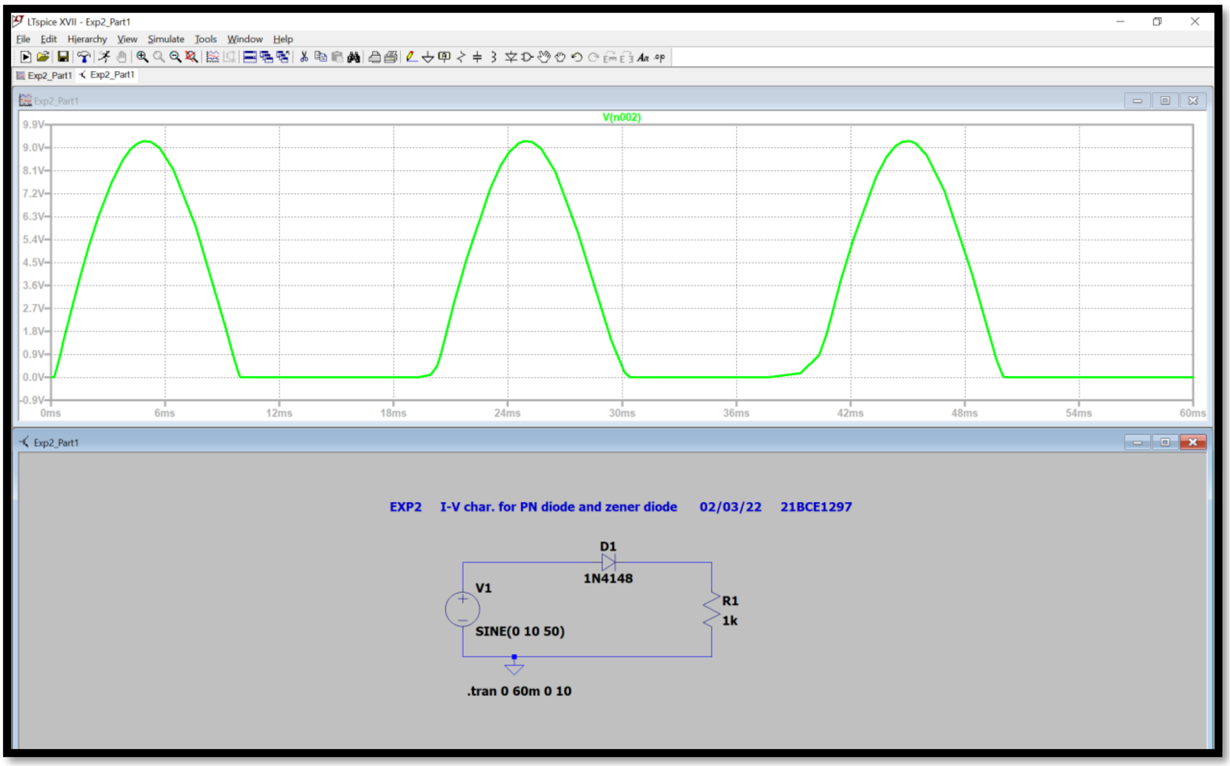
2) Reverse Bias



3) Zener Diode



4) Transient Analysis



Conclusion:

$V = 560\ mv$
$I = 600\ \mu A$

$$\boxed{Static\ Resistance = \frac{560 \times 10^{-3}}{600 \times 10^{-6}} = 933.33\ \Omega}$$

Inferences:

- Threshold voltage and breakdown voltage for zener diode is clearly visible.
- In transient analysis output is (10V - Threshold Voltage). So it is around 9.3V as threshold voltage is around 0.7 V.
- For static resistance calculate ratio by taking values from linear region and NOT exponential region.
- Label vd properly.

Reg. No. 21BCE1297 Name: Vidhi Shah Date of Submission: 15/03/22

Experiment 3

Aim:

Working and simulation of Half Wave Rectifier and Full Wave Rectifier.

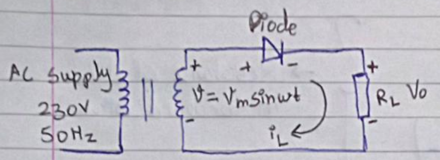
Tools and Apparatus:

LTSpice, Capacitor, Resistor, Diodes, Voltage Source

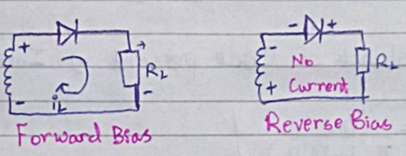
Theory and Design:

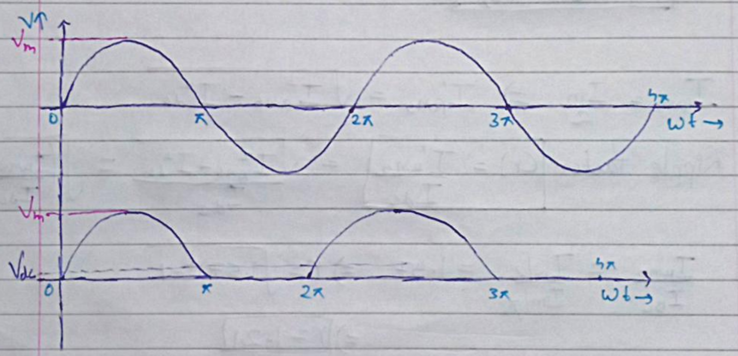
- Half wave rectifier :

$\boxed{AC} \rightarrow$ Transformer (Stepdown) $\rightarrow$ Rectifier $\rightarrow$ filter $\rightarrow$ Regulator $\rightarrow$ $\boxed{DC\ o/p}$



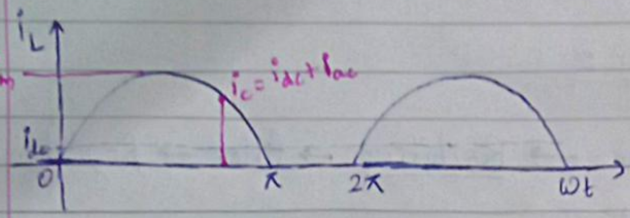
V_m = Maxm Voltage





① Peak Inverse Voltage (PIV) :

- Maximum voltage available in the reverse bias cycle across the diode terminal.
- When the input reaches its peak value (V_m) in the negative half cycle, the voltage across the diode is maximum. This voltage is PIV



Max current

$i_m = \frac{V_m}{R_L}$

$i_L = i_m \sin \omega t$

↳ Total instantaneous Current

② $\boxed{I_{avg} = I_{dc} = \frac{I_m}{\pi}}$

$\boxed{V_{dc} = I_{dc} \times R_L = \frac{I_m}{\pi} R_L}$

→ Resistance of diode in forward bias

If resistance of diode present $\Rightarrow I_m = \frac{V_m}{R_L + r_d}$

$\Rightarrow \boxed{V_{dc} = \frac{V_m}{\pi(1 + r_d/R_L)}}$

③ $I_{RMS} = \frac{I_m}{2} \Rightarrow I'_{RMS} = \sqrt{I^2_{RMS} - I^2_{dc}}$

Ripple factor $\boxed{(r) = \frac{I'_{RMS}}{I_{dc}}} = \frac{\sqrt{I^2_{RMS} - I^2_{dc}}}{I_{dc}} = \sqrt{\left(\frac{I_{RMS}}{I_{dc}}\right)^2 - 1}$

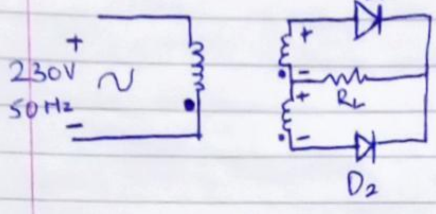
$\frac{I_{RMS}}{I_{DC}} = \frac{I_m/2}{I_m/\pi} = 1.57 \Rightarrow r = \sqrt{(1.57)^2 - 1}$

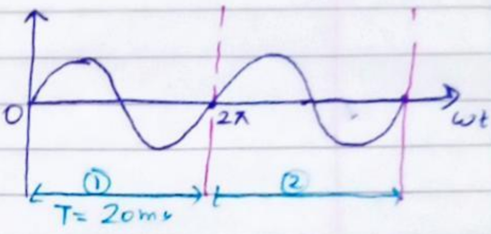
$\Rightarrow \boxed{r = 1.21}$

* The ripple factor for half-wave rectifier is more than 1. Ripple voltage exceeds the DC ~~current~~ Voltage. Therefore, we say half-wave rectifier converts AC to DC.

- ## Full Wave Rectifier:

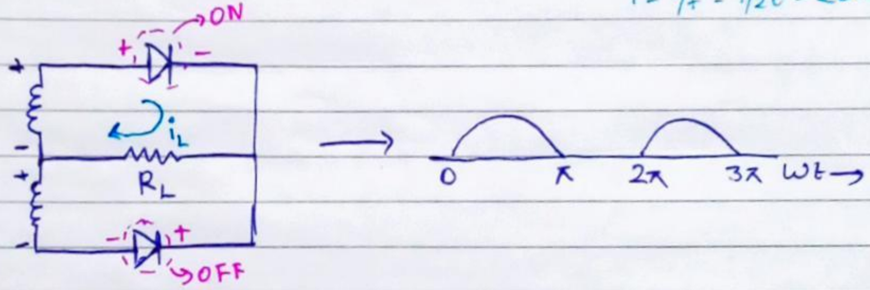
① **Center tapped:**

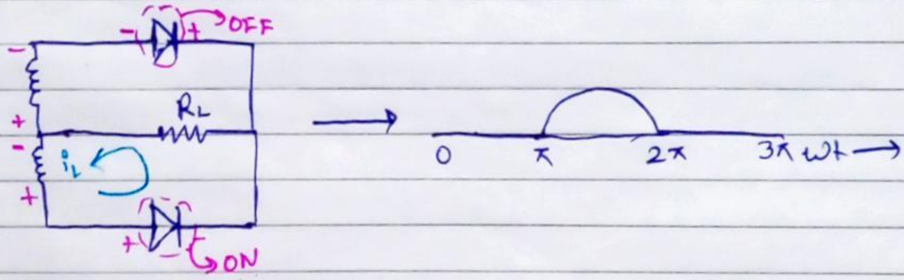


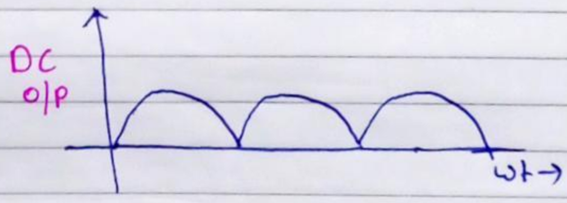


$f = 50Hz$

$T = 1/f = 1/20 = 20ms$

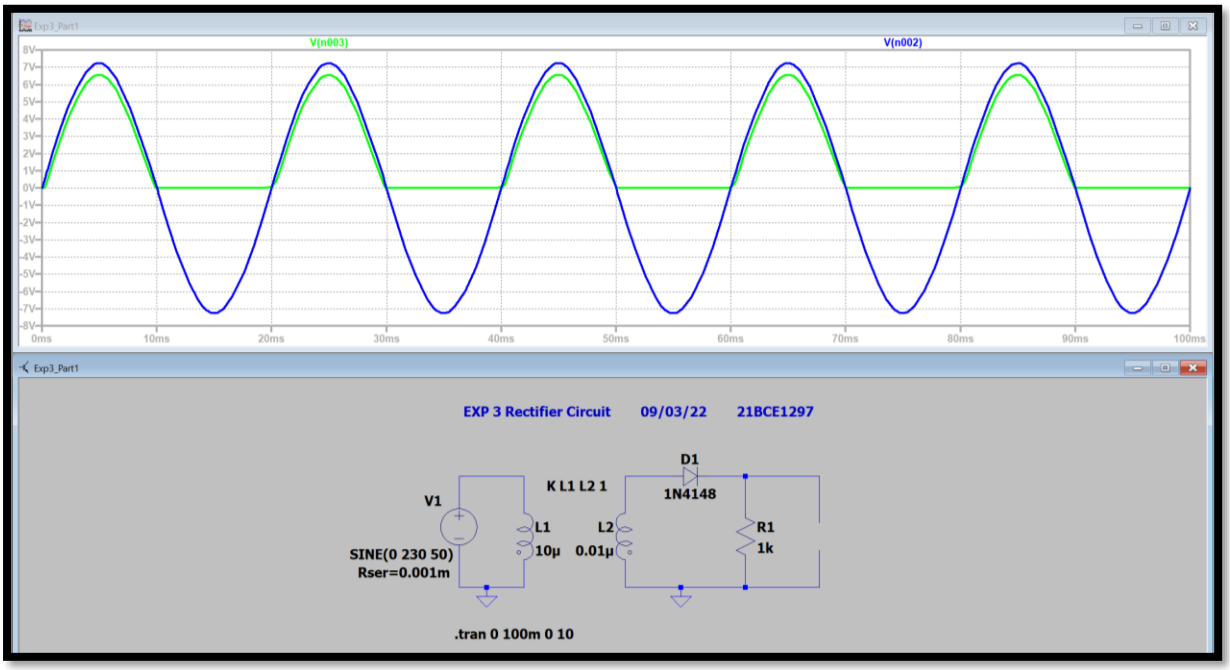






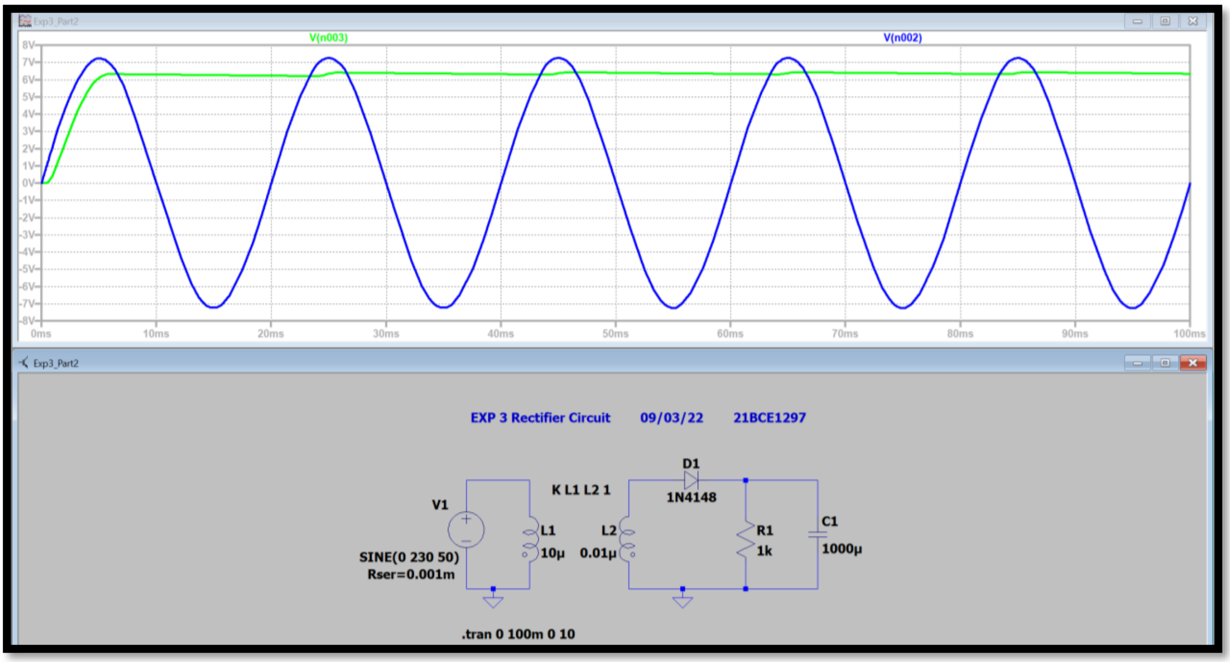
Simulation Results:

1) Half Wave Rectifier without capacitor

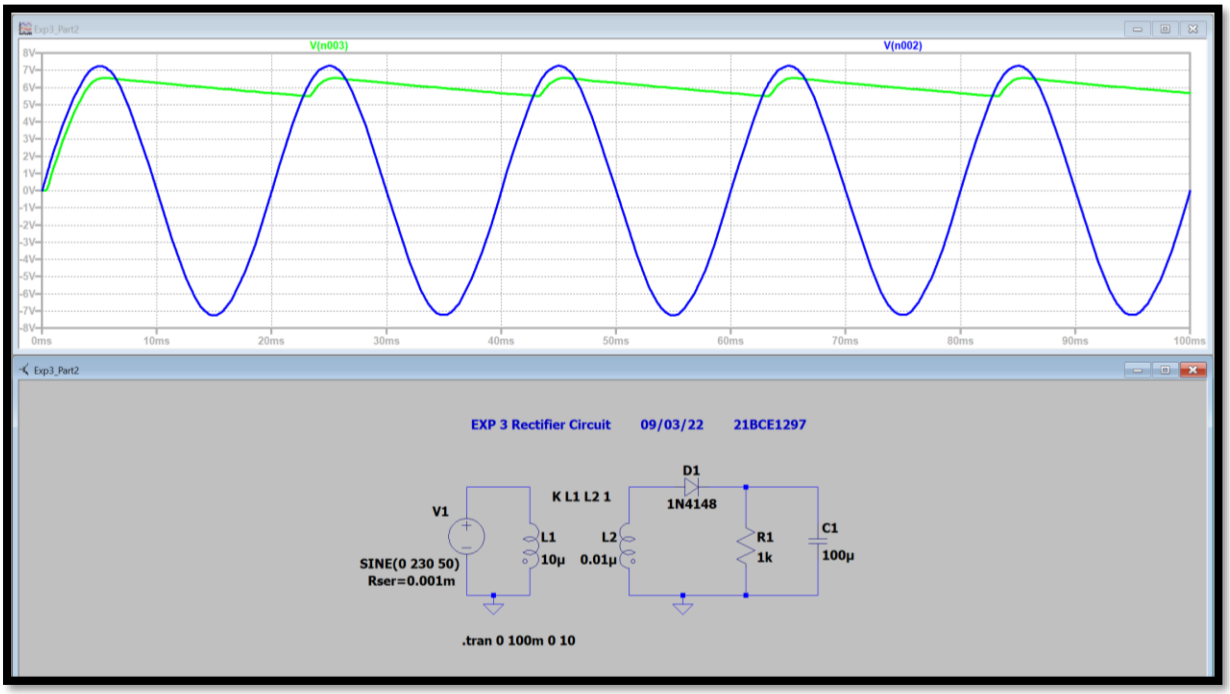


2) Half Wave Rectifier

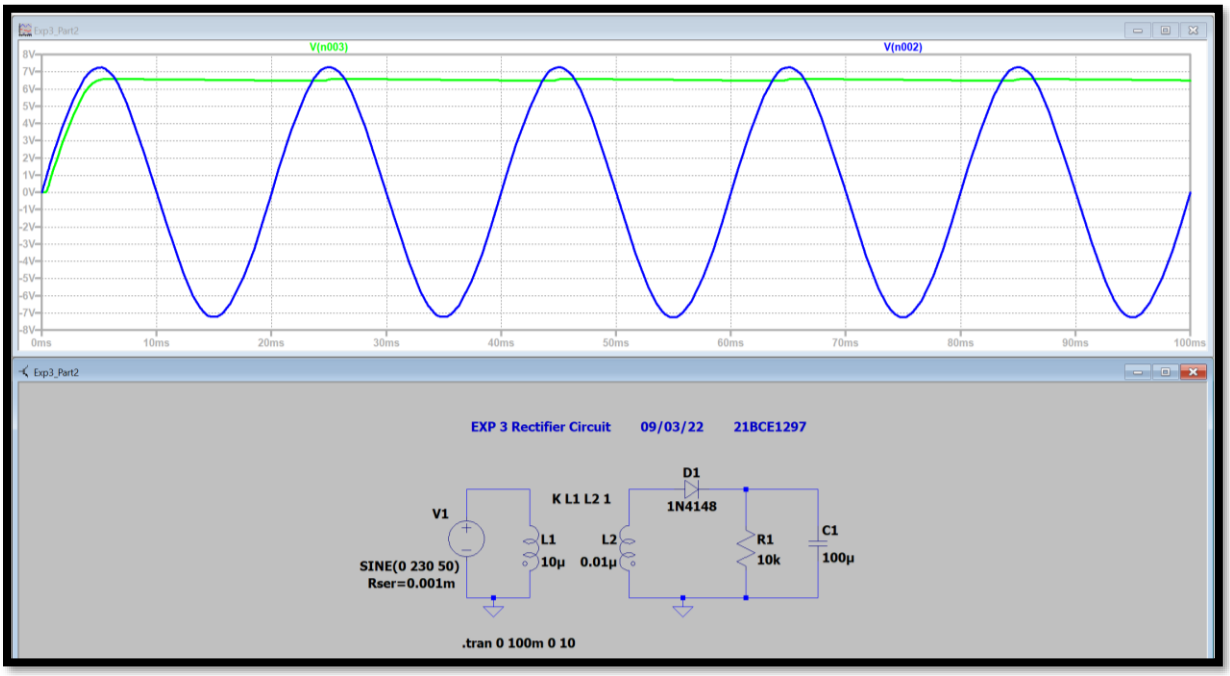
a) R = 1k Ω, C = 1000µ



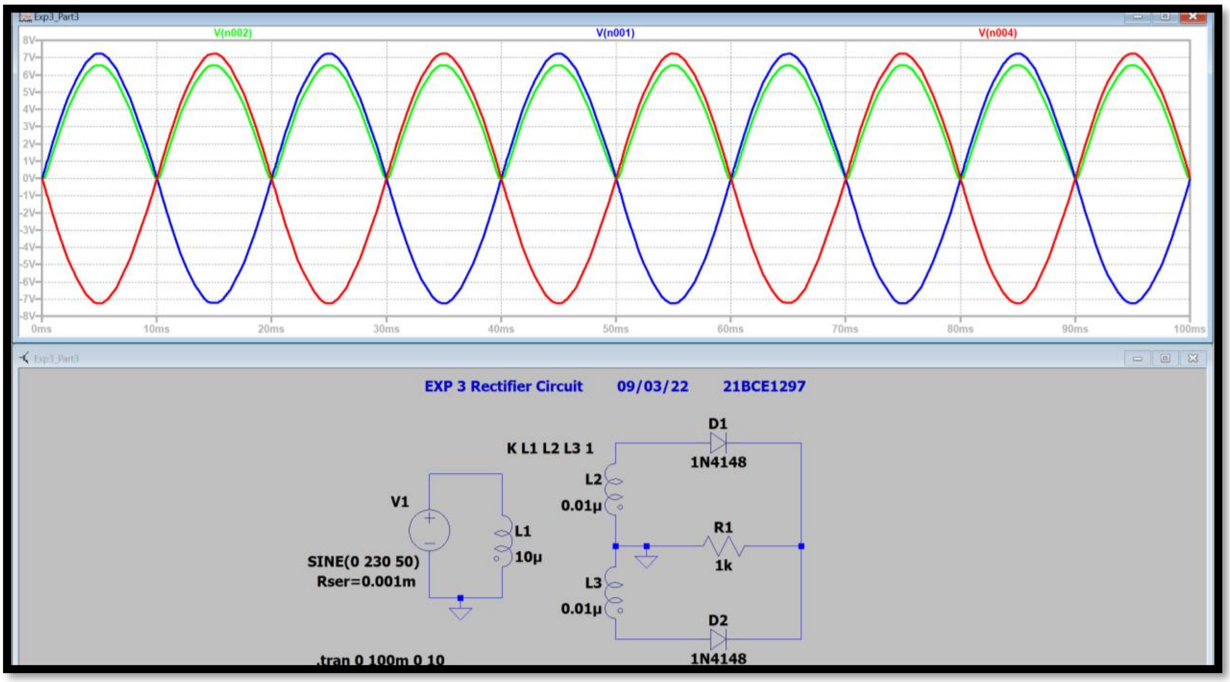
b) R = 1k Ω, C = 100µ



c) R = 10k Ω, C = 100µ



3) Full Wave Center Tapped Rectifier



Conclusion:

1. **Cutting Voltage** for **Half Wave Rectifier** = 7.25 – 6.58 = **0.67 V**
2. **Cutting Voltage** for **Full Wave Rectifier** = 7.23 – 6.55 = **0.68 V**

Inferences:

1. Rectifiers are used to convert AC voltage to DC Voltage
2. Transformers are used for stepping down AC voltage
3. While stimulation connect diode in proper direction
4. Changing R and C values in half wave rectifier affects the DC output wave form
5. Difference between voltages gives cutting voltage which is approximately 0.7 for silicon diodes.

Reg. No. 21BCE1297 Name: Vidhi Shah Date of Submission: 05/04/22

Experiment 4

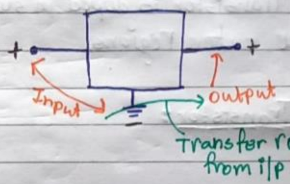
Aim:
Study of input and output characteristics of CE BJT (Common Emitter Bipolar Junction Transistor) amplifier using LTSpice.

Tools and Apparatus:
LTSpice, Transistor, Resistors, Voltage Source

Theory and Design:

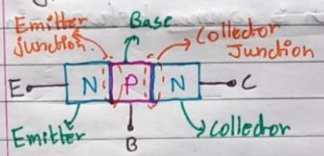
• TRANSISTOR: (Transfer + Resistor)

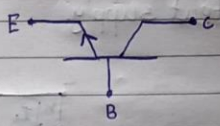
→ Transistor is transfer of resistance from one port to another port.
→ Device having 3 ports and 2 junctions.



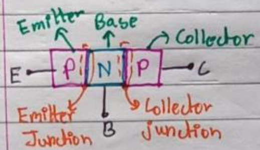
→ Transistor acts as two pn junction diodes attached back-to-back.

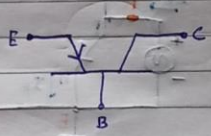
→ Types:

① 



3 ports:
① Collector
② Emitter
③ Base

② 

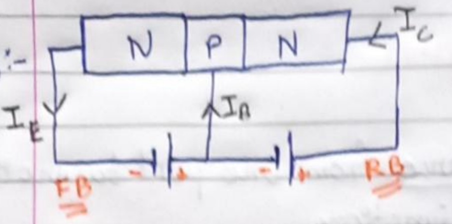


2 junctions:
① Emitter junction
② Collector junction

→ 4 ways to bias: (Region of Operation)

	Emitter Junction	Collector Junction	Region of Operation
1.	FB	RB	Active Region
2.	FB	FB	Saturation Region
3.	RB	RB	Cut off Region
4.	RB	FB	Reverse Active Region

eg:-



→ Active Region

50 to 200

$\boxed{I_E = I_C + I_B}$, $\boxed{I_C = \beta I_B}$, $I_C >> I_B$

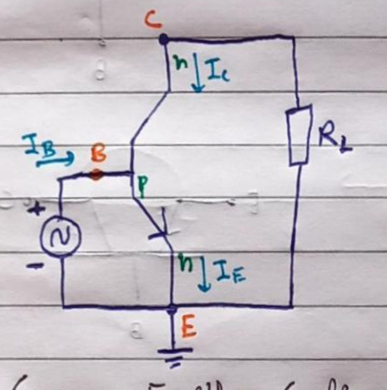
mA μA

* I_B is very small. Transistor is doped in such a way that middle region is thinner than the outer regions.

→ <u>Configuration of Transistor</u> :

① Common Emitter
② Common Collector
③ Common Base

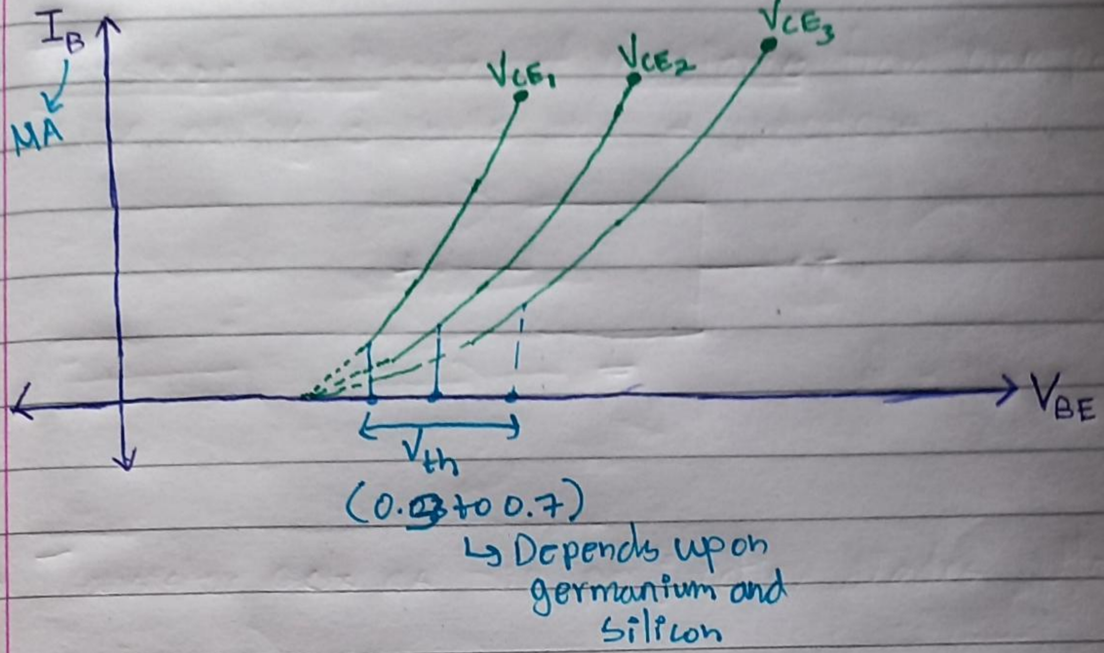
Decided by the terminal which is common between input supply and output supply.



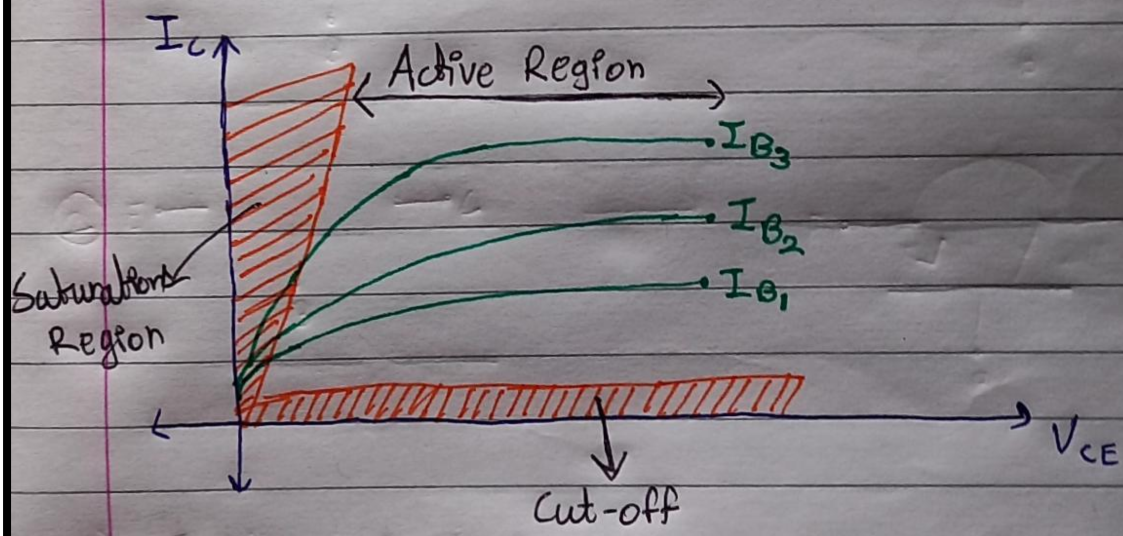
Common Emitter Configuration
(Active Region)

→ Transistor can be used as switch, amplifier and oscillator.

→ Input Characteristics :

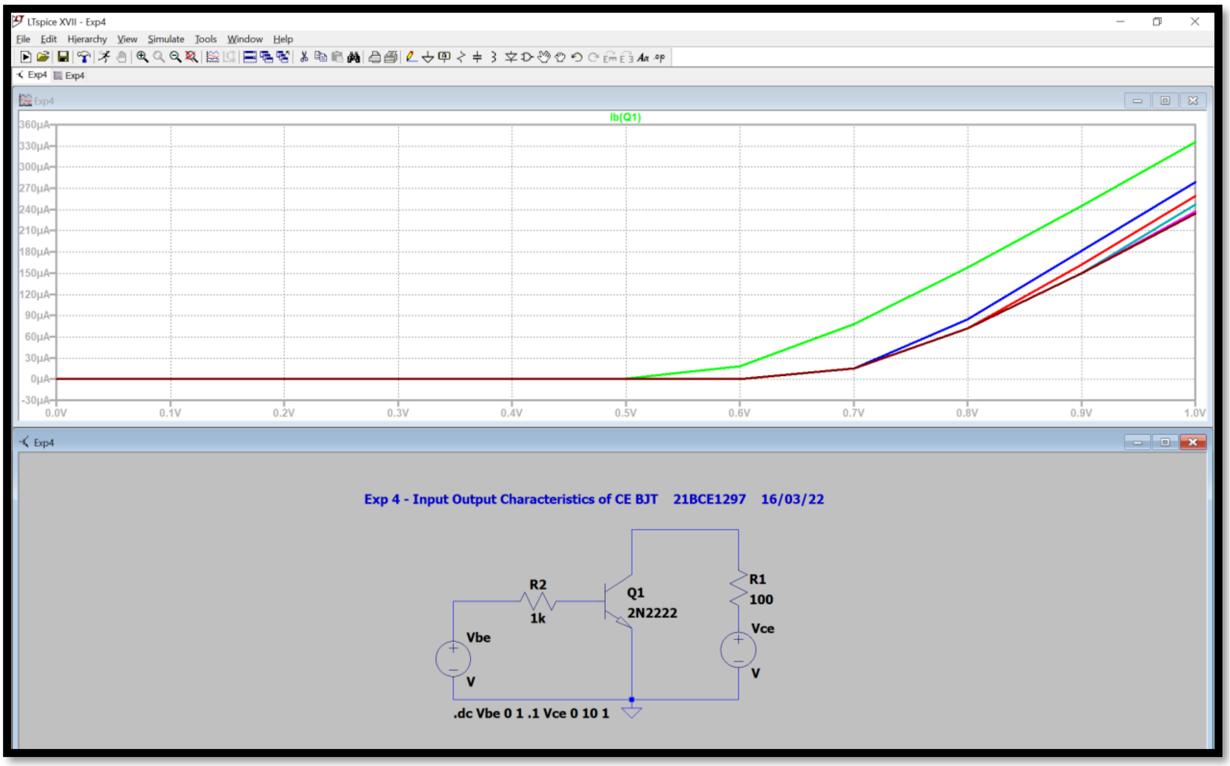


→ Output Characteristics :

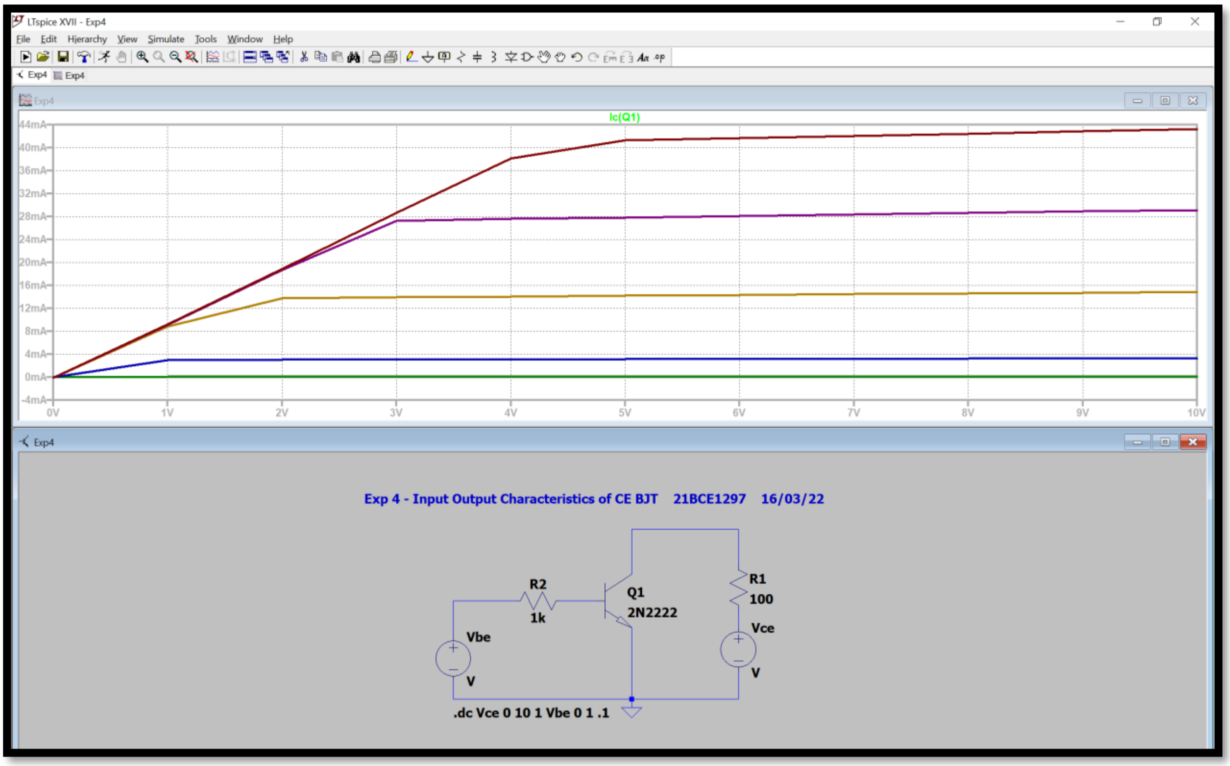


Simulation Results:

1. Input Characteristics



2. Output Characteristics



Conclusion:

1. **Input Characteristics:**
   a. **For V_{CE1} (Green)**
      i. V_{BE1} = 800 mV -> I_{B1} = 157.87 μA
      ii. V_{BE2} = 900 mV -> I_{B2} = 244.98 μA
      iii. Change in V_{BE} = 100 mV, Change in I_B = 87.11 μA
      iv. $\frac{\Delta I_B}{\Delta V_{BE}}$ = 0.87

   b. **For I_B = 210 μA**
      i. V_{CE1} -> V_{BE1} = 859.84 mV (Green)
      ii. V_{CE2} -> V_{BE2} = 929.04 mV (Blue)
      iii. V_{CE3} -> V_{BE3} = 949.23 mV (Red)

2. **Output Characteristics:**
   a. **For V_{CE} = 7V**
      i. I_{B5} -> I_C = 42.07 mA (Brown)
      ii. I_{B4} -> I_C = 28.37 mA (Purple)
      iii. I_{B3} -> I_C = 14.47 mA (Yellow)

Inferences:

1. Transistors transfer resistance.
2. Transistors can be used as amplifiers ($I_C >> I_B$).
3. Select npn transistor
4. Keep first source in DC Sweep as V_{BE} for input characteristics and as V_{CE} for output characteristics.
5. While plotting graph, click on the respective transistor terminal and not the wire.
6. Connect all wires properly.

Reg. No. 21BCE1297 Name: Vidhi Shah Date of Submission: 07/04/22

Experiment 5

Aim:

Zener diode as a voltage regulator using line regulation.

Tools and Apparatus:

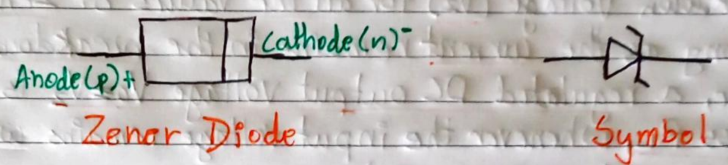
- http://vlabs.iitkgp.ernet.in/be/exp10/index.html#
- Zener Diode, Resistors, Multimeter, DC Voltage Source

Theory and Design:

- Zener Diode:

→ A zener diode is a special kind of diode which permits current to flow in the forward direction like a standard diode, but it will also allow it to flow in the reverse direction when the voltage is above the breakdown voltage or "zener voltage".

→ Zener diodes are designed so that their breakdown voltage is much lower.



→ In a standard diode, the Zener voltage is high, and the diode is permanently damaged if a reverse current above that value is allowed to pass through it.

→ In the reverse bias direction, there is practically no reverse current flow until the breakdown voltage is reached.

→ When this occurs there is a sharp increase in reverse current.

→ Varying amount of reverse current can pass through the Zener diode without damaging it.

→ The breakdown voltage or Zener Voltage (V_Z) across the diode remains relatively constant.

Zener diode as a Voltage Regulator:

→ A voltage regulator is an electronic circuit that provides a stable DC voltage independent of the load current, temperature and AC line voltage variations.

→ A zener diode of breakdown voltage (V_Z) is reverse connected to an input voltage source (V_S) across a load resistance (R_L) and a series resistor (R_S).

→ The voltage across the Zener diode will remain steady at its breakdown voltage (V_Z) for all the values of Zener current (I_Z) as long as the current remains in the breakdown region.

→ Hence, a regulated DC output voltage $V_O = V_Z$ is obtained across R_L, whenever the input voltage remains within a minimum and maximum voltage.

→ There are 2 types of regulations:

① Line Regulation: Series resistance (R_S) and Load resistance (R_L) are fixed, only input voltage (V_S) is changing. Output Voltage (V_O) remains the same, as long as the input voltage is maintained above a minimum value.

② Load Regulation: Input Voltage (V_S) is fixed and the Load resistance (R_L) is varying. Output voltage remains the same, as long as the load resistance is maintained above a minimum value.

- **Line Regulation:** R_L is constant, V_S varies, V_S must be sufficiently large to turn the Zener Diode ON.

$$V_L = V_Z = \frac{V_{S_{min}} \times R_L}{(R_S + R_L)}$$

So, the minimum turn-on voltage ($V_{S_{min}}$) is:

$$\boxed{V_{S_{min}} = \frac{V_Z \times (R_S + R_L)}{R_L}}$$

The maximum value of V_S is limited by the maximum zener current ($I_{Z_{max}}$)

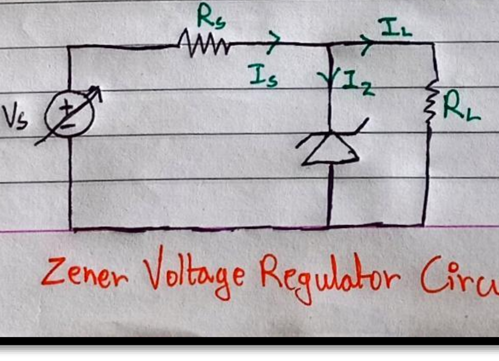
$$I_{R_{max}} = I_{Z_{max}} + I_L$$

I_L is fixed at $\frac{V_Z}{R_L}$, since, $V_L = V_Z$

So maximum V_S is $\boxed{V_{S_{max}} = V_{R_{max}} + V_Z}$ OR $\boxed{V_{S_{max}} = I_{R_{max}} \times R + V_Z}$

$\boxed{\text{For } V_S < V_Z : V_0 = V_S}$

$\boxed{\text{For } V_S > V_Z : V_0 = V_S - I_S \times R_S}$



Zener Voltage Regulator Circuit

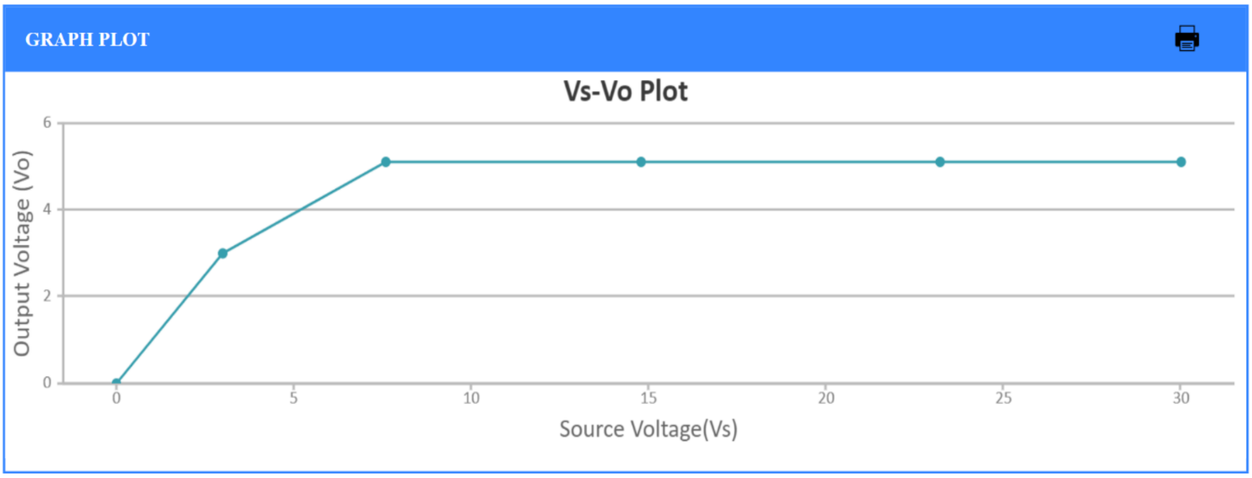
Simulation Results:

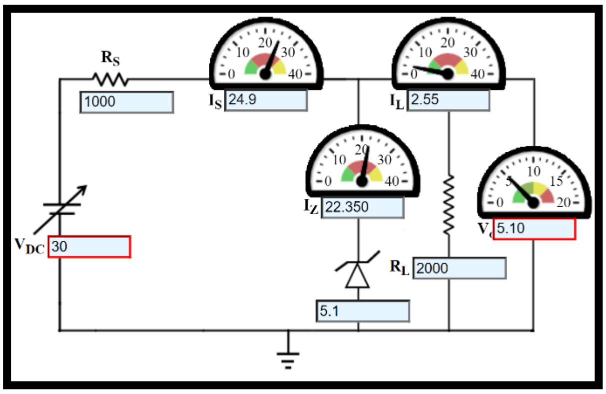
1. **Zener Voltage (V_Z) = 5.1V**
   Series Resistance (R_S) = 1kΩ
   Load Resistance (R_L) = 2kΩ

EXPERIMENTAL TABLE

Zener Voltage(V_Z): 5.1 V
Series Resistance(R_S): 1 KΩ
Load Resistance (R_L): 2 KΩ

Serial No.	Unregulated supply voltage(V_S) V	Load Current(I_L) mAmp	Zener Current(I_Z) mAmp	Regulated Output Voltage(V_O) V	% Voltage Regulation
1	0	2.55	0	0	NaN
2	3	2.55	0	3	100
3	7.6	2.55	-0.050	5.10	71.4
4	14.8	2.55	7.150	5.10	35.7
5	23.2	2.55	15.550	5.10	21.7
6	30	2.55	22.350	5.10	16.7



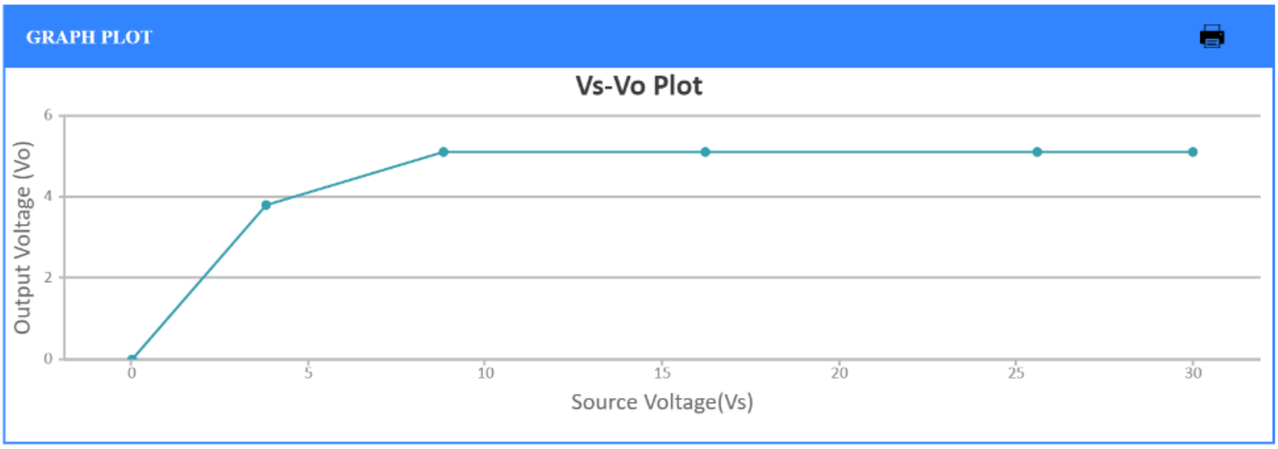


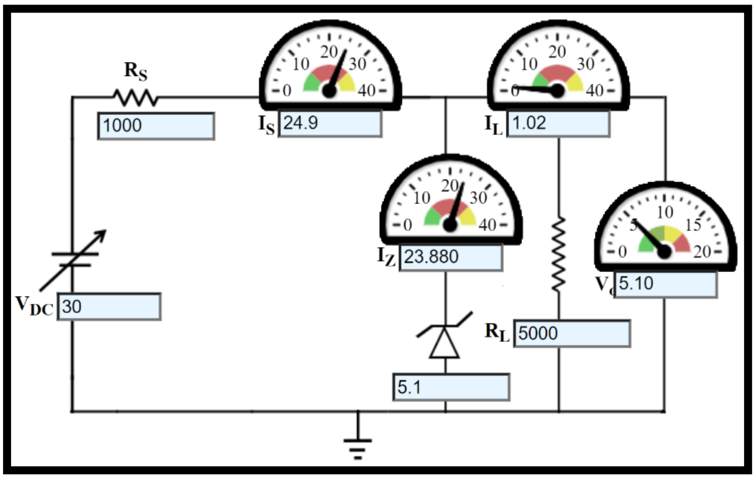
2. **Zener Voltage (V_Z) = 5.1V**
   Series Resistance (R_S) = 1kΩ
   Load Resistance (R_L) = 5kΩ

EXPERIMENTAL TABLE

Zener Voltage(V_Z): 5.1 V
Series Resistance(R_S): 1 KΩ
Load Resistance (R_L): 5 KΩ

Serial No.	Unregulated supply voltage(V_S) V	Load Current(I_L) mAmp	Zener Current(I_Z) mAmp	Regulated Output Voltage(V_O) V	% Voltage Regulation
1	0	1.02	0	0	NaN
2	3.8	1.02	0	3.8	100
3	8.8	1.02	2.680	5.10	62.5
4	16.2	1.02	10.080	5.10	31.3
5	25.6	1.02	19.480	5.10	20.0
6	30	1.02	23.880	5.10	16.7





Conclusion:

1. For constant value of Zener Voltage (**V_z = 5.1V)** and varying values of V_S and R_L
    a. Output Voltage is constant, **V_O = 5.1V**

2. For constant value of **V_z = 5.1V** and varying values of V_S
    a. **R_L = 2kΩ**
        i. Load current is constant, **I_L = 2.55A**
    b. **R_L = 5kΩ**
        i. Load current is constant, **I_L = 1.02A**

Inferences:

1. For all values of Source Voltage greater than Zener Voltage, Output Voltage is constant and is equal to Zener Voltage.
2. If Source Voltage is less than Zener Voltage, Output Voltage will be equal to Source Voltage.
3. To get a straight line graph of constant voltage always keep Source Voltage greater than Zener Voltage.
4. **$I_S = I_L + I_Z$**
    a. I_S and I_Z are regulated in such a way that I_L remains constant for a constant value of R_L and therefore V_O remains the same.
    b. If R_L changes then all current values change accordingly (Inversely Proportional) and therefore V_O still remains the same.

Reg. No. 21BCE1297 Name: Vidhi Shah Date of Practical: 24/04/22

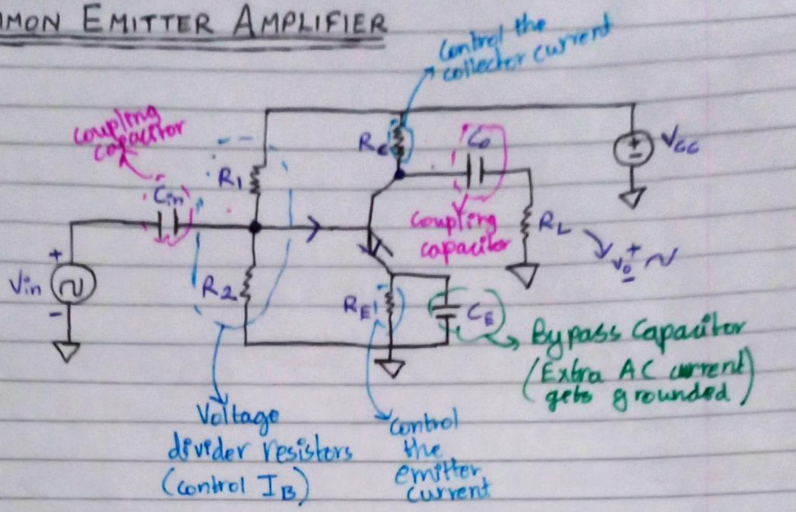
Experiment 6

Aim:
AC and transient analysis of CE (Common Emitter) amplifier using LTSpice.

Tools and Apparatus:
LTSpice, Transistor, Resistors, Capacitors, Voltage Sources

Theory and Design:

→ COMMON EMITTER AMPLIFIER

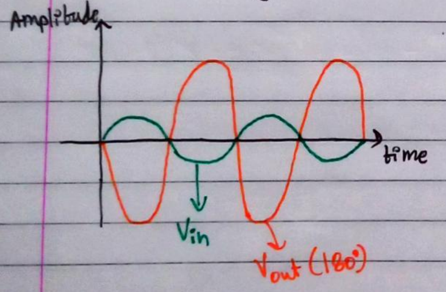


- Coupling capacitors: Allow only AC current and block DC current

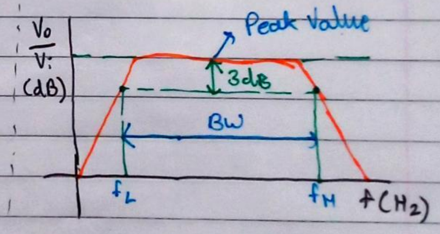
→ It is called common emitter configuration as emitter terminal is common between input and output.

→ Values of resistors are selected such that transistor is in active region and Base current (I_B) is minimum.

→ Transient Analysis:

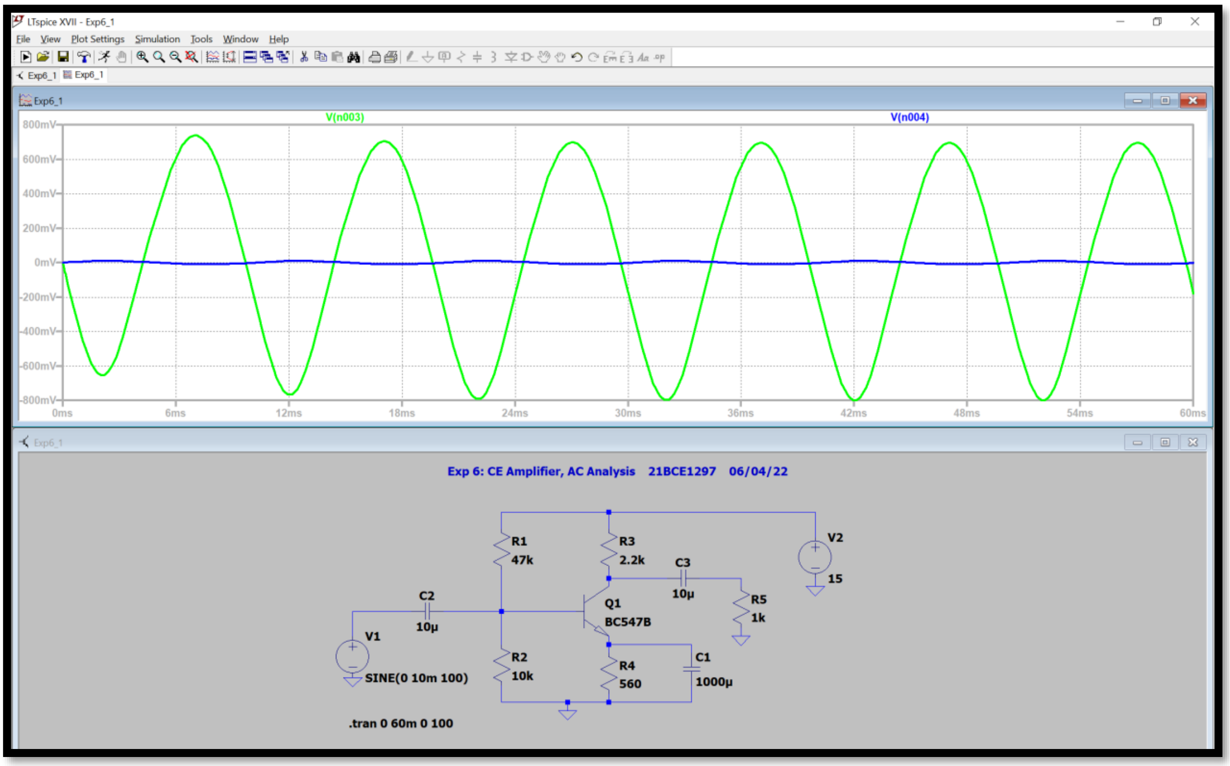


→ AC Analysis:

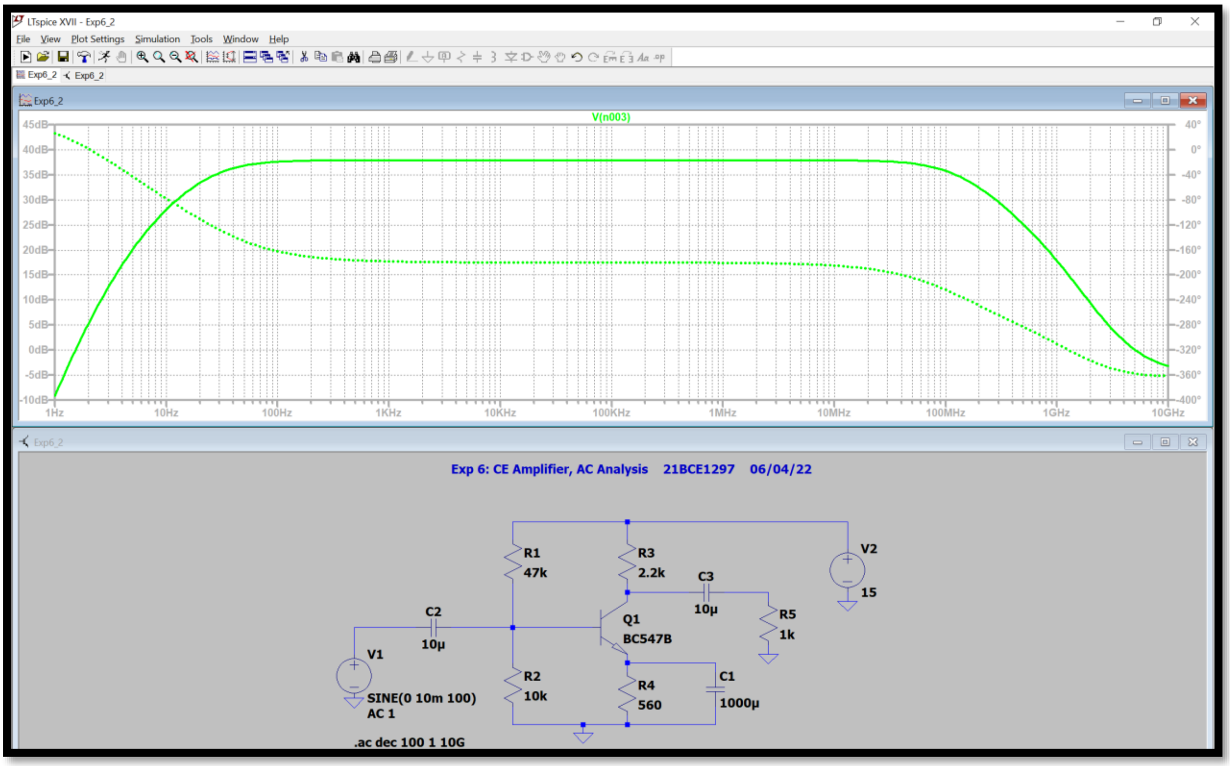


Simulation Results:

1. Transient Analysis



2. AC Analysis



Conclusion:

1. **Transient Analysis:**
   a. Gain $= \frac{V_o}{V_i} = \frac{695.754}{9.497} = 73.26$
2. **AC Analysis:**
   a. Peak Value, $\frac{V_o}{V_i}$ = 37.8 dB
   b. Gain $= 10^{\frac{37.8}{20}} = 77.62$
   c. Half Power Values = 37.8 – 3 = 34.8 Db
   d. f_L = 26.2 Hz, f_H = 129.3 MHz
      i. **Amplifier Bandwidth = f_L - f_H = 129.29 MHz**
      ii. **Bandwidth for Constant Phase = 20MHz - 200Hz = 19.99 MHz**

Inferences:

1. It is a common emitter configuration as emitter terminal is common between input and output.
2. Resistors are selected such that transistor remains in active region and base current is minimum.
3. As we can see in transient analysis signal is amplified almost by 73 times.
4. The value of emitter capacitor enhances the amplification of AC signal.
5. Bandwidth is equal to upper limit as lower limit is negligible in comparison.
6. Connect the voltage biasing resistors properly.

Reg. No. 21BCE1297 **Name: Vidhi Shah** **Date of Submission: 22/04/22**

Experiment 7

Aim:
Study and simulation of MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor) characteristics using LTSpice.

Tools and Apparatus:
LTSpice, MOSFET Transistor, Resistors, Voltage Sources

Theory and Design:

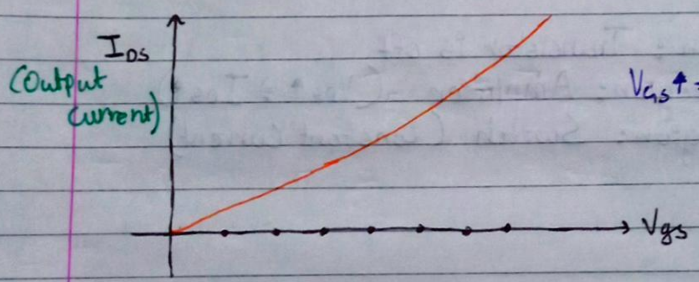
⇒ MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor):

MOSFET is a voltage controlled device.

$$\boxed{I_D = K(V_{gs} - V_{th})^2}$$

I_D: Drain Current
V_{gs}: Gate to Source Voltage
V_{th}: Threshold Voltage (~2-5V)

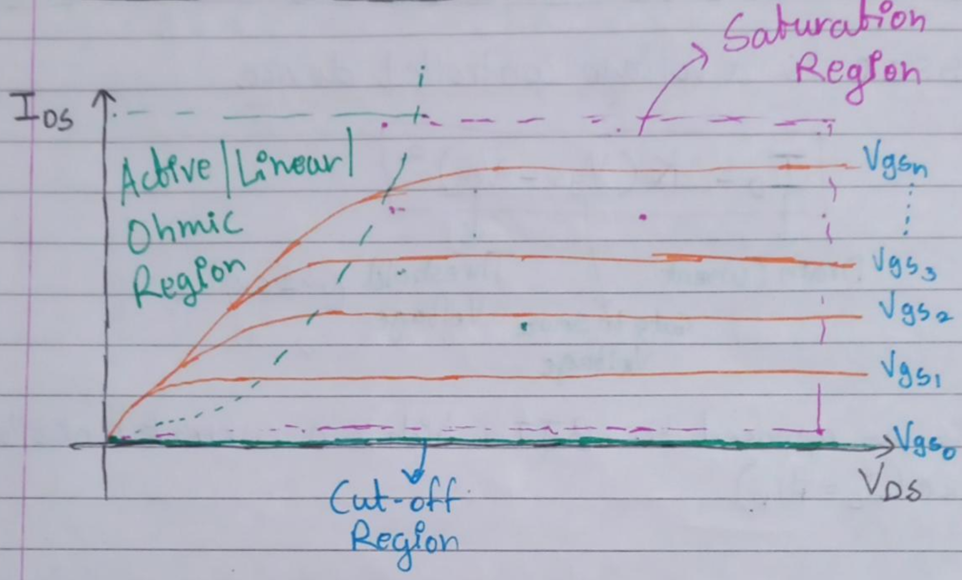
This is as opposed to BJT which is a current controlled device ($i_c = \beta i_b$)



MOSET → Drain / Gate / Source (3 terminal Device)

- Depletion
  - P
  - N
- Enhancement
  - P
  - N

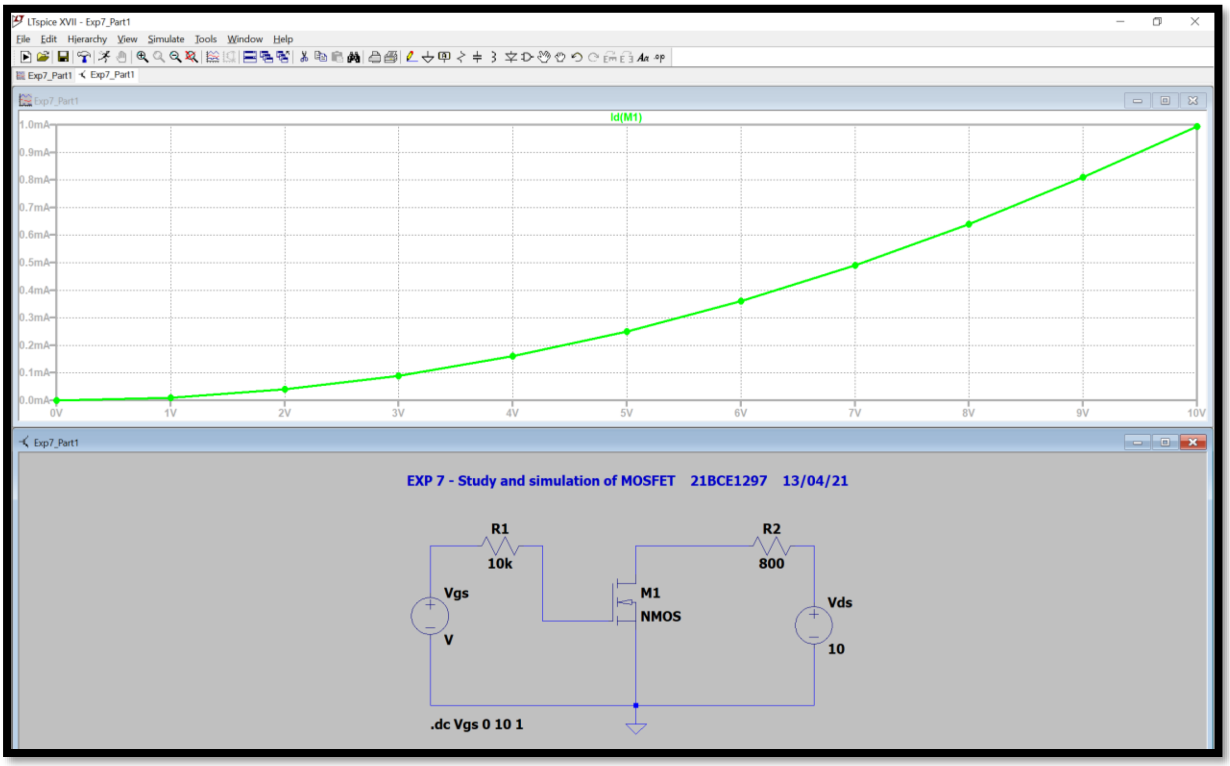
→ Transfer Characteristics :



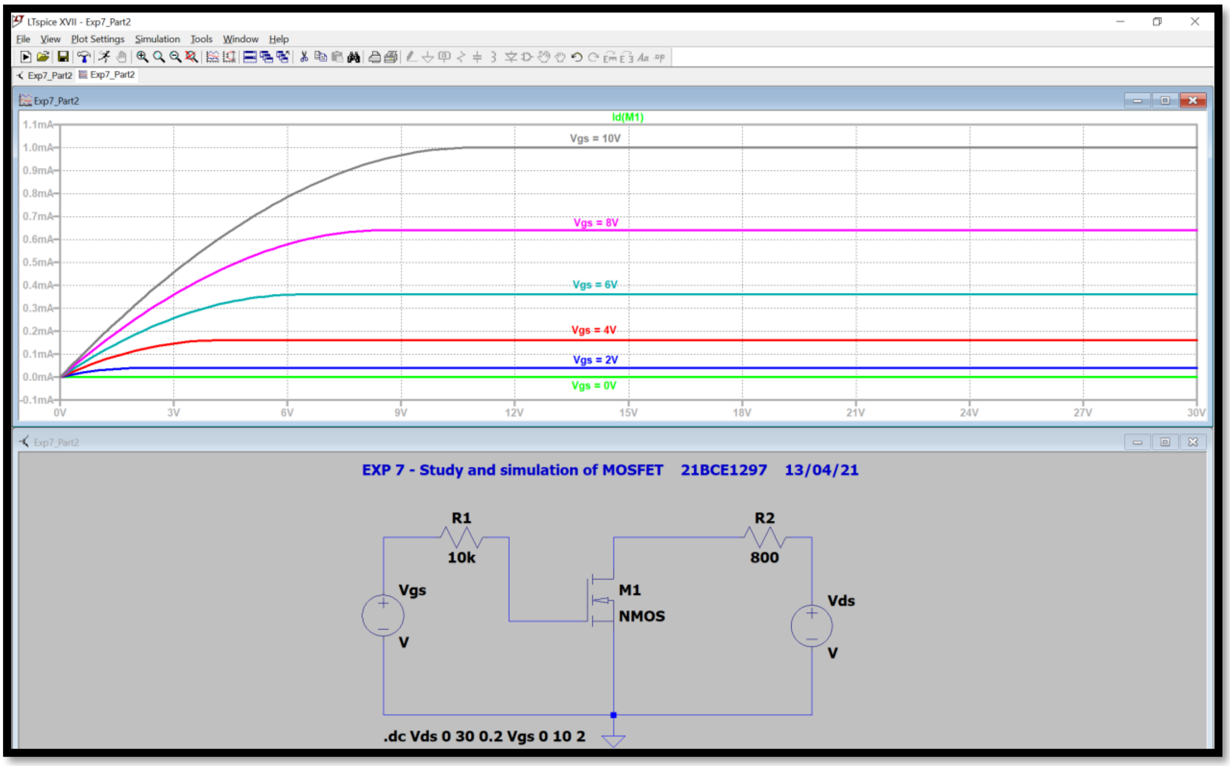
① Cut-off region : Transistor is off.
② Linear / ohmic region : Amplifier ($V_{DS}\uparrow \Rightarrow I_{DS}\uparrow$)
③ Saturation region : Switch (constant current)

Simulation Results:

1. Output Characteristics



2. Transfer Characteristics



Conclusion:

1. **Output Characteristics:**
   - I_{DS} increases as V_{GS} increases.
2. **Transfer Characteristics:**
   - I_{DS} increases linearly with respect to V_{DS} in Active/Linear/Ohmic region.
   - I_{DS} remains constant with respect to V_{DS} in Saturation region.

Inferences:

1. $\boxed{I_{DS} = K\,(V_{GS}-V_{TH})^2}$
   a. Therefore, I_{DS} increases as V_{GS} increases in output characteristics of MOSFET
2. VGS = 0V is **Cut Off Region**:
   a. Transistor is in **off** state.
3. **Linear/Ohmic Region**:
   a. Transistor acts as an **amplifier** as **current increases** with increase in voltage
4. **Saturation Region**:
   a. Transistor acts as a **switch** as **current remains constant** with respect to voltage
5. In transfer characteristics keep first source as V_{DS} and second source as V_{GS}.

Reg. No. 21BCE1297 Name: Vidhi Shah Date of Submission: 25/05/22

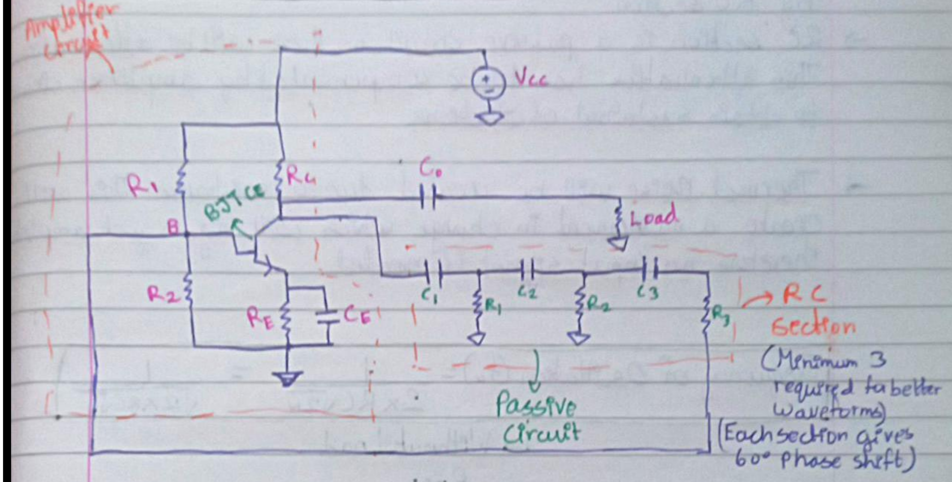
Experiment 8

Aim:
Simulation of RC Phase Shift Oscillator using LT Spice

Tools and Apparatus:
LTSpice, BJT Transistor, Resistors, Capacitors, Voltage Sources

Theory and Design:

⇒ RC Phase Shift Oscillator :



→ As we are using BJT in Common Emitter configuration, the output signal will be 180° out of phase with input signal.
→ This signal is passed through RC section. Therefore it will be 360° out of phase OR exact same phase as that of input signal.
→ This will create sustained oscillations.
→ Signals are generated without any input source.
→ Positive feedback is created through RC Phase shift and smooth sinusoidal waveform is generated with particular frequency

* There should be:
1. Positive Feedback
2. Same phase shift between input and output signals (0° or 360°)
3. No input signal needed

* 2 types of gains:
1. Circuit Gain (A)
2. Feedback Gain (β)

$\boxed{A\beta = 1}$

→ For $\boxed{A\beta = 1}$, any loss or gain in the circuit shout be compensate by RC section.

→ RC section is a passive circuit so there will be attenuation. This attenuation has to be compensated by amplifier circuit to obtain sustained oscillations.

→ Thermal noise will be created due to resistance. This will create a movement in charge which will again get amplified therefore no input signal is needed.

$$\boxed{\text{Frequency of Oscillation } (f_o) = \frac{1}{2\pi RC\sqrt{2N}} = \frac{1}{\sqrt{2\pi RC\sqrt{6}}}}$$

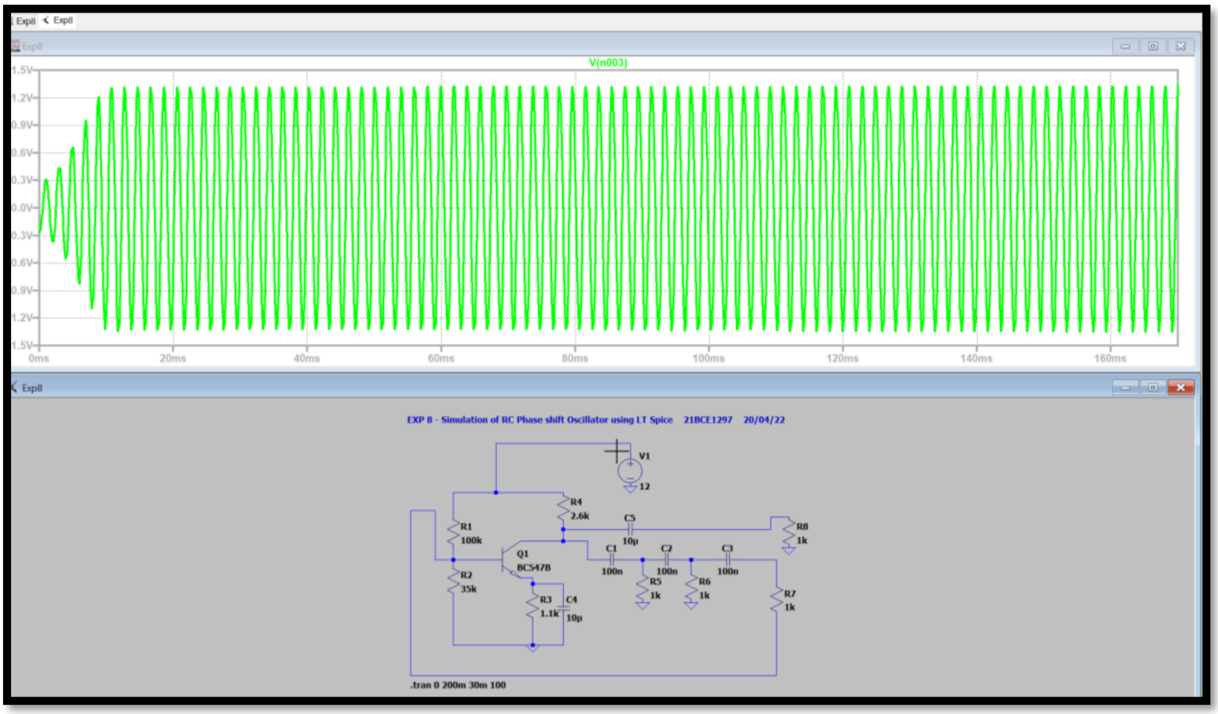
↳ Without Load

Res.

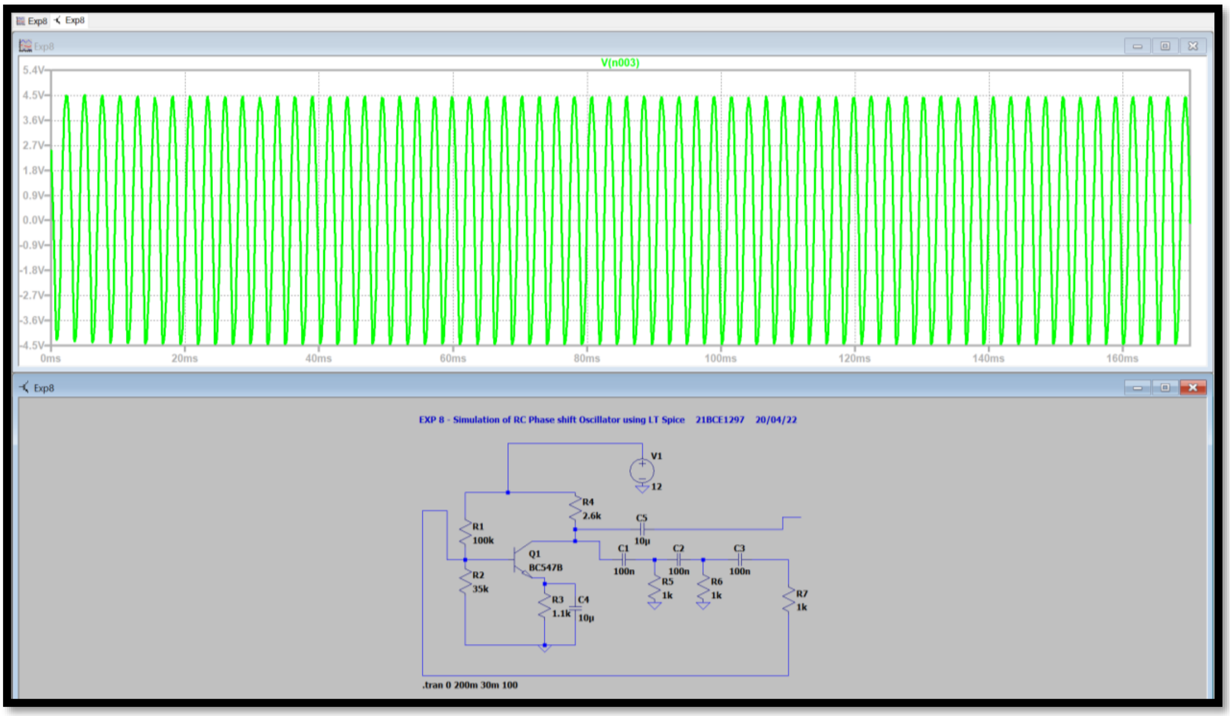
$$\boxed{\text{Frequency of Oscillation } (f_o) = \frac{1}{2\pi RC\sqrt{6+4\frac{R_L}{R}}}}$$

Simulation Results:

1. With Load



2. Without Load



Conclusion:

1. With Load:

- $f_0 = \frac{1}{T} = \frac{1}{63.80-61.87} \times 10^3$ = 517.15 Hz (Simulated)
- $f_0 = \frac{1}{2\pi RC\sqrt{2N}} = \frac{1}{2\pi(1k\Omega)(100nF)\sqrt{6}}$ = 649.75 Hz (Calculated)

2. Without Load:

- $f_0 = \frac{1}{T} = \frac{1}{62.41-59.82} \times 10^3$ = 386.6 Hz (Simulated)
- $f_0 = \frac{1}{2\pi RC\sqrt{2N+4\times\frac{R_C}{R}}} = \frac{1}{2\pi(1k\Omega)(100nF)\sqrt{6+4\times\frac{2.6}{1}}}$ = 393.005 Hz (Calculated)

Inferences:

1. **Oscillation frequency (f_0)**:
   a. With Load: 500-600 Hz
   b. Without Load: 350-400 Hz
2. It gives positive feedback and no input source is needed.
3. Minimum 3 RC sections should be connected to obtain better waveform
4. Marginal error occurs between stimulated and calculated values due to loading effect.
5. Connect all components properly.

Reg. No. 21BCE1297 Name: Vidhi Shah Date of Submission: 03/06/22

Experiment 9

Aim:
To simulate and verify basic Logic Gates and Boolean Functions.

Tools and Apparatus:
DC Voltage Source, AND, NAND, OR, NOR, NOT, XOR and XNOR gates.

Theory:

Truth Tables:

Input		Output					
A	B	AND	NAND	OR	NOR	XOR	XNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

Input	Output
X	NOT
0	1
1	0

1. $x = \overline{A \cdot B(C + D)}$

Input				Output
A	B	C	D	x
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
1	0	0	0	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	1
0	1	1	0	1

Input				Output
A	B	C	D	x
0	1	0	1	1
0	0	1	1	1
1	1	1	0	0
1	0	1	1	1
1	1	0	1	0
0	1	1	1	1
1	1	1	1	0

2. $y = AC + B\overline{C} + \overline{A}BC$

Input			Output
A	**B**	**C**	y
0	0	0	0
1	0	0	0
0	1	0	1
0	0	1	0
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1

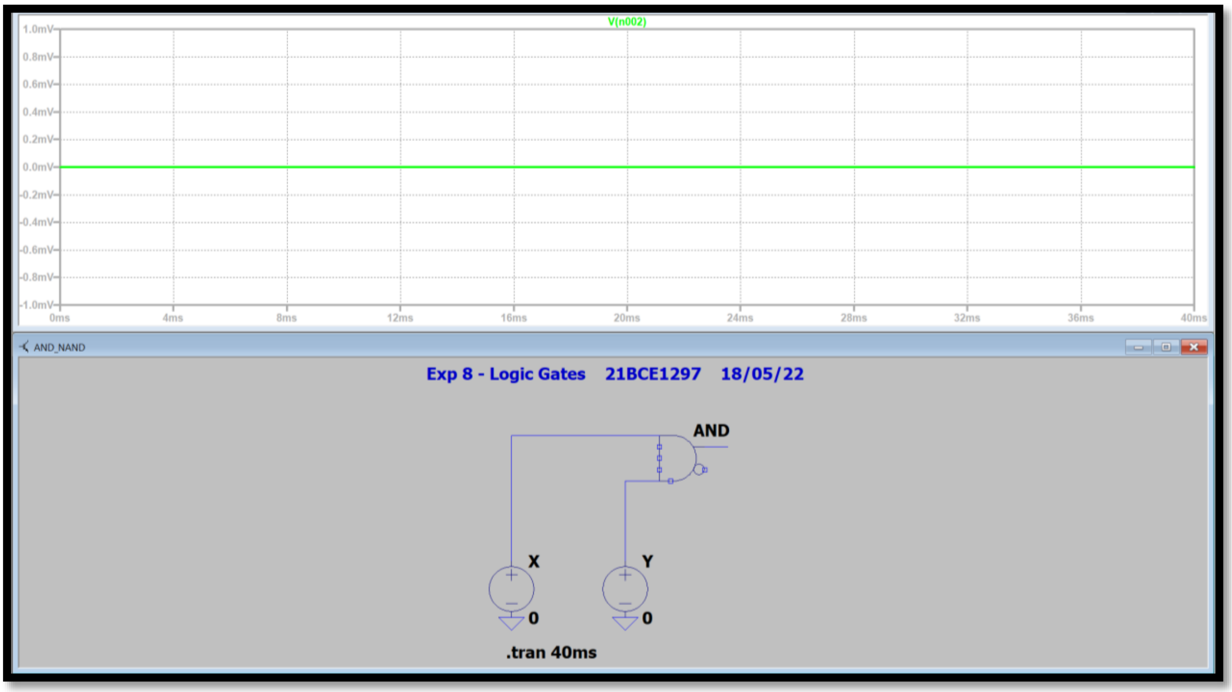
3. $z = \overline{A + B + \overline{C}D\overline{E}} + \overline{B}C\overline{D}$

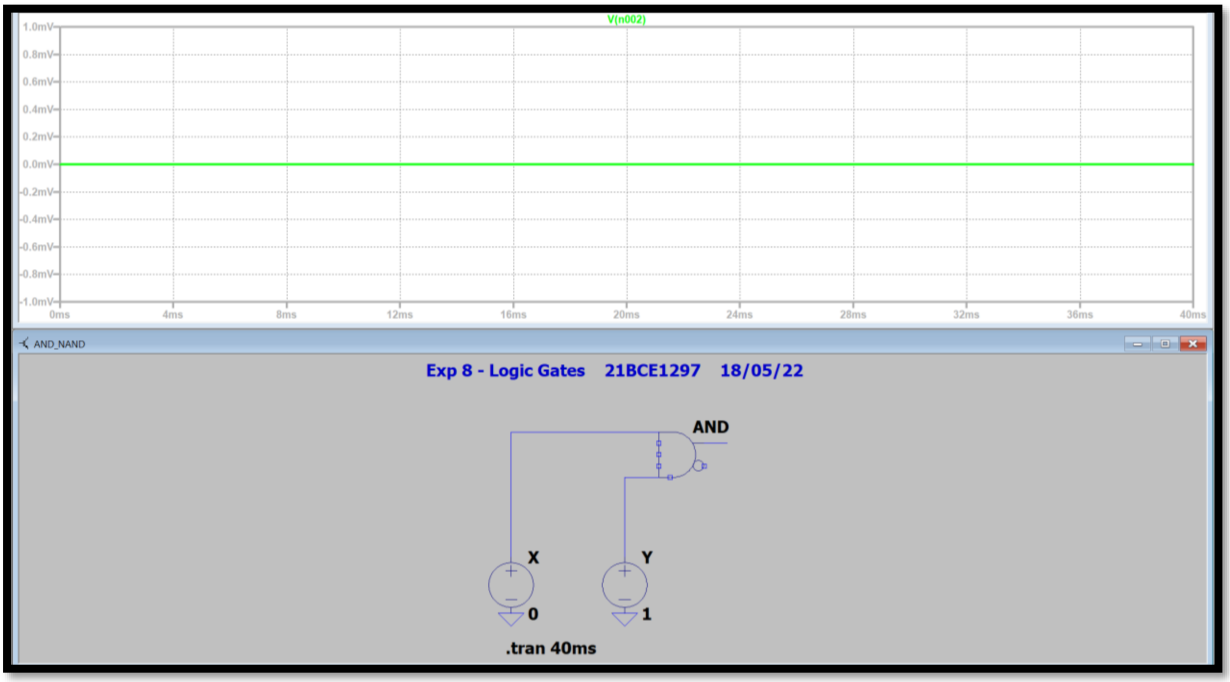
Input					Output
A	**B**	**C**	**D**	**E**	z
0	0	0	0	0	1
1	0	0	0	0	0
0	1	0	0	0	0
0	0	1	0	0	1
0	0	0	1	0	0
0	0	0	0	1	1
1	1	0	0	0	0
1	0	1	0	0	1
1	0	0	1	0	0
1	0	0	0	1	0
0	1	1	0	0	0
0	1	0	1	0	0
0	1	0	0	1	0
0	0	1	1	0	1
0	0	1	0	1	1
0	0	0	1	1	1
1	1	1	0	0	0
1	1	0	1	0	0
1	1	0	0	1	0
1	0	1	1	0	0
1	0	1	0	1	1

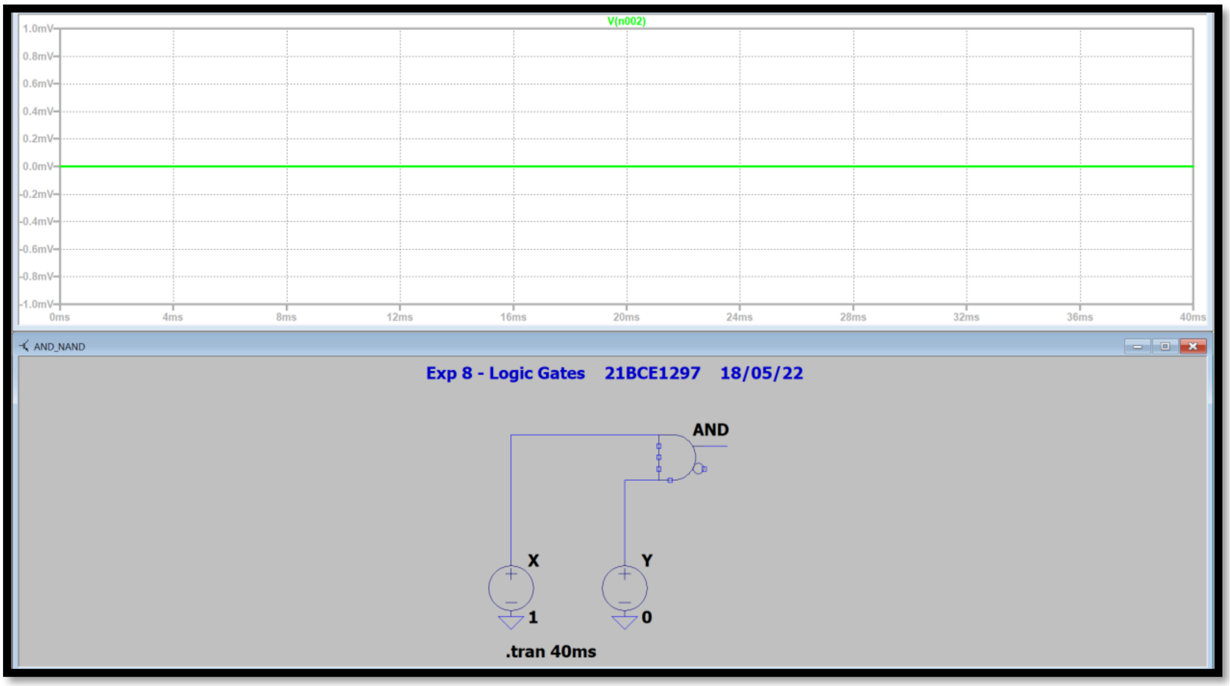
Input					Output
A	**B**	**C**	**D**	**E**	z
1	0	0	1	1	0
0	1	1	1	0	0
0	1	1	0	1	0
0	1	0	1	1	0
0	0	1	1	1	1
1	1	1	1	0	0
1	1	1	0	1	0
1	1	0	1	1	0
1	0	1	1	1	0
0	1	1	1	1	0
1	1	1	1	1	0

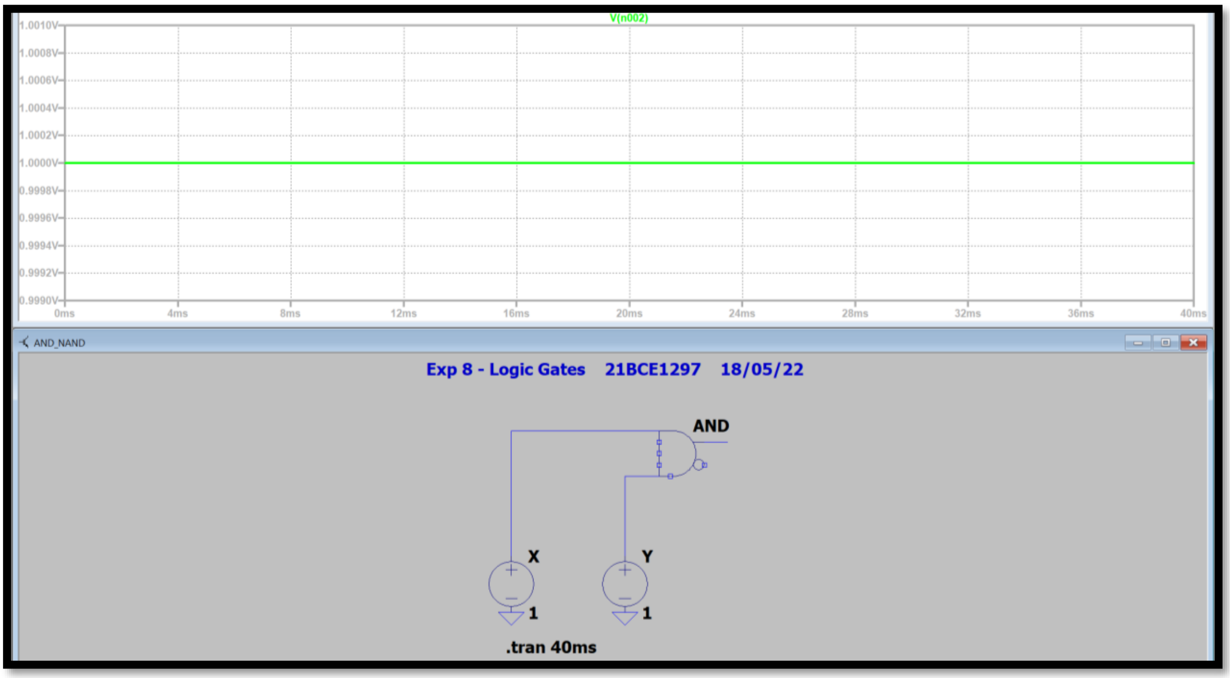
Simulation Results:

4. AND Gate

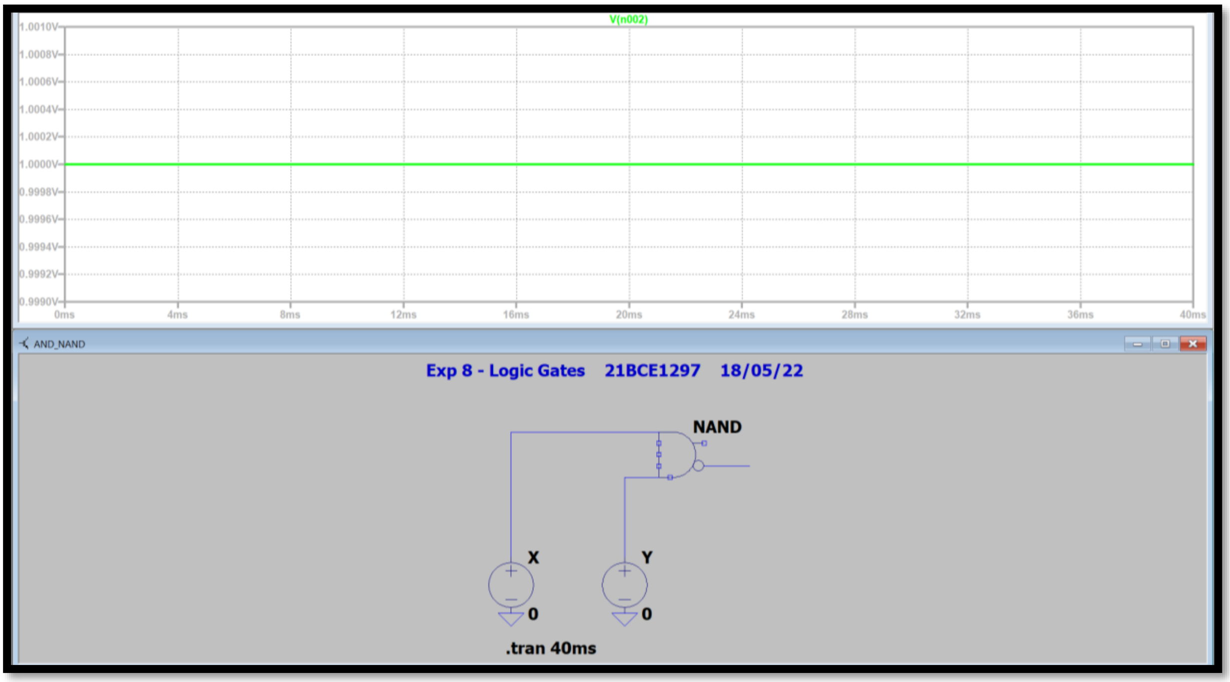


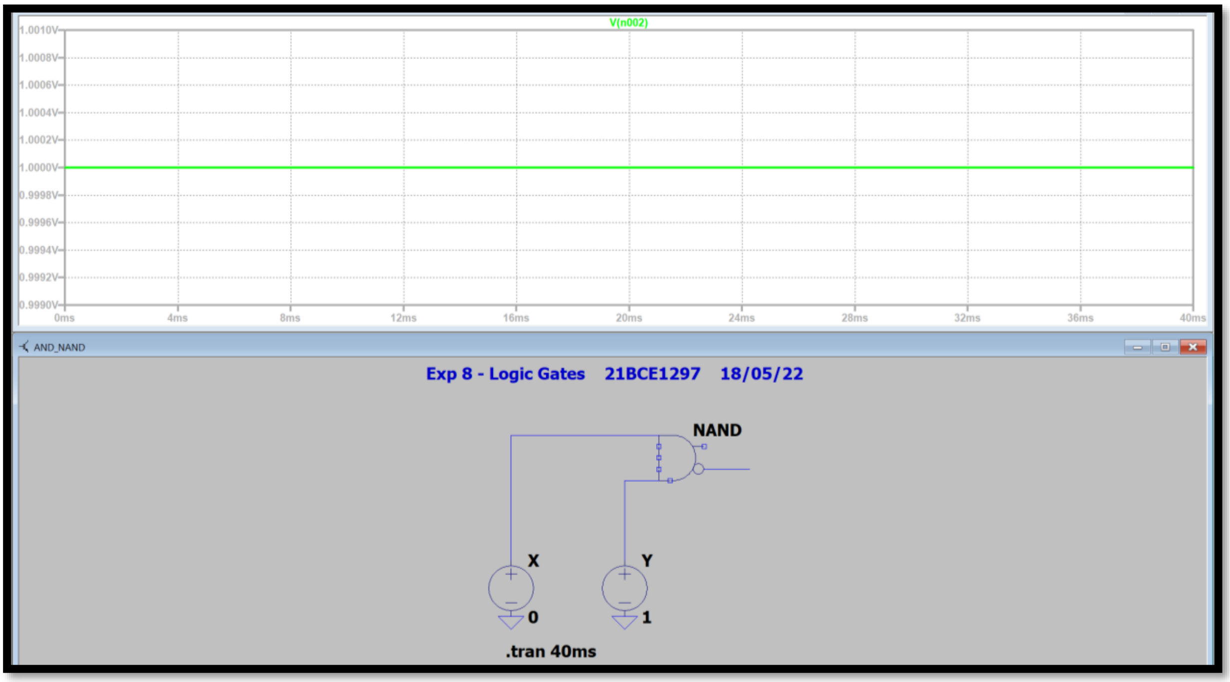


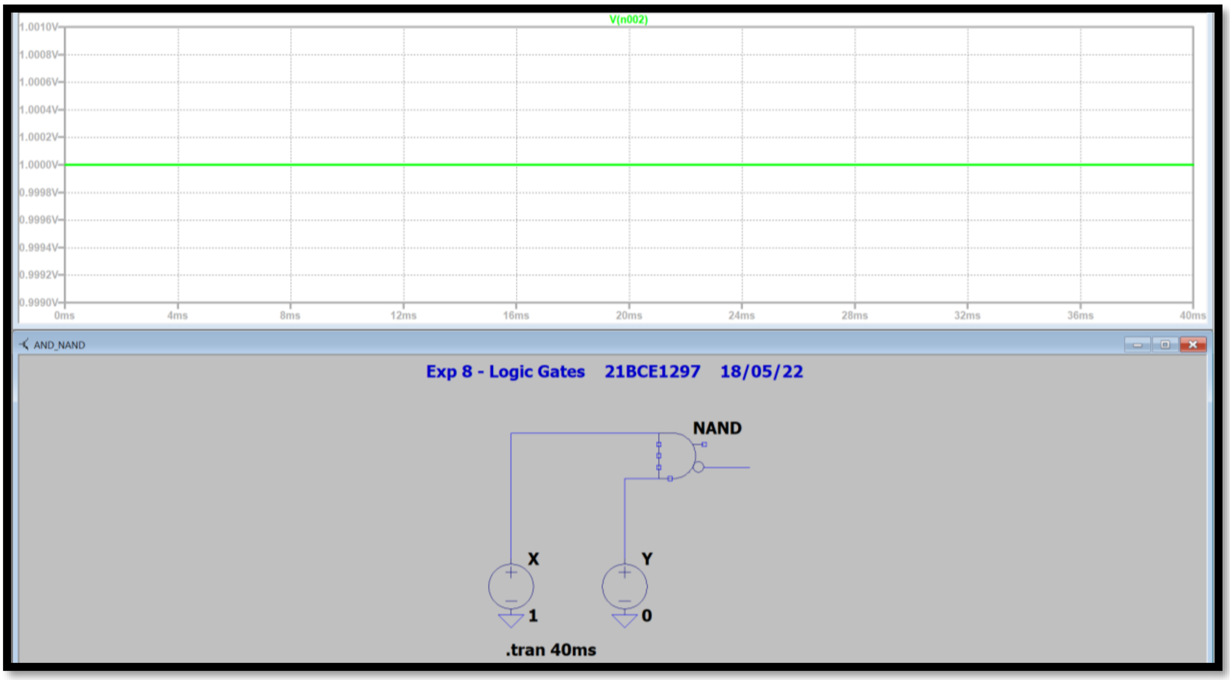

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
AND
X
Y
1
0
.tran 40ms

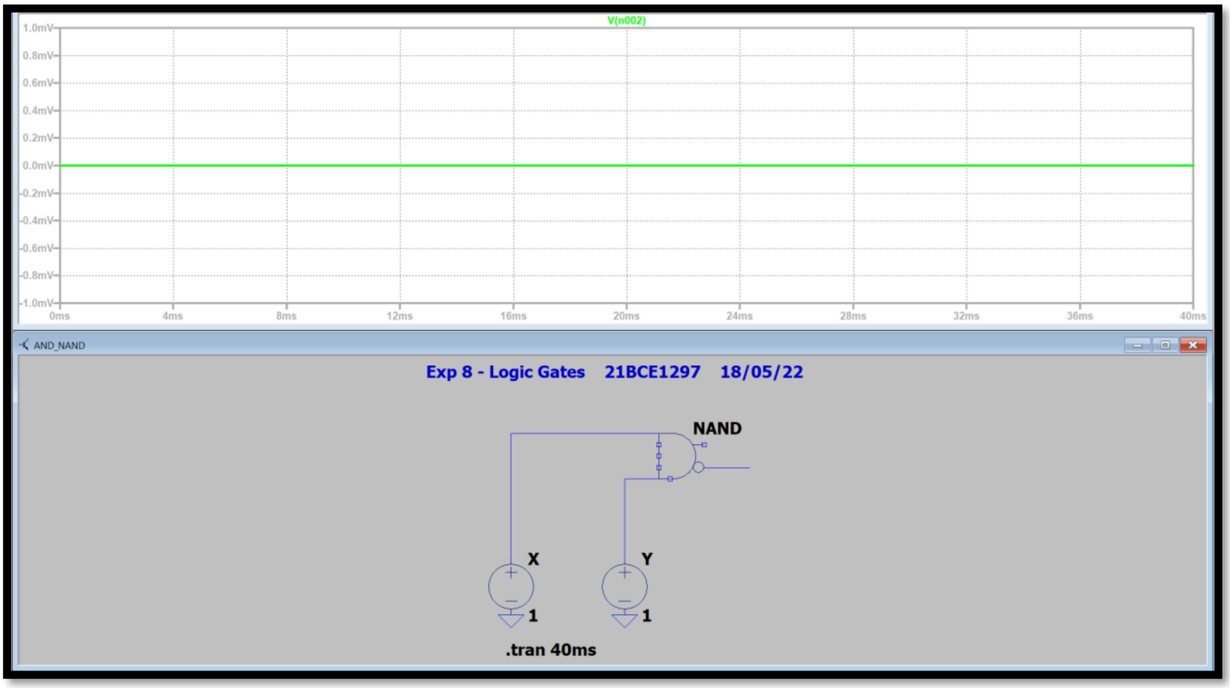

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
AND
X
Y
1
1
.tran 40ms

5. NAND Gate

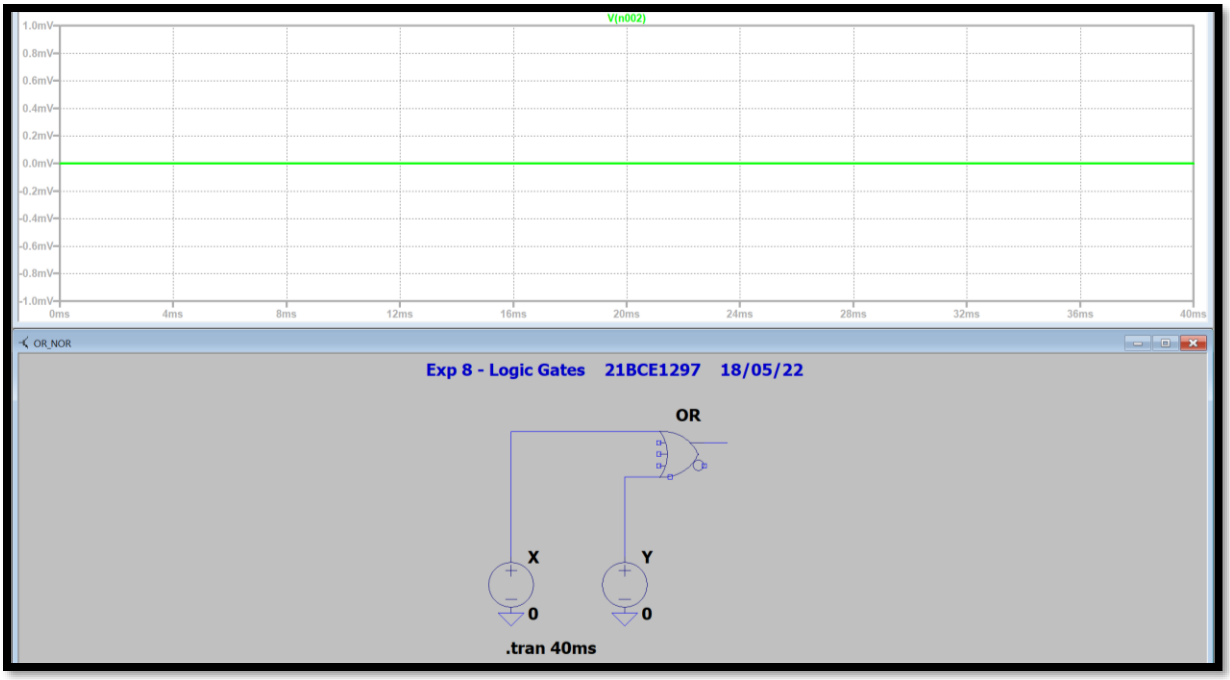

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
NAND
X
Y
0
0
.tran 40ms

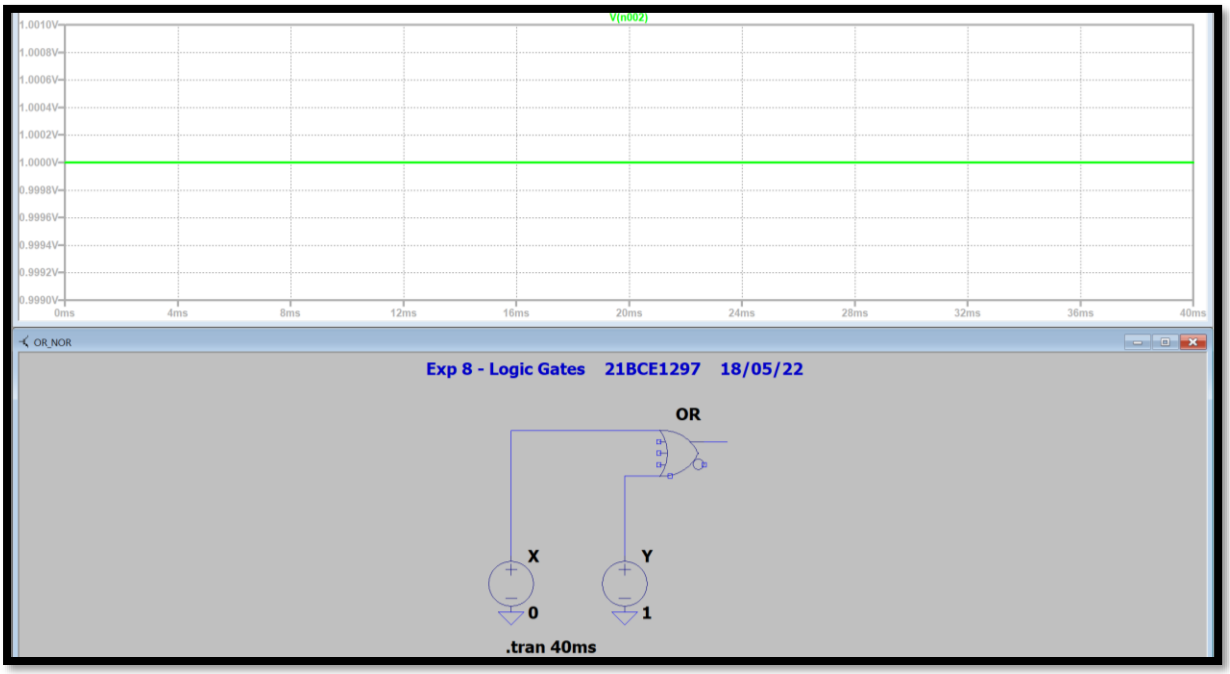

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
NAND
X
Y
0
1
.tran 40ms

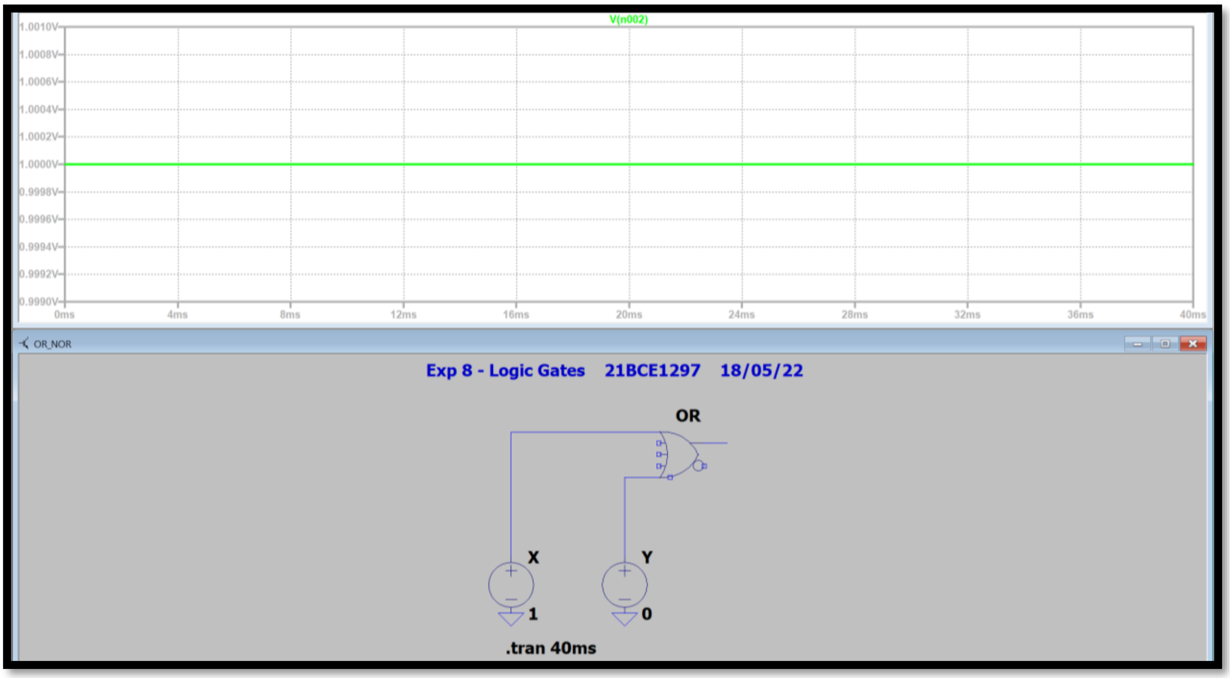

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
NAND
X
Y
1
0
.tran 40ms

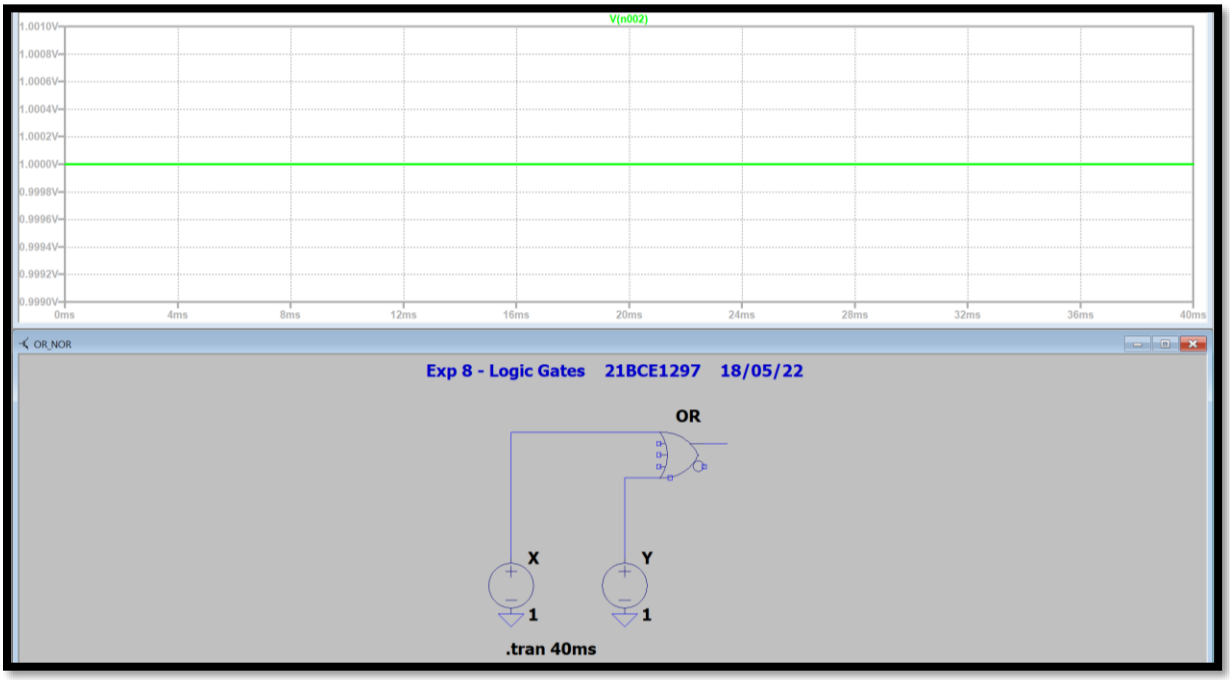

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
NAND
X
Y
1
1
.tran 40ms

6. OR Gate

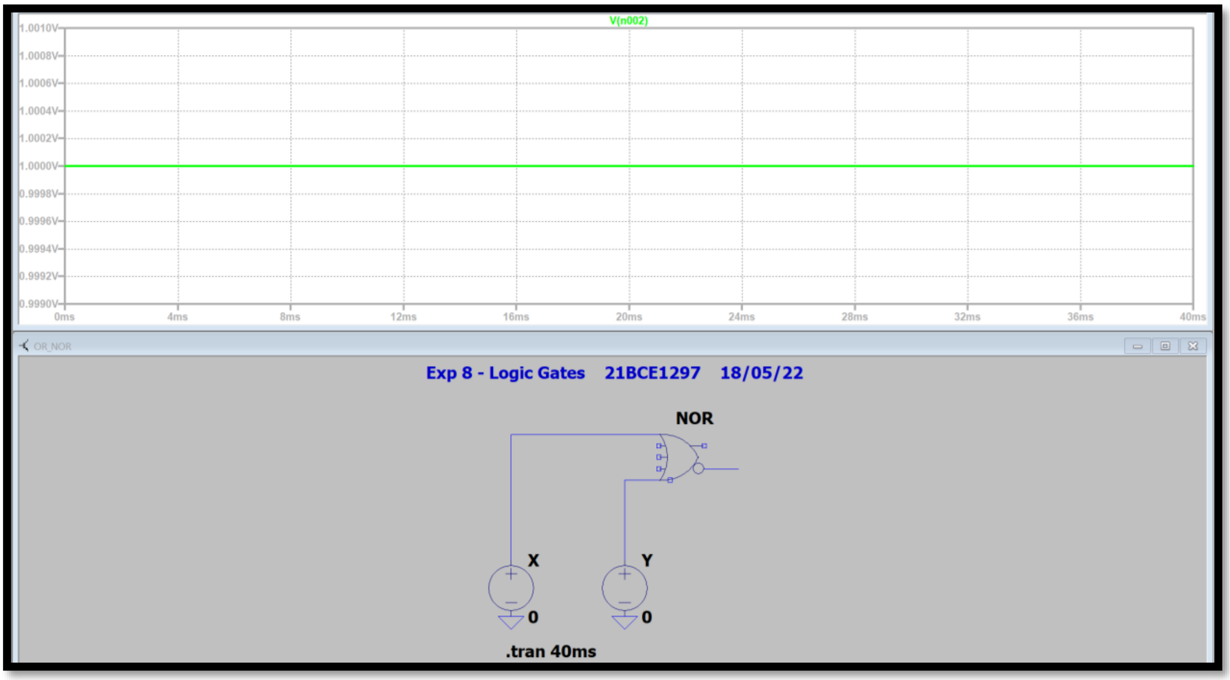

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
OR
X
Y
0
0
.tran 40ms


V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
OR
X
Y
0
1
.tran 40ms

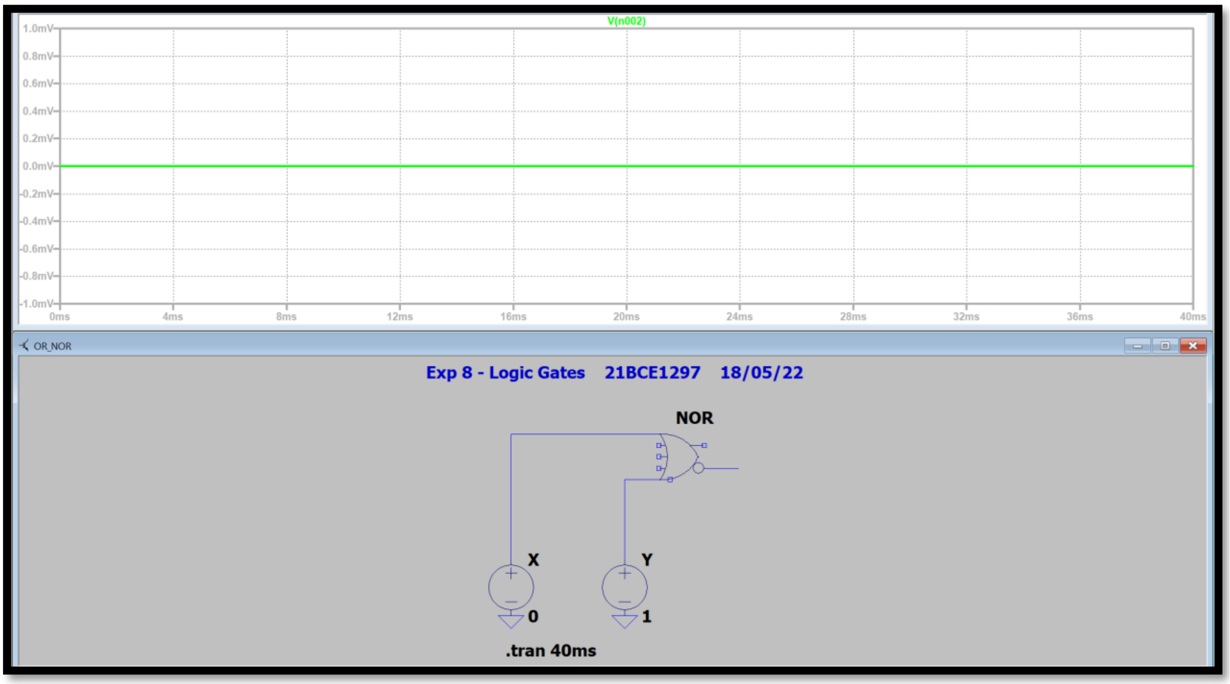

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
OR
X
Y
1
0
.tran 40ms


V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
OR
X
Y
1
1
.tran 40ms

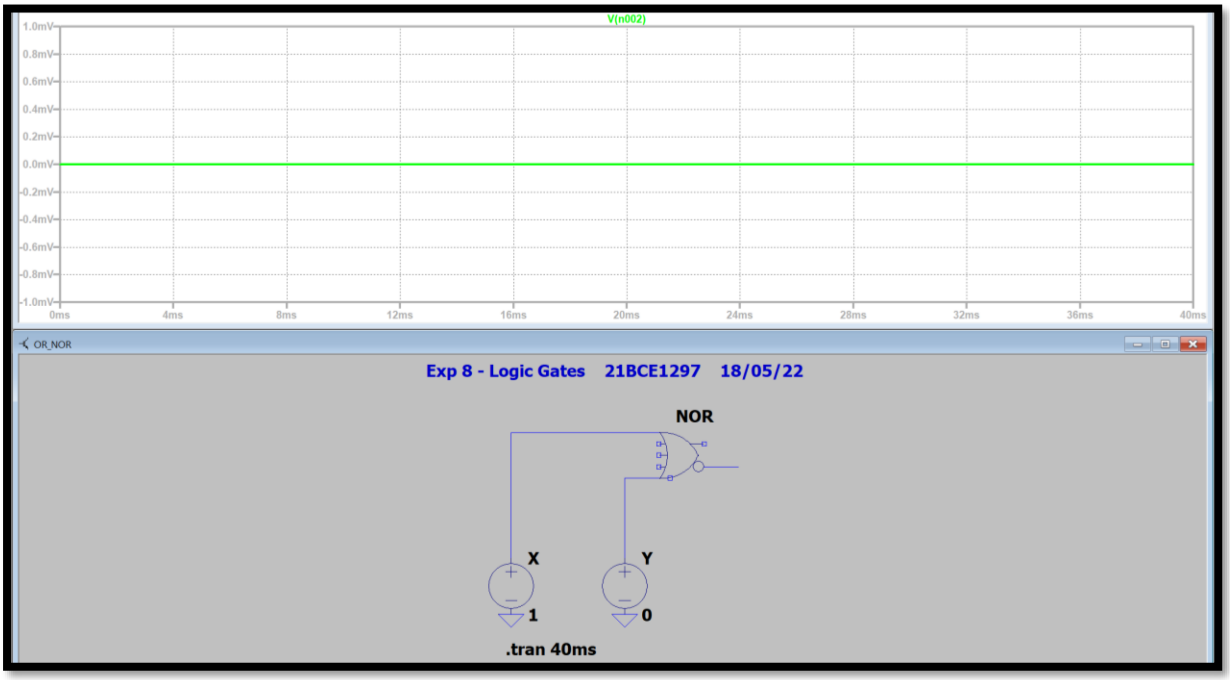
7. NOR Gate

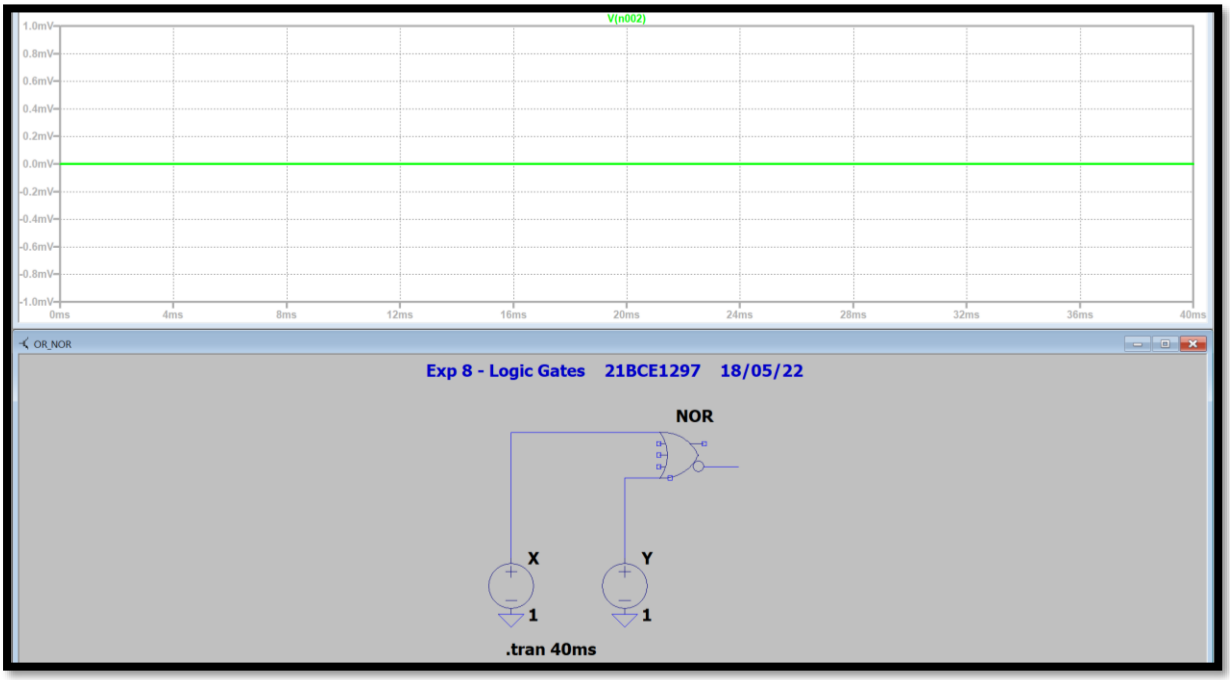


V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOR
X
Y
0
0
.tran 40ms

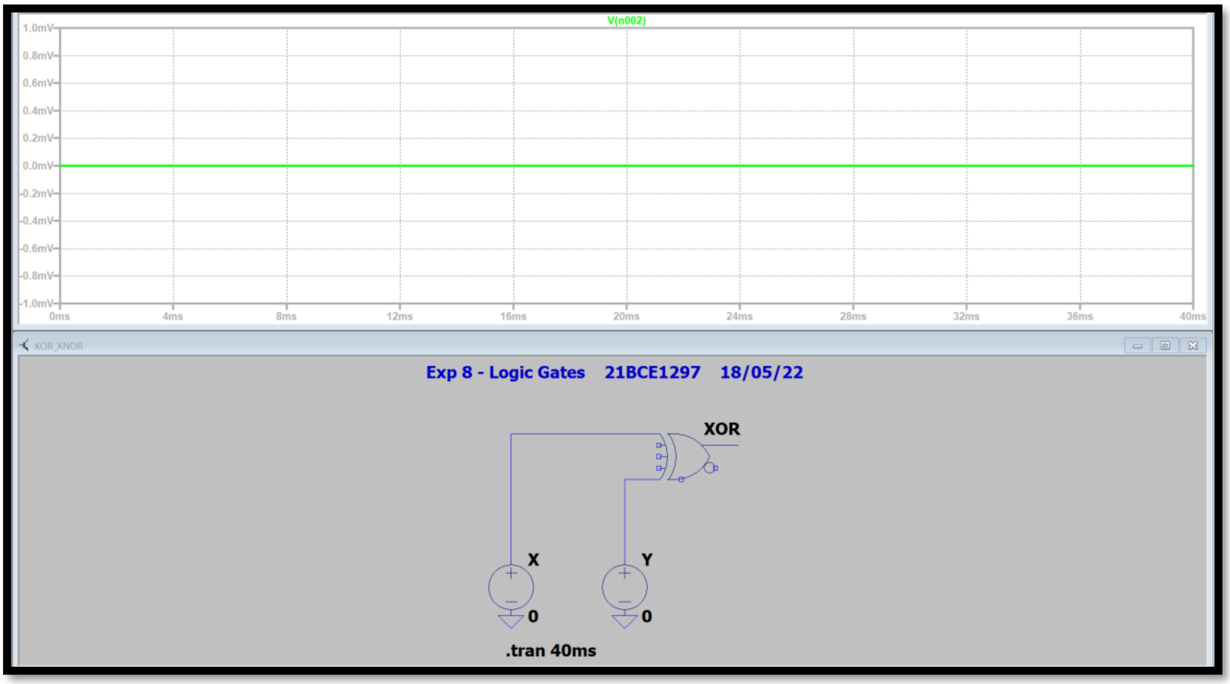


V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOR
X
Y
0
1
.tran 40ms

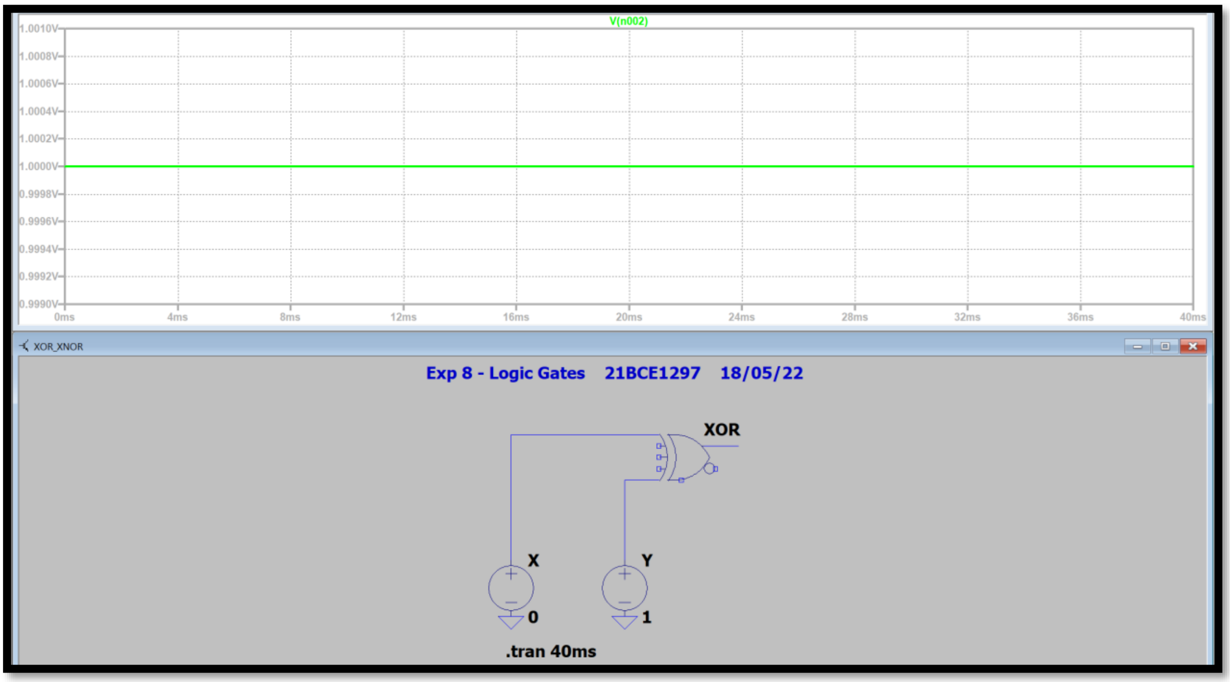

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOR
X
Y
1
0
.tran 40ms


V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOR
X
Y
1
1
.tran 40ms

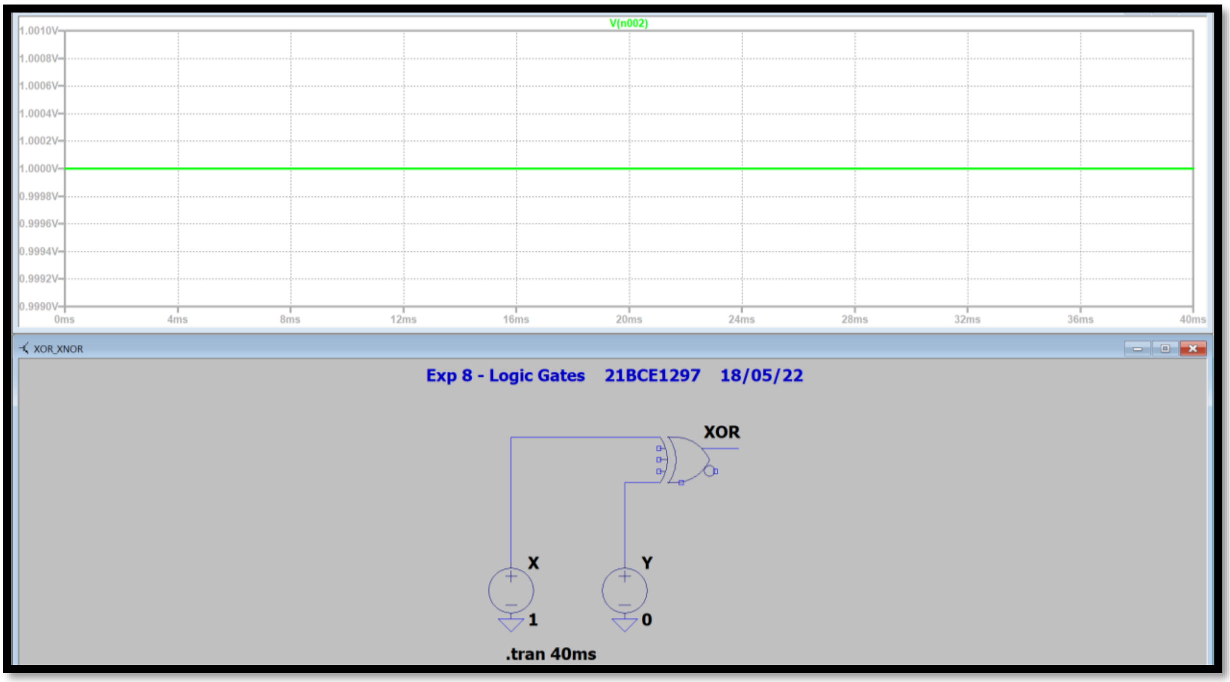
8. XOR Gate



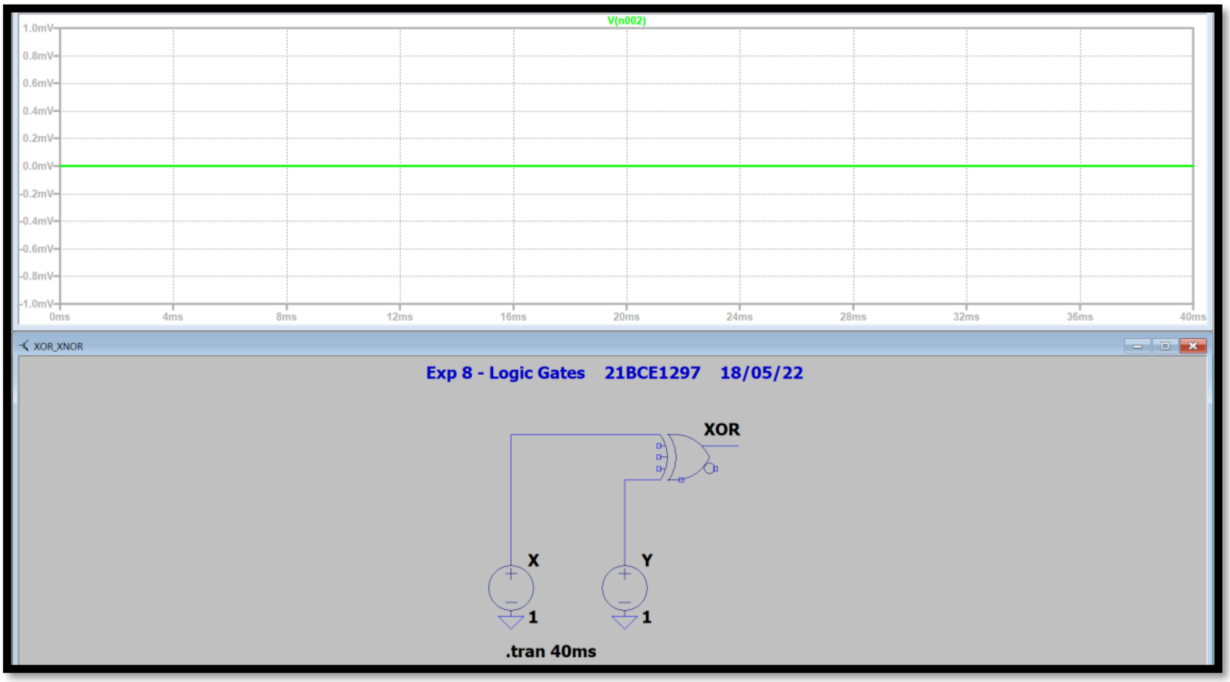
V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XOR
X
Y
0
0
.tran 40ms



V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XOR
X
Y
0
1
.tran 40ms

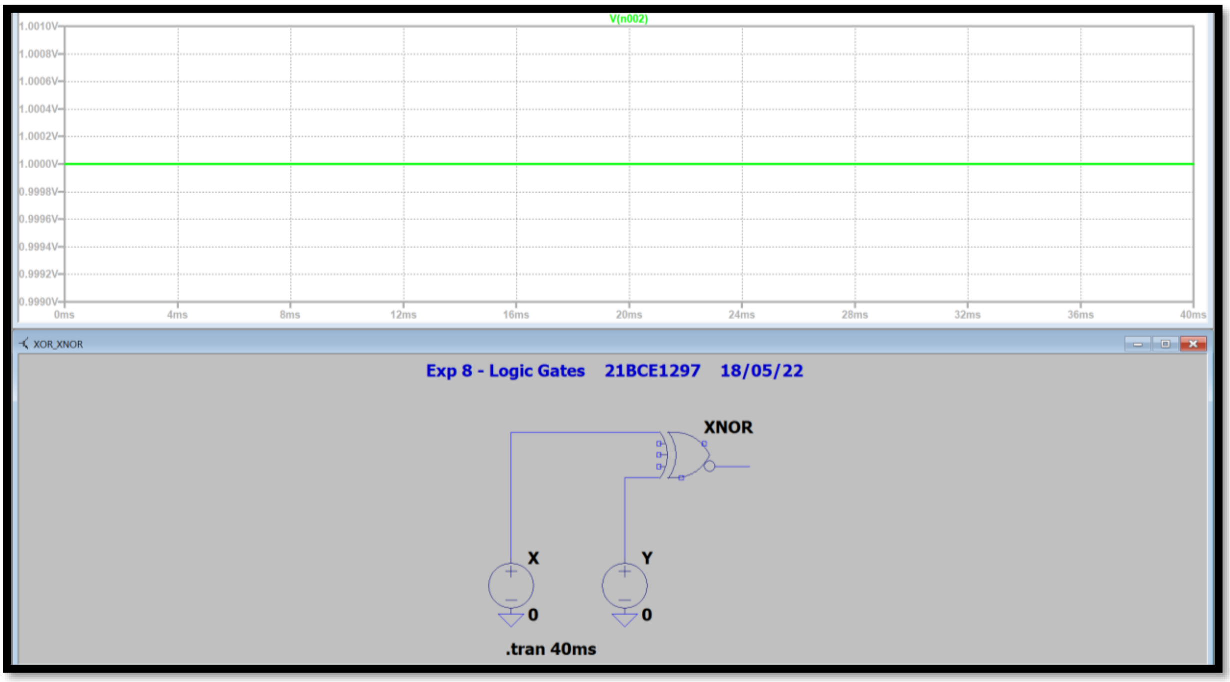


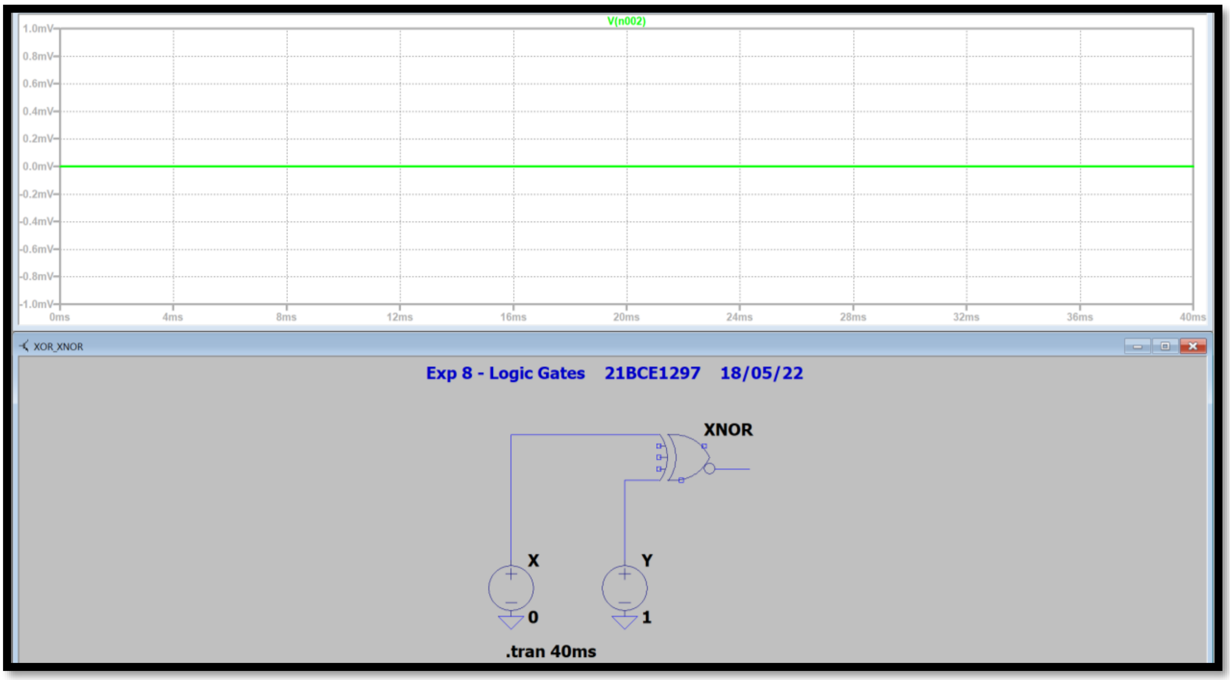
V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XOR
X
Y
1
0
.tran 40ms

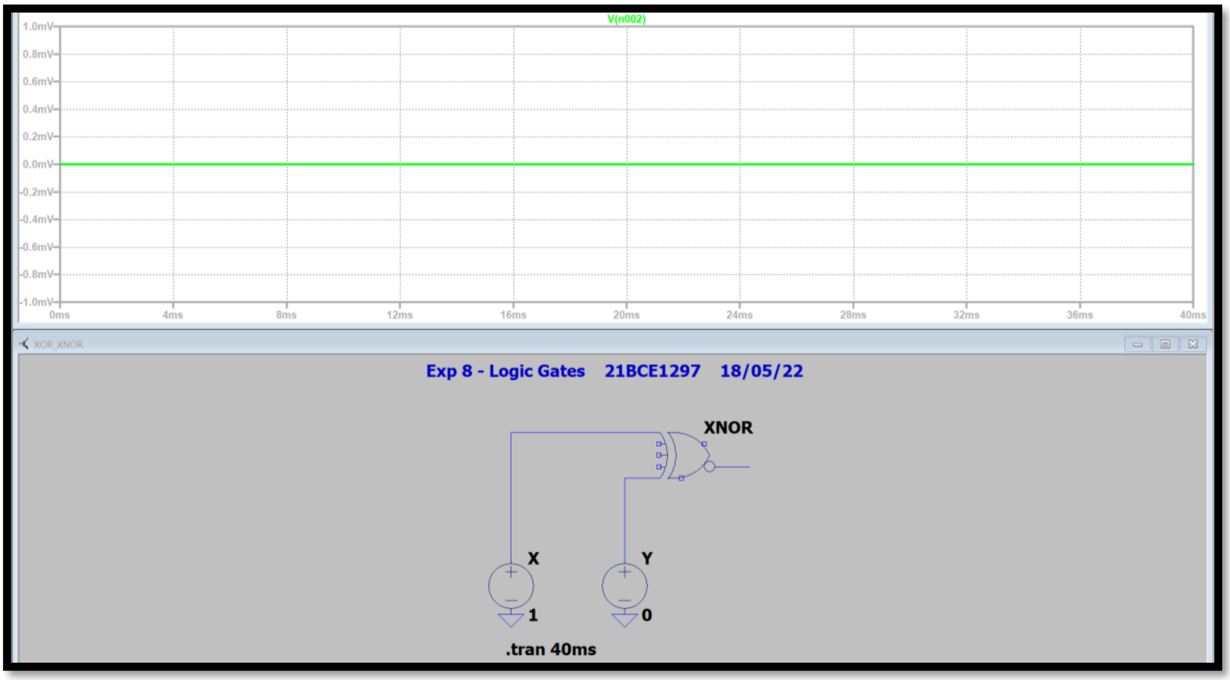


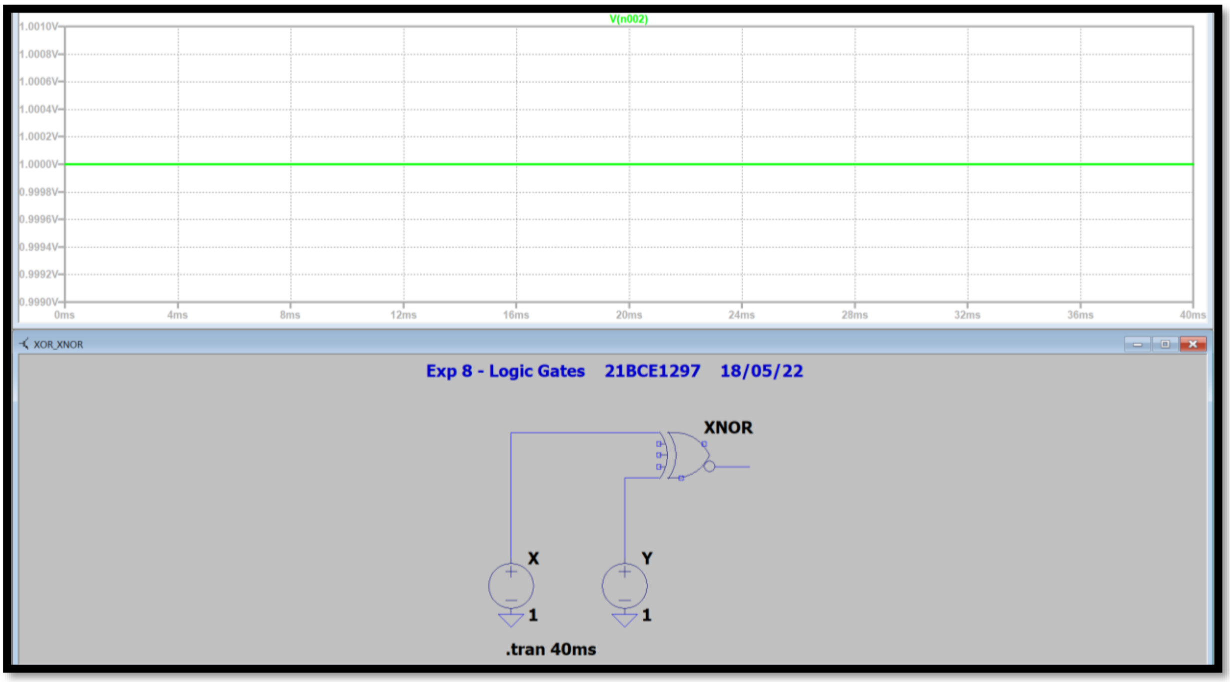
V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XOR
X
Y
1
1
.tran 40ms

9. XNOR Gate

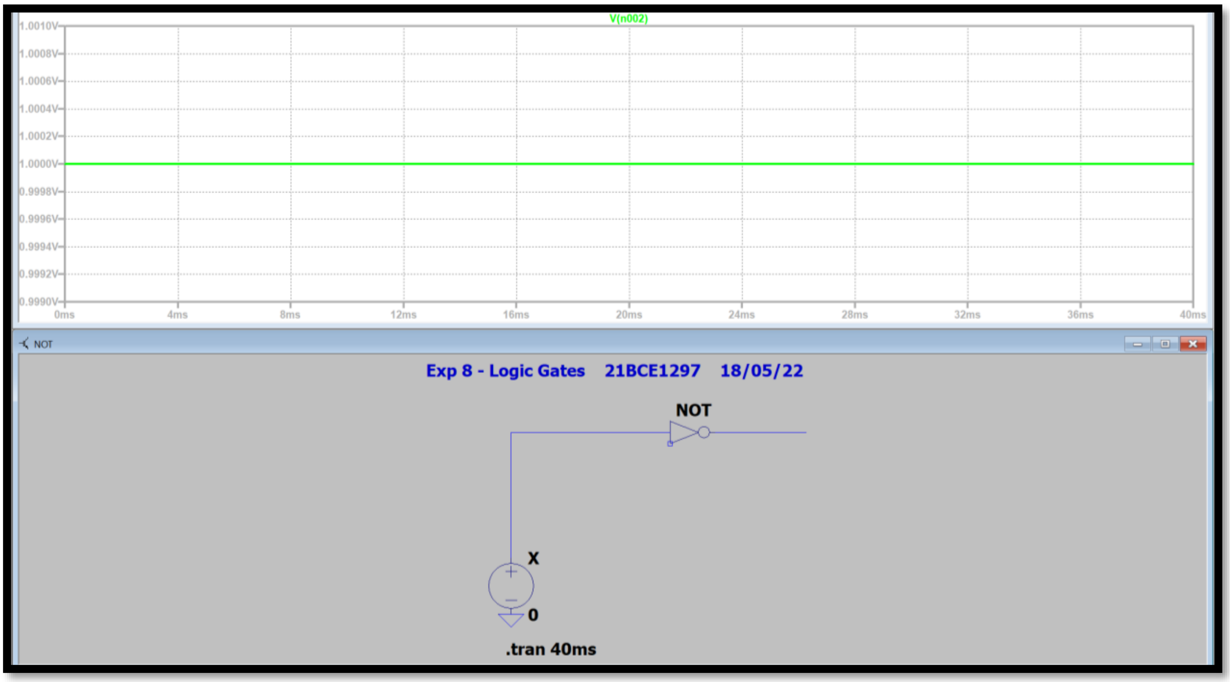

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XNOR
X
Y
0
0
.tran 40ms

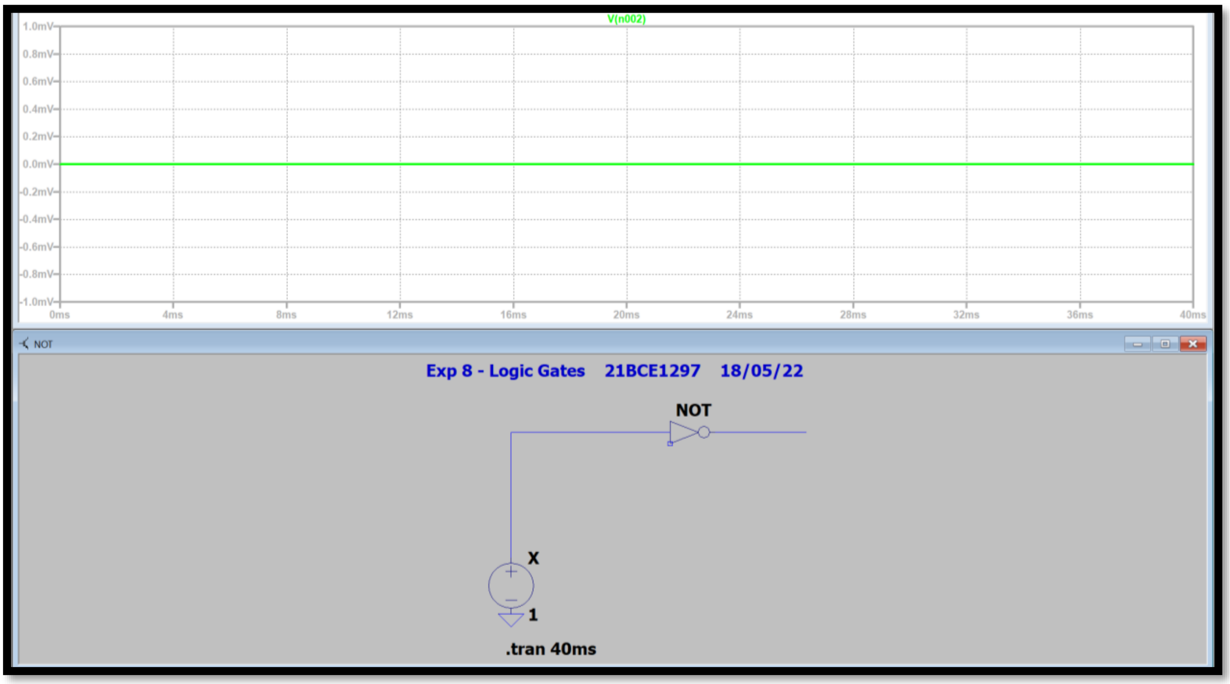

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XNOR
X
Y
0
1
.tran 40ms


V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XNOR
X
Y
1
0
.tran 40ms

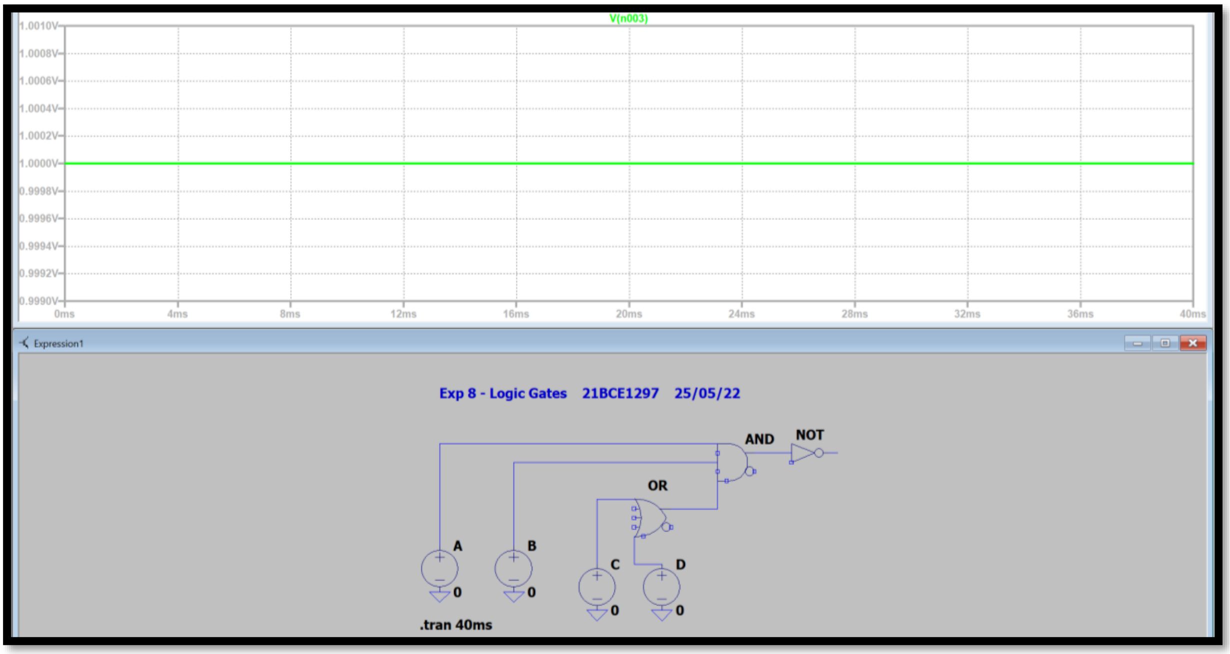

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XNOR
X
Y
1
1
.tran 40ms

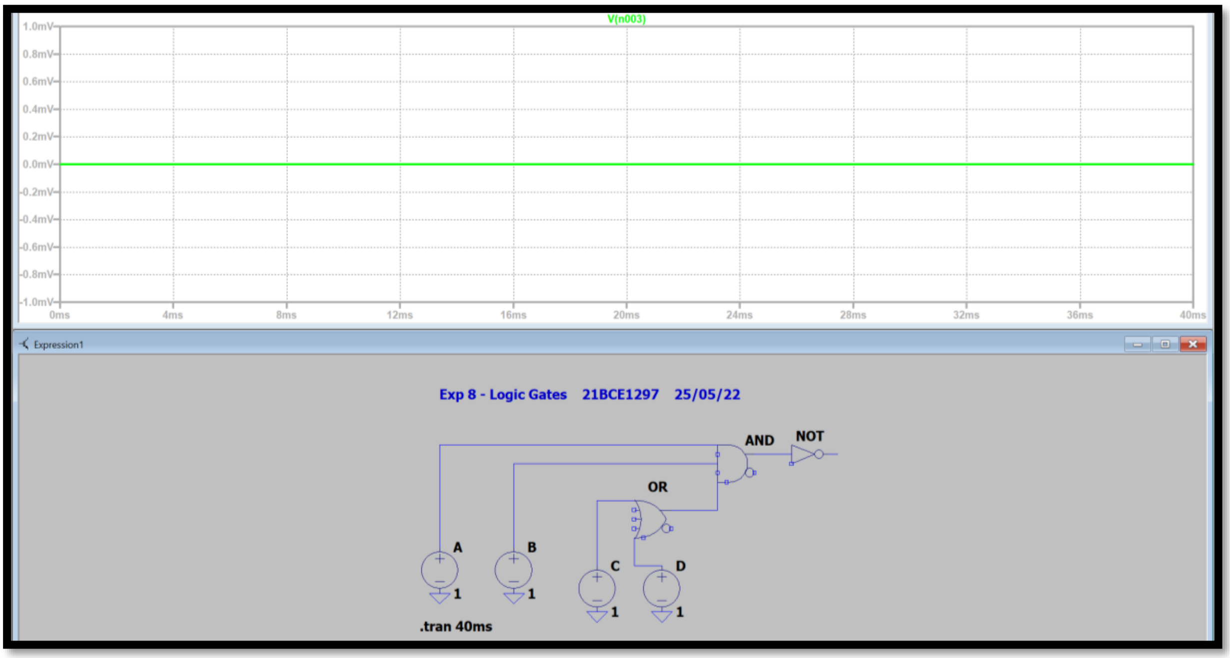
10.NOT Gate


V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
NOT
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOT
X
0
.tran 40ms

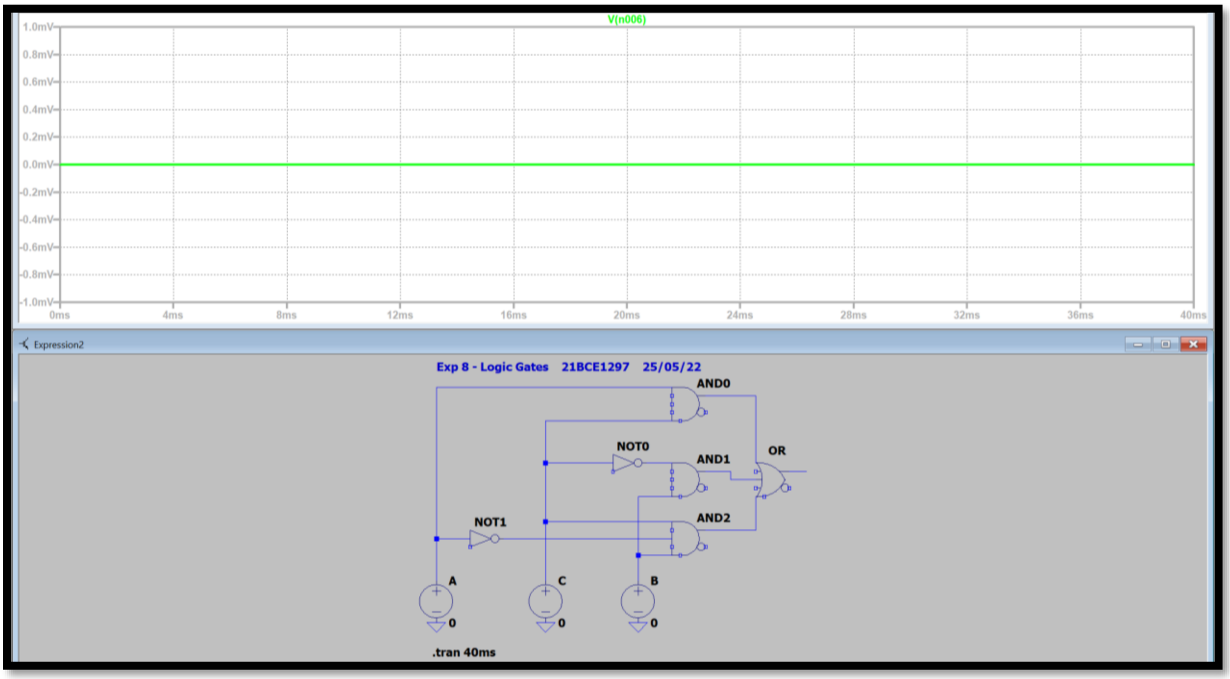

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
NOT
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOT
X
1
.tran 40ms

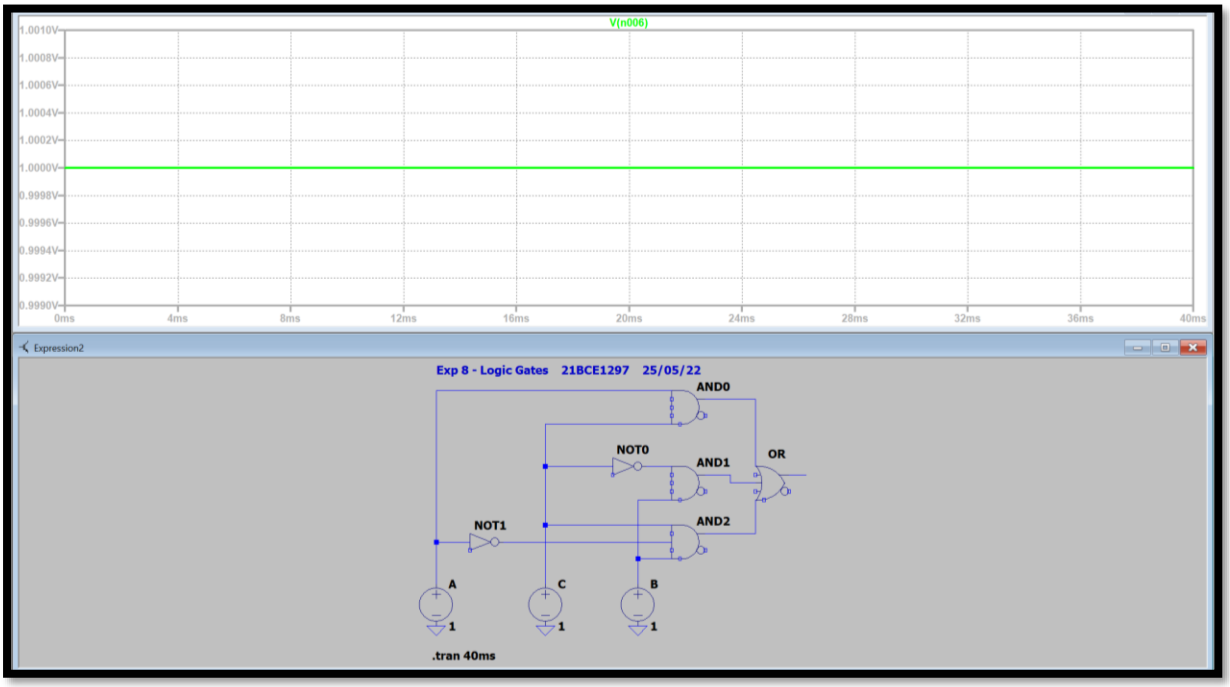
11. $x = \overline{A \cdot B(C + D)}$



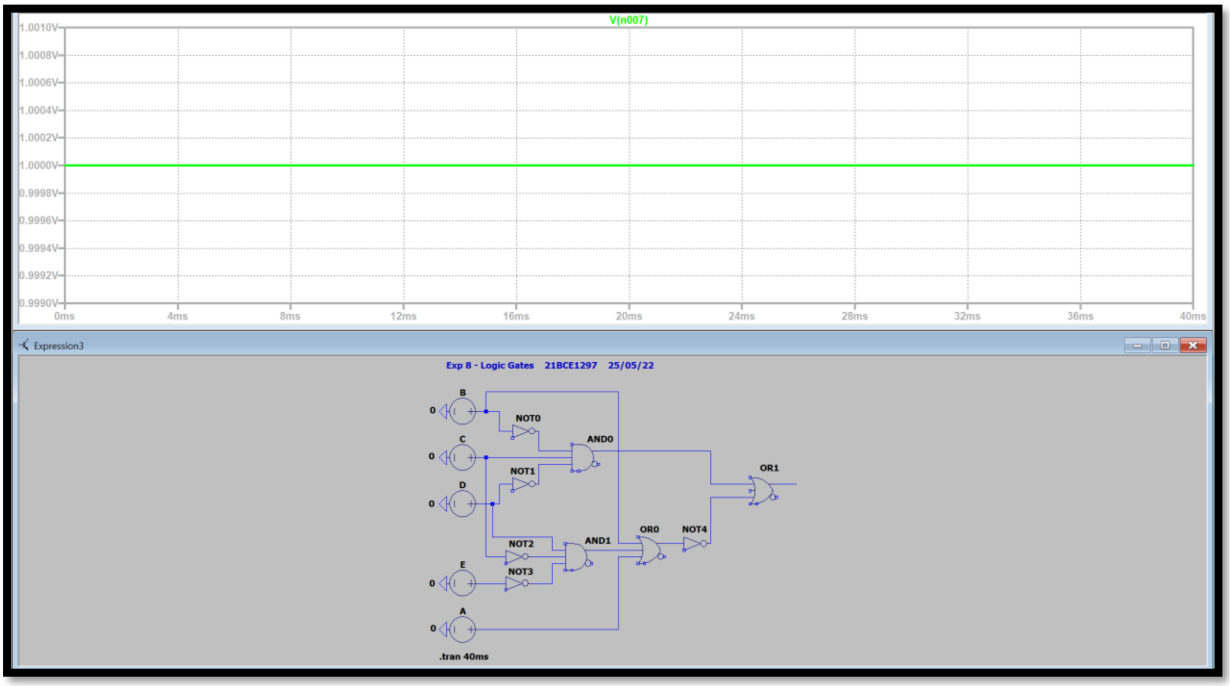


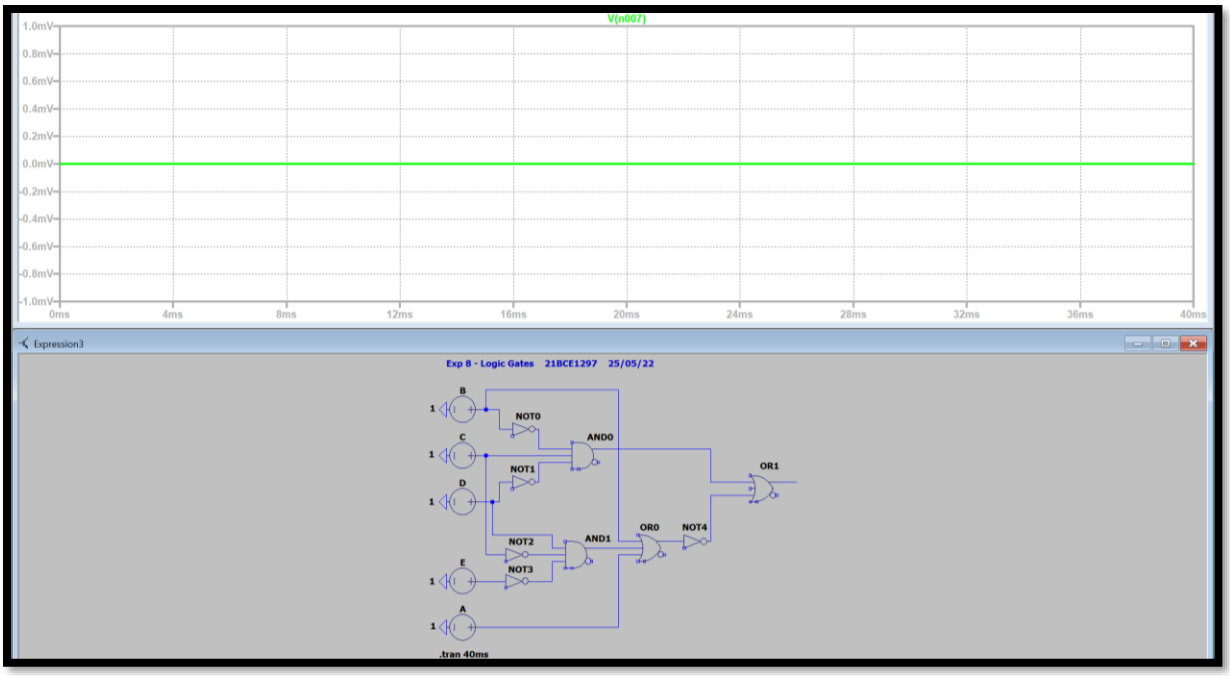
12. $y = AC + B\overline{C} + \overline{A}BC$





13. $z = \overline{A + B + \bar{C}D\bar{E}} + \bar{B}C\bar{D}$





Conclusion:

Hence, we can see that the truth table is verified for all Boolean gates and Boolean functions.

Inferences:

1. $A\ OR\ B = A + B$
2. $A\ AND\ B = A \cdot B$
3. $NOT\ A = \bar{A}$
4. $A\ NOR\ B = \overline{A + B}$
5. $A\ NAND\ B = \overline{A \cdot B}$
6. $A\ XOR\ B = A \cdot B + \overline{A \cdot B}$
7. $A\ XNOR\ B = \overline{A \cdot B + \overline{A \cdot B}}$

Reg. No. 21BCE1297   Name: Vidhi Shah   Date of Submission: 05/06/22

Experiment 10

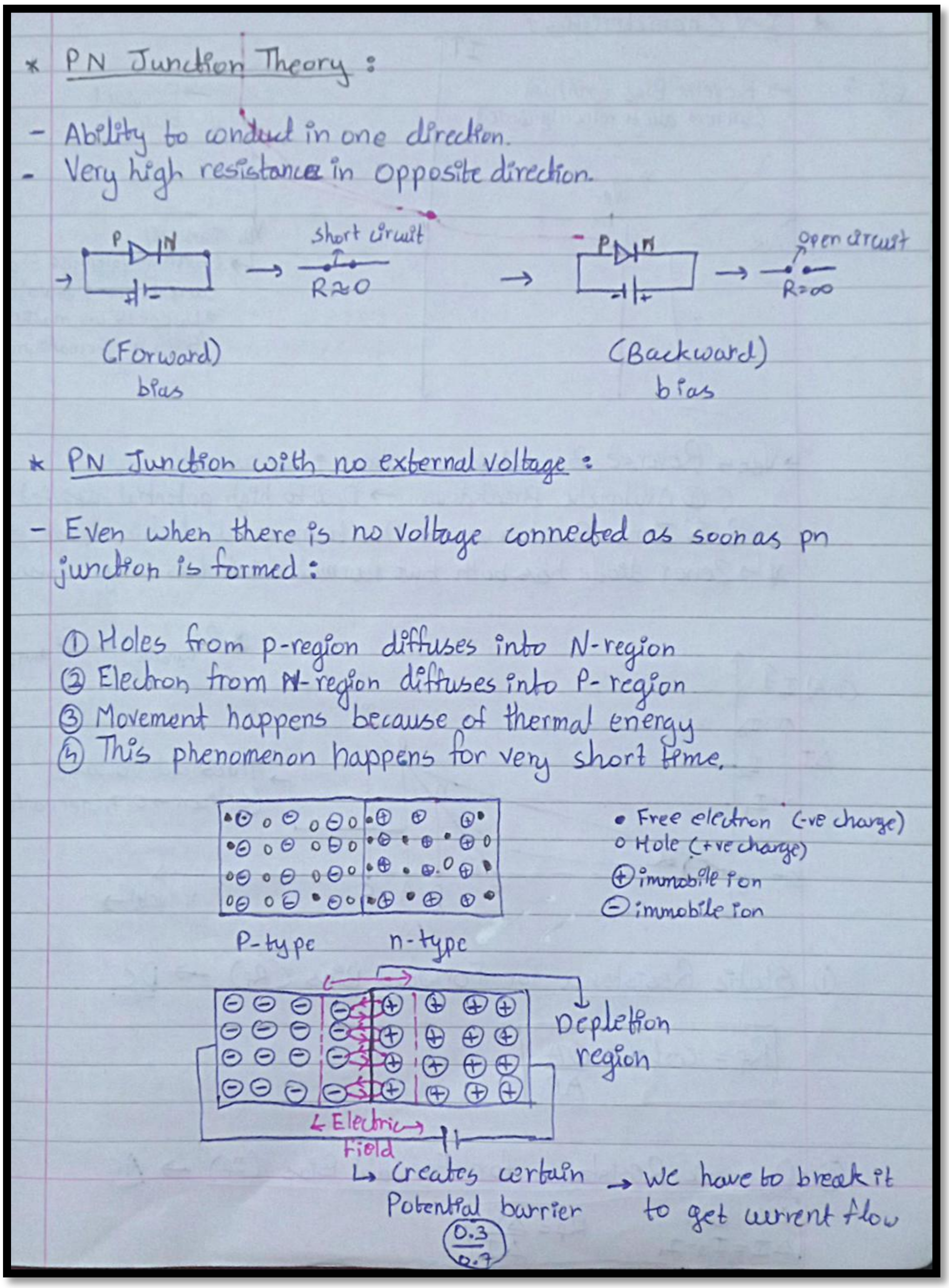
Aim:

Draw I-V characteristics graph for PN Junction diode and Zener Diode

Tools and Apparatus:

LTSpice, PN junction diode, Zener diode, Resistor, Voltmeter, Ammeter, Voltage Source

Theory and Design:



* PN Junction Theory :

- Ability to conduct in one direction.
- Very high resistance in opposite direction.

P N → short circuit R≈0 → P N → open circuit R=∞

(Forward) bias   (Backward) bias

* PN Junction with no external voltage :

- Even when there is no voltage connected as soon as pn junction is formed :

① Holes from p-region diffuses into N-region
② Electron from N-region diffuses into P-region
③ Movement happens because of thermal energy
④ This phenomenon happens for very short time.

• Free electron (-ve charge)
o Hole (+ve charge)
⊕ immobile ion
⊖ immobile ion

P-type   n-type

Depletion region

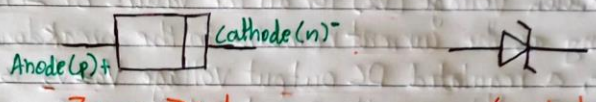
Electric Field

↳ Creates certain Potential barrier (0.3 / 0.7) → We have to break it to get current flow

• **Zener Diode:**

→ A zener diode is a special kind of diode which permits current to flow in the forward direction like a standard diode, but it will also allow it to flow in the reverse direction when the voltage is above the breakdown voltage or "zener voltage".

→ Zener diodes are designed so that their breakdown voltage is much lower.



Zener Diode   Symbol

→ In a standard diode, the Zener voltage is high, and the diode is permanently damaged if a reverse current above that value is allowed to pass through it.

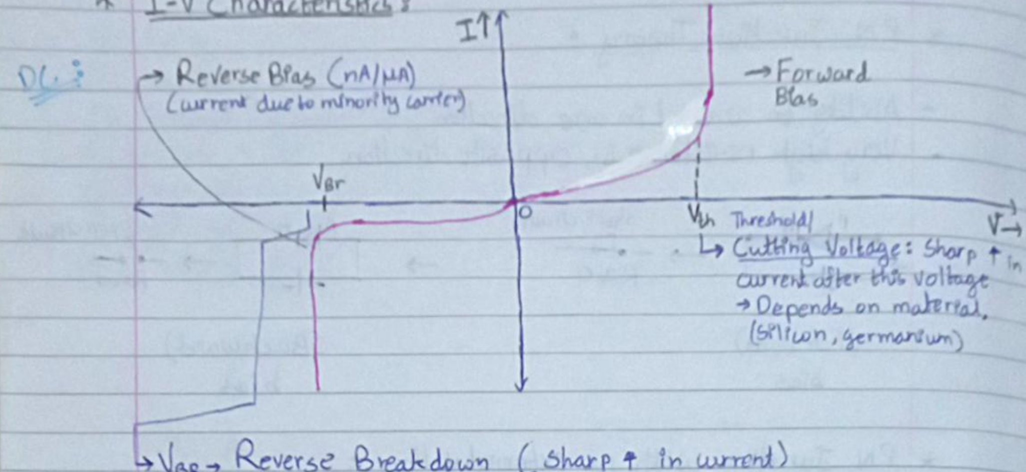
→ In the reverse bias direction, there is practically no reverse current flow until the breakdown voltage is reached.

→ When this occurs there is a sharp increase in reverse current.

→ Varying amount of reverse current can pass through the Zener diode without damaging it.

→ The breakdown voltage or Zener Voltage (V_z) across the diode remains relatively constant.

* I-V Characteristics:



↳ V_{BR} → Reverse Breakdown (Sharp ↑ in current)

① Avalanche Breakdown → Due to high potential applied

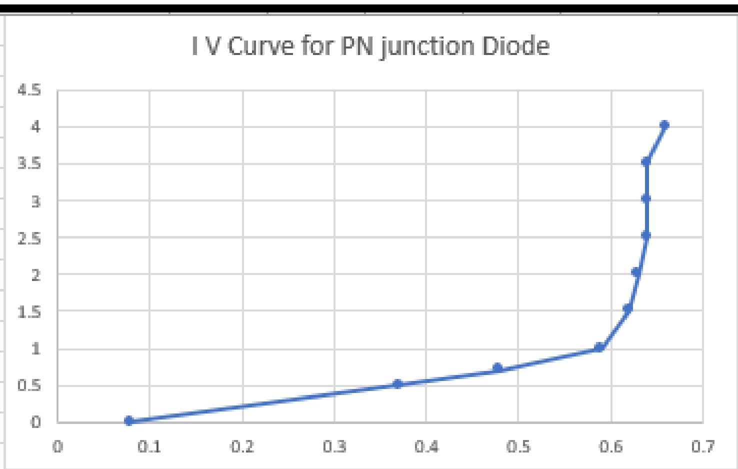
② Zener Breakdown → Due to increased electric field

* ↳ Zener diode has both but normal diode has only avalanche

Hardware Simulation Results:

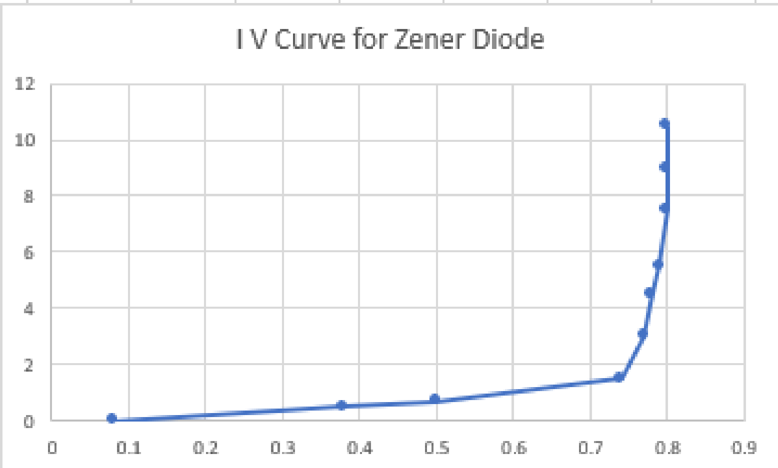
1) PN Junction

V	I
0.08	0
0.37	0.5
0.48	0.7
0.59	1
0.62	1.5
0.63	2
0.64	2.5
0.64	3
0.64	3.5
0.66	4

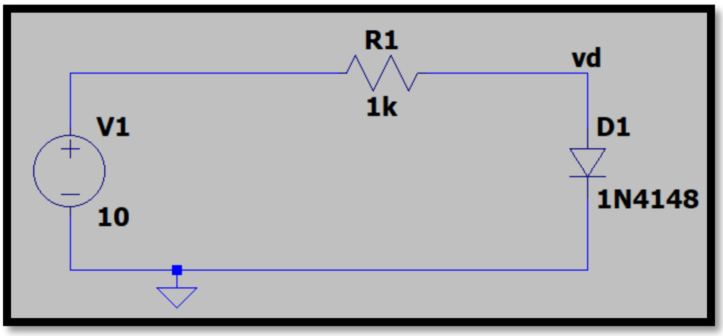


2) Zener Diode

V	I
0.08	0
0.38	0.5
0.5	0.7
0.74	1.5
0.77	3
0.78	4.5
0.79	5.5
0.8	7.5
0.8	9
0.8	10.5

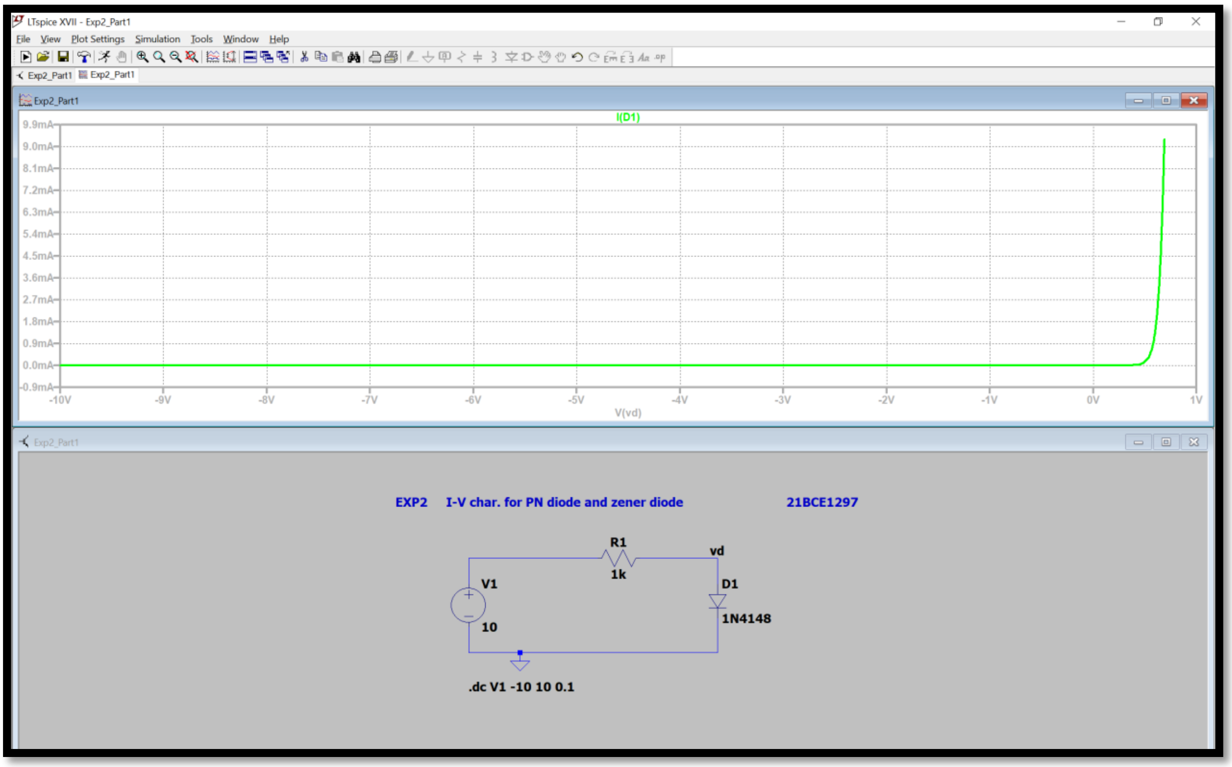


Circuit Diagram:

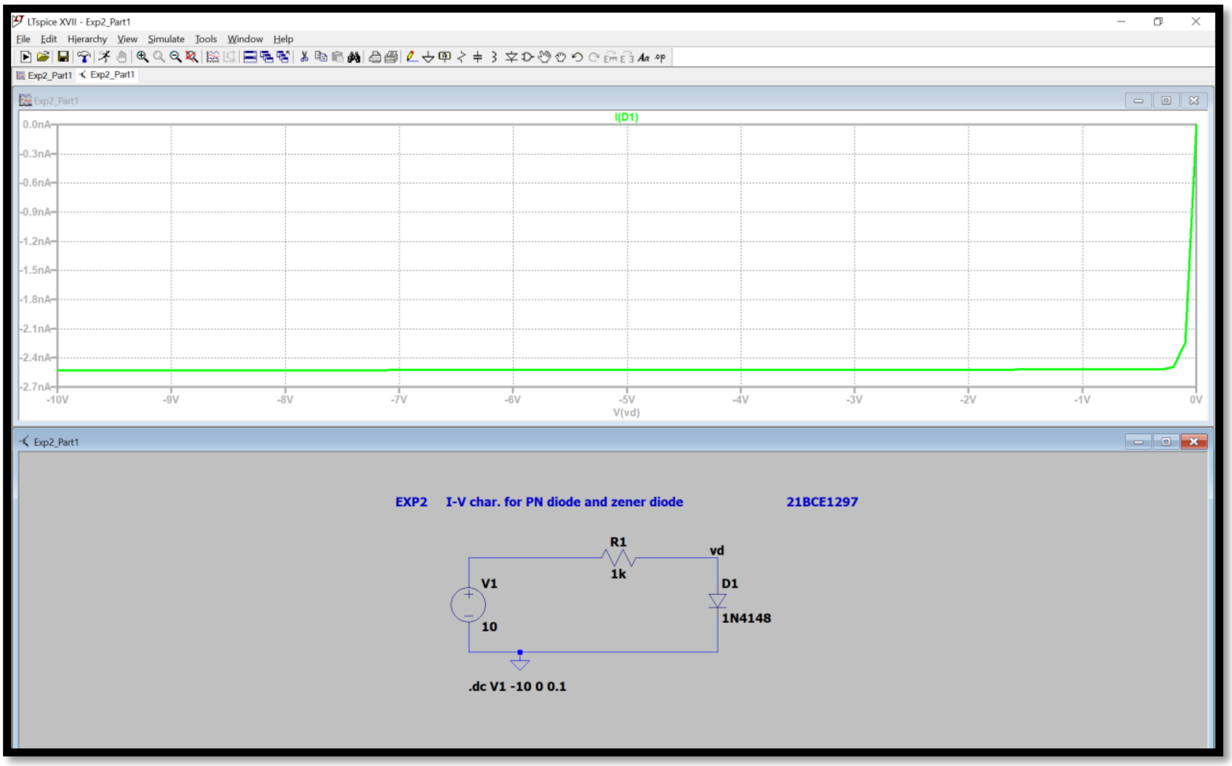


Software Simulation Results:

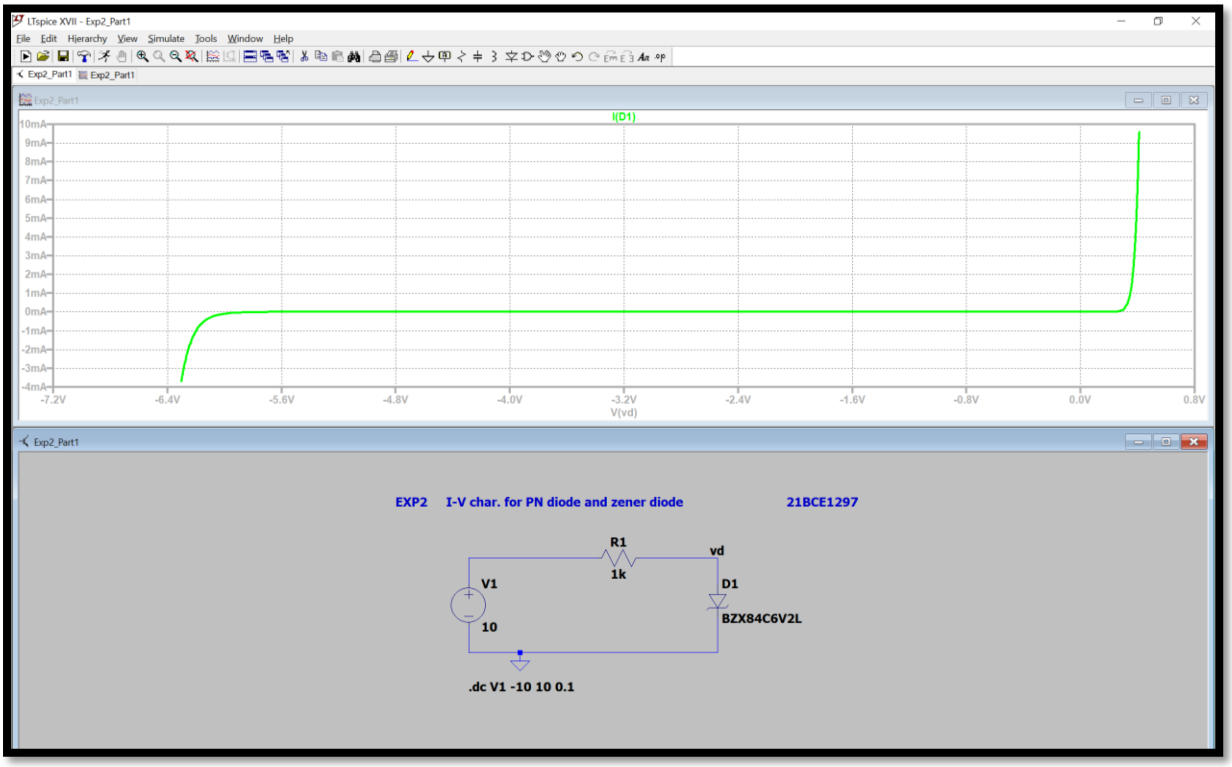
1) Forward Bias



2) Reverse Bias



3) Zener Diode



Conclusion:

I-V Characteristics curve of PN Junction diode and Zener diode is verified.

Inferences:

1. Threshold voltage and breakdown voltage for Zener diode and PN junction diode is clearly visible.
2. Connect all wires properly and tightly.
3. Label vd properly