Reg. No. 21BCE1297 Name: Vidhi Shah Date of Practical: 18/04/22 & 25/04/22

Experiment 9

Aim:

To simulate and verify basic Logic Gates and Boolean Functions.

Tools and Apparatus:

DC Voltage Source, AND, NAND, OR, NOR, NOT, XOR and XNOR gates.

Theory:

Truth Tables:

Input		Output					
A	**B**	**AND**	**NAND**	**OR**	**NOR**	**XOR**	**XNOR**
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

Input	Output
X	**NOT**
0	1
1	0

1. $x = \overline{A \cdot B(C + D)}$

Input				Output
A	**B**	**C**	**D**	x
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
1	0	0	0	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	1
0	1	1	0	1

Input				Output
A	**B**	**C**	**D**	x
0	1	0	1	1
0	0	1	1	1
1	1	1	0	0
1	0	1	1	1
1	1	0	1	0
0	1	1	1	1
1	1	1	1	0

2. $y = AC + B\overline{C} + \overline{A}BC$

Input			Output
A	**B**	**C**	y
0	0	0	0
1	0	0	0
0	1	0	1
0	0	1	0
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1

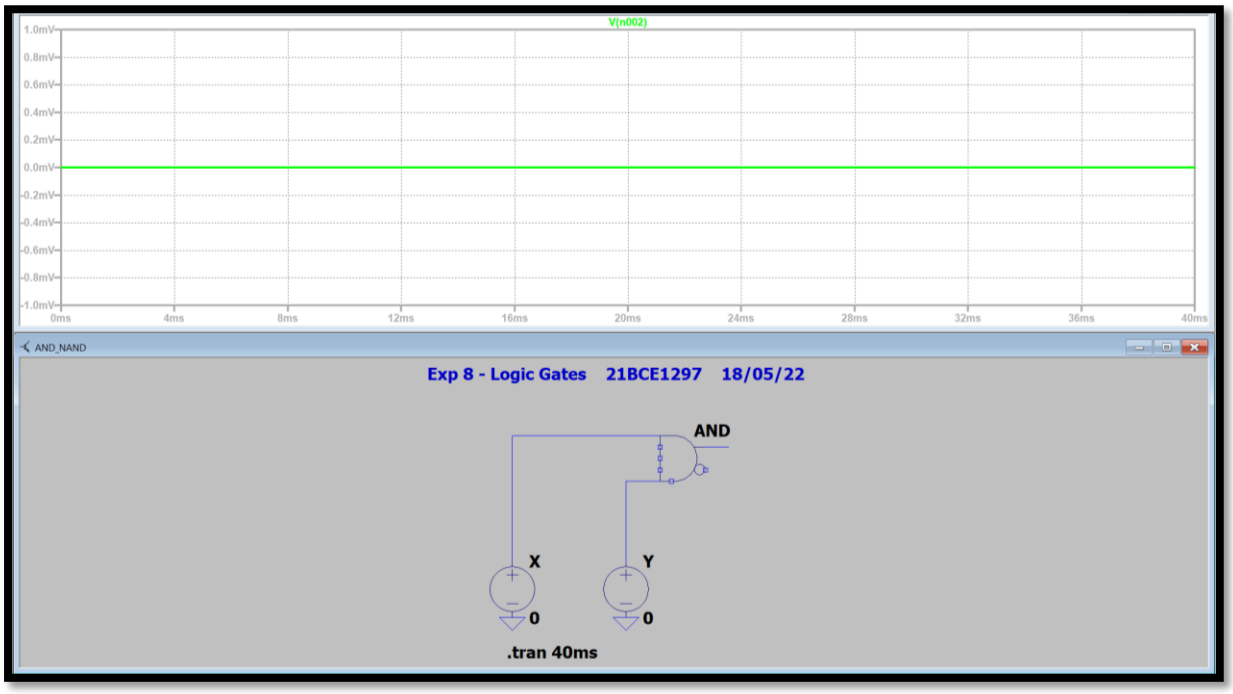
3. $z = \overline{A + B + \overline{C}D\overline{E}} + \overline{B}C\overline{D}$

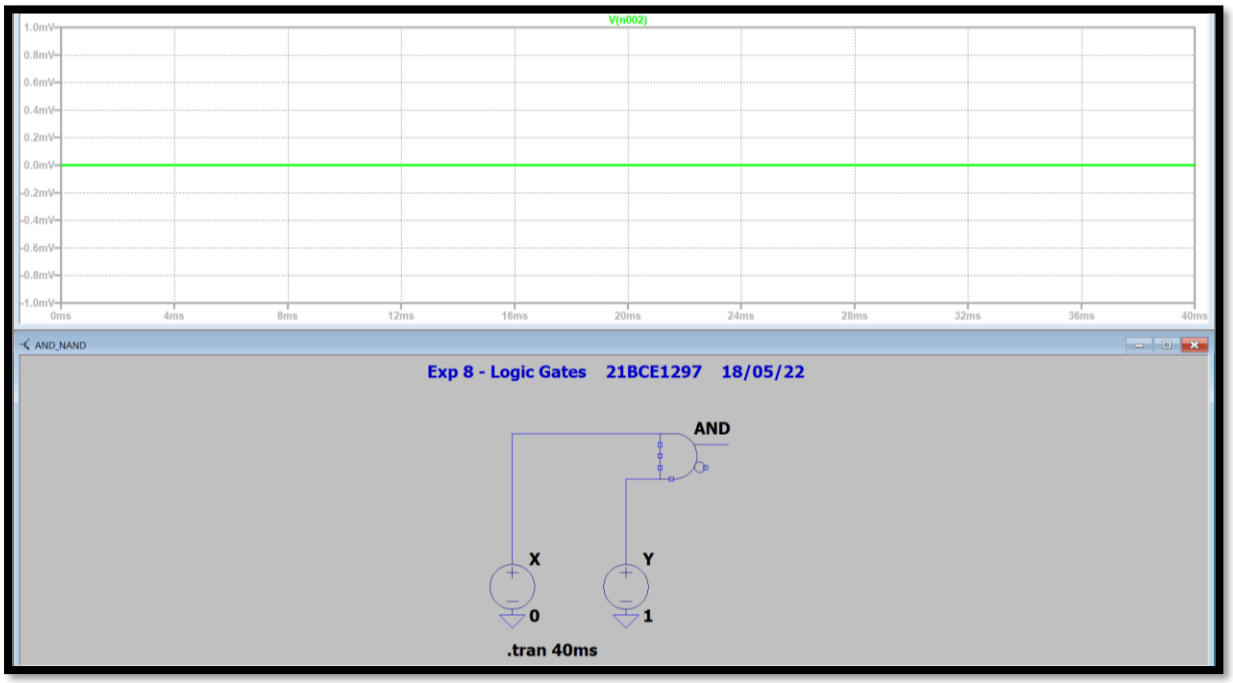
Input					Output
A	**B**	**C**	**D**	**E**	z
0	0	0	0	0	1
1	0	0	0	0	0
0	1	0	0	0	0
0	0	1	0	0	1
0	0	0	1	0	0
0	0	0	0	1	1
1	1	0	0	0	0
1	0	1	0	0	1
1	0	0	1	0	0
1	0	0	0	1	0
0	1	1	0	0	0
0	1	0	1	0	0
0	1	0	0	1	0
0	0	1	1	0	1
0	0	1	0	1	1
0	0	0	1	1	1
1	1	1	0	0	0
1	1	0	1	0	0
1	1	0	0	1	0
1	0	1	1	0	0
1	0	1	0	1	1

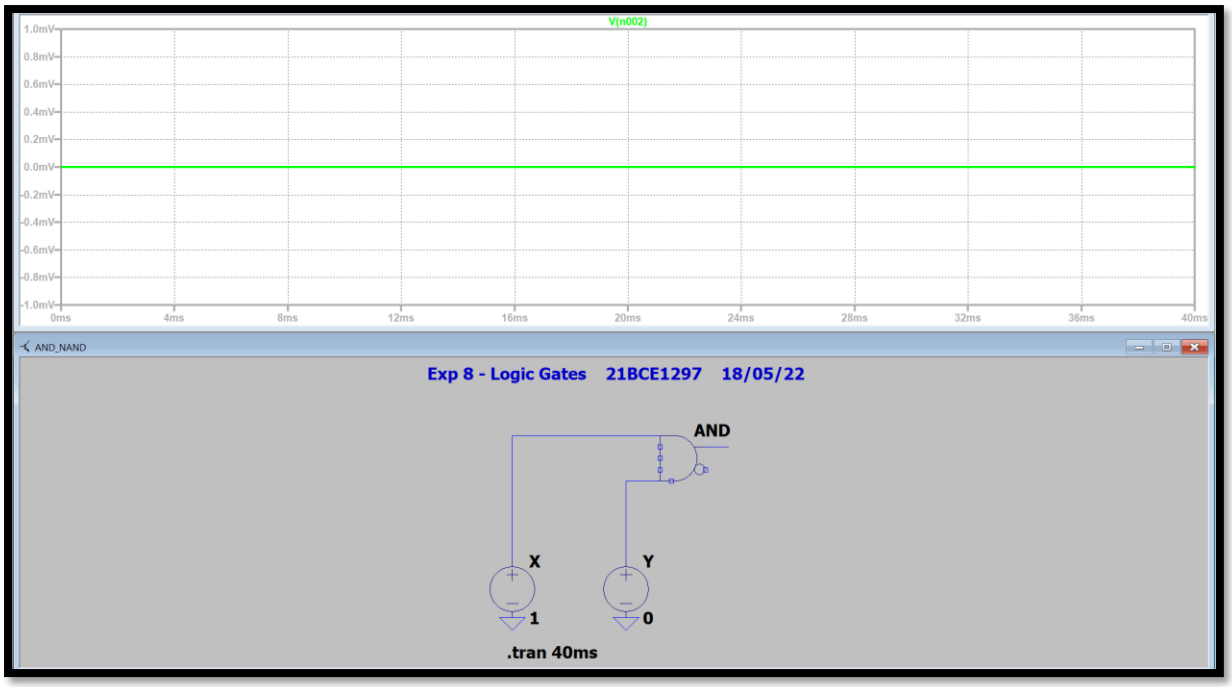
Input					Output
A	**B**	**C**	**D**	**E**	z
1	0	0	1	1	0
0	1	1	1	0	0
0	1	1	0	1	0
0	1	0	1	1	0
0	0	1	1	1	1
1	1	1	1	0	0
1	1	1	0	1	0
1	1	0	1	1	0
1	0	1	1	1	0
0	1	1	1	1	0
1	1	1	1	1	0

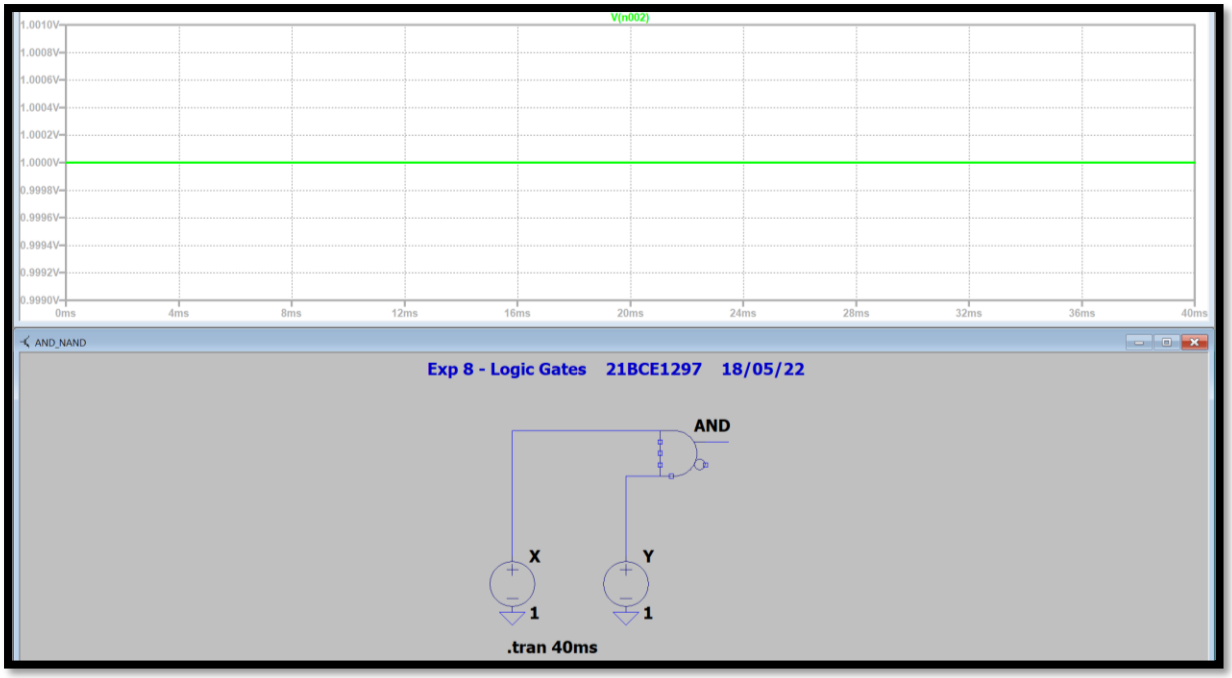
Simulation Results:

4. AND Gate

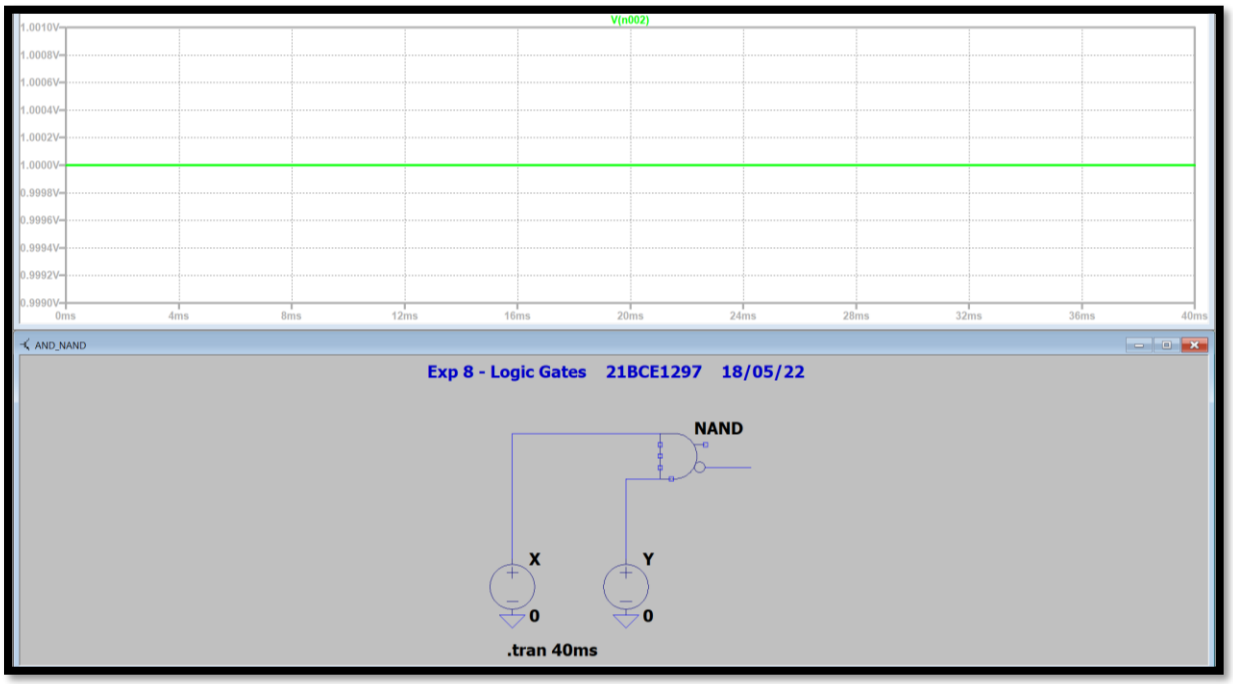


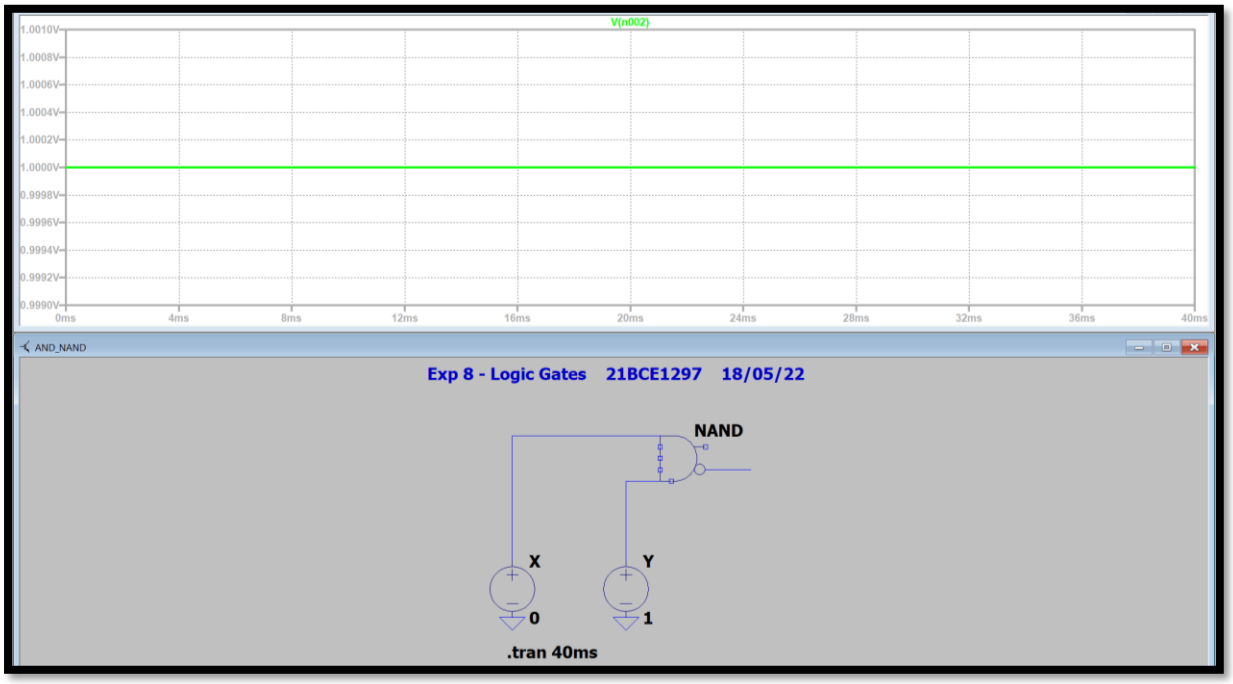


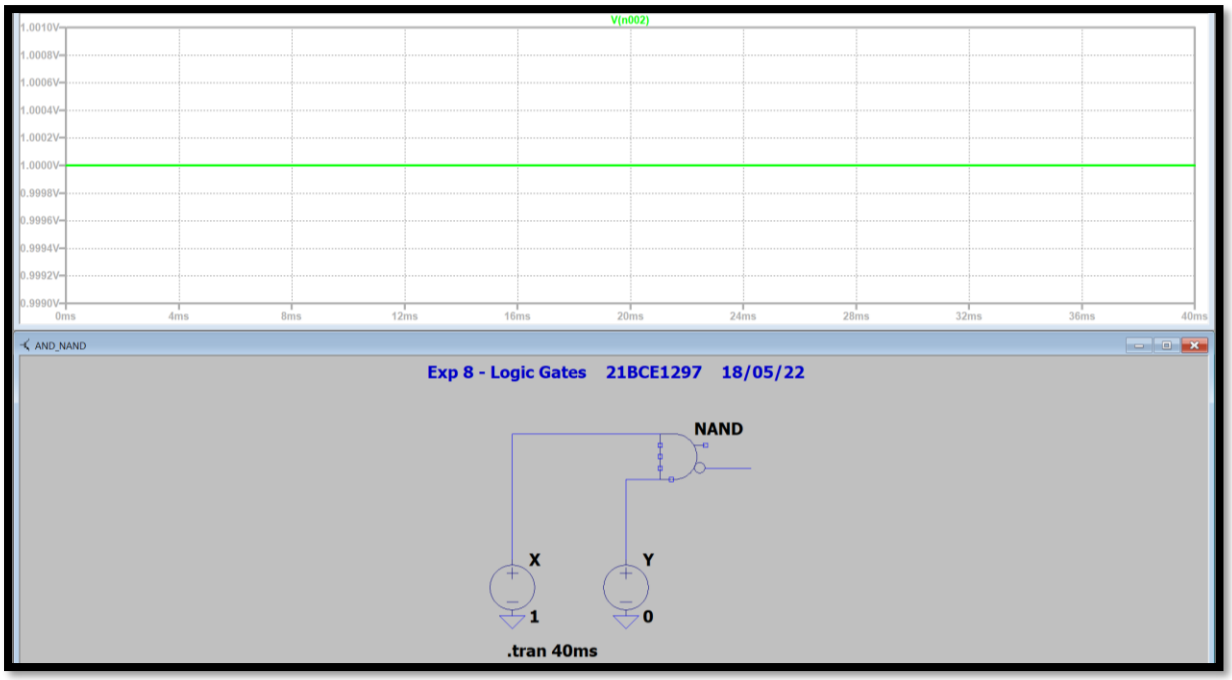

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
AND
X
Y
1
0
.tran 40ms

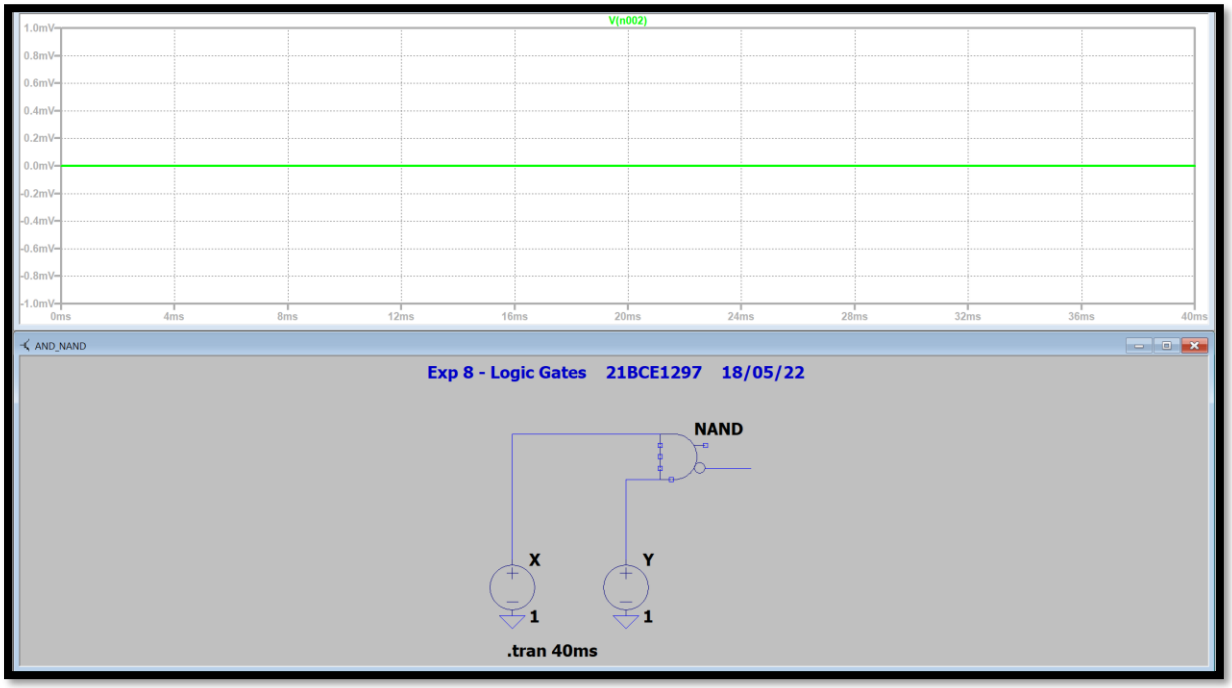

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
AND
X
Y
1
1
.tran 40ms

5. NAND Gate

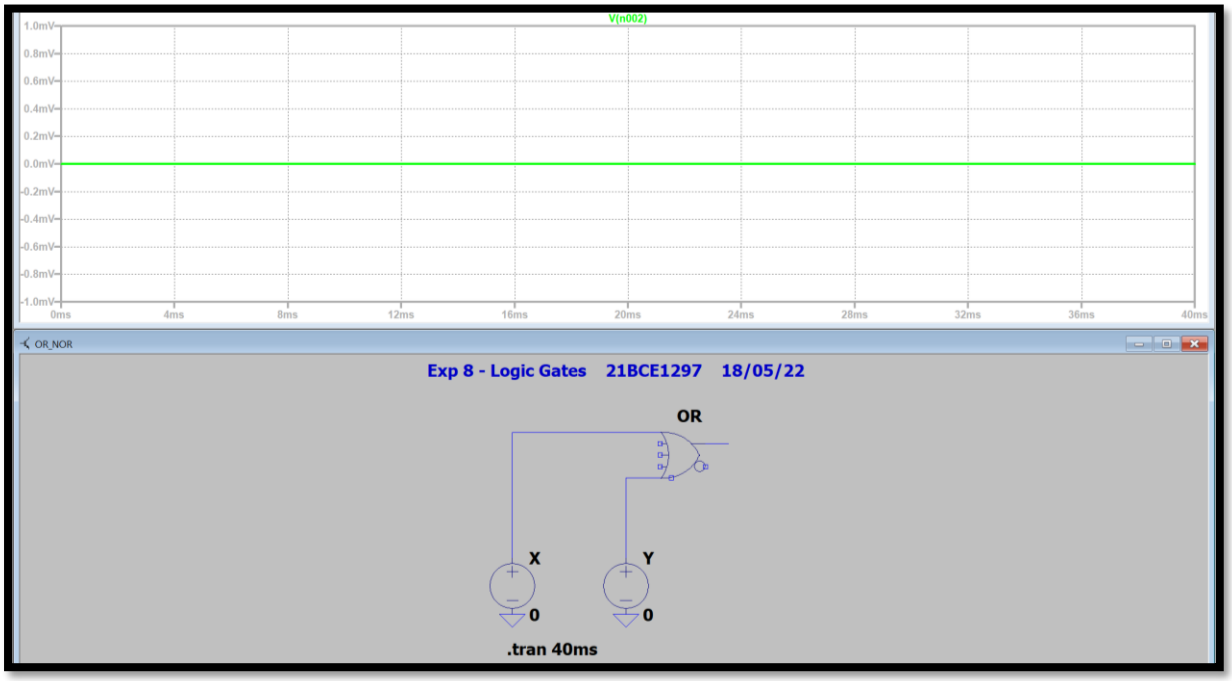

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
NAND
X
Y
0
0
.tran 40ms

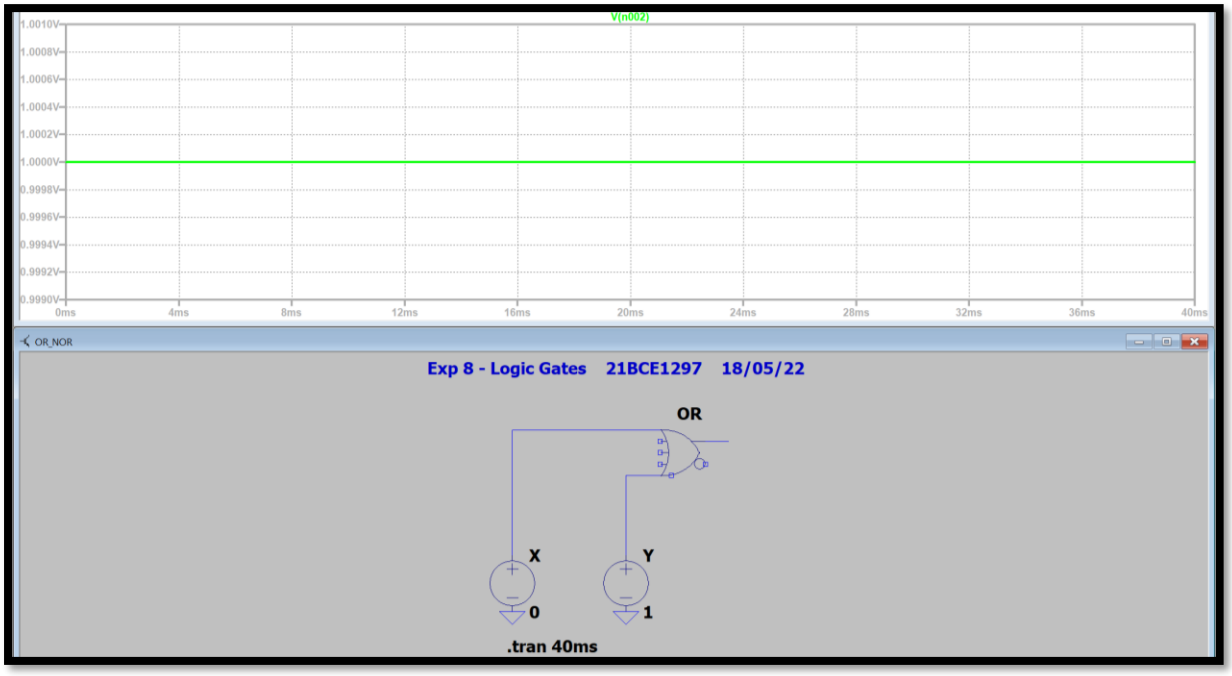

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
NAND
X
Y
0
1
.tran 40ms

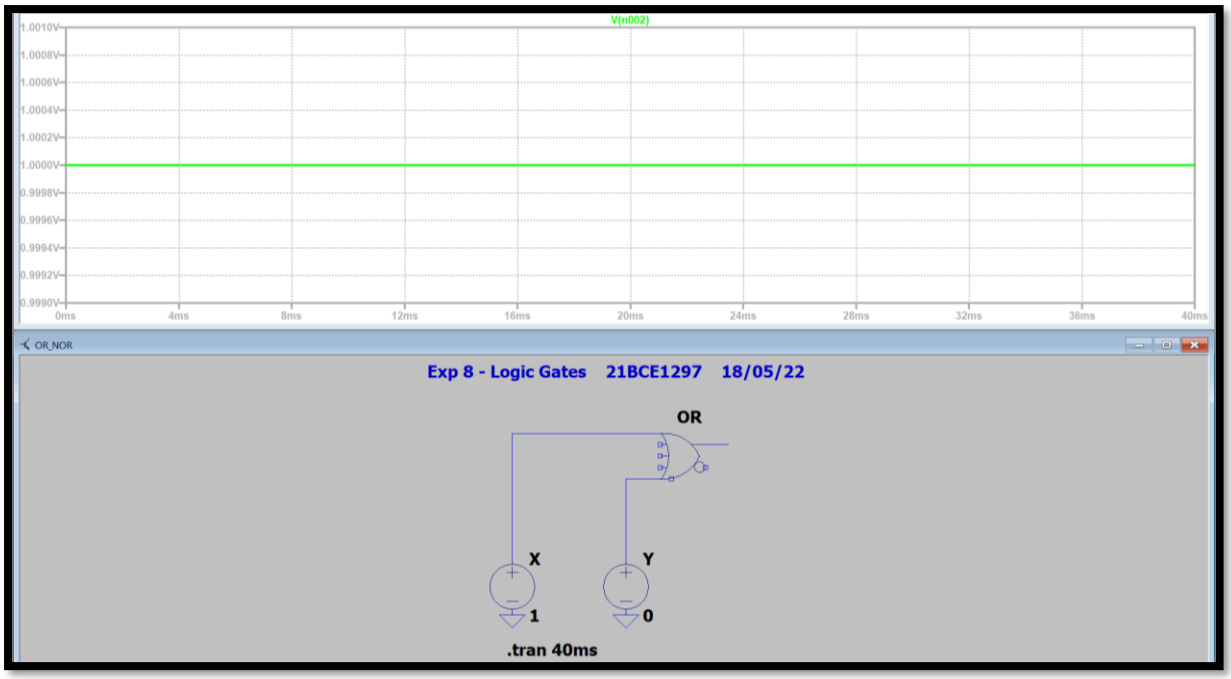

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
NAND
X
Y
1
0
.tran 40ms

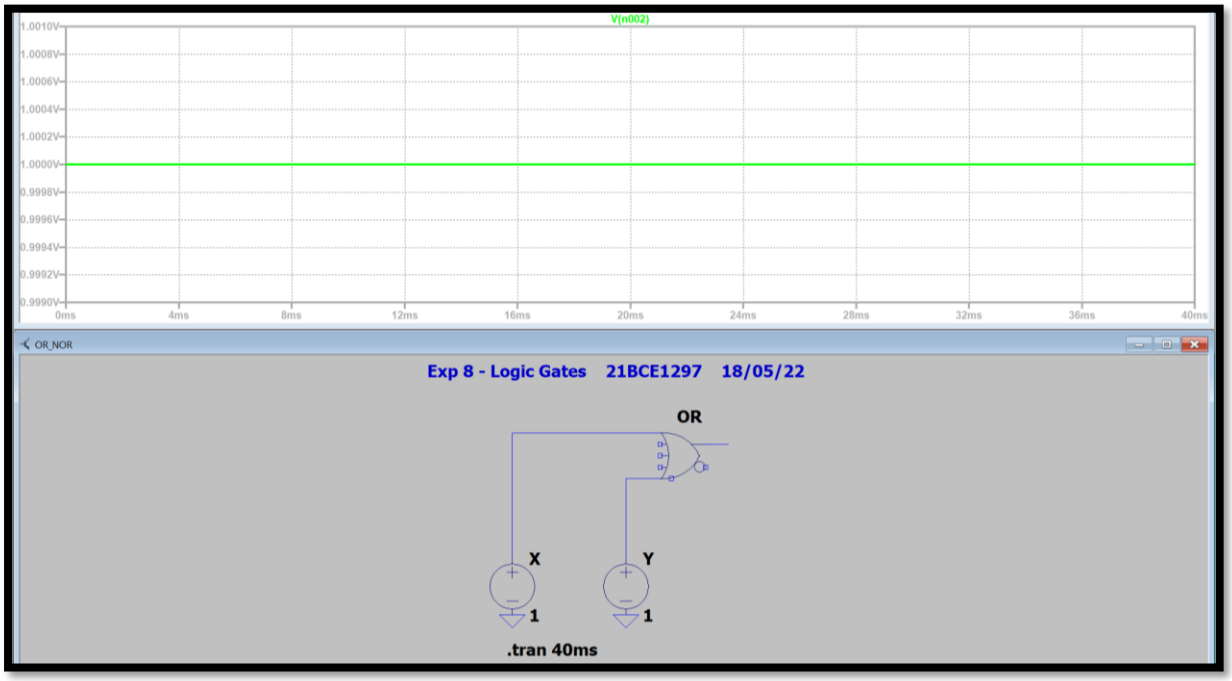

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
AND_NAND
Exp 8 - Logic Gates 21BCE1297 18/05/22
NAND
X
Y
1
1
.tran 40ms

6. OR Gate

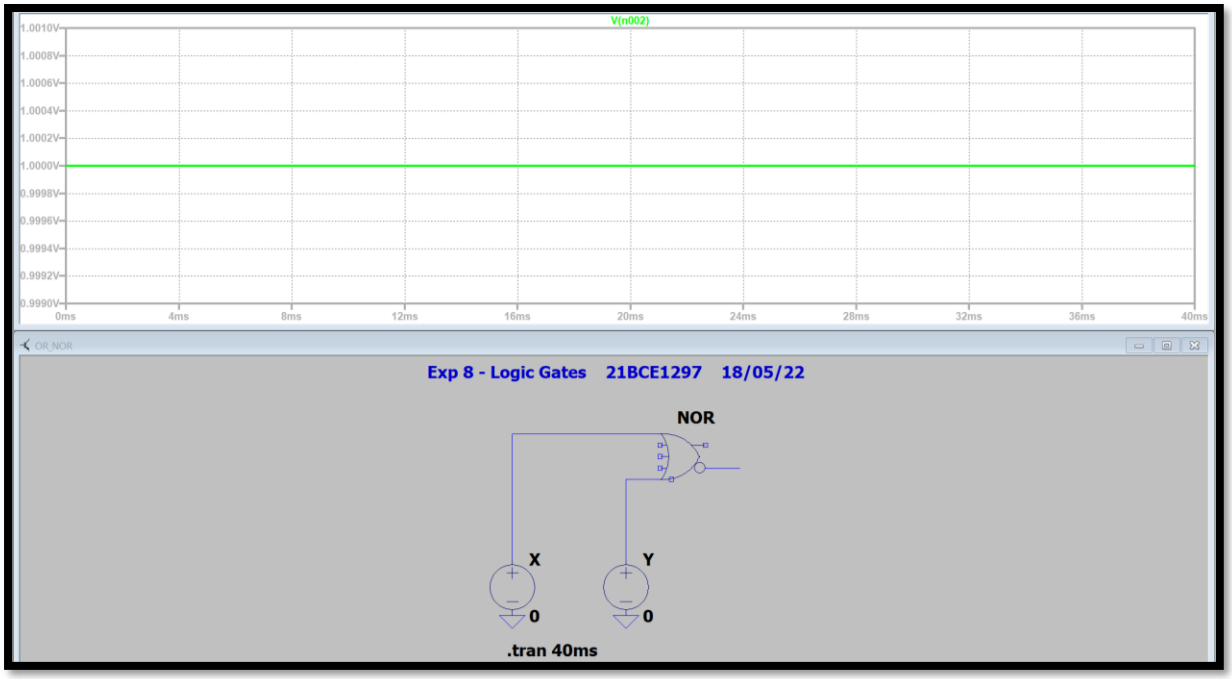

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
OR
X
Y
0
0
.tran 40ms

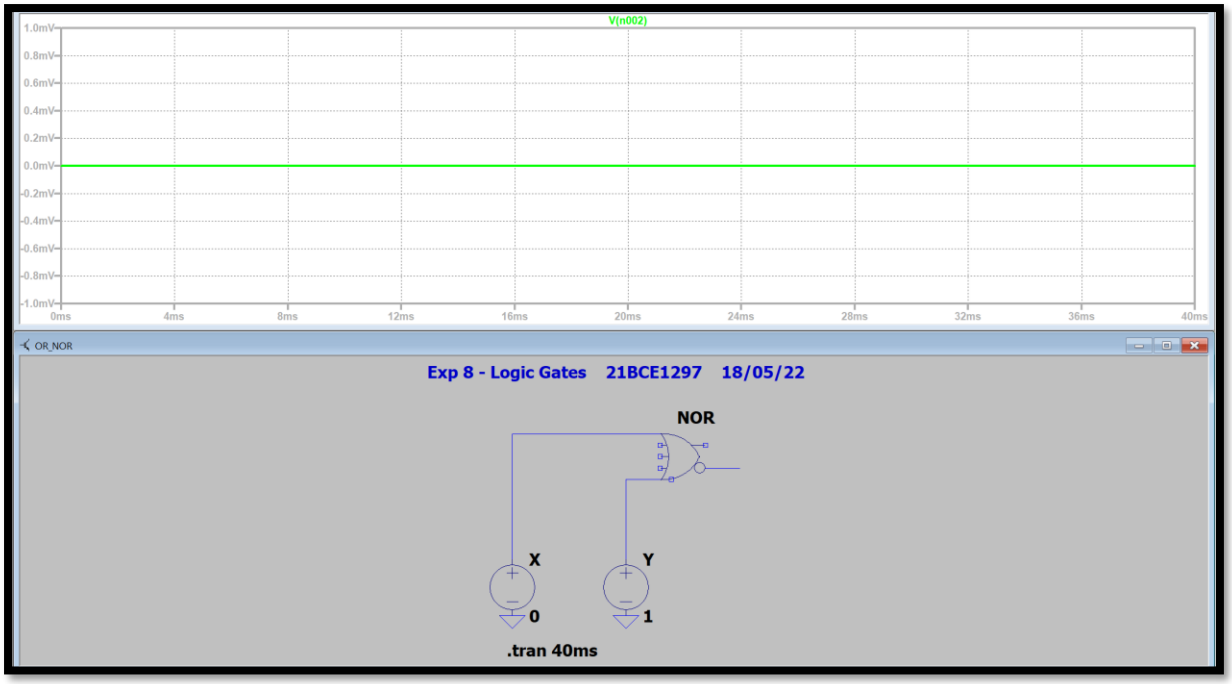

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
OR
X
Y
0
1
.tran 40ms

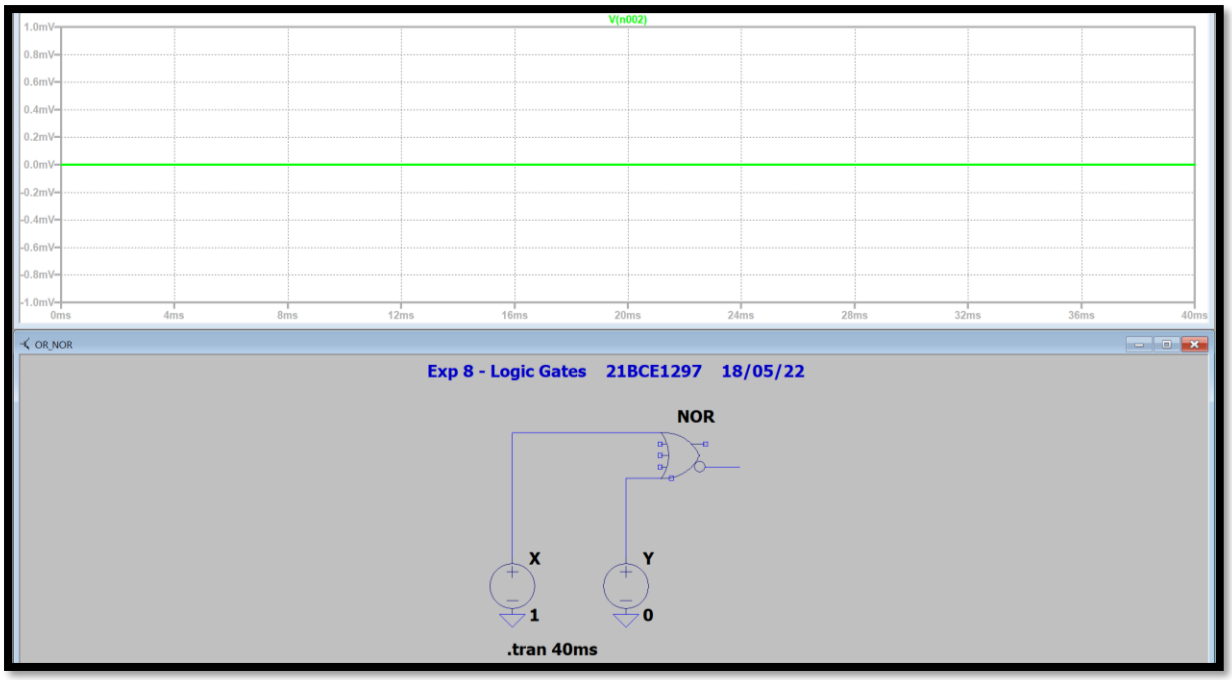

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
OR
X
Y
1
0
.tran 40ms

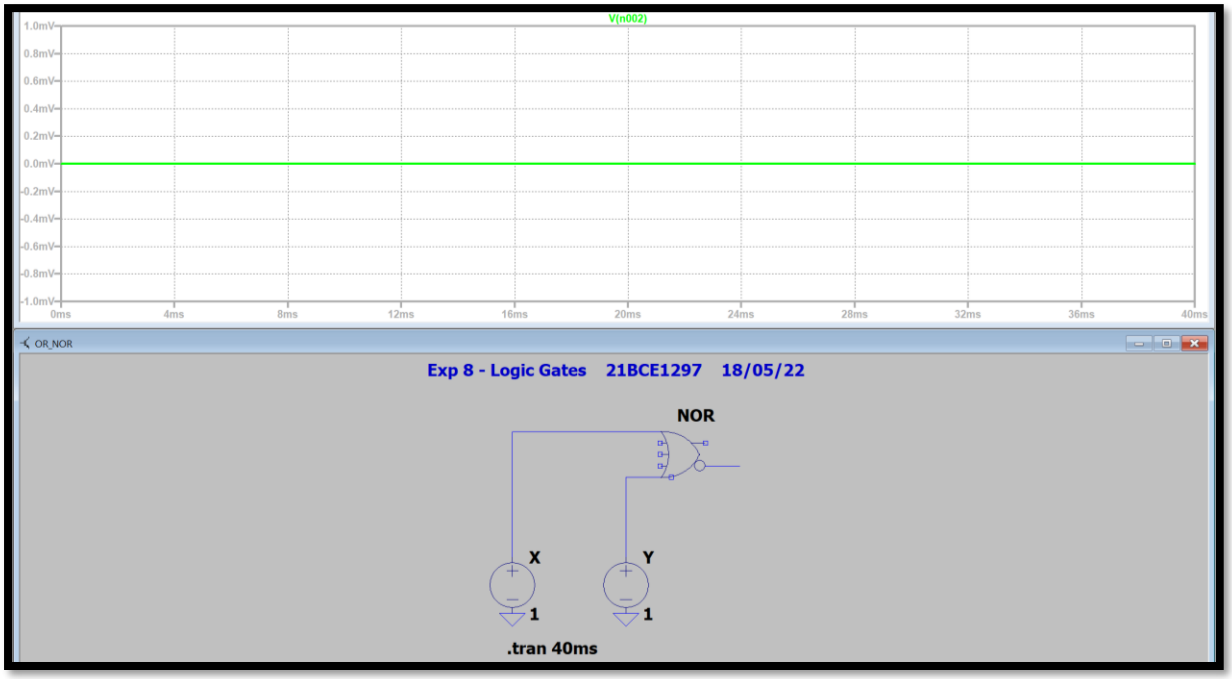

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
OR
X
Y
1
1
.tran 40ms

7. NOR Gate

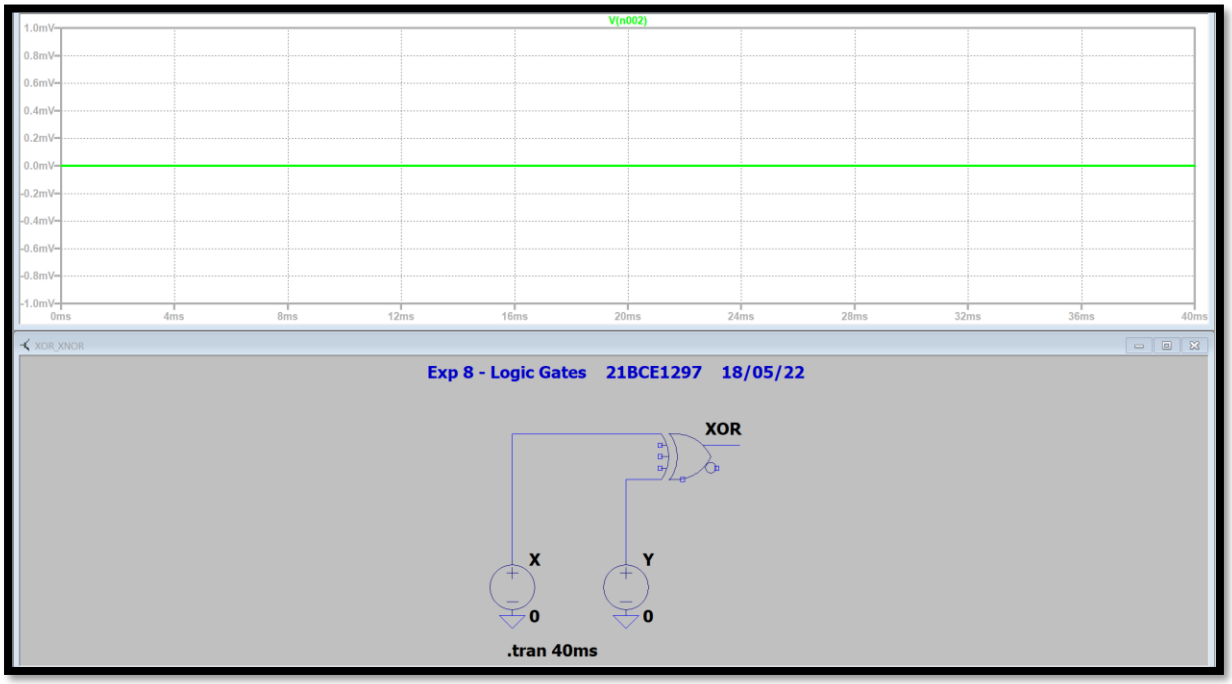

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOR
X
Y
0
0
.tran 40ms

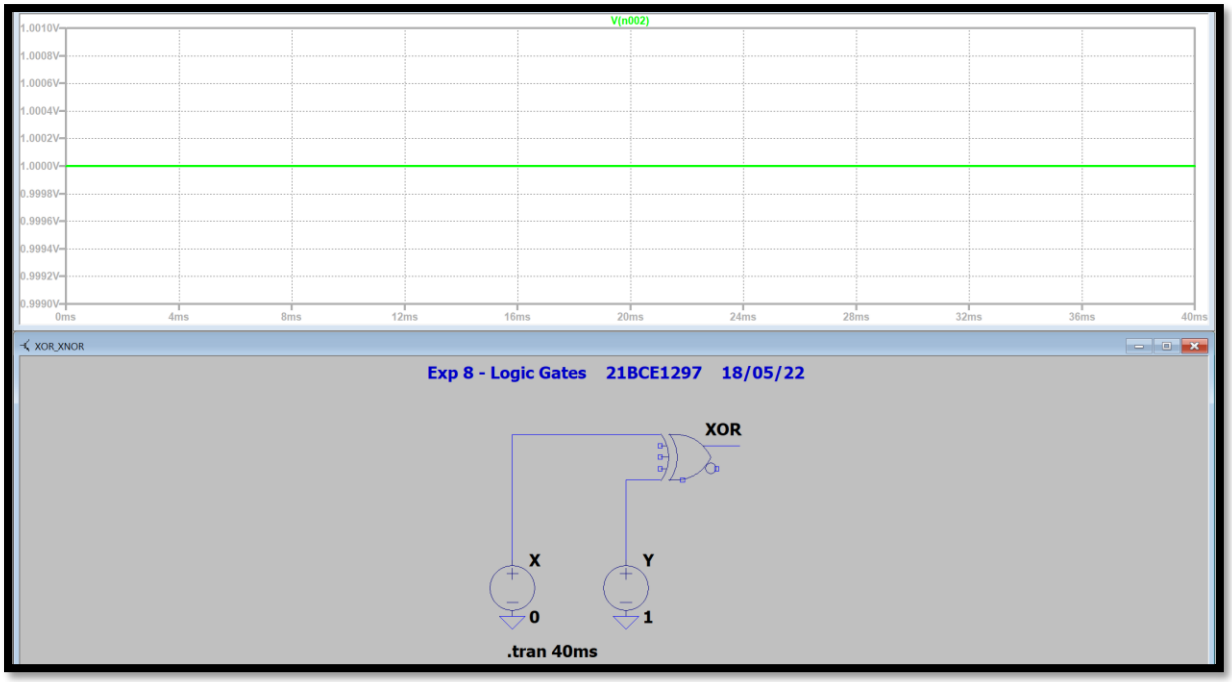

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOR
X
Y
0
1
.tran 40ms

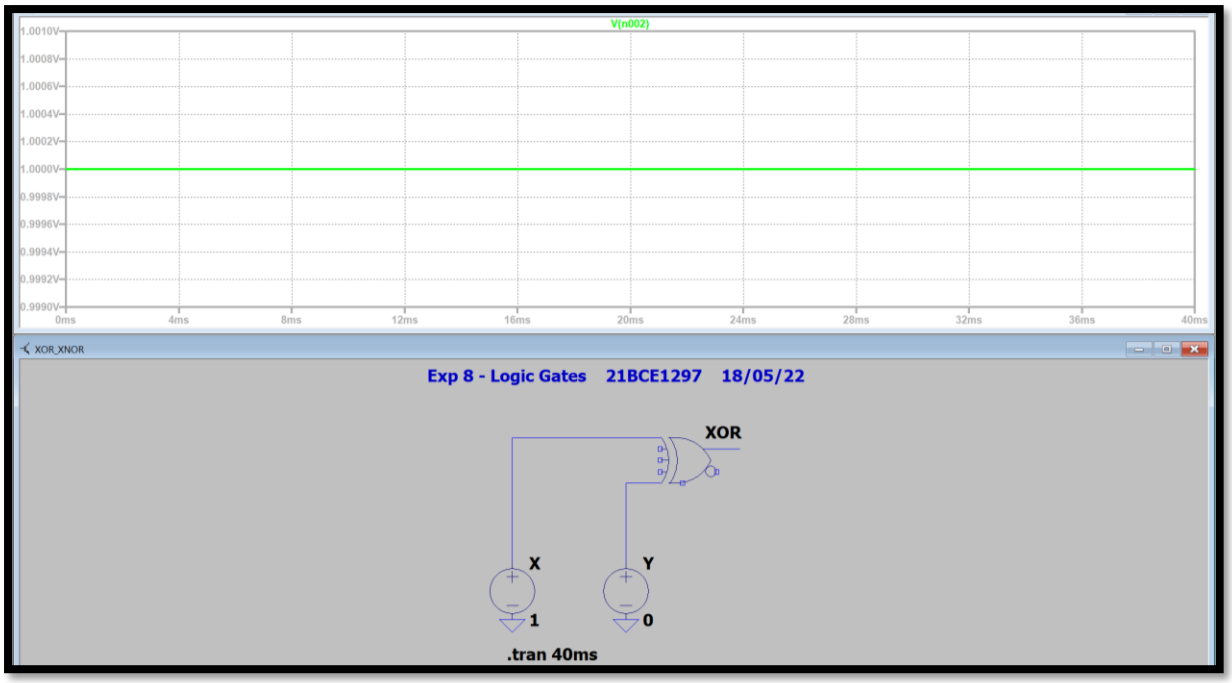

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOR
X
Y
1
0
.tran 40ms

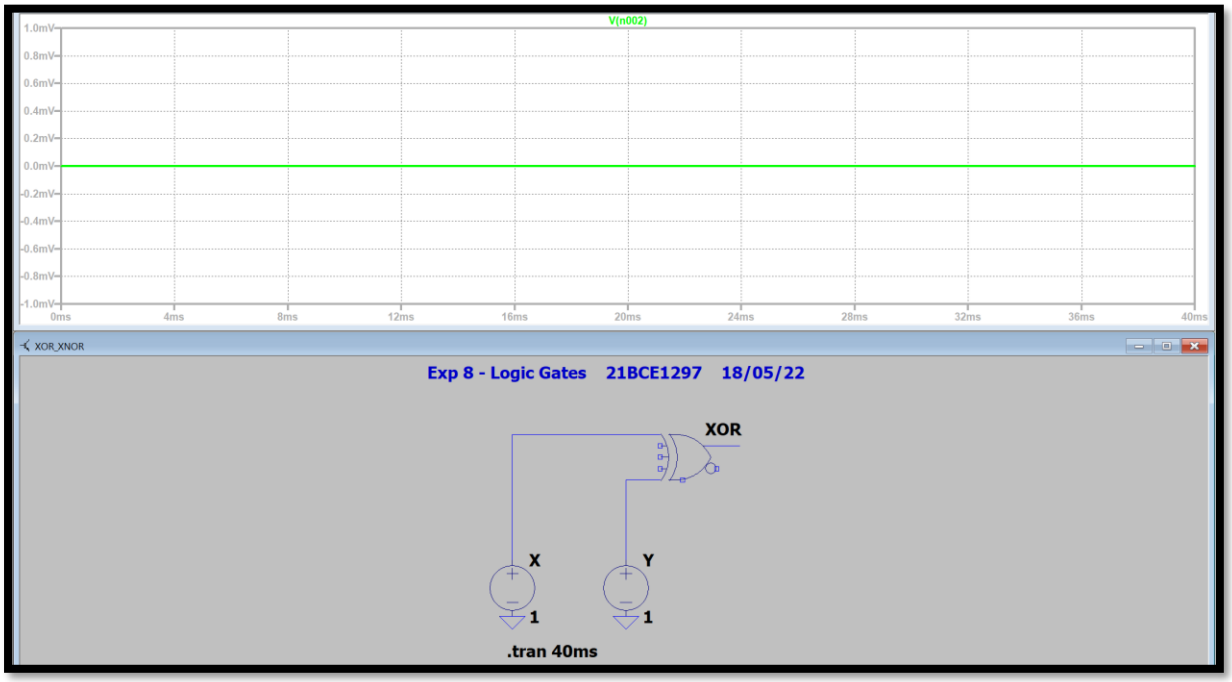

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
OR_NOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOR
X
Y
1
1
.tran 40ms

8. XOR Gate

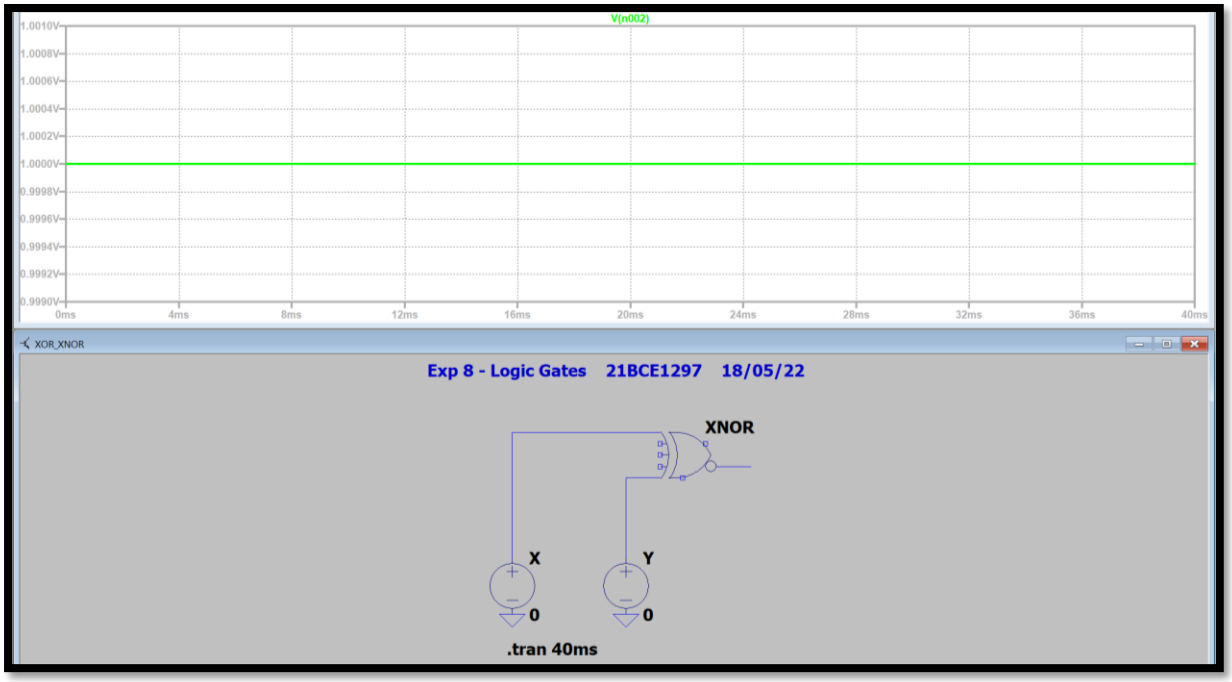

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XOR
X
Y
0
0
.tran 40ms

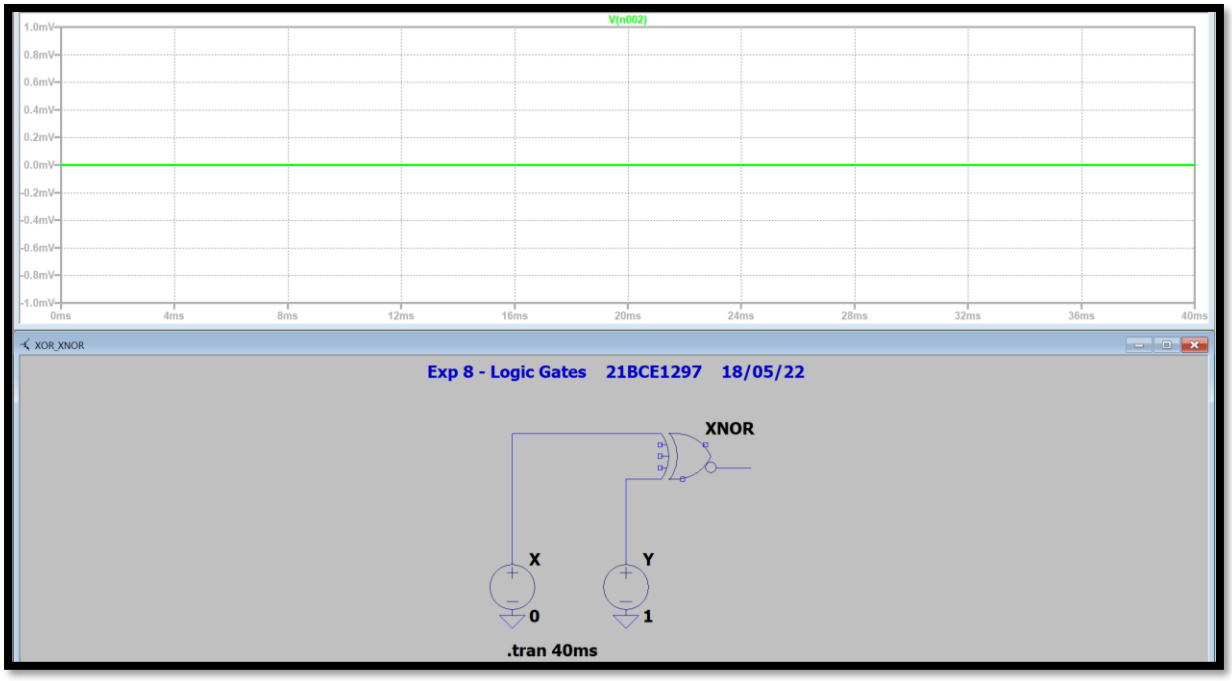

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XOR
X
Y
0
1
.tran 40ms

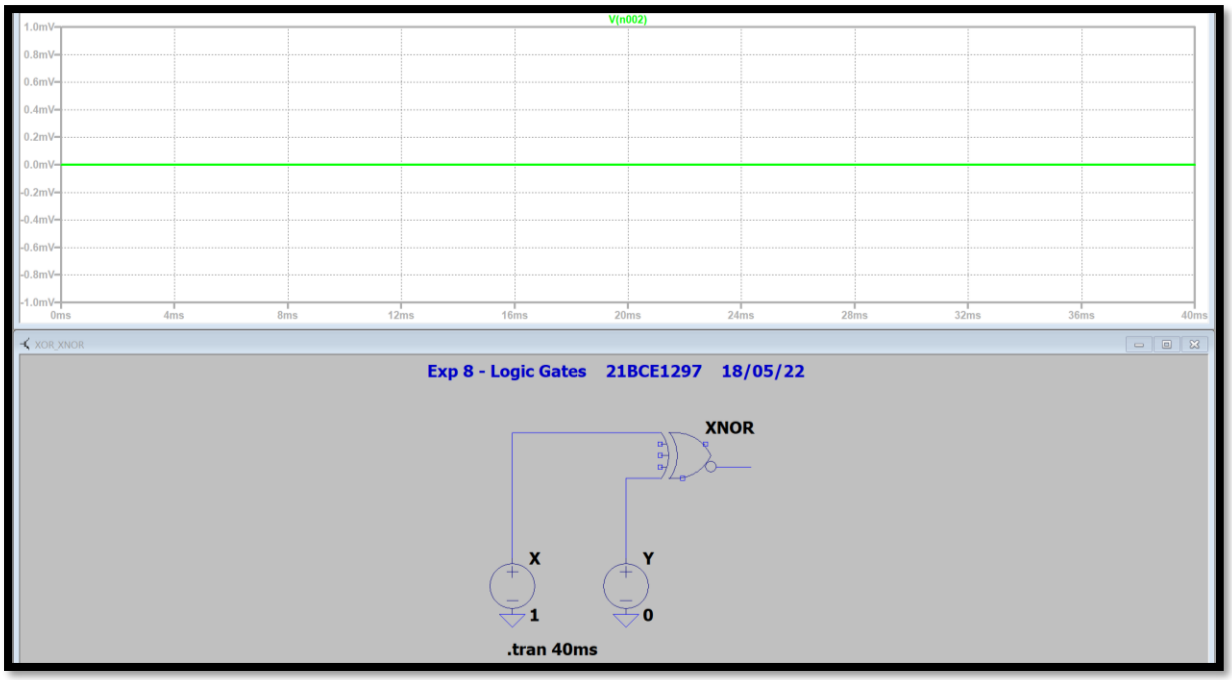

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XOR
X
Y
1
0
.tran 40ms

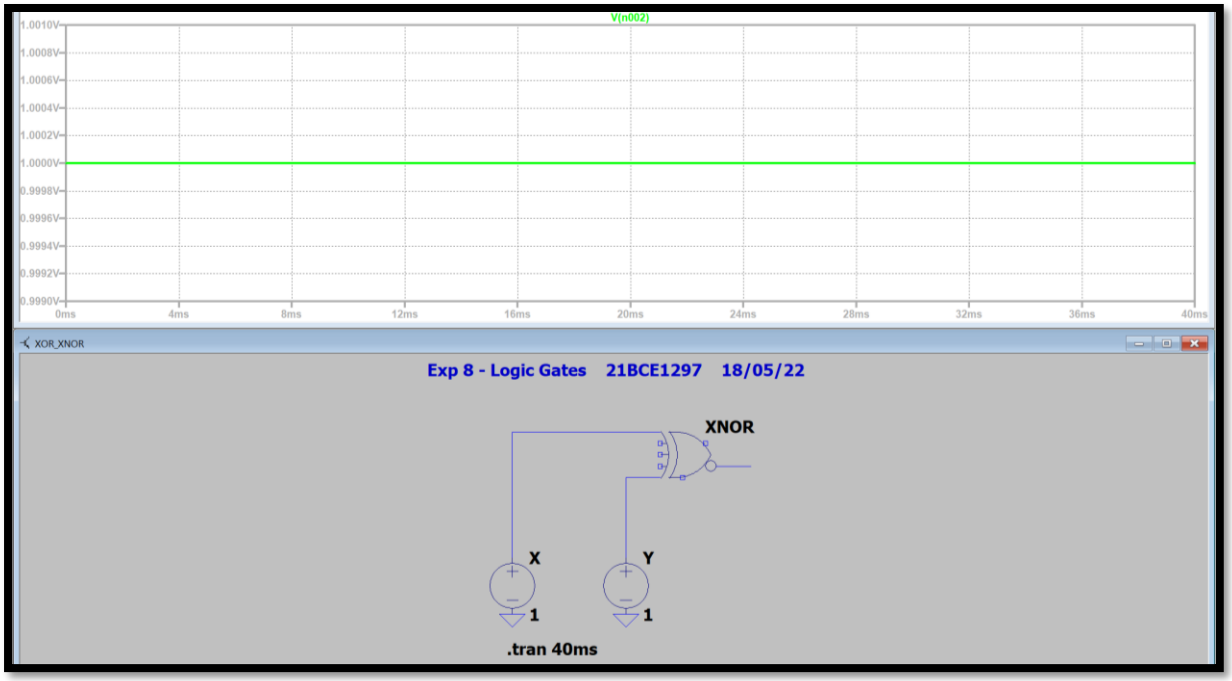

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XOR
X
Y
1
1
.tran 40ms

9. XNOR Gate

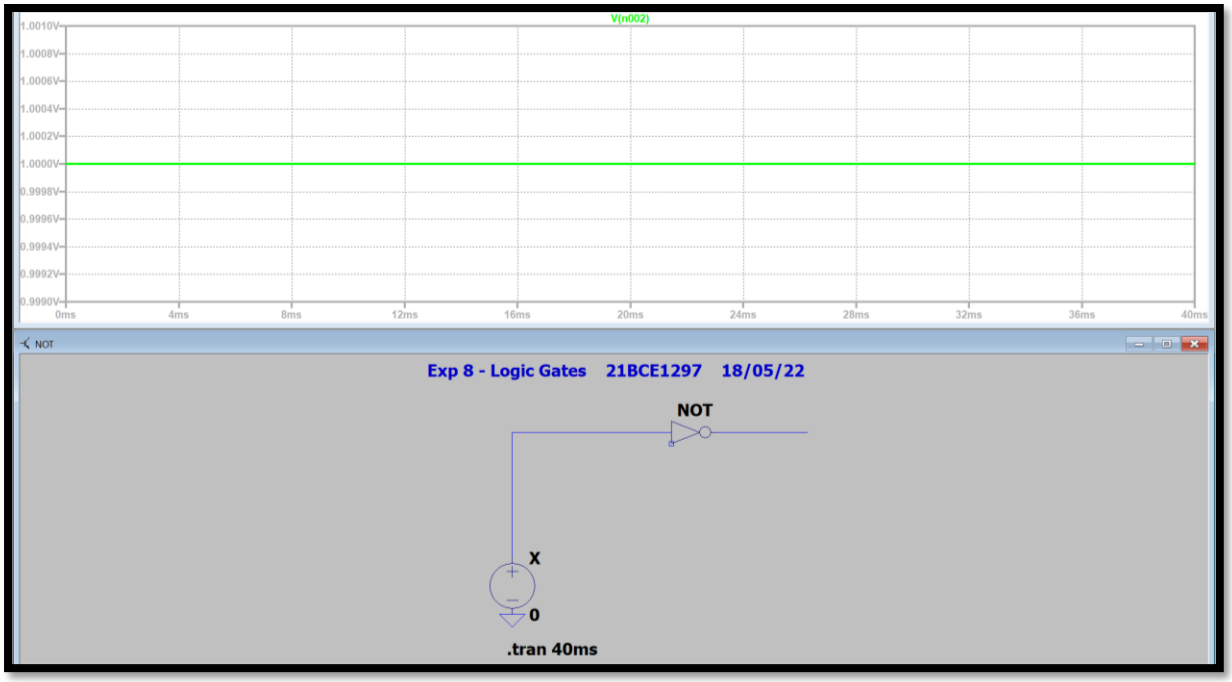

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XNOR
X
Y
0
0
.tran 40ms

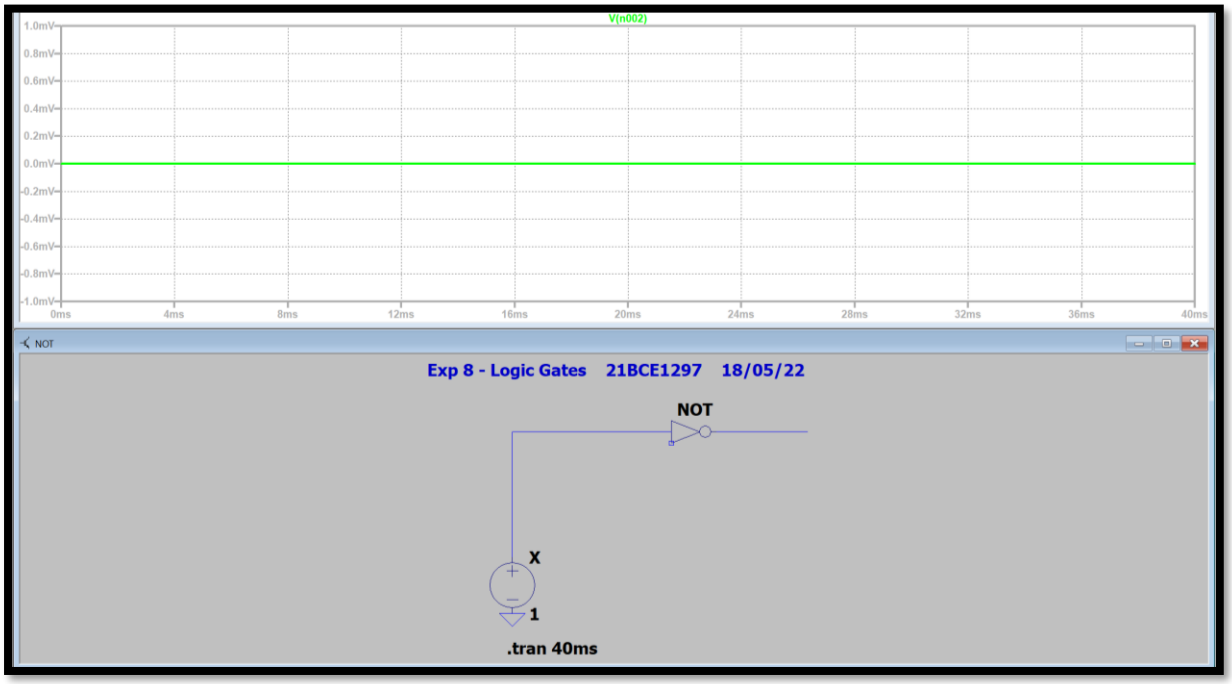

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XNOR
X
Y
0
1
.tran 40ms


V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XNOR
X
Y
1
0
.tran 40ms

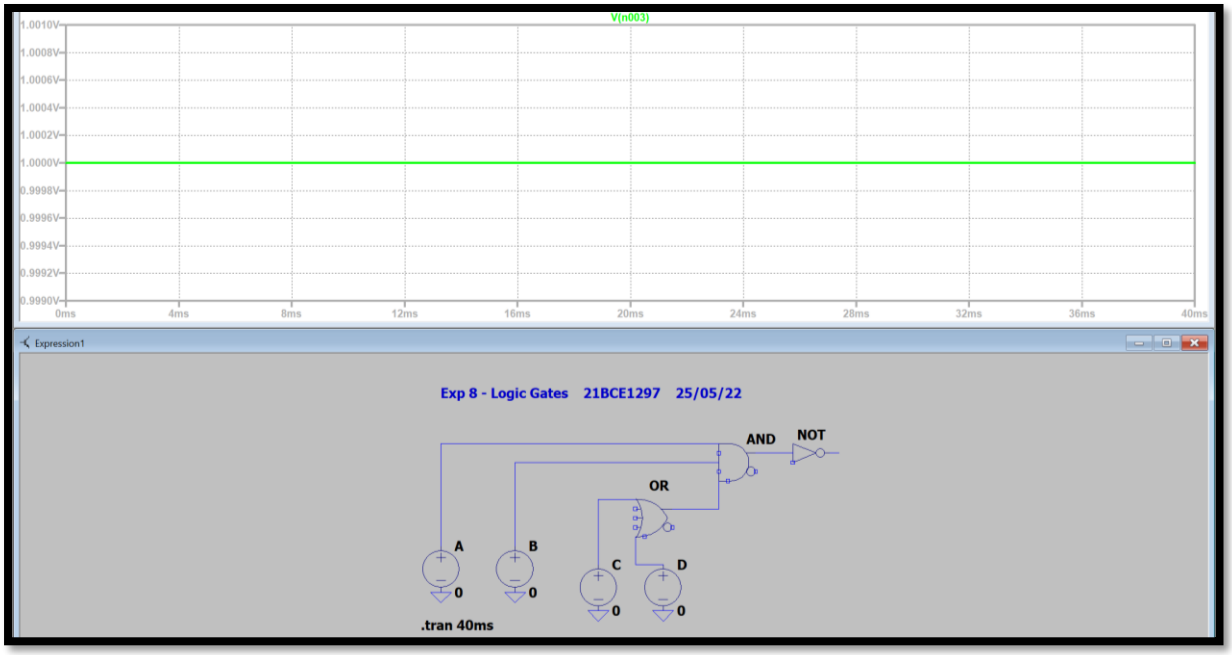

V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
XOR_XNOR
Exp 8 - Logic Gates 21BCE1297 18/05/22
XNOR
X
Y
1
1
.tran 40ms

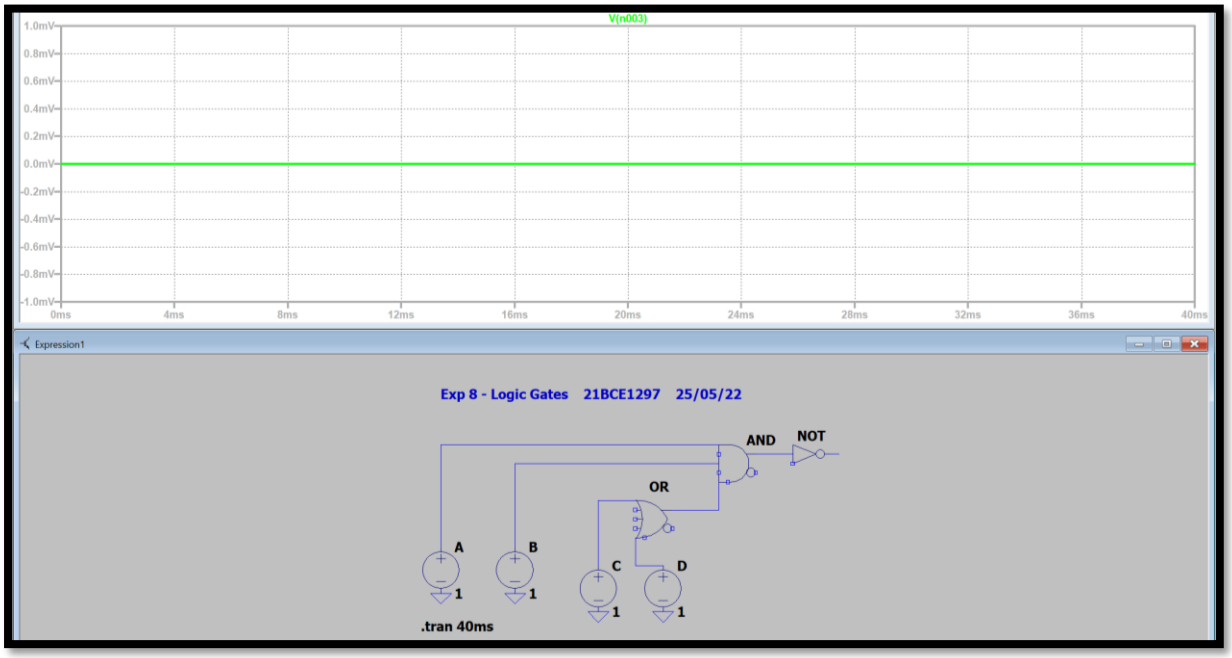
10.NOT Gate


V(n002)
1.0010V
1.0008V
1.0006V
1.0004V
1.0002V
1.0000V
0.9998V
0.9996V
0.9994V
0.9992V
0.9990V
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
NOT
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOT
X
0
.tran 40ms

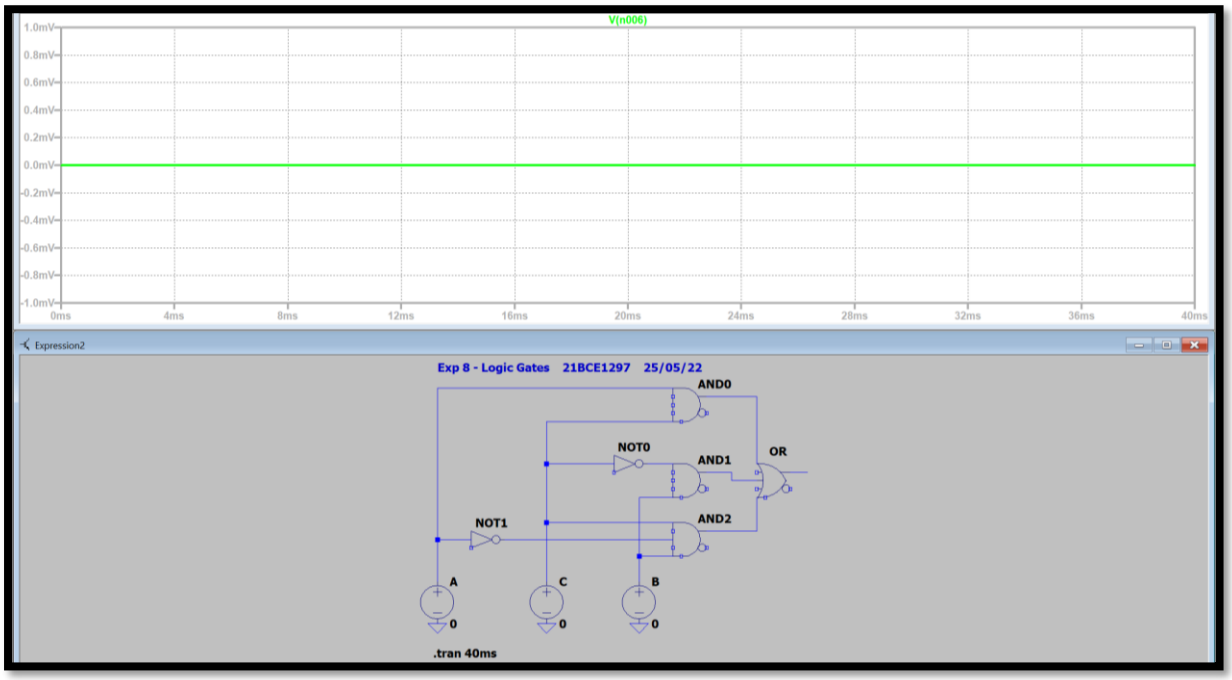

V(n002)
1.0mV
0.8mV
0.6mV
0.4mV
0.2mV
0.0mV
-0.2mV
-0.4mV
-0.6mV
-0.8mV
-1.0mV
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
NOT
Exp 8 - Logic Gates 21BCE1297 18/05/22
NOT
X
1
.tran 40ms

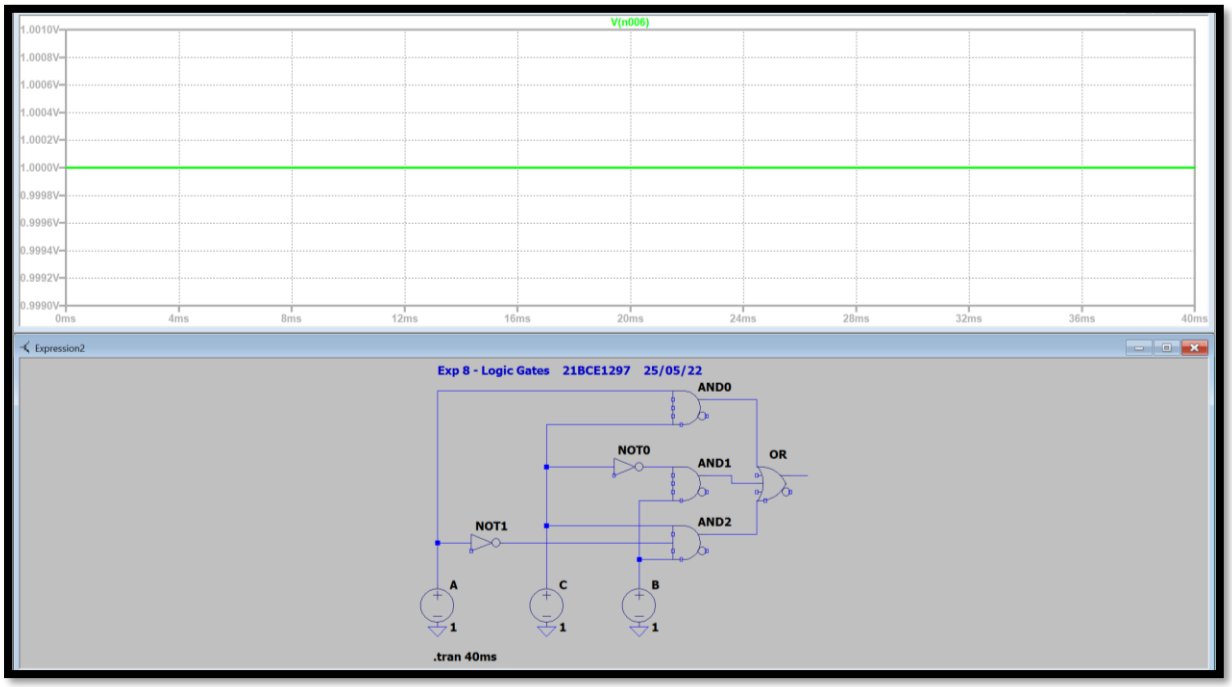
11. $x = \overline{A \cdot B(C + D)}$



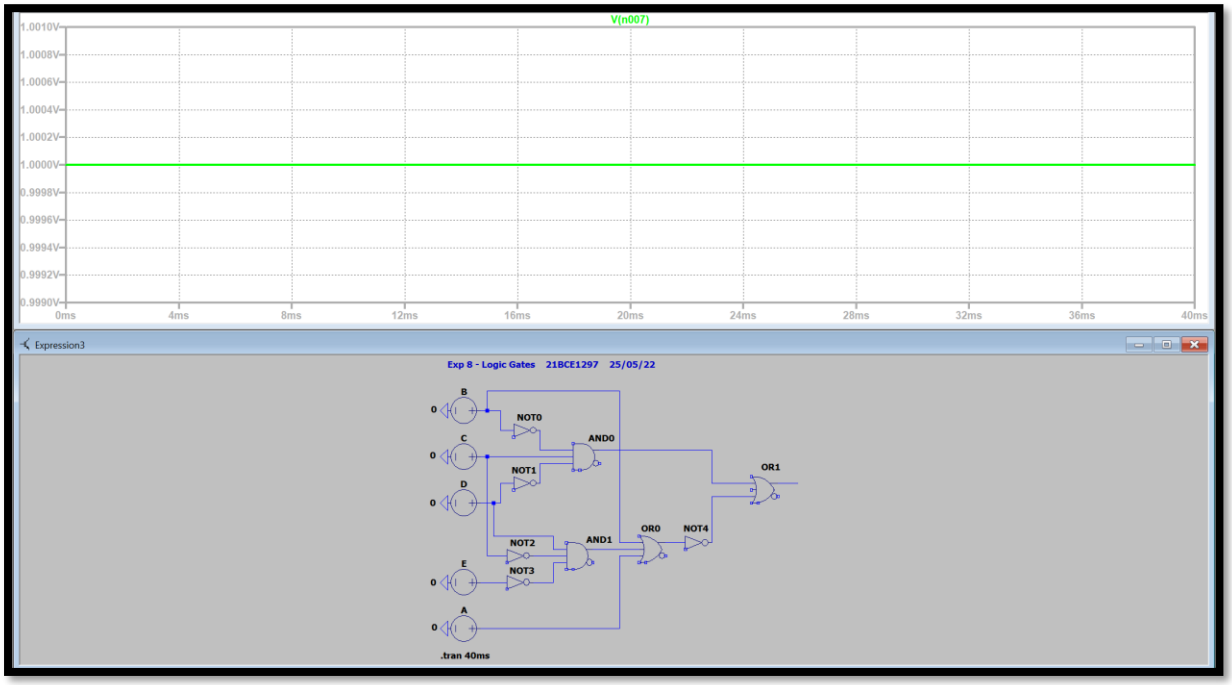


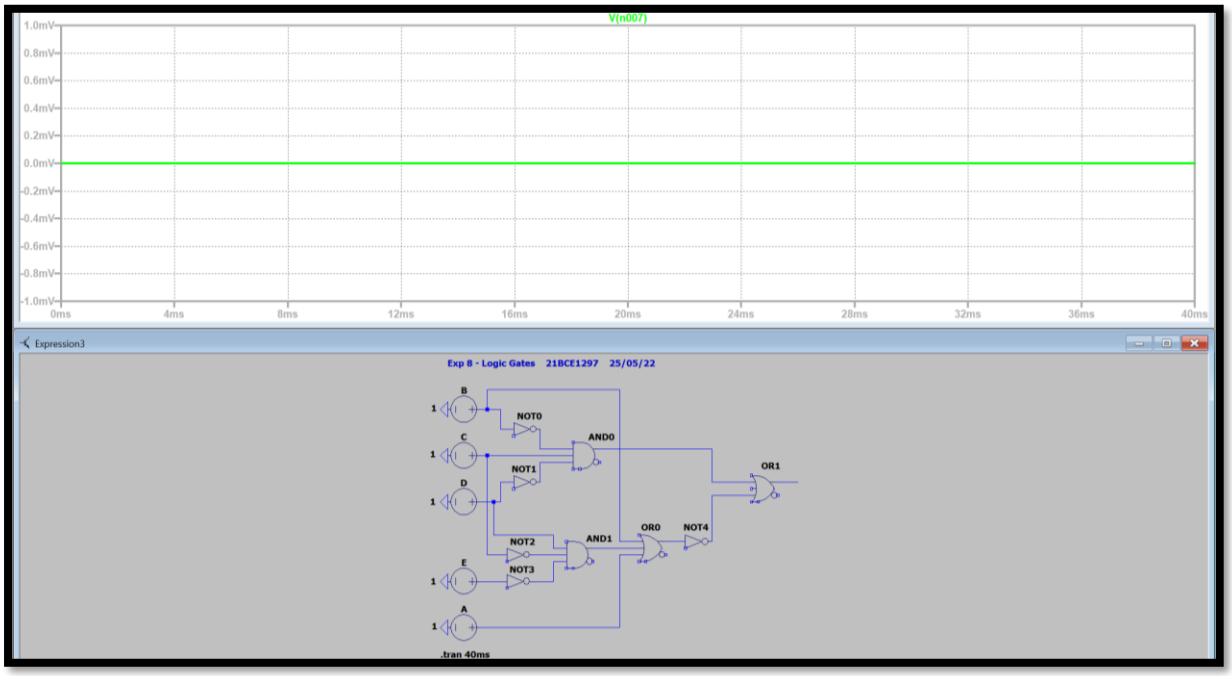
12. $y = AC + B\bar{C} + \bar{A}BC$





13. $z = \overline{A + B + \bar{C}D\bar{\bar{E}} + \bar{B}C\bar{D}}$





Conclusion:

Hence, we can see that the truth table is verified for all Boolean gates and Boolean functions.

Inferences:

1. $A\ OR\ B = A + B$
2. $A\ AND\ B = A \cdot B$
3. $NOT\ A = \bar{A}$
4. $A\ NOR\ B = \overline{A + B}$
5. $A\ NAND\ B = \overline{A \cdot B}$
6. $A\ XOR\ B = A \cdot B + \overline{A \cdot B}$
7. $A\ XNOR\ B = \overline{A \cdot B + \overline{A \cdot B}}$